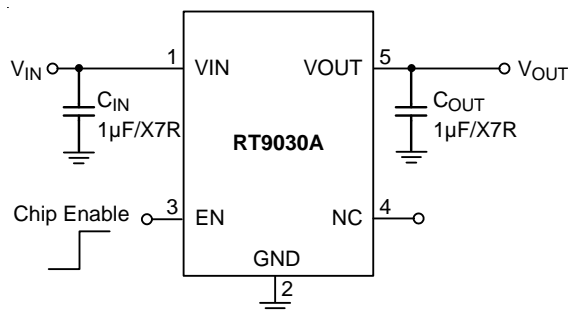


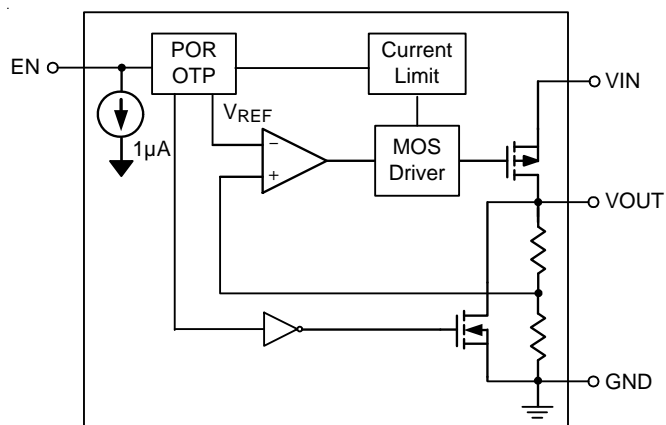
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	Supply Input.
2	GND	Ground.
3	EN	Enable Input Logic, Active High. When the EN pin is open, it will be pulled low internally.
4	NC	No Internal Connection.
5	VOUT	Regulator Output.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ----- 6V
- EN Input Voltage ----- 6V
- Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$
SOT-23-5 ----- 0.400W
- Package Thermal Resistance (Note 2)
SOT-23-5, θ_{JA} ----- 250°C/W
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
HBM (Human Body Model) ----- 2kV
MM (Machine Model) ----- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage Range ----- 1.5V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 0.5\text{V}$, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT} = 1\mu\text{F}/X5\text{R}$ (Ceramic), $T_A = 25^\circ\text{C}$, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Noise Voltage		V _{ON}	I _{OUT} = 0mA	--	30	--	μV _{RMS}
Output Voltage Accuracy (Fixed Output Voltage)		ΔV _{OUT}		−2	0	2	%
Quiescent Current (Note 5)		I _Q	I _{OUT} = 0mA	--	25	50	μA
Shutdown Current		I _{SHDN}	V _{EN} = 0V	--	0.7	1.5	μA
Current Limit		I _{LIM}	R _{LOAD} = 0Ω, 1.5V ≤ V _{IN} < 5.5V	350	600	--	mA
Dropout Voltage (Note 6)		V _{DROP}	V _{OUT} = 1.2V to 1.4V, I _{OUT} = 300mA	50	400	550	mV
			V _{OUT} = 1.5V to 2.4V, I _{OUT} = 300mA	40	250	400	
			V _{OUT} = 2.5V to 3.3V, I _{OUT} = 300mA	20	150	300	
Load Regulation (Note 7) (Fixed Output Voltage)		ΔV _{LOAD}	V _{IN} = (V _{OUT} + 0.6V) to 5.5V, I _{OUT} = 1mA to 300mA	--	--	1	%
EN Threshold Voltage	Logic-High	V _{IH}		1.6	--	5.5	V
	Logic-Low	V _{IL}		0	--	0.3	
EN Pin Current		I _{EN}		--	1	3	μA
Power Supply Rejection Rate	f = 1kHz	PSRR		--	−67	--	dB
	f = 10kHz			--	−55	--	
	f = 100kHz			--	−40	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	ΔV_{LINE}	$V_{IN} = (V_{OUT} + 0.6V)$ to 5.5V, $I_{OUT} = 1mA$ to 300mA	--	0.01	0.2	%/V
Thermal Shutdown Temperature	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at $T_A = 25^\circ\text{C}$ on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

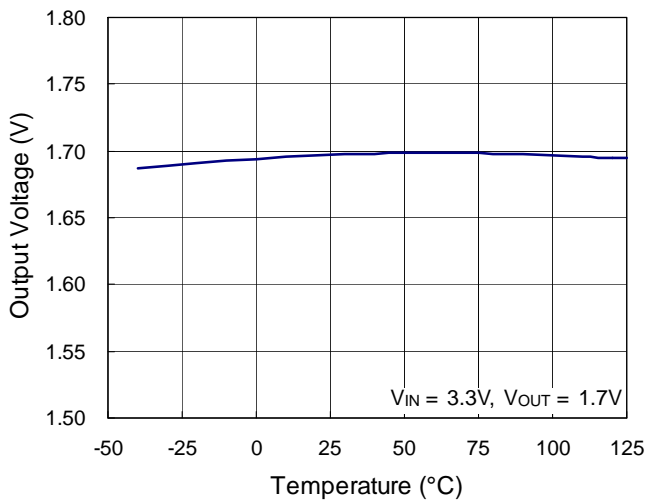
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition ($I_{OUT} = 0mA$). The total current drawn from the supply is the sum of the load current plus the ground pin current.

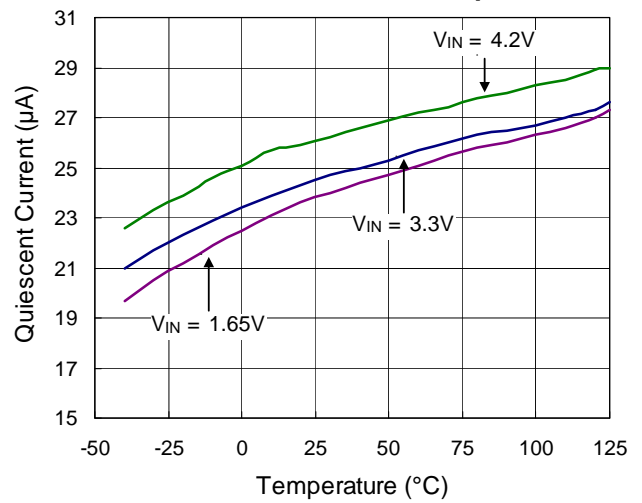
Note 6. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)} - 100mV$.

Typical Operating Characteristics

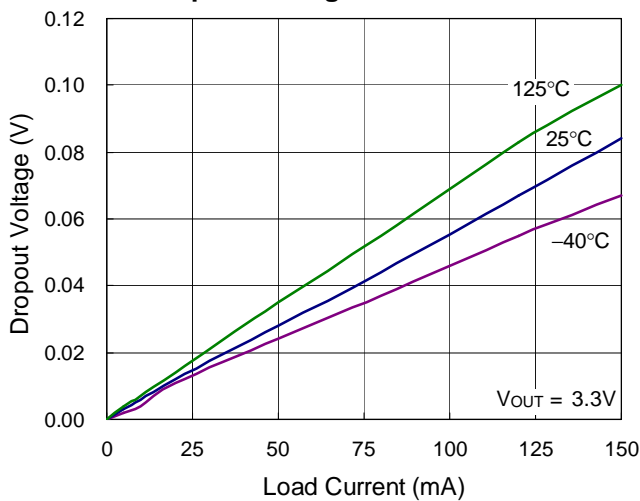
Output Voltage vs. Temperature



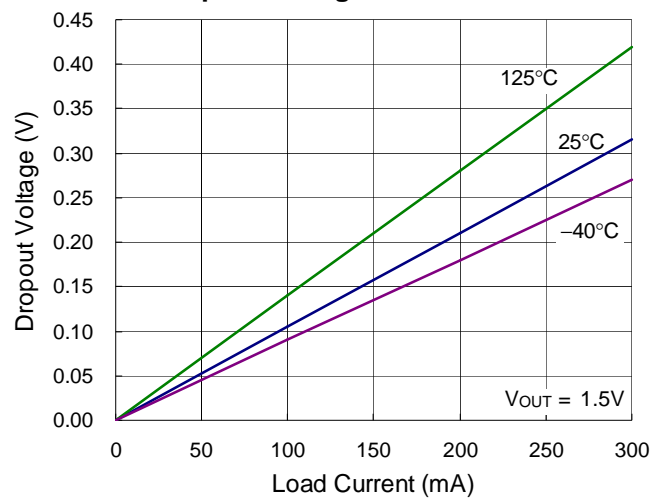
Quiescent Current vs. Temperature



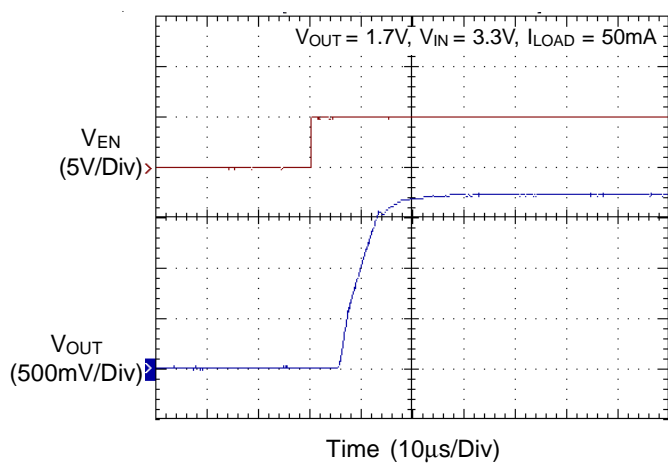
Dropout Voltage vs. Load Current



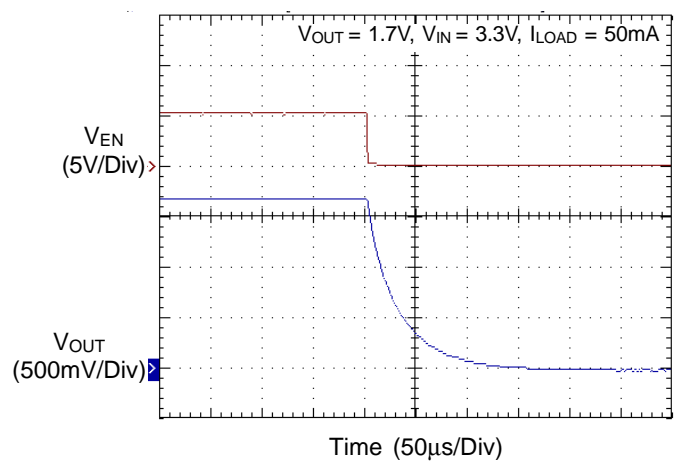
Dropout Voltage vs. Load Current



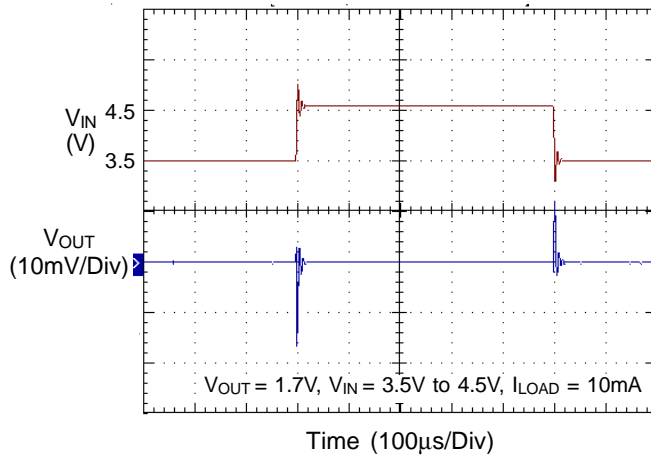
Power On from EN



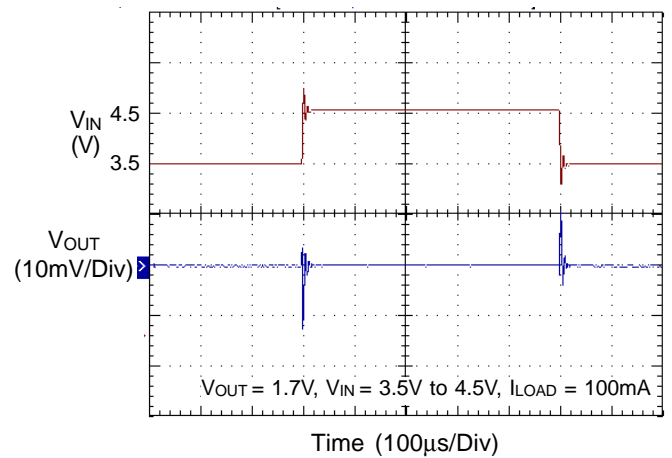
Power Off from EN



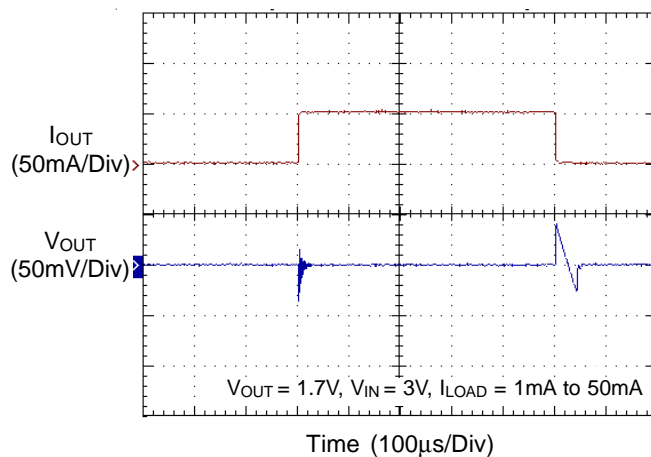
Line Transient Response



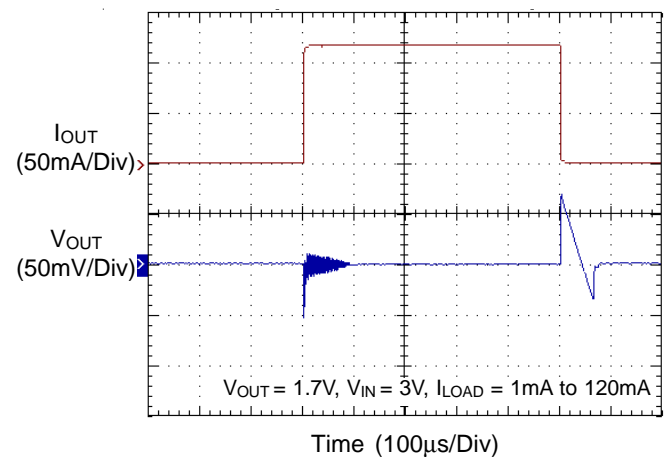
Line Transient Response



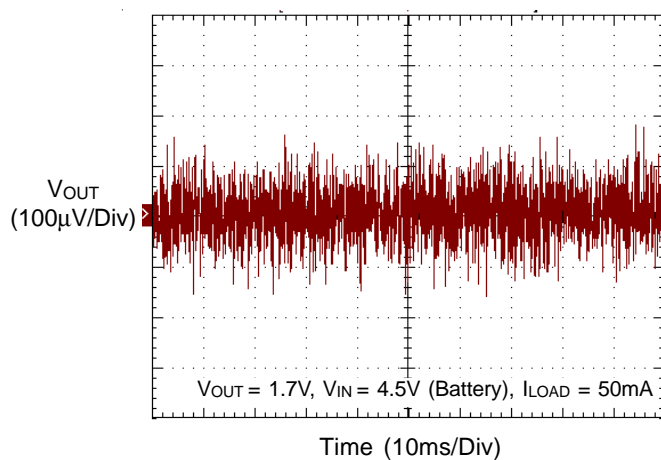
Load Transient Response



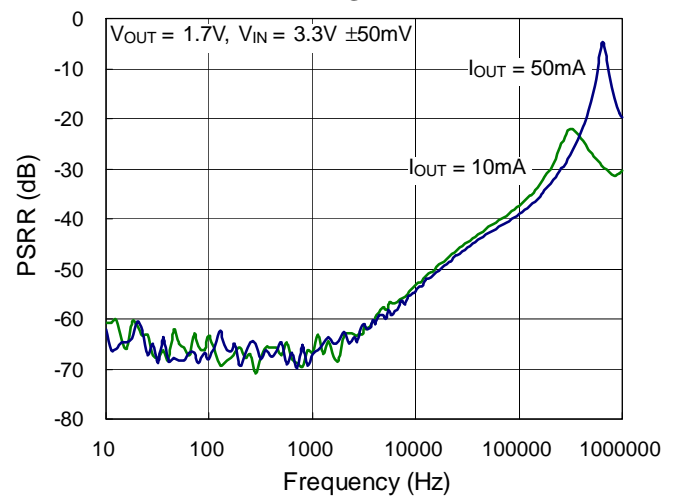
Load Transient Response



Noise



PSRR



Applications Information

Capacitor Selection

In order to confirm the regulator stability and performance, X7R/X5R or other better quality ceramic capacitor should be selected.

Like any low-dropout regulator, the external capacitors used with the RT9030A must be carefully selected for regulator stability and performance. Use at least 1μF of capacitor on the RT9030A's input and the amount of capacitance can be increased without limit. The input capacitor should be located in less than 0.5 inch from the input pin of the IC and returned to a clean analog ground. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance in all LDOs application. The RT9030A is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the RT9030A output ensures stability. Output capacitor with larger capacitance can reduce noise and improve load transient response, stability and PSRR. The output capacitor should be located in less than 0.5 inch from the VOUT pin of the RT9030A and returned to a clean analog ground.

Enable

The RT9030A goes into shutdown mode when the EN pin is in a logic low condition. During this condition, the pass transistor, error amplifier and bandgap are turned off, reducing the supply current to 0.7μA typical. The EN pin can be directly tied to VIN to keep the part on.

Current limit

The RT9030A contains an independent current limiter, which monitors and limits the output current to 600mA (typ.) by controlling the gate voltage of the pass transistor. The output can be shorted to ground indefinitely without damaging the part.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For SOT-23-5 packages, the thermal resistance, θ_{JA} , is 250°C/W on a standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (250^\circ\text{C/W}) = 0.400\text{W for}$$

SOT-23-5 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} . The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

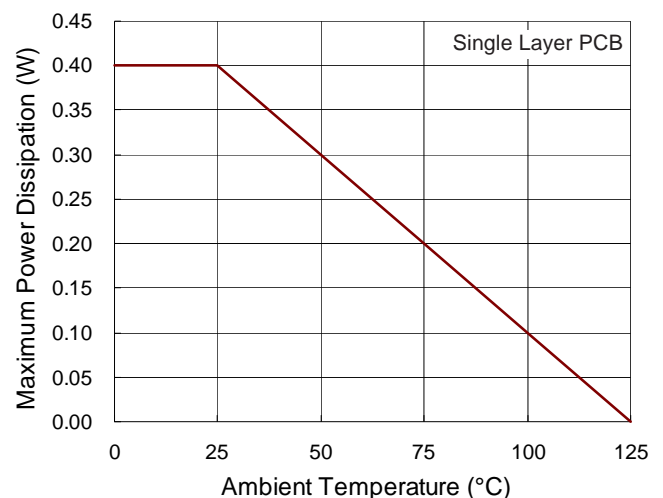


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PCB Layout is necessary for better performance. The following guidelines should be followed for good PCB layout.

- ▶ Place the input and output capacitors as close as possible to the IC.
- ▶ Keep VIN and VOUT trace as possible as short and wide.
- ▶ Use a large PCB ground plane for maximum thermal dissipation.

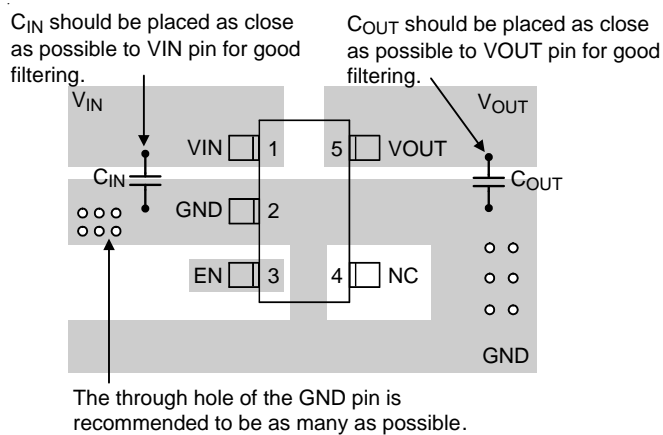
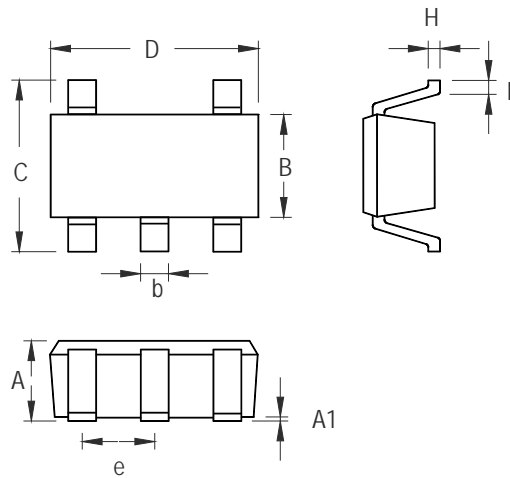


Figure 2. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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