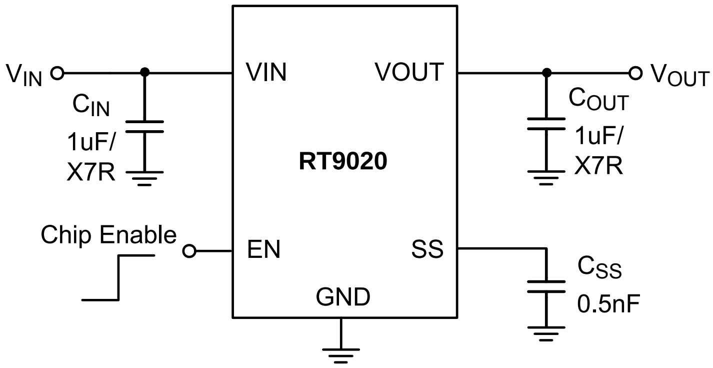
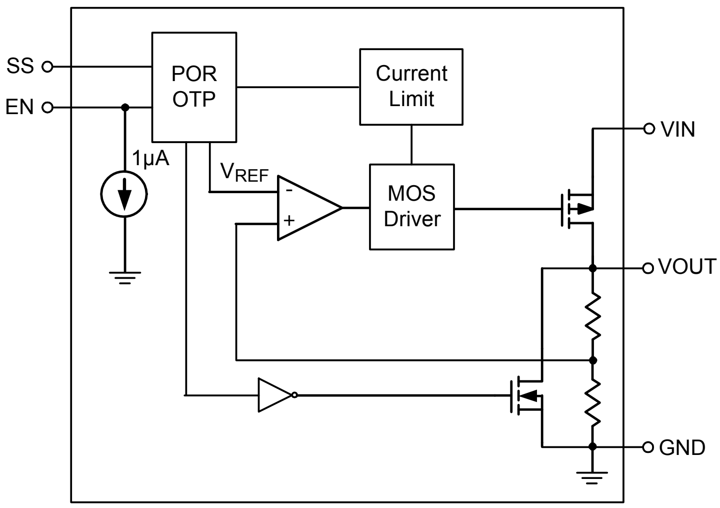
Typical Application Circuit



Functional Pin Description

Pin Number	Pin Name	Pin Function
1	VIN	Supply input.
2	GND	Common ground.
3	EN	Enable input logic, active high. When the EN goes to a logic low, the device will be shutdown.
4	SS	Soft start.
5	VOUT	Regulator output.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOT-23-5 ---------- 0.4W
  SC-70-5 ---------- 0.3W
- Package Thermal Resistance (Note 2)
  SOT-23-5, θ_{JA} ---------- 250°C/W
  SC-70-5, θ_{JA} ---------- 333°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 2.2V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1μF (Ceramic), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.2	--	5.5	V
Output Noise Voltage	V_{ON}	V_{OUT} = 1.5V, C_{OUT} = 1μF, I_{OUT} = 0mA, C_{SS} = 1nF	--	40	--	μV_{RMS}
Output Voltage Accuracy (Fixed Output Voltage)	ΔV_{OUT}	I_{OUT} = 10mA	–2	0	+2	%
Quiescent Current (Note 5)	I_Q	V_{EN} = 5V, I_{OUT} = 0mA	--	25	50	μA
Standby Current	I_{STBY}	V_{EN} = 0V	--	0.7	1.5	μA
Current Limit	I_{LIM}	R_{LOAD} = 0Ω, 2.2V ≤ V_{IN} < 2.6V	0.4	0.7	1.05	A
		R_{LOAD} = 0Ω, 2.7V ≤ V_{IN} ≤ 5.5V	0.5	0.8	1.05	
Dropout Voltage (Note 6)	V_{DROP}	I_{OUT} = 400mA, 2.2V ≤ V_{IN} < 2.7V	--	160	320	mV
		I_{OUT} = 500mA, 2.7V ≤ V_{IN} ≤ 5.5V	--	250	400	
Load Regulation (Note 7) (Fixed Output Voltage)	ΔV_{LOAD}	1mA < I_{OUT} < 400mA 2.2V ≤ V_{IN} < 2.7V	--	--	0.6	%
		1mA < I_{OUT} < 500mA 2.7V ≤ V_{IN} ≤ 5.5V	--	--	1	
Soft Start Time		V_{OUT} = 2.5V, C_{SS} = 1nF	--	0.7	1	ms

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Threshold	Logic-Low Voltage	V_{IL}		0	--	0.6	V
	Logic-High Voltage	V_{IH}		1.6	--	5.5	
Enable Pin Current		I_{EN}		0.1	1	5	μA
Power Supply Rejection Rate	f = 10kHz	PSRR	I_{OUT} = 10mA	--	−55	--	dB
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT}+0.5) to 5.5V, I_{OUT} = 1mA	--	0.01	0.2	%/V
Thermal Shutdown Temperature		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	30	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

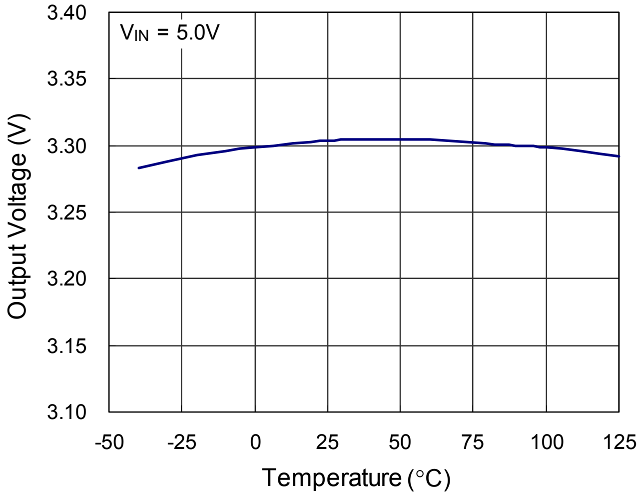
Note 6. The dropout voltage is defined as V_{IN} -V_{OUT}, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ - 100mV.

Note 7. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 10mA to 500mA.

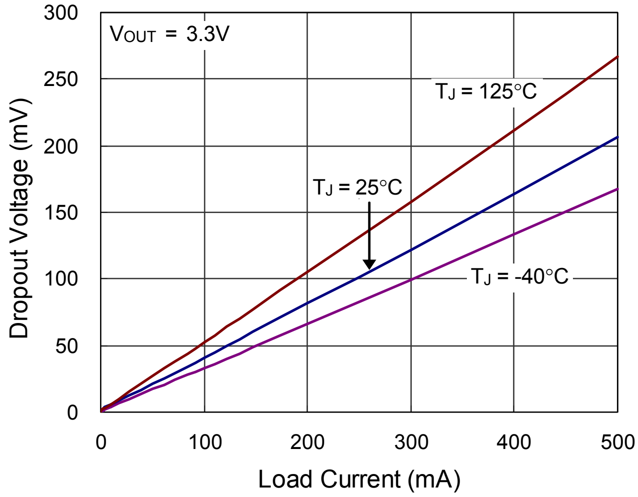
Typical Operating Characteristics

(C_{IN} = C_{OUT} = 1uF/X7R, C_{SS} = 1nF, unless otherwise specified)

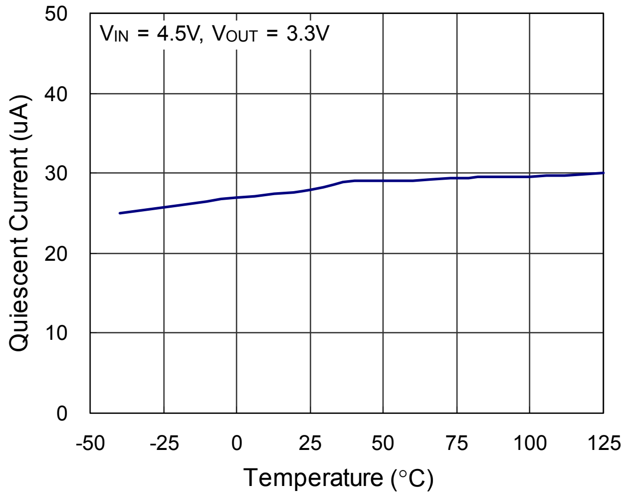
Output Voltage vs. Temperature



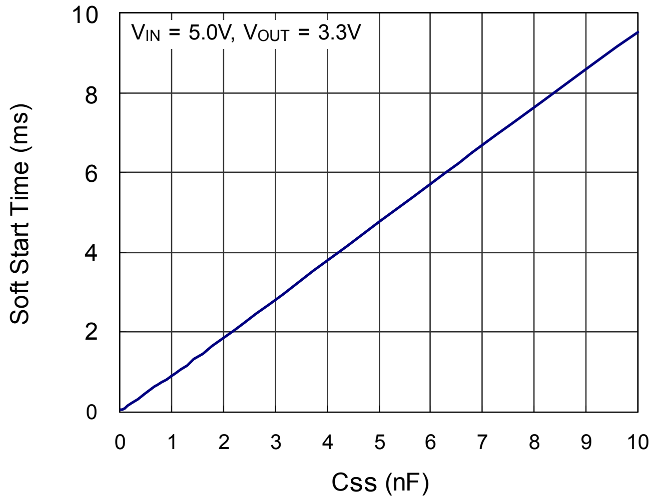
Dropout Voltage vs. Load Current



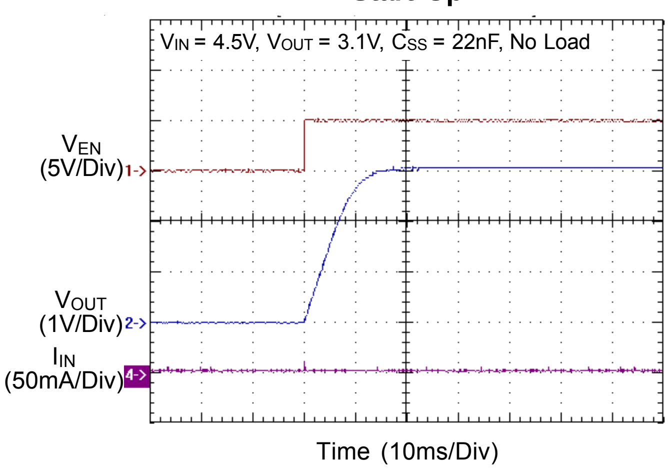
Quiescent Current vs. Temperature



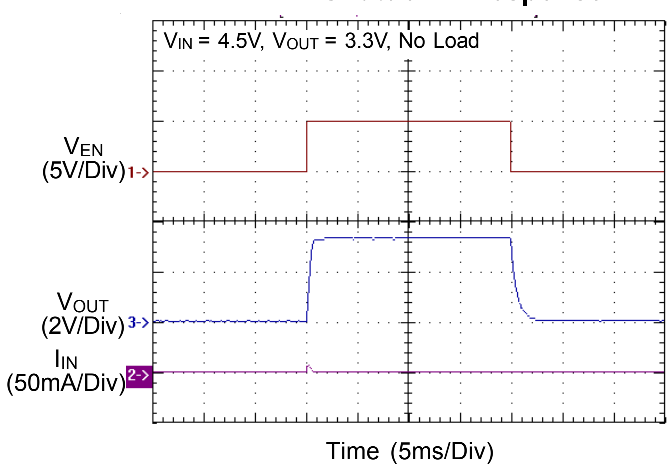
Soft Start Time

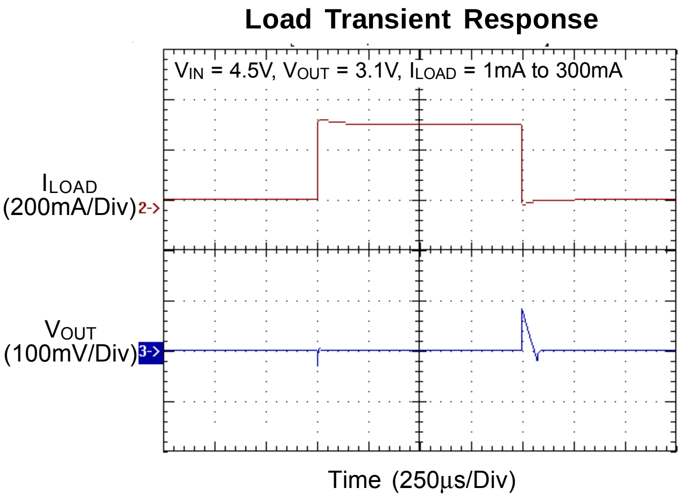


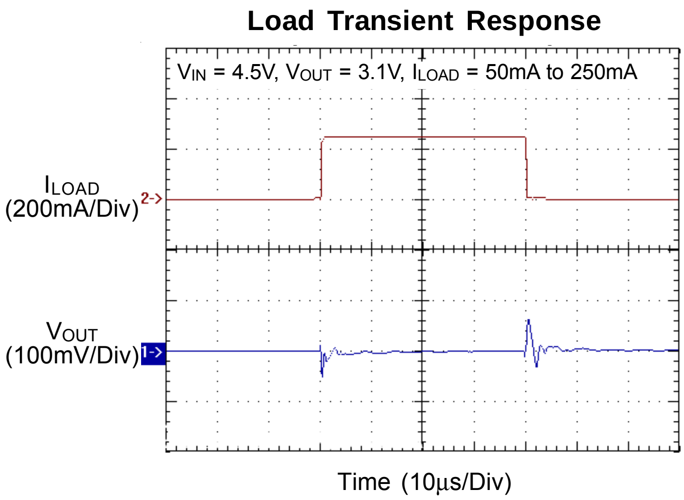
Start Up

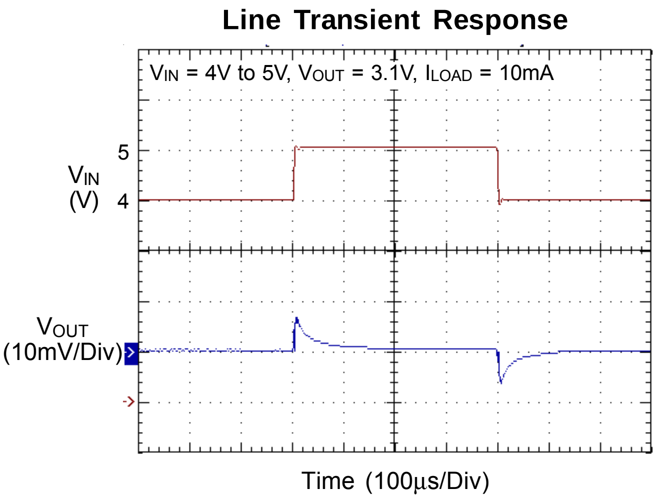


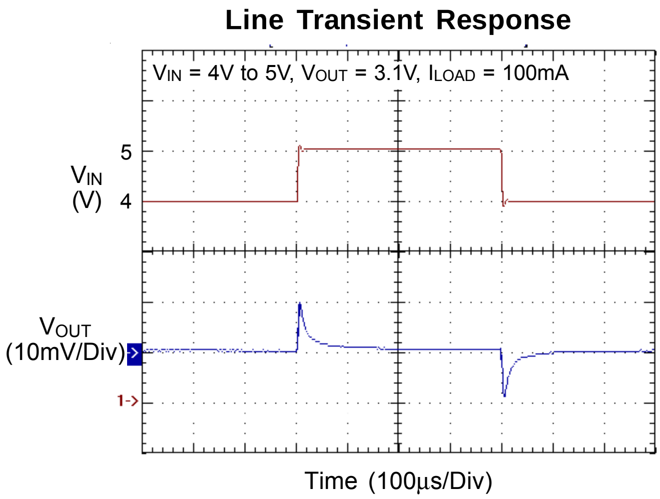
EN Pin Shutdown Response

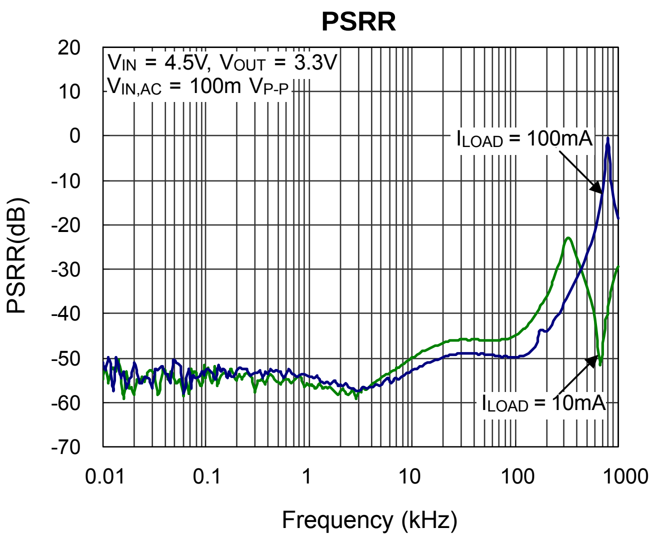


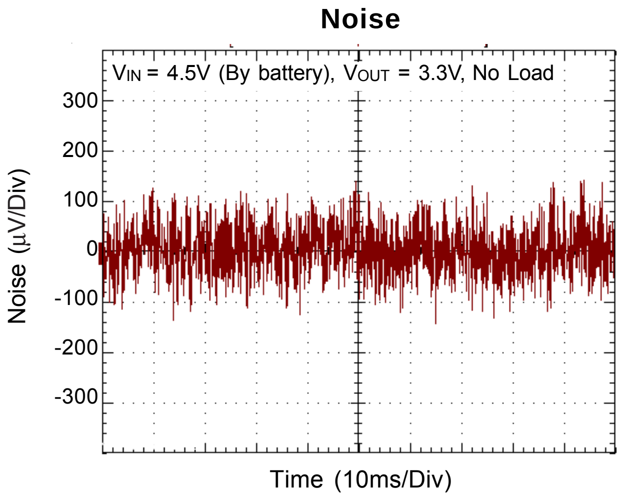

Load Transient Response
VIN = 4.5V, VOUT = 3.1V, ILOAD = 1mA to 300mA
ILOAD (200mA/Div)
VOUT (100mV/Div)
Time (250μs/Div)


Load Transient Response
VIN = 4.5V, VOUT = 3.1V, ILOAD = 50mA to 250mA
ILOAD (200mA/Div)
VOUT (100mV/Div)
Time (10μs/Div)


Line Transient Response
VIN = 4V to 5V, VOUT = 3.1V, ILOAD = 10mA
VIN (V)
5
4
VOUT (10mV/Div)
Time (100μs/Div)


Line Transient Response
VIN = 4V to 5V, VOUT = 3.1V, ILOAD = 100mA
VIN (V)
5
4
VOUT (10mV/Div)
Time (100μs/Div)


PSRR
VIN = 4.5V, VOUT = 3.3V
VIN,AC = 100m VP-P
ILOAD = 100mA
ILOAD = 10mA
PSRR(dB)
20
10
0
-10
-20
-30
-40
-50
-60
-70
0.01
0.1
1
10
100
1000
Frequency (kHz)


Noise
VIN = 4.5V (By battery), VOUT = 3.3V, No Load
Noise (μV/Div)
300
200
100
0
-100
-200
-300
Time (10ms/Div)

Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9020 must be carefully selected for regulator stability and performance. The recommended input and output capacitors should be 1μF or greater X7R/X5R ceramic.The input capacitor must be located a distance not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9020 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR > 20mΩ on the RT9020 output ensures stability. The RT9020 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9020 and returned to a clean analog ground.

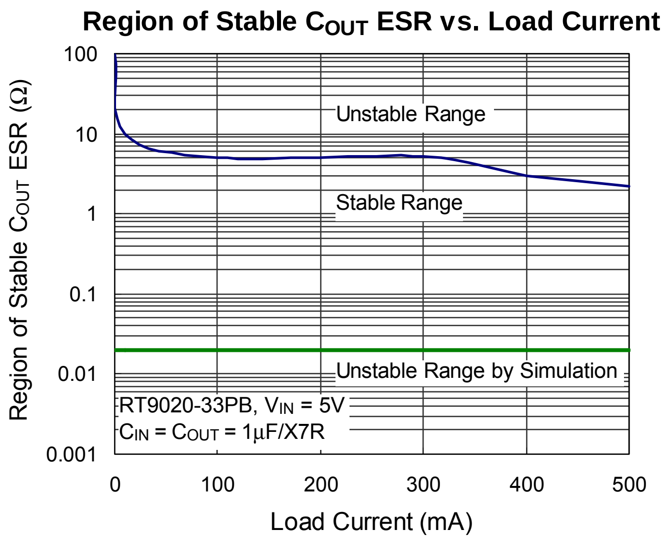


Figure 1

Enable

The RT9020 goes into shutdown mode when the EN pin is in a logic low condition. During this condition, the RT9020 has an EN pin to turn on or turn off regulator, When the EN pin is logic high, the regulator will be turned on. The supply current in shutdown mode is as low as 0.7μA typically. The EN pin may be directly tied to V_{IN} to keep the part on.

PSRR

The power supply rejection ratio (PSRR) is defined as the gain from the input to output divided by the gain from the supply to the output. The PSRR is found to be

$$PSRR = 20 \times \log\left(\frac{\Delta Gain\ Error}{\Delta Supply}\right)$$

Note that when heavy load measuring, Δsupply will cause Δtemperature. And Δtemperature will cause Δoutput voltage change. So the heavy load PSRR measuring includes temperature effect.

Current limit

The RT9020 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.7A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Considerations

Thermal protection limits power dissipation in RT9020. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the operated ambient temperature. The junction to ambient thermal resistance θ_{JA} (θ_{JA} is layout dependent) for SOT-23-5 package is 250°C/W and SC-70-5 package is 333°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / 250 = 0.400W for SOT-23-5 packages

$P_{D(MAX)}$ = (125°C − 25°C) / 333 = 0.300W for SC-70-5 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 2 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

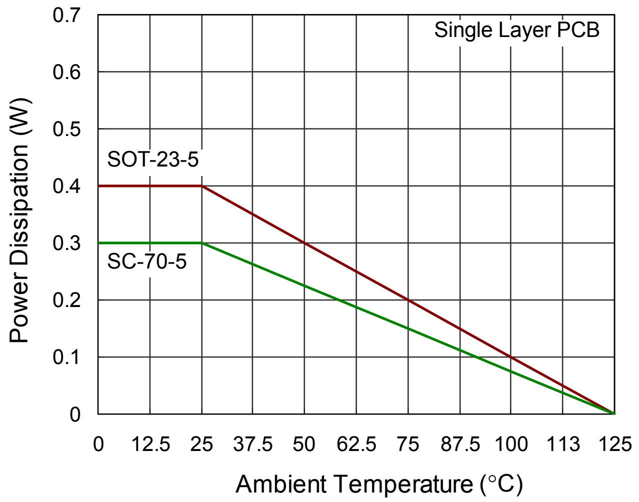
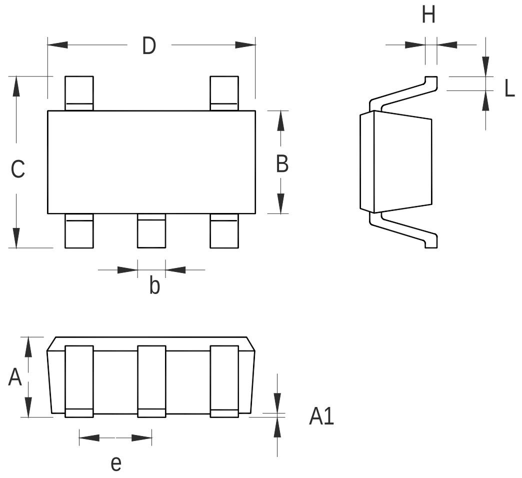


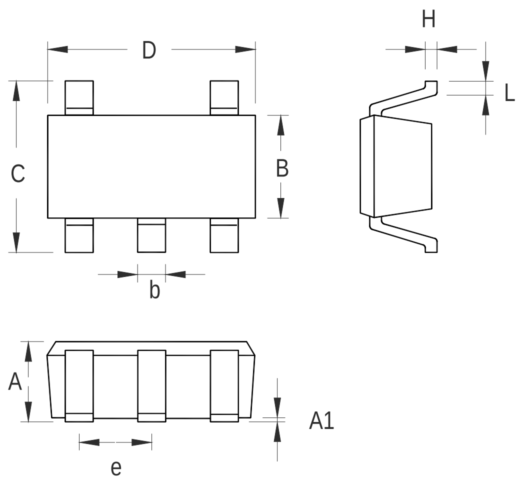
Figure 2. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

SC-70-5 Surface Mount Package

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