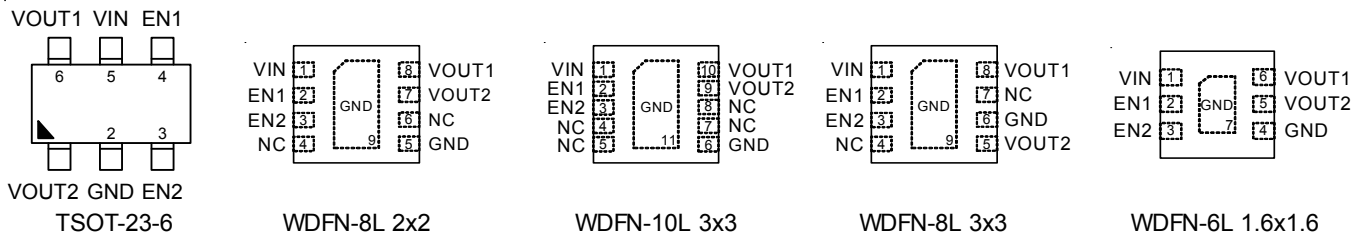
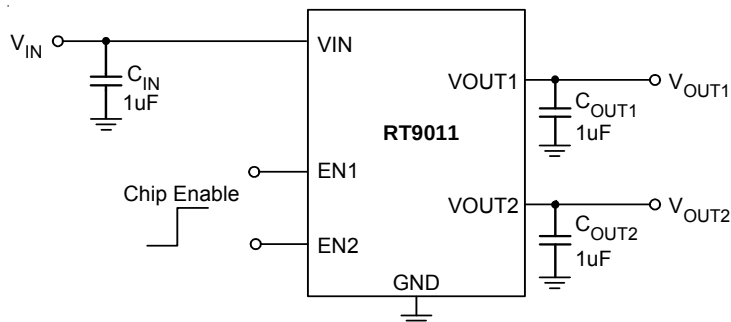


Pin Configuration

(TOP VIEW)



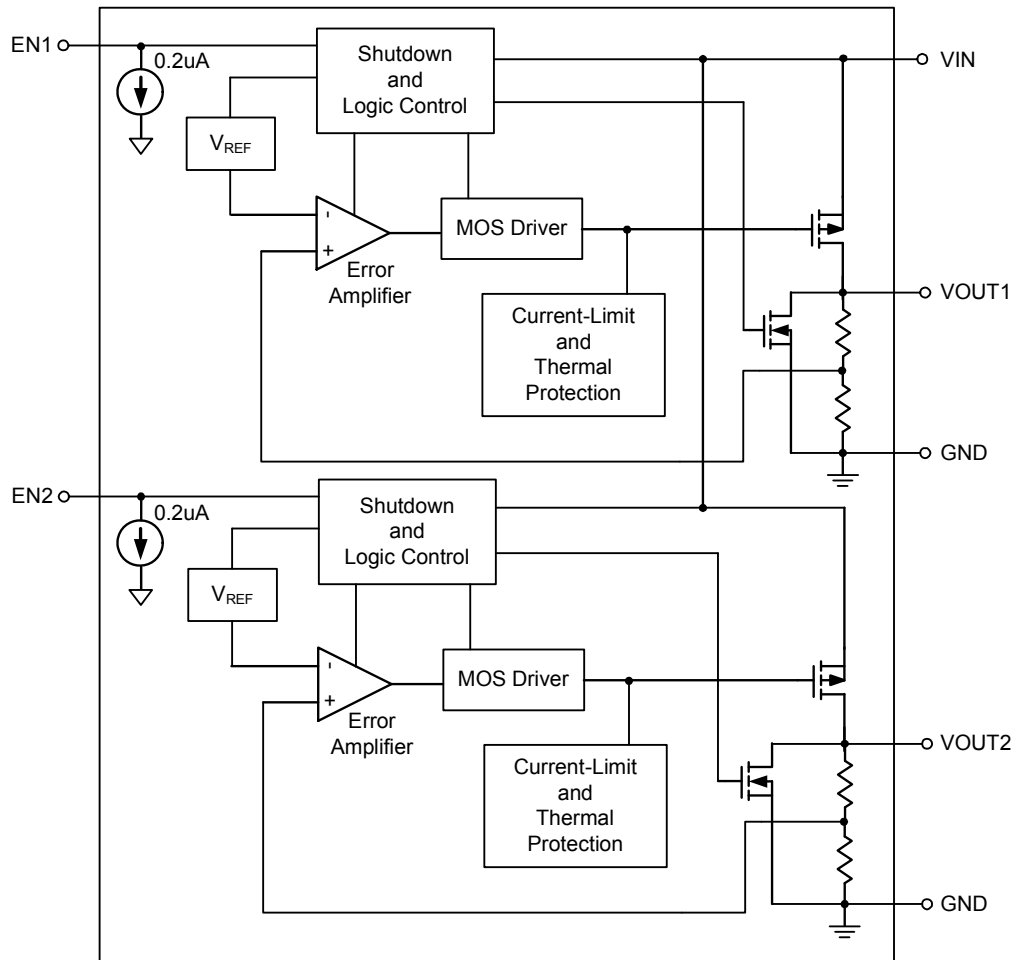
Typical Application Circuit



Functional Pin Description

Pin No.					Pin Name	Pin Function
TSOT-23-6	WDFN-8L 2x2	WDFN-10L 3x3	WDFN-8L 3x3	WDFN-6L 1.6x1.6		
5	1	1	1	1	VIN	Supply input.
4	2	2	2	2	EN1	Chip enable1 (Active high).
3	3	3	3	3	EN2	Chip enable2 (Active high).
2	5, Exposed Pad (9)	6, Exposed Pad (11)	6, Exposed Pad (9)	4, Exposed Pad (7)	GND	Common ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
1	7	9	5	5	VOUT2	Channel 2 output voltage.
6	8	10	8	6	VOUT1	Channel 1 output voltage.
--	4, 6	4, 5, 7, 8	4, 7	--	NC	No internal connection.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

• Supply Input Voltage	-----	-0.3V to 7V
• Other I/O Pin Voltages	-----	-0.3V to 7V
• Power Dissipation, P_D @ $T_A = 25^\circ\text{C}$		
TSOT-23-6	-----	0.455W
WDFN-8L 2x2	-----	0.606W
WDFN-10L 3x3	-----	0.926W
WDFN-8L 3x3	-----	0.926W
WDFN-6L 1.6x1.6	-----	0.571W
• Package Thermal Resistance (Note 2)		
TSOT-23-6, θ_{JA}	-----	220°C/W
WDFN-8L 2x2, θ_{JA}	-----	165°C/W
WDFN-10L 3x3, θ_{JA}	-----	108°C/W
WDFN-8L 3x3, θ_{JA}	-----	108°C/W
WDFN-6L 1.6x1.6, θ_{JA}	-----	175°C/W
• Junction Temperature	-----	150°C
• Lead Temperature (Soldering, 10 sec.)	-----	260°C
• Storage Temperature Range	-----	-65°C to 150°C
• ESD Susceptibility (Note 3)		
HBM (Human Body Mode)	-----	2kV
MM (Machine Mode)	-----	200V

Recommended Operating Conditions (Note 4)

• Supply Input Voltage	-----	2.5V to 5.5V
• Enable Input Voltage	-----	0V to 5.5V
• Junction Temperature Range	-----	-40°C to 125°C
• Ambient Temperature Range	-----	-40°C to 85°C

Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $V_{EN} = V_{IN}$, $C_{IN} = C_{OUT} = 1\mu\text{F}$, $T_A = -40^\circ\text{C}$ to 85°C , unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage		$V_{IN} = 2.5V$ to $5.5V$	2.5	--	5.5	V
Dropout Voltage (Note 5)	V_{DROP}	$I_{OUT} = 300mA$	--	240	330	mV
Output Voltage Range	V_{OUT}		1.2	--	3.5	V
V_{OUT} Accuracy	ΔV	$I_{OUT} = 1mA$ to $300mA$	-3	--	+3	%
Line Regulation	ΔV_{LINE}	$V_{IN} = (V_{OUT} + 0.3V)$ to $5.5V$ or $V_{IN} > 2.5V$, whichever is larger	--	--	0.2	%/V
Load Regulation	ΔV_{LOAD}	$1mA < I_{OUT} < 300mA$	--	--	0.6	%
Current Limit		$R_{LOAD} = 1\Omega$	330	450	700	mA
Quiescent Current	I_Q	$V_{EN} > 1.5V$	--	58	80	μA
Shutdown Current	I_{Q_SD}	$V_{EN} < 0.4V$	--	--	1	μA
EN Threshold	V_{IH}	$V_{IN} = 2.5V$ to $5.5V$, Power On	1.5	--	--	V
	V_{IL}	$V_{IN} = 2.5V$ to $5.5V$, Shutdown	--	--	0.4	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage TC			--	100	--	ppm/°C
V _{OUT} Discharge Resistance in Shutdown (Note 6)		V _{IN} = 5V, EN1 = EN2 = GND	--	3	--	kΩ
EN Pull Low Current	I _{EN}		--	0.2	--	μA
Thermal Shutdown	T _{SD}		--	170	--	°C
Thermal Shutdown Hysteresis	ΔT _{SD}		--	40	--	°C
PSRR V _{IN} = V _{OUT} + 1V, C _{OUT} = 2.2μF I _{LOAD} = 50mA	PSRR	f = 100Hz	--	70	--	dB
		f = 1kHz	--	70	--	
		f = 10kHz	--	70	--	
		f = 100kHz	--	54	--	
		f = 200kHz	--	45	--	
		f = 300kHz	--	38	--	
Output Voltage Noise		C _{OUT1} = C _{OUT2} = 10μF, 10Hz to 100kHz, I _{OUT1} = I _{OUT2} = 1mA	--	100	--	uVrms

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

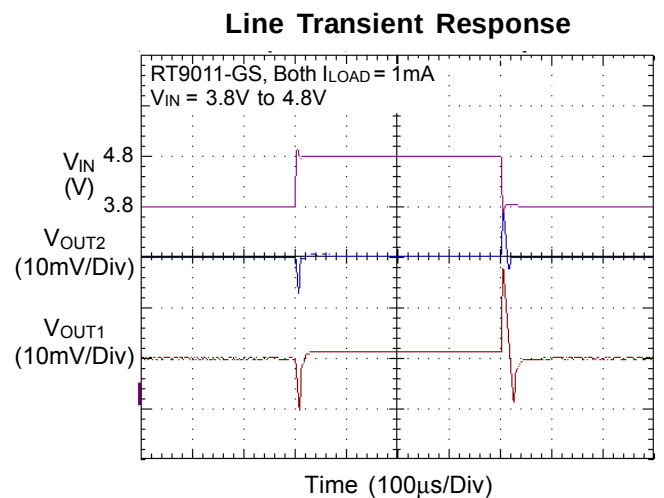
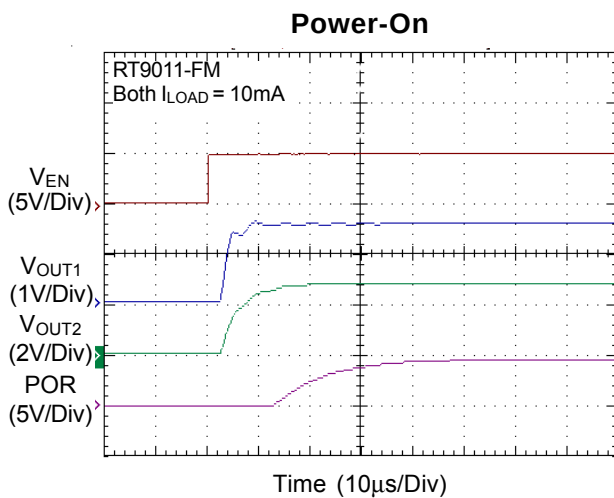
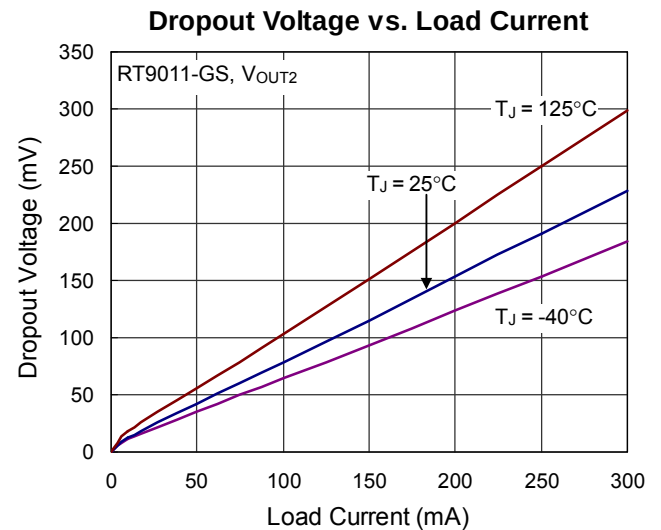
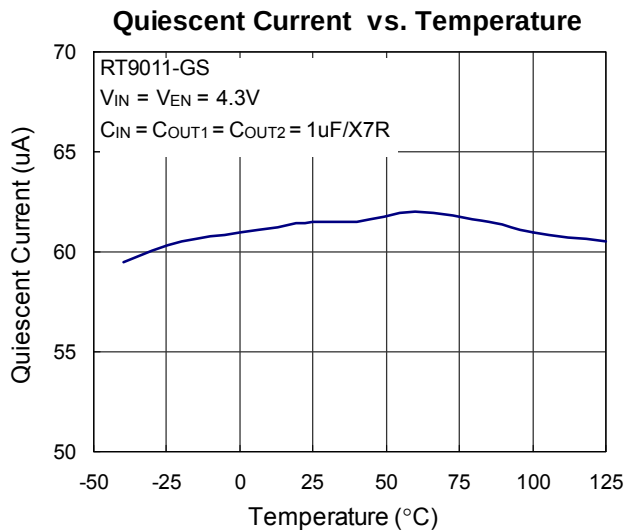
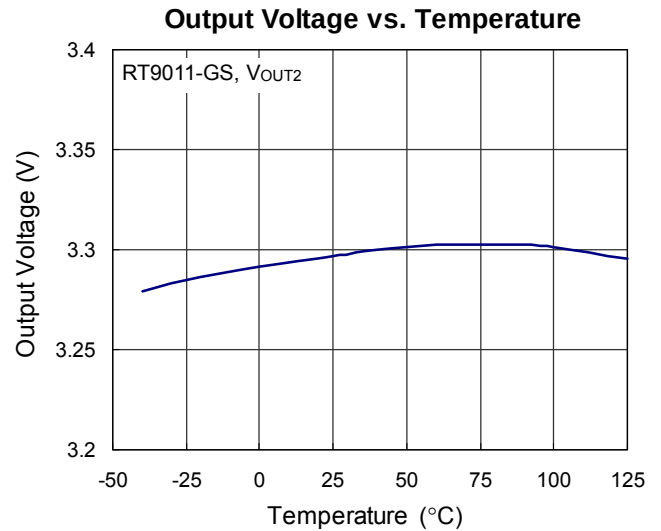
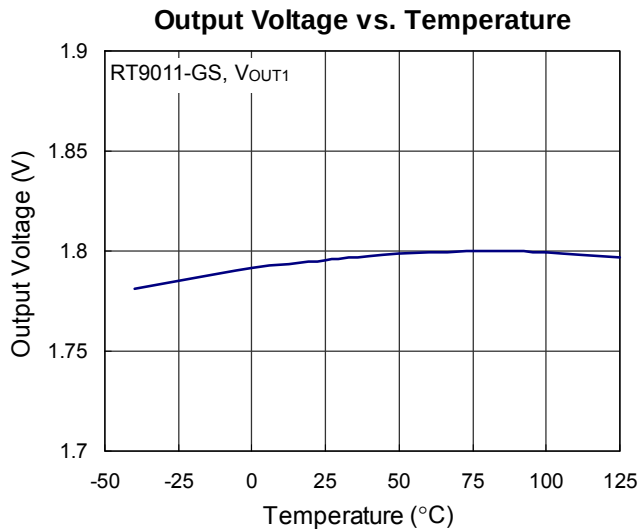
Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

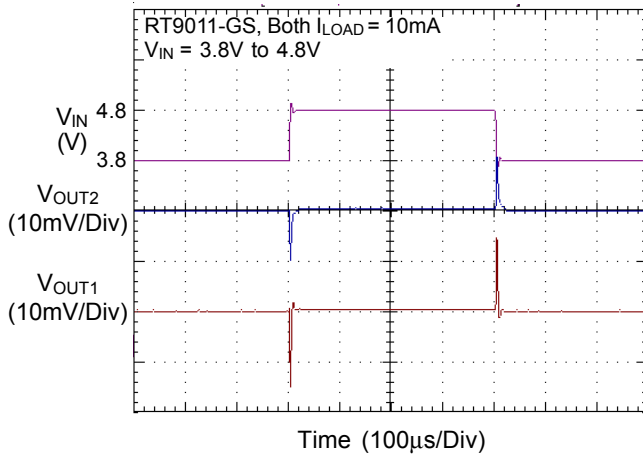
Note 5. The dropout voltage is defined as V_{IN} - V_{OUT}, which is measured when V_{OUT} is V_{OUT(NORMAL)} - 100mV.

Note 6. It is guaranteed by design.

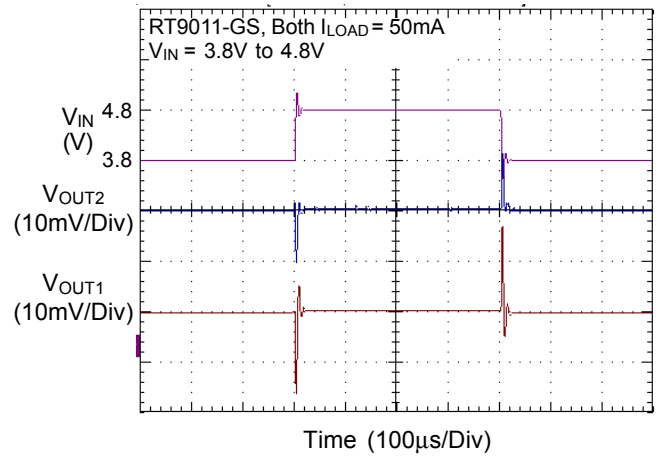
Typical Operating Characteristics



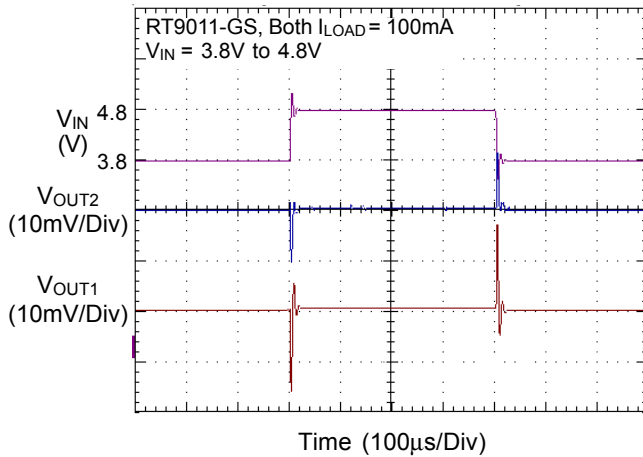
Line Transient Response



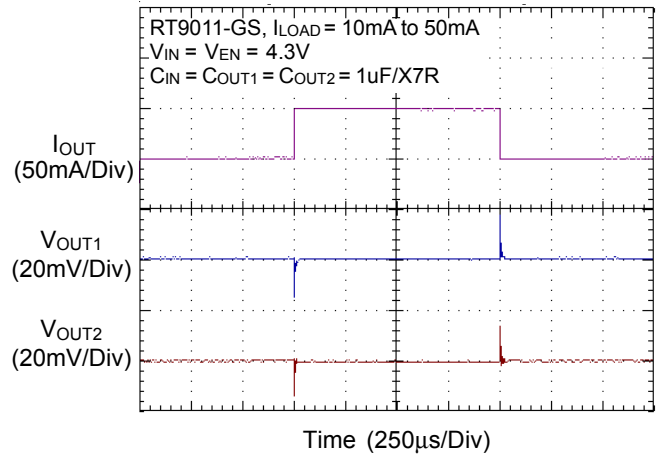
Line Transient Response



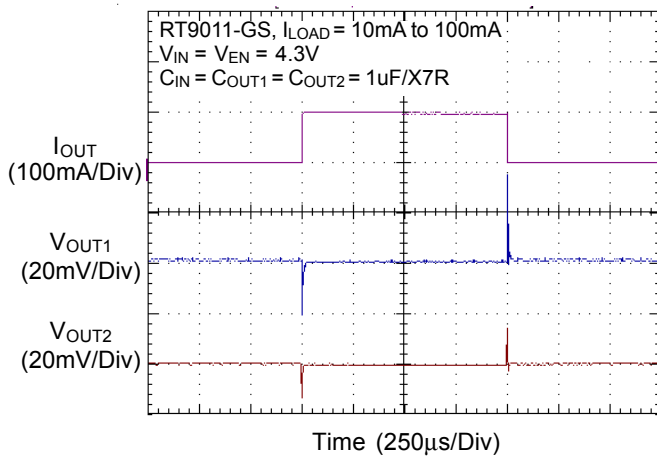
Line Transient Response



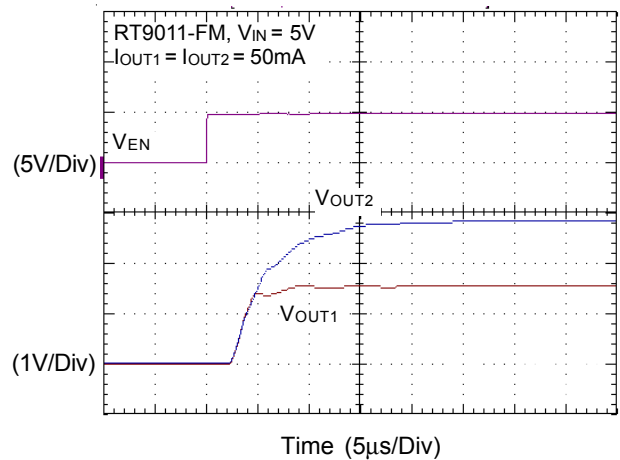
Load Transient Response



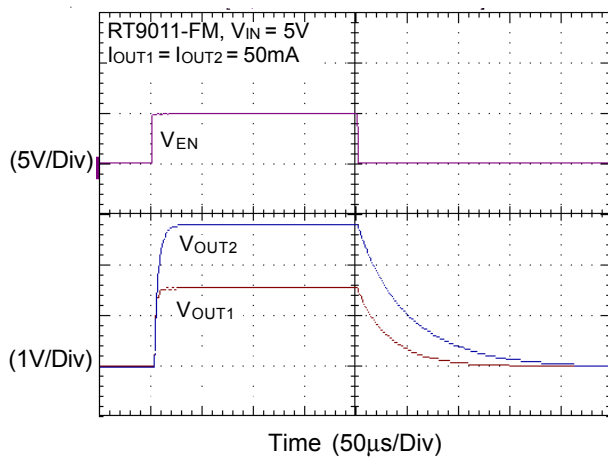
Load Transient Response



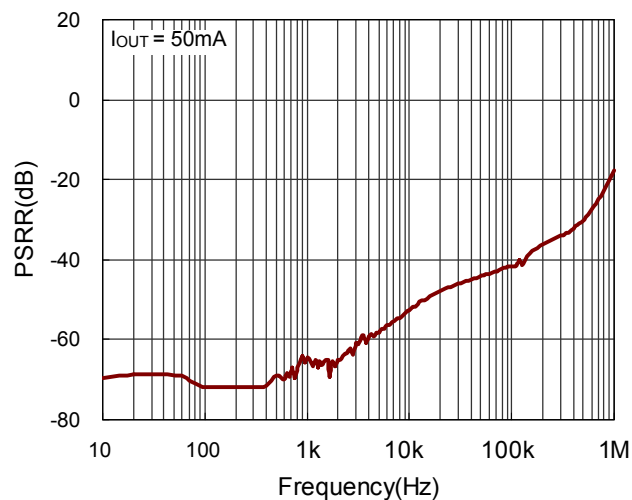
Start Up



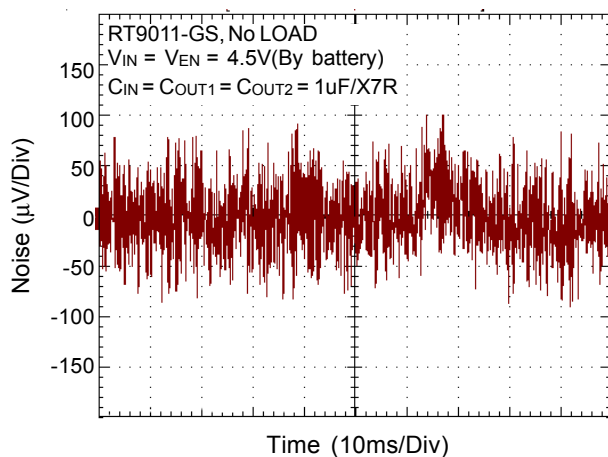
EN Pin Shutdown Response



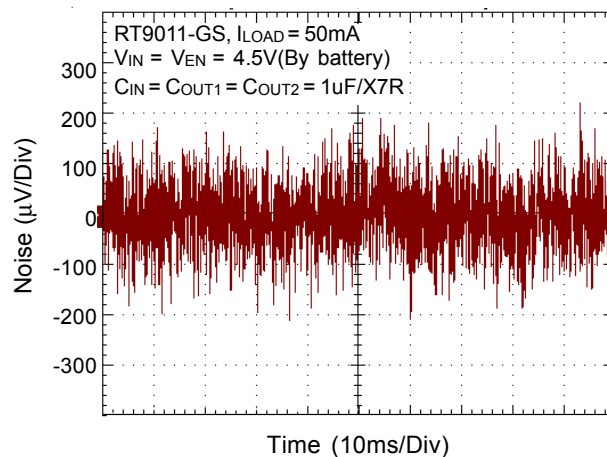
PSRR



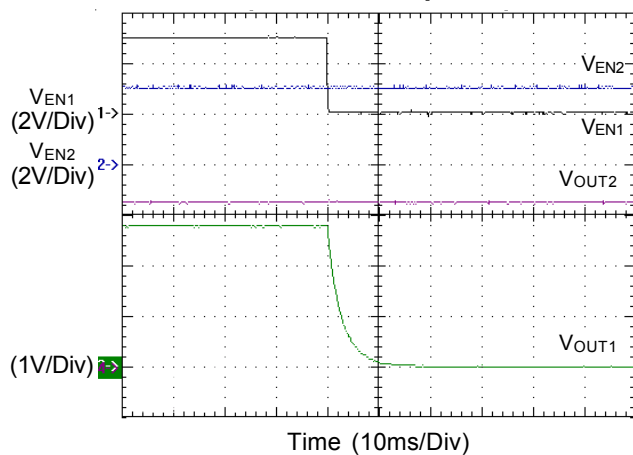
Noise



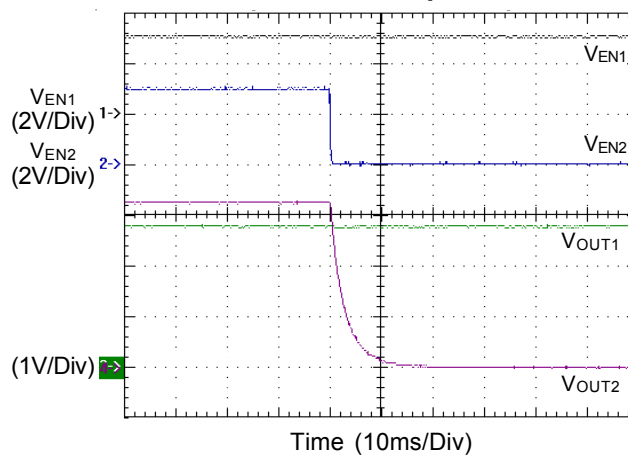
Noise



EN1 Pin Response



EN2 Pin Response



Applications Information

Like any low-dropout regulator, the external capacitors used with the RT9011 must be carefully selected for regulator stability and performance. Using a capacitor whose value is $> 1\mu\text{F}$ on the RT9011 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9011 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least $1\mu\text{F}$ with ESR is $> 20\text{m}\Omega$ on the RT9011 output ensures stability. The RT9011 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1. shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the RT9011 and returned to a clean analog ground.

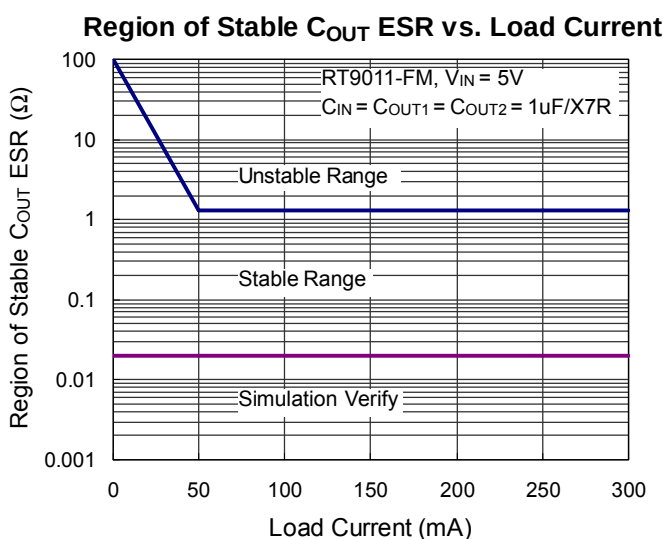


Figure 1. Stable Cout ESR Range

Thermal Considerations

Thermal protection limits power dissipation in RT9011. When the operation junction temperature exceeds 170°C , the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turns on again after the junction temperature cools by 40°C . RT9011 lowers its OTP trip level from 170°C to 110°C when output short circuit occurs ($V_{OUT} < 0.4\text{V}$) as shown in Figure 2. It limits IC case temperature under 100°C and provides maximum safety to customer while output short circuit occurring.

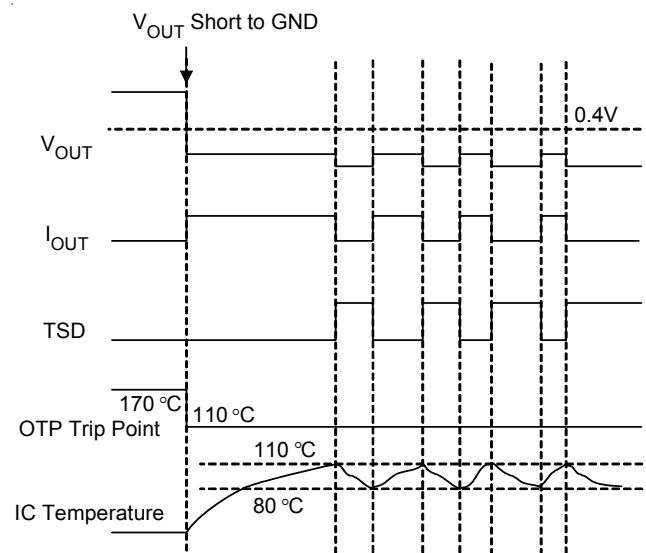


Figure 2. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C . The power dissipation definition in device is :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9011, the maximum junction temperature is 125°C. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for TSOT-23-6 is 220°C/W, WDFN-8L 2x2 is 165°C/W, WDFN-10L 3x3 is 108°C/W, WDFN-8L 3x3 is 108°C/W and WDFN-8L 1.6x1.6 is 175°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated by following formula :

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (220^\circ\text{C/W}) = 0.455\text{W for TSOT-23-6 packages}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (165^\circ\text{C/W}) = 0.606\text{W for WDFN-8L 2x2 packages}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (108^\circ\text{C/W}) = 0.926\text{W for WDFN-10L 3x3 packages}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (108^\circ\text{C/W}) = 0.926\text{W for WDFN-8L 3x3 packages}$$

$$P_{D(\text{MAX})} = (125^\circ\text{C} - 25^\circ\text{C}) / (175^\circ\text{C/W}) = 0.571\text{W for WDFN-6L 1.6x1.6 packages}$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(\text{MAX})}$ and thermal resistance θ_{JA} . For RT9011 packages, the Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

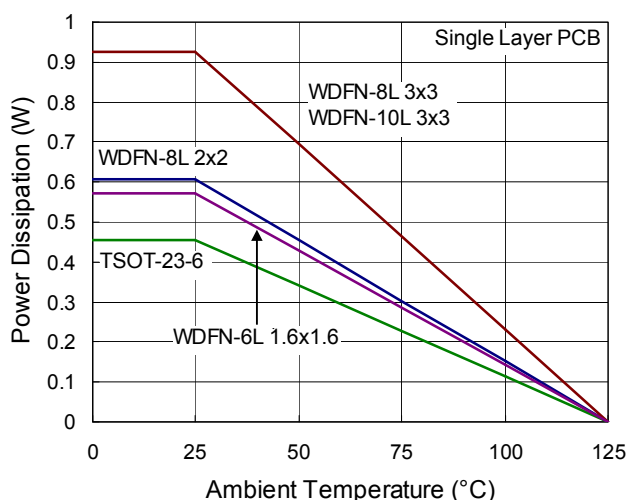
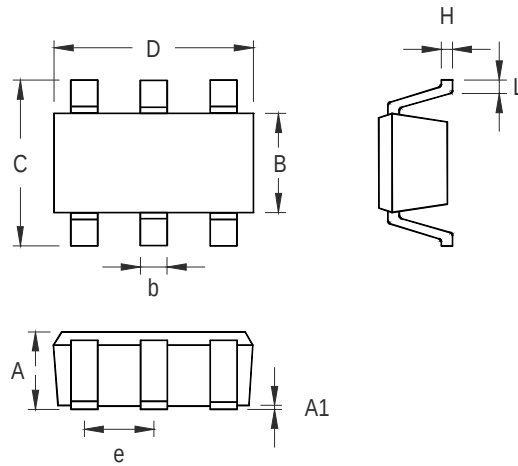


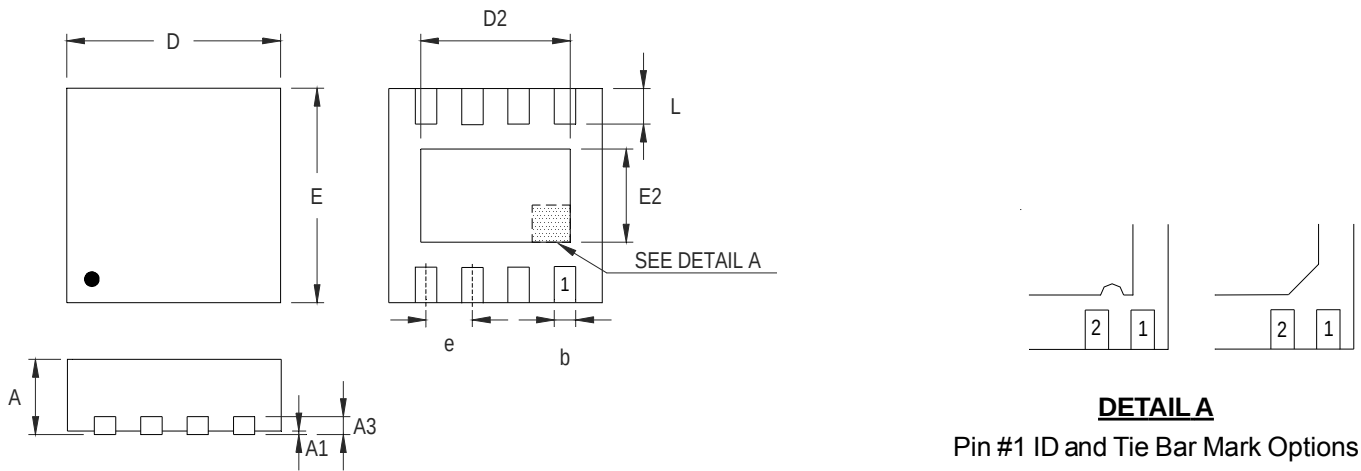
Figure 3. Derating Curves for RT9011 Packages

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.300	0.559	0.012	0.022
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-6 Surface Mount Package



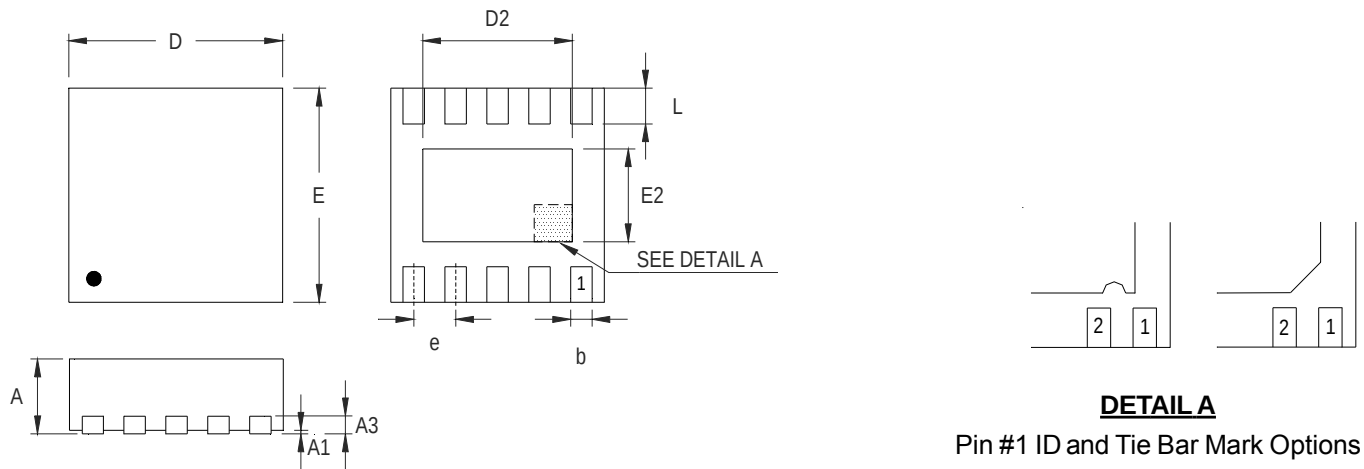
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.950	2.050	0.077	0.081
D2	1.000	1.250	0.039	0.049
E	1.950	2.050	0.077	0.081
E2	0.400	0.650	0.016	0.026
e	0.500		0.020	
L	0.300	0.400	0.012	0.016

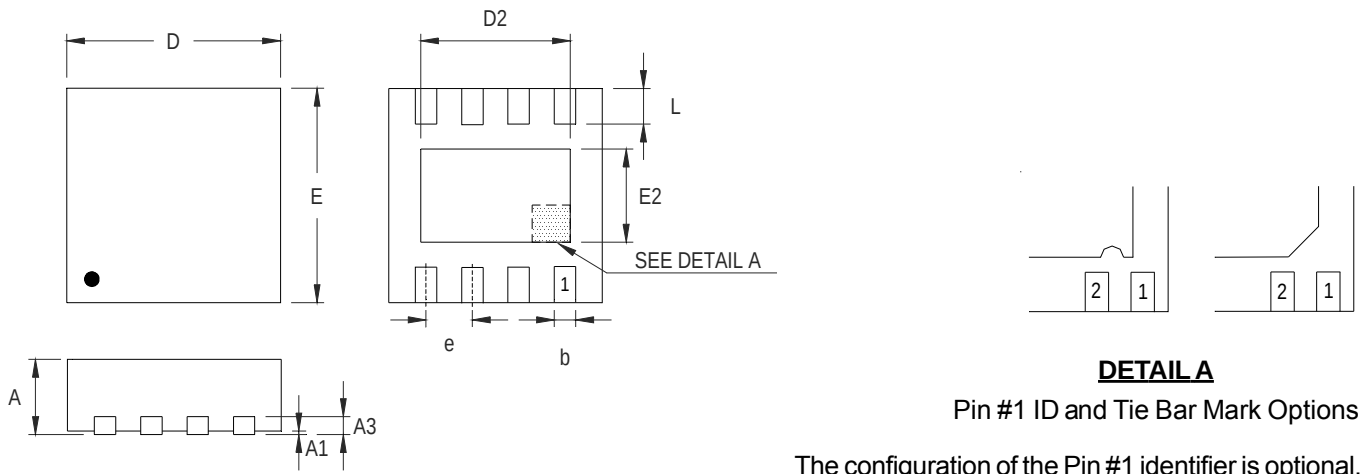
W-Type 8L DFN 2x2 Package



Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

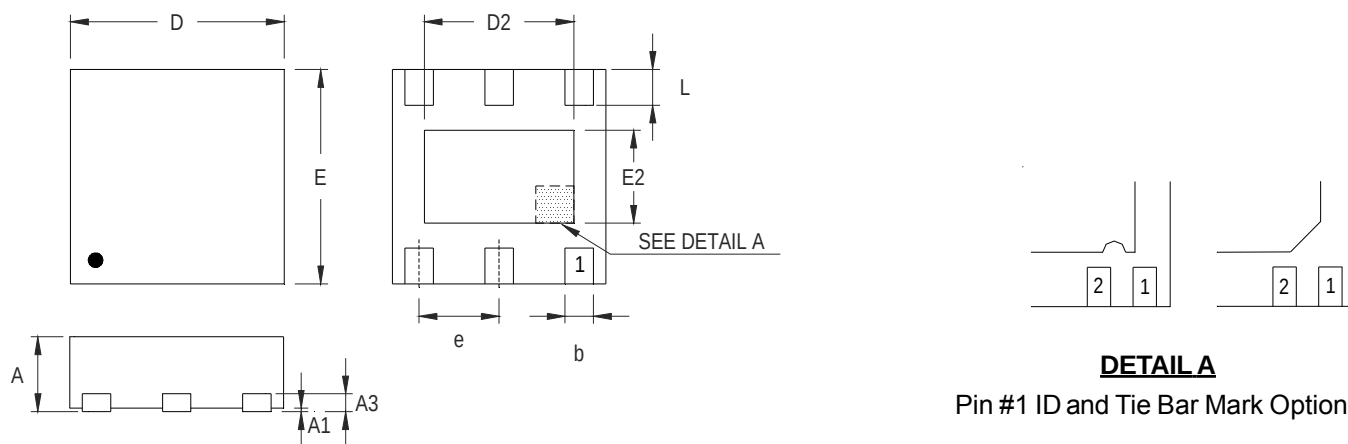
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	2.950	3.050	0.116	0.120
D2	2.100	2.350	0.083	0.093
E	2.950	3.050	0.116	0.120
E2	1.350	1.600	0.053	0.063
e	0.650		0.026	
L	0.425	0.525	0.017	0.021

W-Type 8L DFN 3x3 Package



DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.550	1.650	0.061	0.065
D2	0.950	1.050	0.037	0.041
E	1.550	1.650	0.061	0.065
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.190	0.290	0.007	0.011

W-Type 6L DFN 1.6x1.6 Package

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