# **Absolute Maximum Rating**

Rating	Symbol	Value	Units
Peak Pulse Current ( $t_p = 8/20\mu s$ )	I <sub>PP</sub>	4.5	A
ESD per IEC 61000-4-2 (Air) <sup>(1)</sup> ESD per IEC 61000-4-2 (Contact) <sup>(1)</sup>	V <sub>ESD</sub>	±20 ±17	kV
Operating Temperature	T <sub>J</sub>	-40 to +125	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	оС

# **Electrical Characteristics (T=25°C unless otherwise specified)**

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Reverse Stand-Off Voltage	V <sub>RWM</sub>	Any I/O to GND				3.3	V
Reverse Breakdown Voltage	V <sub>BR</sub>	$I_{BR} = 10\mu A$		7	8	9	V
Poverse Leakage Current	V <sub>RWM</sub> = 3.3V	T = 25°C		0.01	0.05	μΑ	
Reverse reakage Chileni	Any I/O to GND	T = 125°C			0.150		
Clamping Voltage V <sub>C</sub>	\	tp = 8/20µs Any I/O to GND	$I_{pp} = 1A$		2.5	3.5	- V
	V <sub>C</sub>		I <sub>pp</sub> = 4.5A		3.5	4.5	
ESD Clamping Voltage <sup>2</sup> V <sub>C</sub>	V	t 0.3/100	I <sub>pp</sub> = 16A		5.5		V
	V <sub>C</sub>	tp = 0.2/100ns	I <sub>pp</sub> = -16A		-3		
Dynamic Resistance (positive) <sup>2,3</sup>	R <sub>DYN</sub>	tp = 0.2/100ns			0.15		Ω
Dynamic Resistance (negative) <sup>2,3</sup>	R <sub>DYN</sub>	tp = 0.2/100ns			0.14		12
Junction Capacitance	C <sub>J</sub>	$V_R = 0V$ , $f = 1MHz$ , Any I/O to GND			0.60	0.65	nE
		$V_R = 0V, f = 1MHz,$	Between I/O pins		0.30	0.40	pF

### Notes

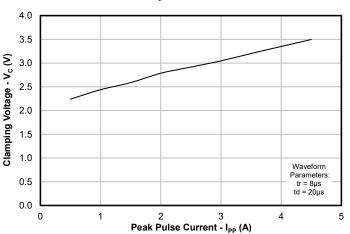
<sup>1)</sup> Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.

<sup>2)</sup> Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns,  $I_{TLP}$  and  $V_{TLP}$  averaging window: t1 = 70ns to t2 = 90ns.

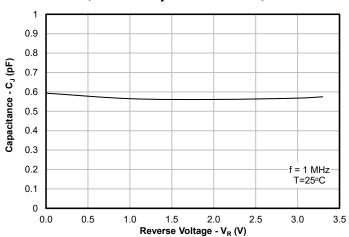
<sup>3)</sup> Dynamic resistance calculated from  $\rm I_{\rm TLP} = 4A$  to  $\rm I_{\rm TLP} = 16A$ 

# **Typical Characteristics**

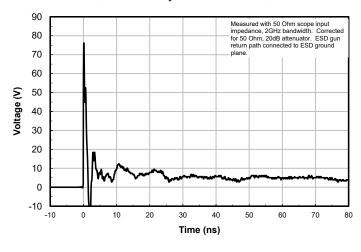
# Clamping Voltage vs. Peak Pulse Current (Between any I/O and Ground)



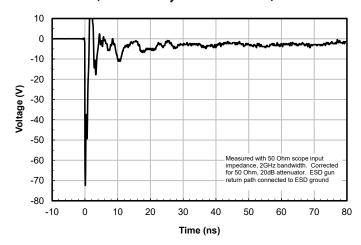
# Junction Capacitance vs. Reverse Voltage (Between any I/O and Ground)



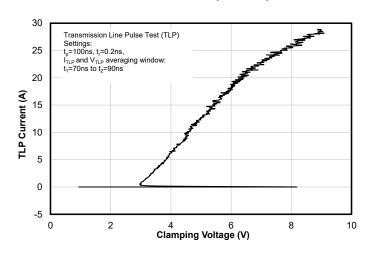
# ESD Clamping (+8kV Contact per IEC 61000-4-2) (Between any I/O and Ground)



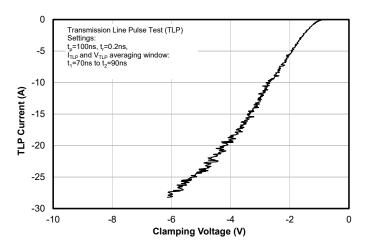
ESD Clamping (-8kV Contact per IEC 61000-4-2) (Between any I/O and Ground)



### **TLP Characteristic (Positive)**



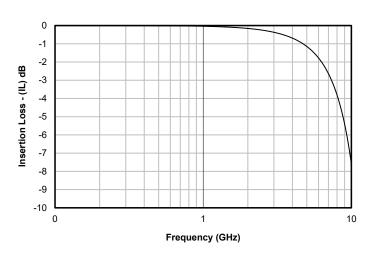
### TLP Characteristic (Negative)



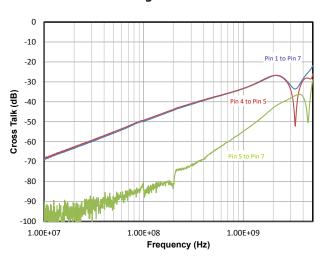
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# **Typical Characteristics (Continued)**

**Insertion Loss - S21** 



## **Analog Crosstalk**



## **Application Information**

### **Protecting USB 3.0 Ports**

RClamp3346P is designed to protect all six USB 3.0 SuperSpeed and high speed differential lines. PCB traces enter and exit each I/O pin and ground is connected at pin 2. For best results, it is recommended that the ground connection be made using a filled via-in-pad. The via should be filled with a conductive paste. This technique saves board space and reduces parasitic inductance in the ground path. Figures 2 and 3 are examples of how to route high speed differential traces through the RClamp3346P. Differential impedance of each pair can easily be controlled for USB 3.0 (85 Ohms +/-15%).

The RClamp3346P should be placed as close to the connector as possible for optimum ESD performance. Internal construction of the RClamp3346P has been optimized to minimize series inductance within the package. This helps to reduce the ESD peak clamping voltage. Dynamic resistance is extremely low (typically 0.15 Ohms) further reducing the ESD clamping voltage.

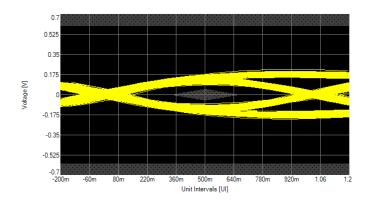


Figure 1 - USB 3.0 Eye Diagram with RClamp3346P

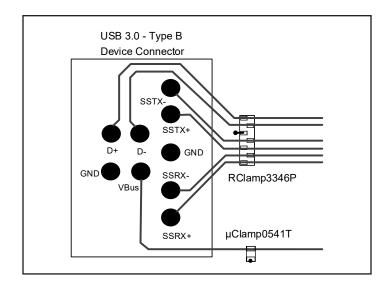


Figure 2 - Example USB 3.0 Layout (Type B Device Connector)

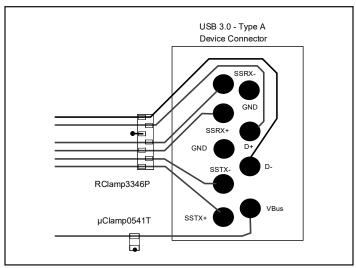


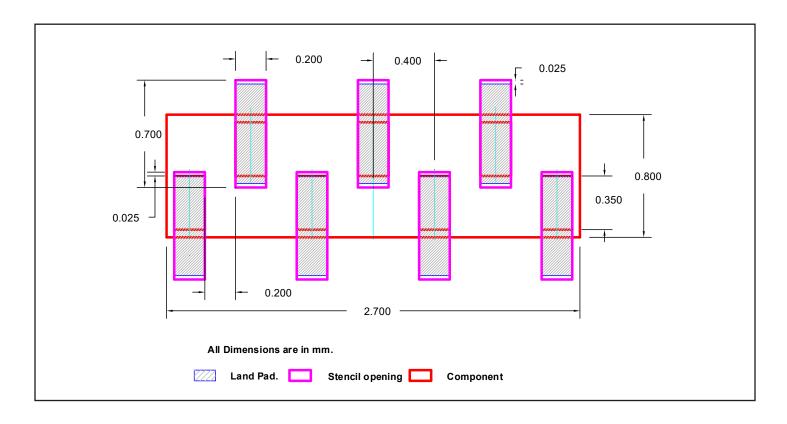
Figure 3 - Example USB 3.0 Layout (Type A Device Connector)

# **Application Information**

## **Assembly Guidelines**

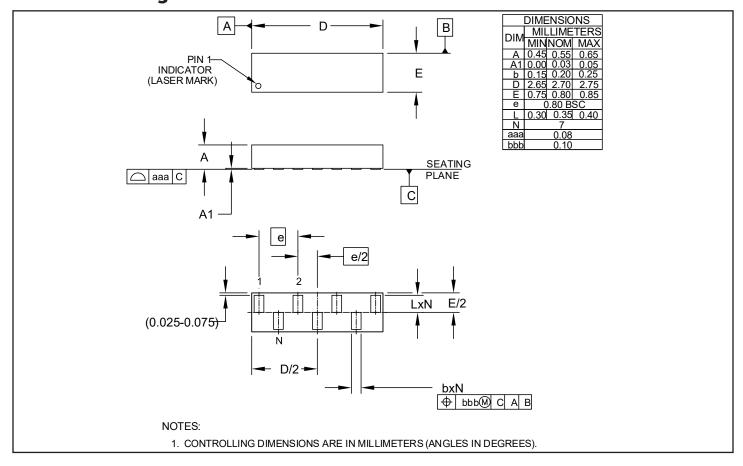
The small size of this device means that some care must be taken during the mounting process to insure reliable solder joint. Semtech's recommended assembly guidelines for mounting this device are shown in the Table 1. Figure 4 details Semtech's recommended aperture. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Assembly Parameter	Recommendation		
Solder Stencil Design	Laser cut, Electro-Polished		
Aperture shape	Rectangular with rounded corners		
Solder Stencil Thickness	0.100 mm (0.004")		
Solder Paste Type	Type 4 size sphere or smaller		
Solder Reflow Profile	Per JEDEC J-STD-020		
PCB Solder Pad Design	Non-Solder mask defined		
PCB Pad Finish	OSP OR NiAu		

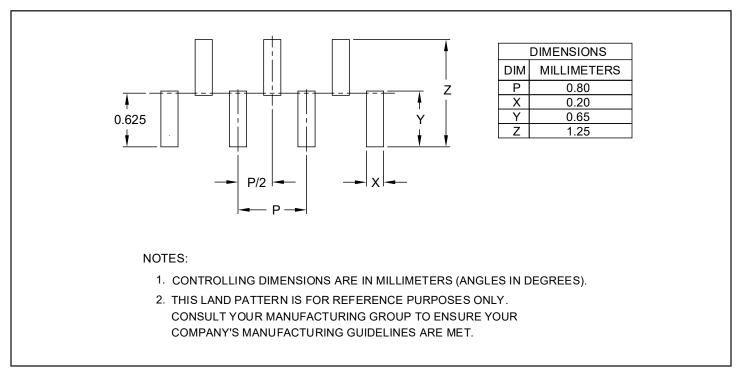


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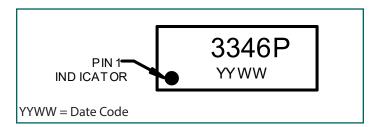
## **Outline Drawing - SGP2708N7**



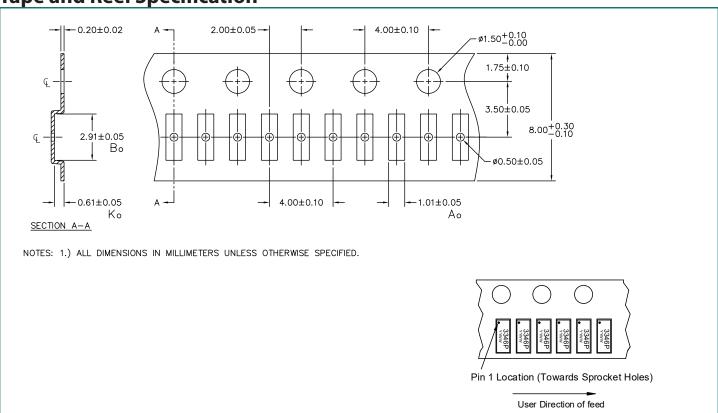
## Land Pattern - SGP2708N7



# **Marking Code**



**Tape and Reel Specification** 



**Ordering Information** 

Part Number	Qty per Reel	Reel Size
RClamp3346P.TNT	10,000	7"

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