

Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Current ($t_p = 8/20\mu s$)	I_{PP}	4.5	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V_{ESD}	± 20 ± 17	kV
Operating Temperature	T_J	-40 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

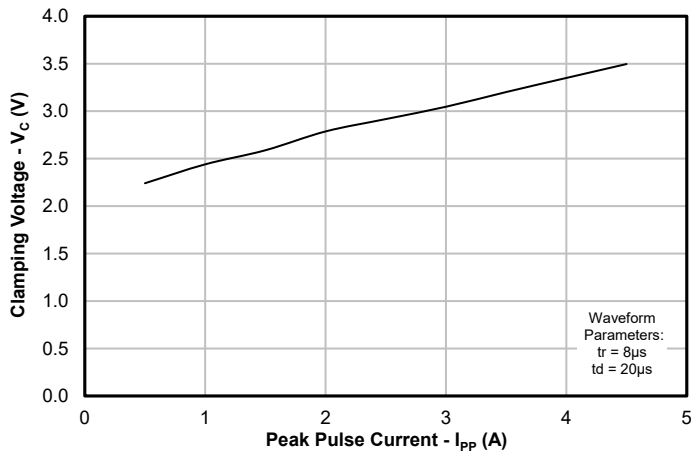
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	Any I/O to GND			3.3	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 10\mu A$	7	8	9	V
Reverse Leakage Current	I_R	$V_{RWM} = 3.3V$ Any I/O to GND	$T = 25^\circ C$	0.01	0.05	μA
			$T = 125^\circ C$		0.150	
Clamping Voltage	V_C	$t_p = 8/20\mu s$ Any I/O to GND	$I_{PP} = 1A$	2.5	3.5	V
			$I_{PP} = 4.5A$	3.5	4.5	
ESD Clamping Voltage ²	V_C	$t_p = 0.2/100ns$	$I_{PP} = 16A$	5.5		V
			$I_{PP} = -16A$	-3		
Dynamic Resistance (positive) ^{2,3}	R_{DYN}	$t_p = 0.2/100ns$		0.15		Ω
Dynamic Resistance (negative) ^{2,3}	R_{DYN}	$t_p = 0.2/100ns$		0.14		
Junction Capacitance	C_J	$V_R = 0V, f = 1MHz, \text{Any I/O to GND}$		0.60	0.65	pF
		$V_R = 0V, f = 1MHz, \text{Between I/O pins}$		0.30	0.40	

Notes

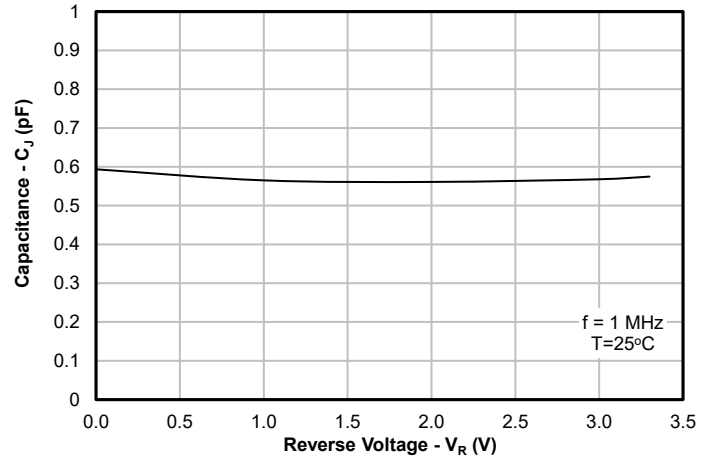
- 1) Measured with a 20dB attenuator, 50 Ohm scope input impedance, 2GHz bandwidth. ESD gun return path connected to ESD ground plane.
- 2) Transmission Line Pulse Test (TLP) Settings: $t_p = 100ns$, $t_r = 0.2ns$, I_{TLP} and V_{TLP} averaging window: $t_1 = 70ns$ to $t_2 = 90ns$.
- 3) Dynamic resistance calculated from $I_{TLP} = 4A$ to $I_{TLP} = 16A$

Typical Characteristics

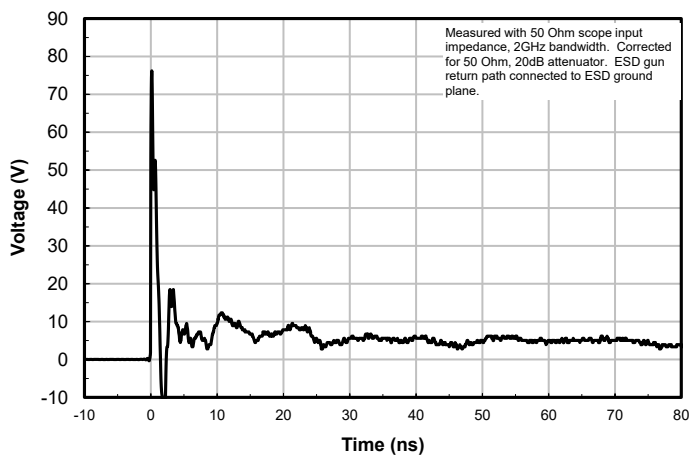
**Clamping Voltage vs. Peak Pulse Current
(Between any I/O and Ground)**



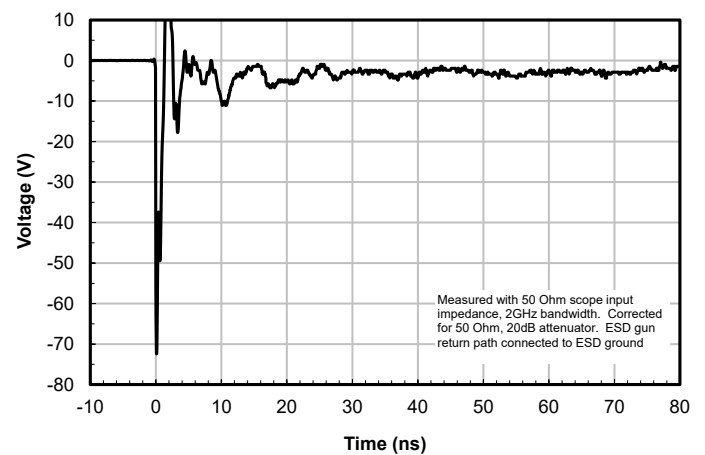
**Junction Capacitance vs. Reverse Voltage
(Between any I/O and Ground)**



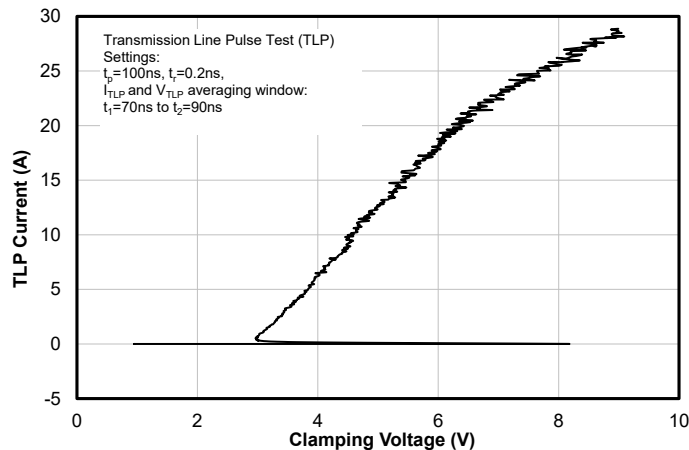
**ESD Clamping (+8kV Contact per IEC 61000-4-2)
(Between any I/O and Ground)**



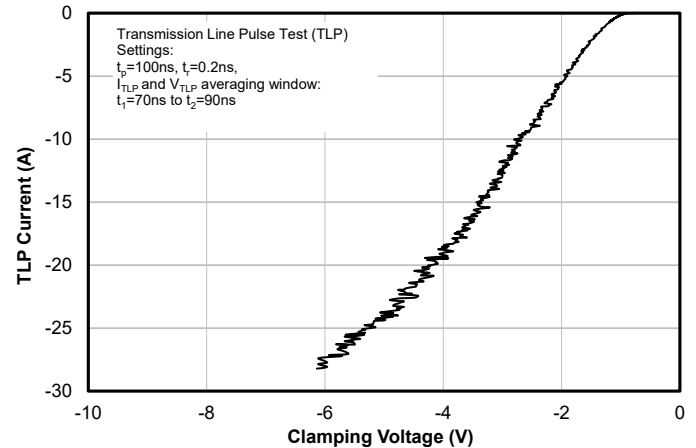
**ESD Clamping (-8kV Contact per IEC 61000-4-2)
(Between any I/O and Ground)**



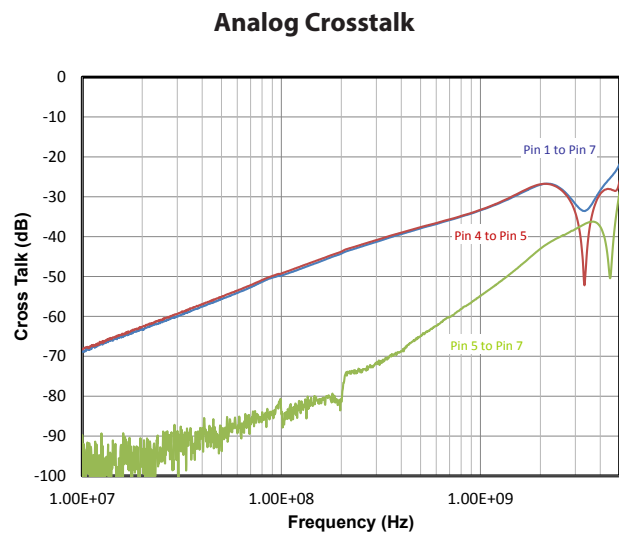
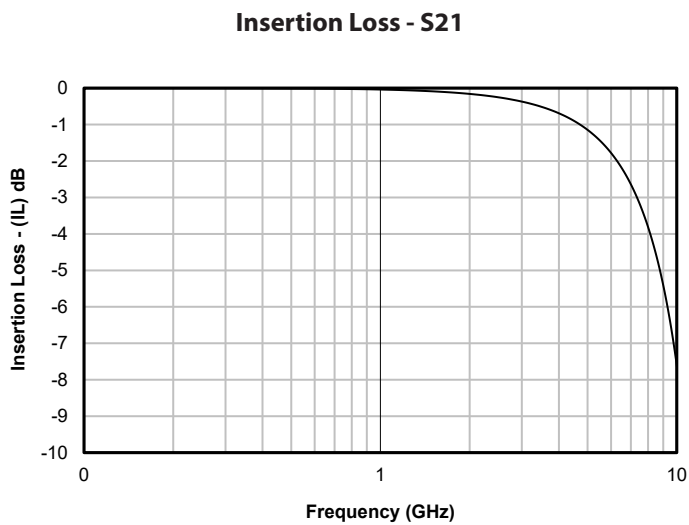
TLP Characteristic (Positive)



TLP Characteristic (Negative)



Typical Characteristics (Continued)



Application Information

Protecting USB 3.0 Ports

RClamp3346P is designed to protect all six USB 3.0 SuperSpeed and high speed differential lines. PCB traces enter and exit each I/O pin and ground is connected at pin 2. For best results, it is recommended that the ground connection be made using a filled via-in-pad. The via should be filled with a conductive paste. This technique saves board space and reduces parasitic inductance in the ground path. Figures 2 and 3 are examples of how to route high speed differential traces through the RClamp3346P. Differential impedance of each pair can easily be controlled for USB 3.0 (85 Ohms +/- 15%).

The RClamp3346P should be placed as close to the connector as possible for optimum ESD performance. Internal construction of the RClamp3346P has been optimized to minimize series inductance within the package. This helps to reduce the ESD peak clamping voltage. Dynamic resistance is extremely low (typically 0.15 Ohms) further reducing the ESD clamping voltage.

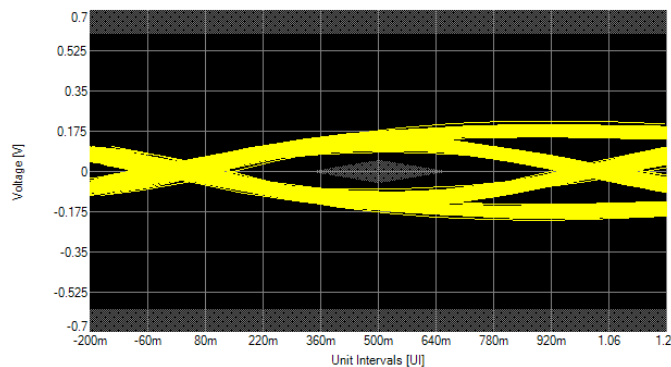


Figure 1 - USB 3.0 Eye Diagram with RClamp3346P

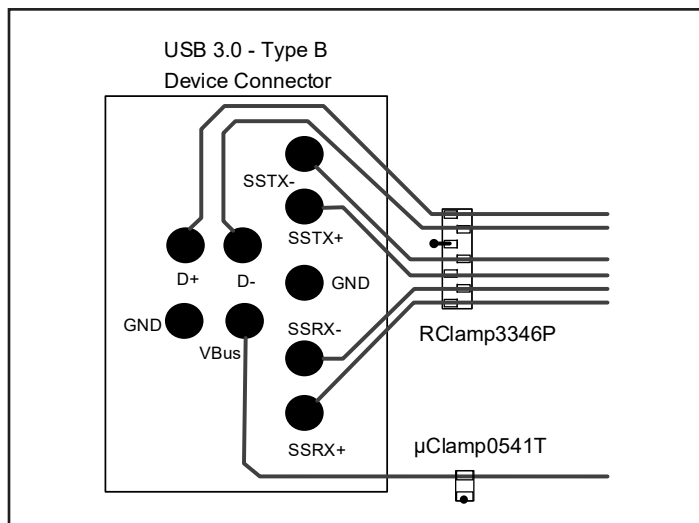


Figure 2 - Example USB 3.0 Layout
(Type B Device Connector)

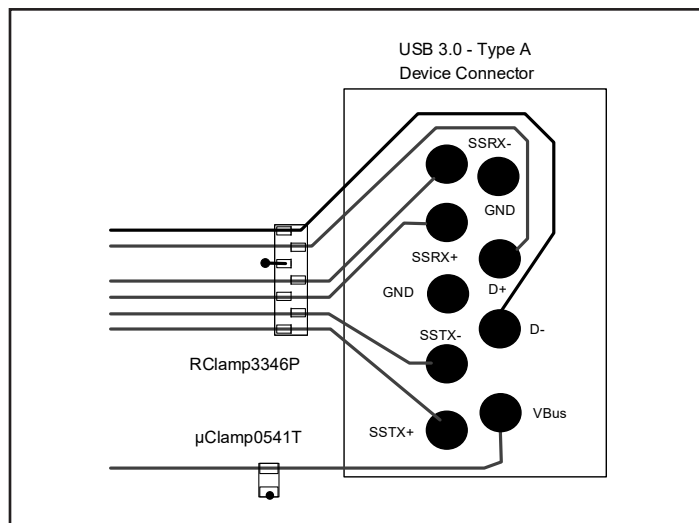
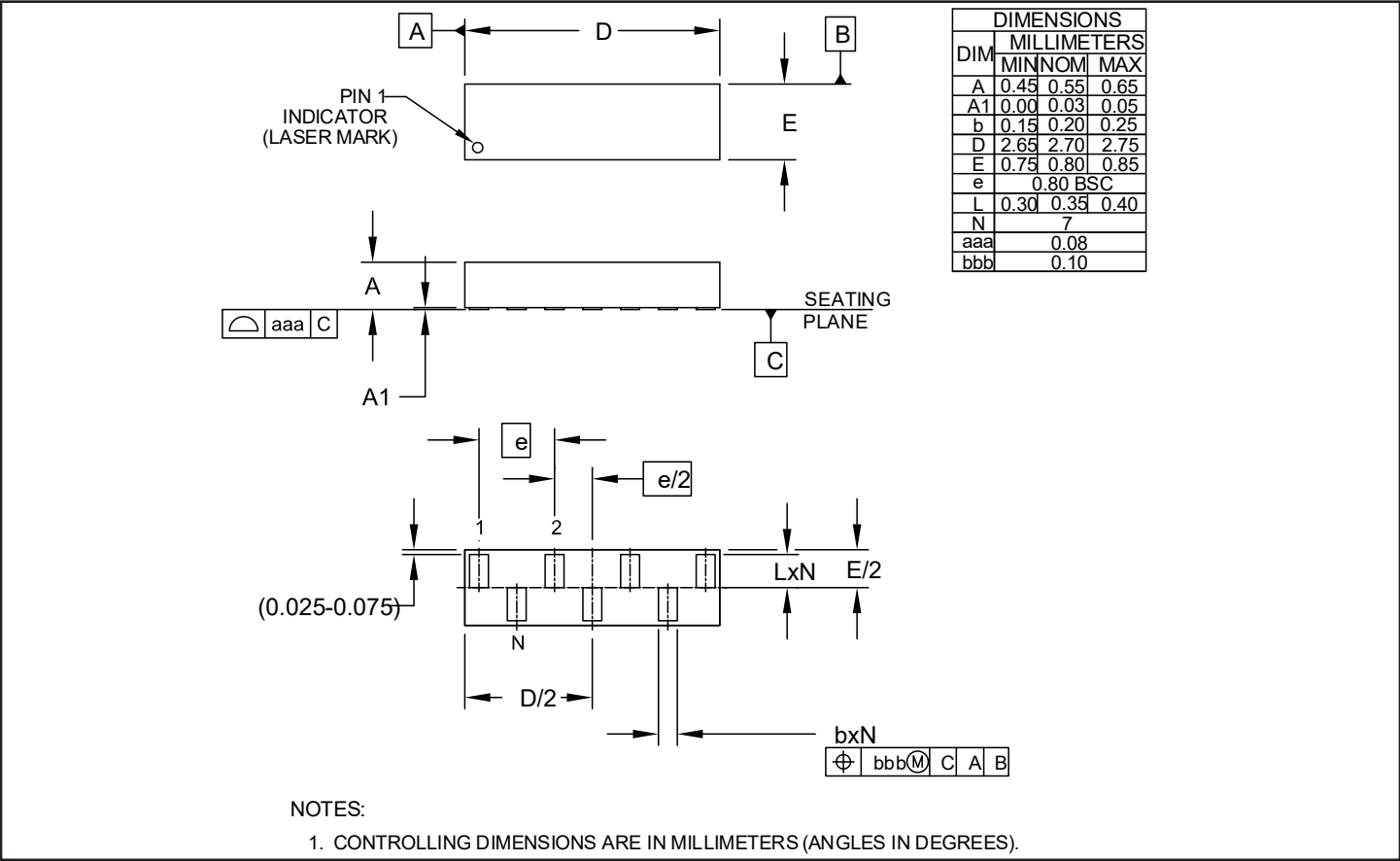
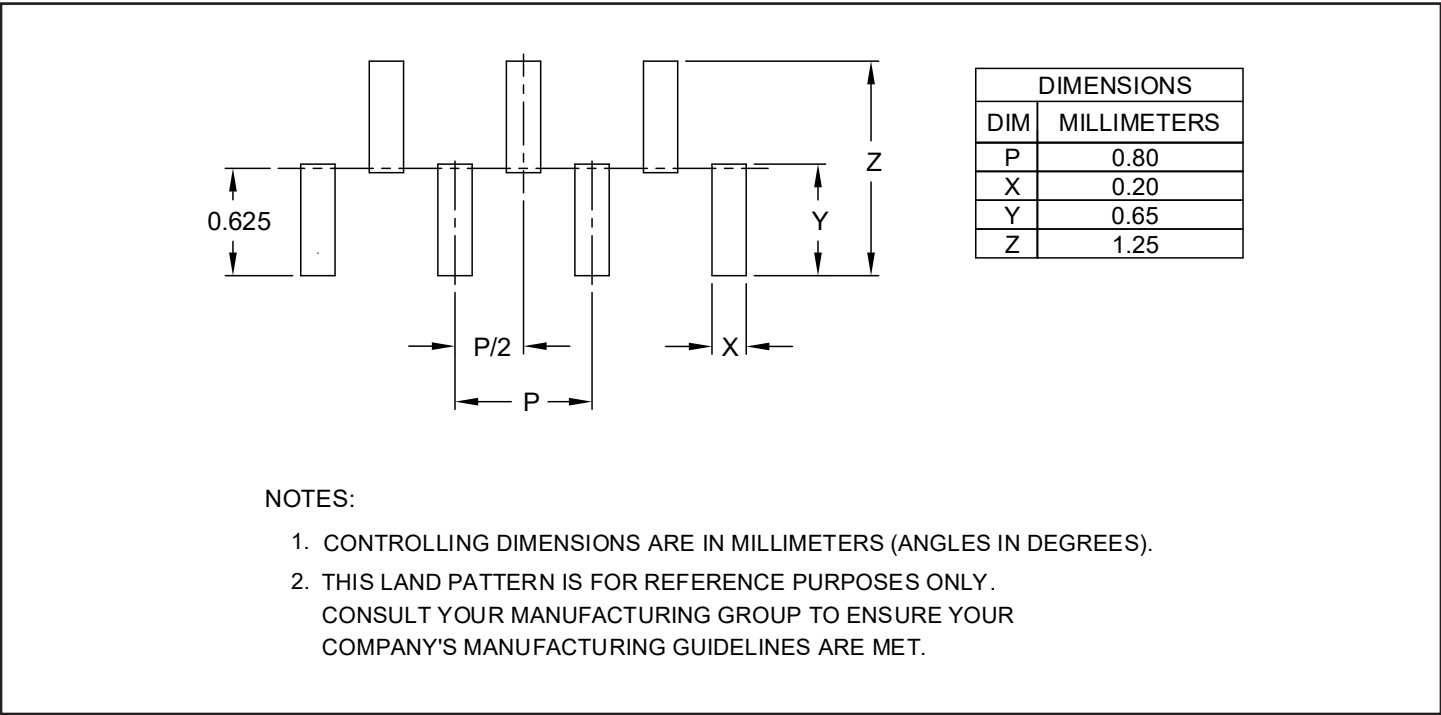


Figure 3 - Example USB 3.0 Layout
(Type A Device Connector)

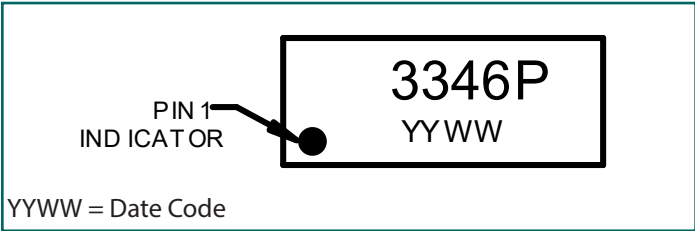
Outline Drawing - SGP2708N7



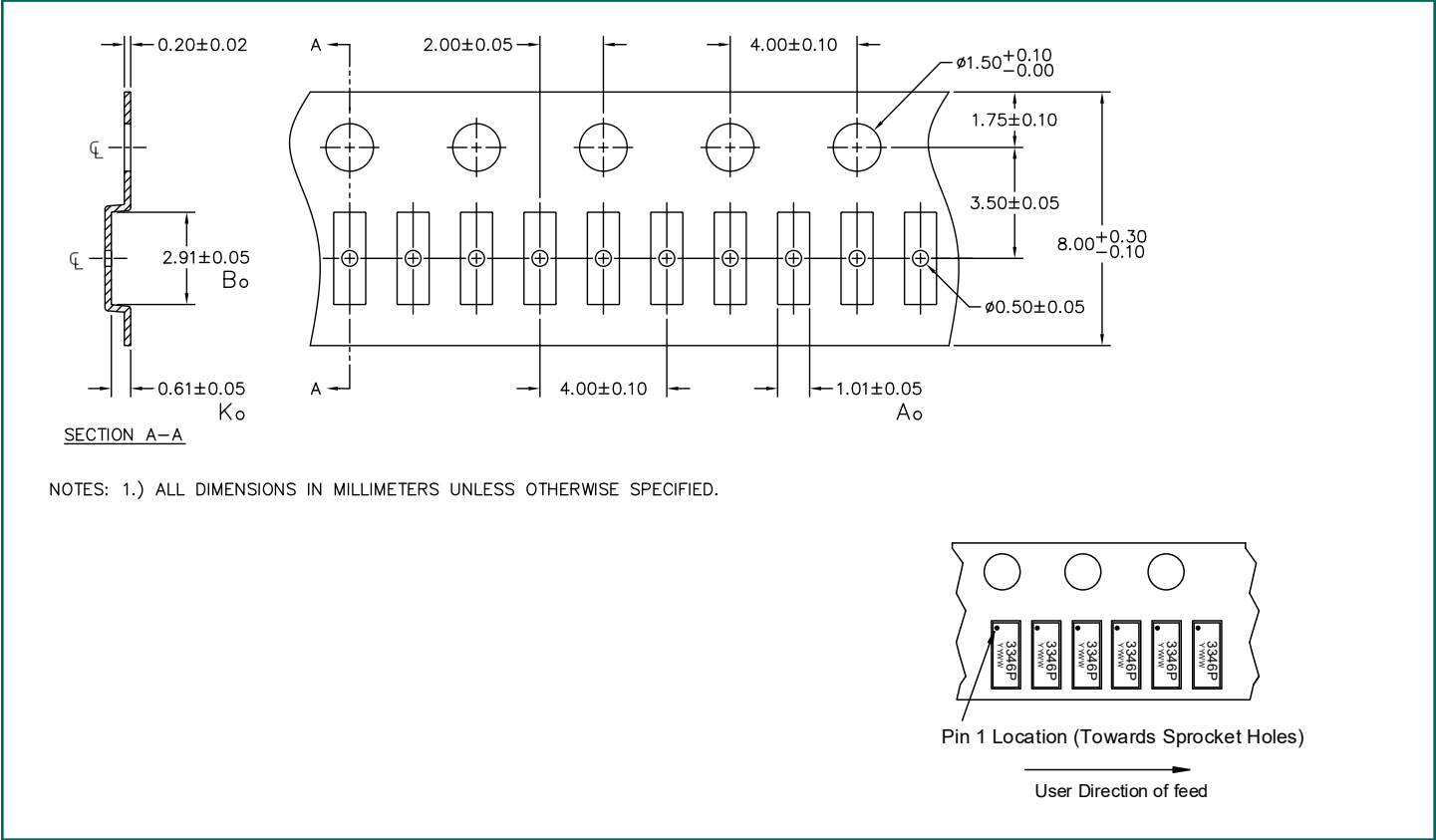
Land Pattern - SGP2708N7



Marking Code



Tape and Reel Specification





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