

Pin Description

PT7M6832- PT7M6837

PT7M6833 SOT23-3 SC70-3	PT7M6832/ PT7M6834 SOT23-3 SC70-3	PT7M6836	PT7M6835/ PT7M6837	Name	Description
1	1	1	1	GND	Ground
-	2	-	4	$\overline{\text{RESET}}$	Reset Output, Open-Drain or Push-Pull, Active-Low. /RESET changes from HIGH to LOW when Vcc drops below the selected reset threshold or /MR is pulled low. /RESET remains LOW for the reset timeout period after Vcc exceeds the device reset threshold and /MR is released high.
2	-	4	-	RESET	Reset Output, Push-Pull, Active-High. RESET changes from LOW to HIGH when the Vcc input drops below the selected reset threshold or /MR is pulled low. RESET remains HIGH for the reset timeout period after Vcc exceeds the device reset threshold and /MR is released high.
-	-	3	3	$\overline{\text{MR}}$	Active-Low Manual Reset Input. Internal 20k Ω pull-up to Vcc. Pull LOW to force a reset. Reset remains active as long as MR is LOW and for the reset timeout period after MR goes HIGH. Leave unconnected or connect to Vcc if unused
3	3	2	2	VCC	Supply Voltage and Monitored Supply

PT7M6838- PT7M6840

PT7M6839	PT7M6838/ PT7M6840	Name	Description
3	3	RESET-IN	Adjustable Reset Threshold Input. High-impedance input for reset comparator. Connect this pin to an external resistive-divider network to set the reset threshold voltage; the typical threshold is 0.44V. Reset is asserted when RESET-IN is below the threshold (VCC is not monitored).
2	2	Vcc	Supply Voltage (1.3V to 5.5V)
1	1	GND	Ground
4	-	RESET	Reset Output, Push-Pull, Active-High. RESET changes from LOW to HIGH when the RESET-IN input drops below the typical reset threshold (0.44V). RESET remains HIGH for the reset timeout period after RESET-IN exceeds the reset threshold.
-	4	$\overline{\text{RESET}}$	Reset Output, Open-Drain or Push-Pull, Active-Low. /RESET changes from HIGH to LOW when RESET-IN drops below the typical reset threshold (0.44V). /RESET remains LOW for the reset timeout period after RESET-IN exceeds the reset threshold.

Block Diagram

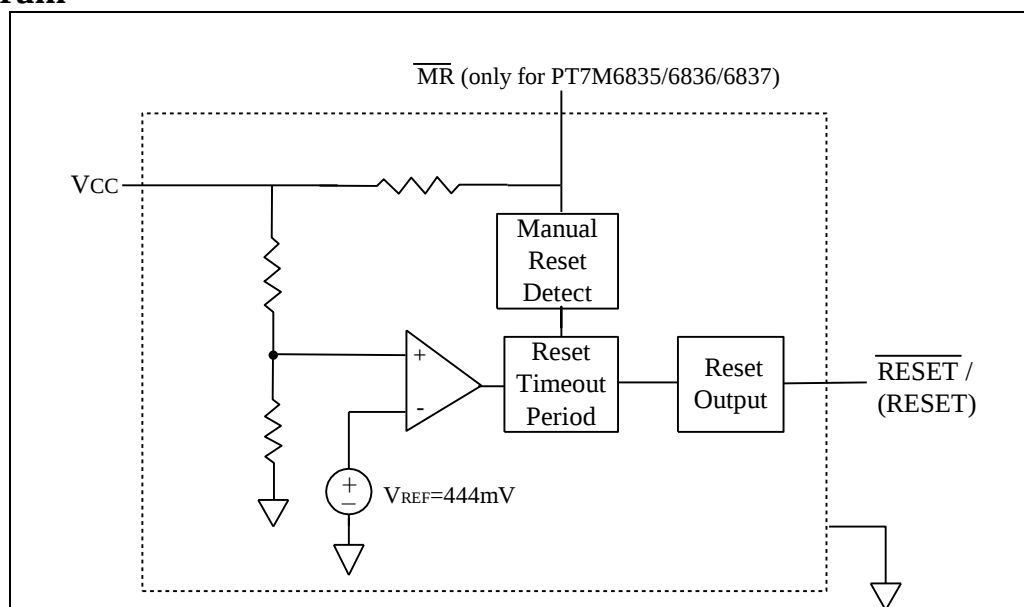


Fig.1 PT7M6832-PT7M6837 Block Diagram

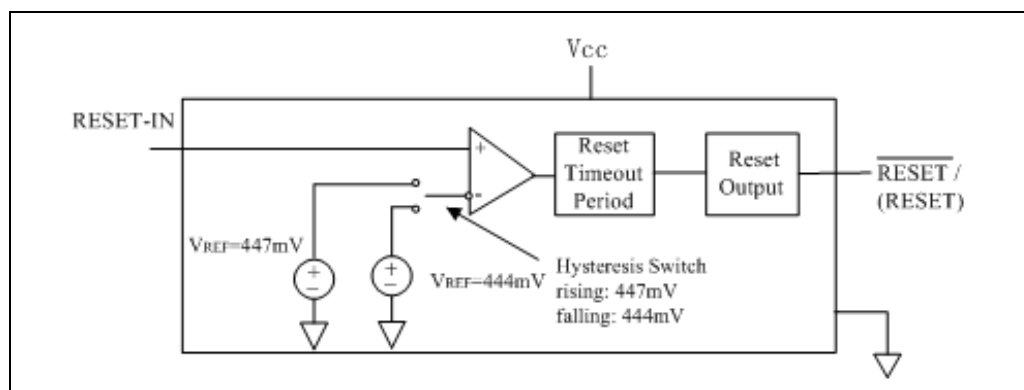


Fig.2 PT7M6838-PT7M6840 Block Diagram

Maximum Ratings

Storage Temperature.....	- 65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (V _{CC} to GND).....	- 0.3V to +6.0V
Open-drain RESET, MR....	- 0.3V to +6.0V
RESET-IN, Push-pull RESET and RESET	-0.3V to +6.0V
DC Input/Output Current	20mA
Power Dissipation.....	245mW

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Electrical Characteristics

(V_{CC} = +0.9V to +5.5V, unless otherwise noted. Typical values are at T_A = +25 °C)

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Reset Active Timeout Period	t _{PD}	D0	-	0.07	-	ms
		D1	1	1.5	2	
		D2	20	30	40	
		D3	140	210	280	
		D4	1120	1680	2240	
V _{CC} or RESET-IN to Reset Delay		V _{CC} falling, step signal from (V _{TH} +100mV) to (V _{TH} -100mV)	-	60	-	µs
Propagation Delay(D0 only)	t _p	V _{CC} rising, step signal from (V _{TH} -100mV) to (V _{TH} +100mV)	-	70	-	µs
Startup Time(D0 only)	-	V _{CC} rising from 0 to 1.1V(t _R <1 µs)	-	150	-	µs
$\overline{\text{MR}}$ Minimum Input Pulse Width	-	$\overline{\text{MR}}$ driven from V _{CC} to 0	2	-	-	µs
$\overline{\text{MR}}$ Glitch Rejection	-	$\overline{\text{MR}}$ driven from V _{CC} to 0	-	100	-	ns
$\overline{\text{MR}}$ to Reset Delay	-	$\overline{\text{MR}}$ driven from V _{CC} to 0	-	500	-	ns

DC Electrical Characteristics

($V_{CC} = +0.9V$ to $+5.5V$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$)

Description	Sym.	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V _{CC}	T _A = -40 ℃ ~+85 ℃, PT7M6832/6835/6838, PT7M6834/6837/6840	0.9	-	5.5	V
		T _A = -40 ℃ ~+85 ℃, PT7M6833/6836/6839	0.85	-	5.5	
		T _A = 0 ℃ ~+85 ℃, PT7M6833/6836/6839	0.75	-	5.5	
		T _A = -40 ℃ ~+85 ℃, PT7M6838/6839/6840	1.5	-	5.5	
Supply Current	I _{CC}	V _{CC} =1.2V, no load , reset not asserted	-	7.5	13	μA
		V _{CC} =1.8V, no load , reset not asserted	-	9	16	
		V _{CC} =3.6V, no load , reset not asserted	-	16	25	
Reset Threshold	V _{TH}	W	1.620	1.665	1.710	V
		V	1.530	1.575	1.620	
		I	1.350	1.388	1.425	
		H (-10 ℃ ~ +85 ℃)	1.275	1.313	1.350	
		G (0 ℃ ~ +85 ℃)	1.080	1.110	1.140	
		F*(0 ℃ ~+85 ℃)	1.020	1.050	1.080	
RESET-IN Threshold	V _{RSTIN}	1.5V<=V _{CC} <=5.5V, RESET-IN falling from high to low(25 ℃)	-2%	444	+2%	
		1.5V<=V _{CC} <=5.5V, RESET-IN rising from low to high(0 ℃ ~85 ℃)	-5%	444	+5%	
Reference voltage temperature coefficient	T _C	Reference voltage temperature coefficient, -40 ℃ ~+85 ℃	-	70	-	ppm/℃
Push-pull $\overline{\text{RESET}}$ Output High Voltage	V _{OH}	V _{CC} >=1.1V, I _{source} =50 μA, reset not asserted	0.8×V _{CC}	-	-	-
		V _{CC} >=1.5V, I _{source} =150 μA, reset not asserted	0.8×V _{CC}	-	-	
		V _{CC} >=1.0V, I _{source} =50 μA, reset asserted	0.8×V _{CC}	-	-	
		V _{CC} >=1.5V, I _{source} =150 μA, reset asserted	0.8×V _{CC}	-	-	
Push-pull $\overline{\text{RESET}}$ Output Low Voltage	V _{OL}	V _{CC} >=1.0V, I _{sink} =80 μA, reset asserted	-	-	0.2×V _{CC}	V
V _{CC} >=1.5V, I _{sink} =200 μA, reset asserted		-	-	0.2×V _{CC}		
Push-pull $\overline{\text{RESET}}$ Output Low Voltage		V _{CC} >=1.1V, I _{sink} =80 μA, reset not asserted	-	-	0.2×V _{CC}	
V _{CC} >=1.5V, I _{sink} =200 μA, reset not asserted		-	-	0.2×V _{CC}		
Open-Drain $\overline{\text{RESET}}$ Output Low Voltage		V _{CC} >=1.0V, I _{sink} =80 μA, reset asserted	-	-	0.15	V
		V _{CC} >=1.5V, I _{sink} =200 μA, reset asserted	-	-	0.2	
$\overline{\text{MR}}$ Input Voltage	V _{IL}	-	-	-	0.3×V _{CC}	V
	V _{IH}	-	0.7×V _{CC}	-	-	
Open-Drain $\overline{\text{RESET}}$ Output Leakage Current	I _{LKG}	V _{CC} > V _{TH} , reset not asserted	-	-	1.0	μA
RESET-IN Leakage Current	I _{RSTIN}	-	-25	-	+25	nA
Reset Threshold Hysteresis	V _{HYS}	-	-	0.75	-	% V _{TH}

Functional Description

Reset Output

The PT7M6832–PT7M6840 assert a reset to prevent code-execution errors during power-up, power-down, or brownout conditions. They also assert a reset signal whenever the V_{CC} supply voltage falls below a preset threshold (PT7M6832–PT7M6837) or RESET-IN falls below the adjustable threshold (PT7M6838–PT7M6840), keeping reset asserted for a fixed timeout delay (Table 2) after V_{CC} or RESET-IN has risen above the reset threshold. The PT7M6832/6835/6838 use a push-pull active-low output, the PT7M6833/6836/6839 have a push-pull active-high output, and the PT7M6834/6837/ 6840 have an open-drain active-low output stage. Connect a pull-up resistor on the PT7M6834/6837/ 6840's RESET output to any supply between 0 and 6V.

Manual Reset Input

Reset remains asserted while $\overline{MR}$ is low, and for a fixed timeout delay after $\overline{MR}$ returns high. This input has an

internal 20kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with CMOS logic level, or with open-drain/collector outputs. To create a manual reset function, connect a normally open momentary switch from $\overline{MR}$ to ground; external debounce circuitry is not required.

RESET-IN

The PT7M6838/6839/6840 features a RESET-IN input for monitoring supply voltages down to 0.44V. An external resistive-divider network can be used to set voltage monitoring thresholds as shown in Fig.3. As the monitored voltage falls, the voltage at RESET-IN decreases and asserts a reset when it falls below the RESET-IN threshold (V_{RSTIN}). The low-leakage current at RESET-IN allows for relatively large-value resistors to be used, which reduce power consumption. For example, for a 0.6V monitored trip level, if R₂ = 200kΩ, then R₁ = 70.3kΩ.

Note: The minimum V_{CC} of 1.3V is required to guarantee the RESET-IN threshold accuracy.

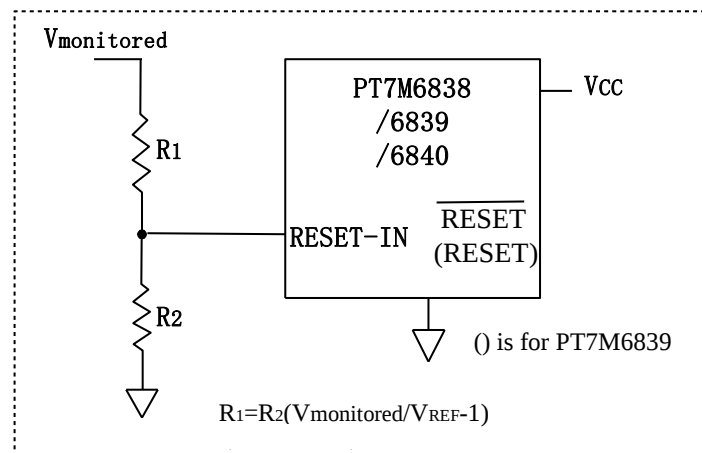


Fig.3 External setting of adjustable threshold

Application Information

Negative-Going VCC Transients

In addition to issuing a reset to the μP during power-up, power-down, and brownout conditions, the PT7M6832–PT7M6840 are relatively immune to short-duration negative-going Vcc transients. A 0.1 μF bypass capacitor mounted as close as possible to the Vcc pin provides additional transient immunity.

Valid Reset Output Down to Vcc = 0

When Vcc falls below 0.9V, the PT7M6832/6835/6838 push-pull RESET output no longer sinks current for it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undetermined voltages. This presents no problem in most applications since most μP and other circuitry are inoperative with Vcc lower than 0.9V. However, in applications where RESET must be valid down to 0, adding a pull-down resistor to RESET causes any stray leakage currents to flow to ground, holding RESET low (Fig.4). R3's value is not critical; 100k Ω is large enough not to load RESET and small enough to pull RESET to ground.

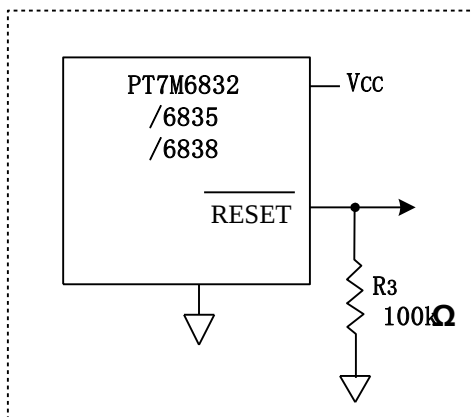


Fig.4 RESET output valid to VCC=0 circuit

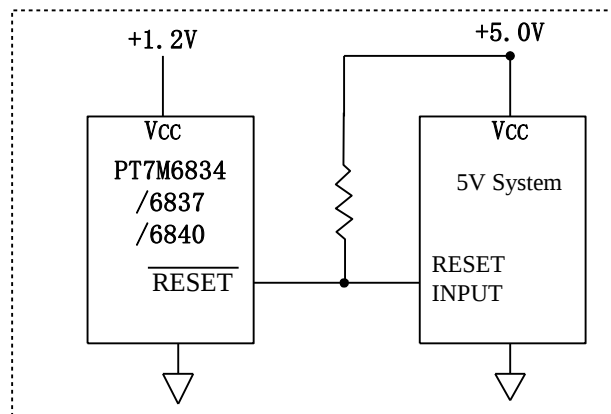


Fig.6 Open-drain Reset output with multiple supplies

A 100k Ω pull-up resistor to Vcc is also recommended for the PT7M6833/PT7M6836/PT7M6839 if RESET is required to remain valid for Vcc < 0.85V.

Interfacing to μPs with Bidirectional Reset Pins

Since the RESET output on the PT7M6834/6837/6840 is open-drain, these devices interface easily with μPs that have bidirectional reset pins. Connecting the μP supervisor's RESET output directly to the μP 's RESET pin with a single pull-up resistor allows either device to assert a reset (Fig.5).

Open-Drain RESET Output with Multiple Supplies

In some systems the open-drain output is used to level-shift from the monitored supply to reset circuitry powered by some other supply (Fig.6).

Note: As the PT7M6834/6837/6840's Vcc decreases, so does the IC's ability to sink current at RESET. Also, with any pull-up, RESET will be pulled high as Vcc declines toward 0. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

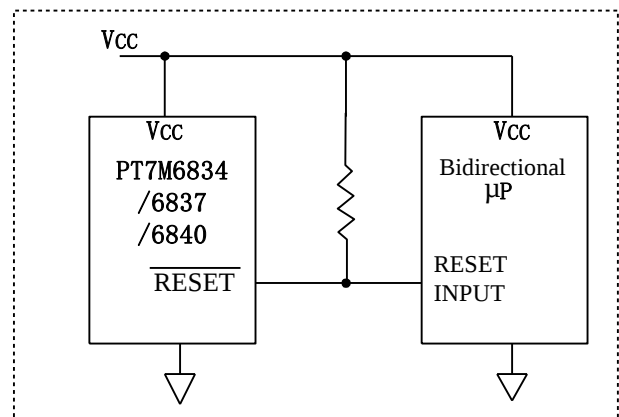
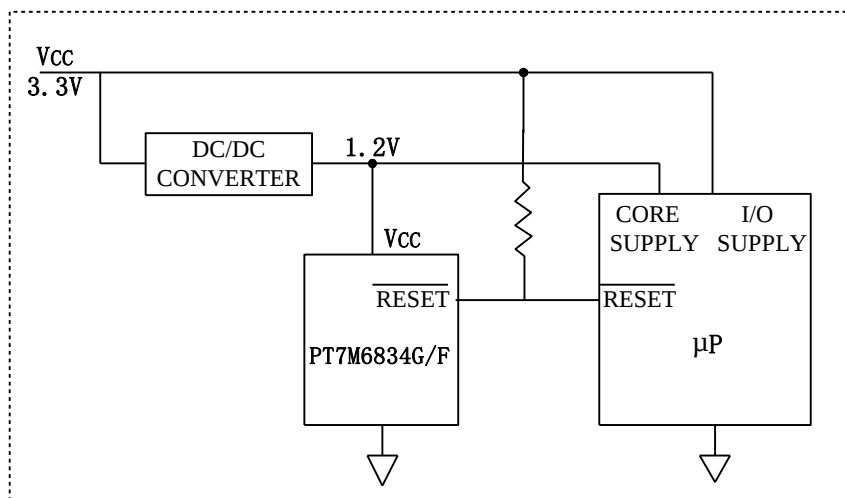


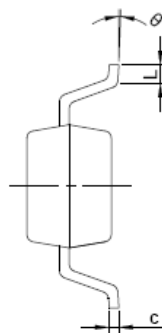
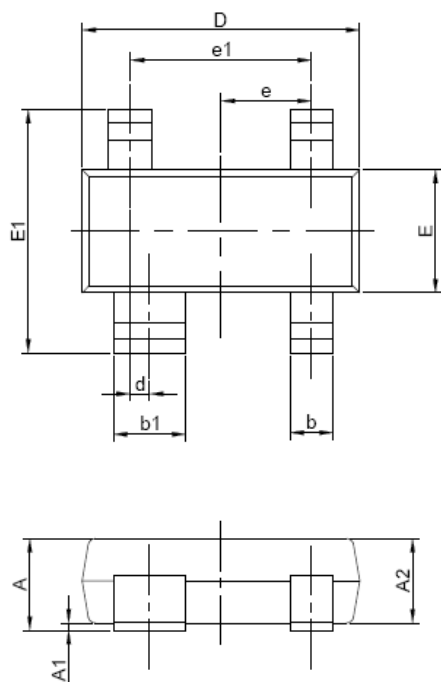
Fig.5 Interfacing to μPs with Bidirectional Reset I/O

Application Circuit



Mechanical Information

TB (SOT143-4L)



PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.90	1.15
A1	0.00	0.10
A2	0.90	1.05
b	0.30	0.50
b1	0.75	0.90
c	0.08	0.15
D	2.80	3.00
d	0.20 TYP	
E	1.20	1.40
E1	2.25	2.55
e	0.95 TYP	
e1	1.80	2.00
L	0.30	0.50
θ	0°	8°

Note:

1. Ref: JEDEC TO-253D



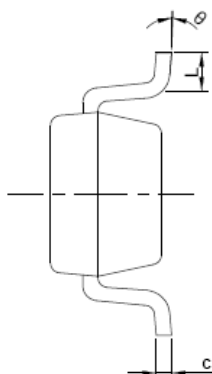
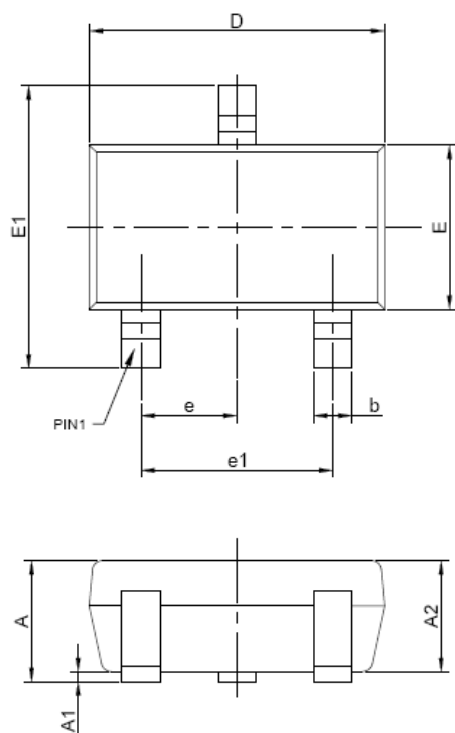
DATE: 06/18/13

DESCRIPTION: 4-Pin, SOT143

PACKAGE CODE: TB (TB4)

DOCUMENT CONTROL#: PD-2146

REVISION: --

TA (SOT23-3L)


PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	1.05	1.25
A1	0.00	0.10
A2	1.05	1.15
b	0.30	0.50
c	0.10	0.20
D	2.82	3.02
E	1.50	1.70
E1	2.65	2.95
e	0.95 BSC	
e1	1.80	2.00
L	0.30	0.80
θ	0°	8°

Note:

1. Ref: JEDEC TO-236H



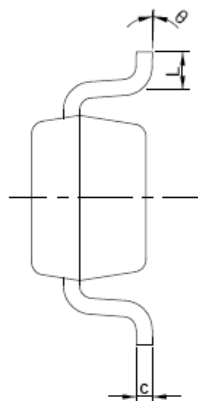
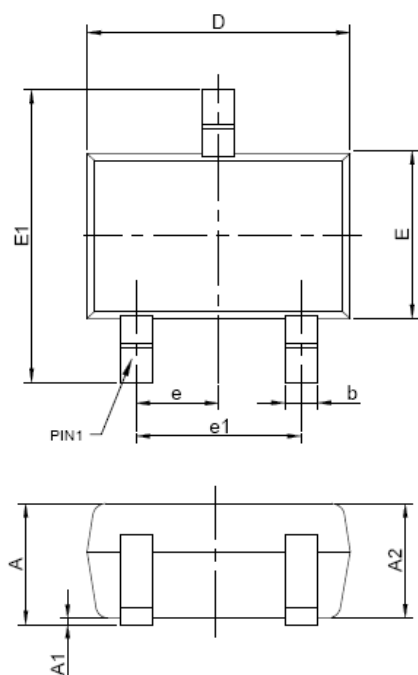
DATE: 06/19/13

DESCRIPTION: 3-Pin, Small Outline Transistor Plastic Package (SOT23)

PACKAGE CODE: TA (TA3)

DOCUMENT CONTROL #: PD-2143

REVISION: --

C3 (SC70-3L)


PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.90	1.10
A1	0.00	0.10
A2	0.90	1.00
b	0.20	0.40
c	0.08	0.15
D	2.00	2.20
E	1.15	1.35
E1	2.15	2.45
e	0.85 TYP	
e1	1.20	1.40
L	0.26	0.46
θ	0°	8°

Note:

1. Ref: JEDEC MO-203B



DATE: 06/18/13

DESCRIPTION: 3-Pin, SOT323 (SC70)

PACKAGE CODE: C (C3)

DOCUMENT CONTROL#: PD-2147

REVISION: --

Ordering Information

Part Number	Package Code	Package
PT7M6832xDxTA3E	TA3	Lead free and Green SOT23-3L
PT7M6832xDxC3E	C3	Lead free and Green SC70-3L
PT7M6833xDxTA3E	TA3	Lead free and Green SOT23-3L
PT7M6833xDxC3E	C3	Lead free and Green SC70-3L
PT7M6834xDxTA3E	TA3	Lead free and Green SOT23-3L
PT7M6834xDxC3E	C3	Lead free and Green SC70-3L
PT7M6835xDxTBE	TB	Lead free and Green SOT143-4L
PT7M6836xDxTBE	TB	Lead free and Green SOT143-4L
PT7M6837xDxTBE	TB	Lead free and Green SOT143-4L
PT7M6838DxTBE	TB	Lead free and Green SOT143-4L
PT7M6839DxTBE	TB	Lead free and Green SOT143-4L
PT7M6840DxTBE	TB	Lead free and Green SOT143-4L

Note:

- “x” refer to threshold. See below table 1
- “Dx” refer to timeout period. See below table 2
- E=Lead-free and Green
- Adding X suffix=Tape/Reel
- Contact Pericom for availability

Table 1 Suffix “x” definition of Threshold

Suffix	Reset Threshold(V)
W	1.665
V	1.575
I	1.388
H	1.313
G	1.110
F	1.050

Table 2 Suffix “Dx” definition of Timeout Period

Suffix	Reset Active Timeout Period(ms)
D0	0.07
D1	1.5
D2	30
D3	210
D4	1680

Function comparison of PT7M6832- PT7M6840

Item	Part No.	Output Open-Drain		Output Push-Pull	
		Active high	Active low	Active high	Active low
1	PT7M6832/6835/6838	-	-	-	√
2	PT7M6833/6836/6839	-	-	√	-
3	PT7M6834/6837/6840	-	√	-	-

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