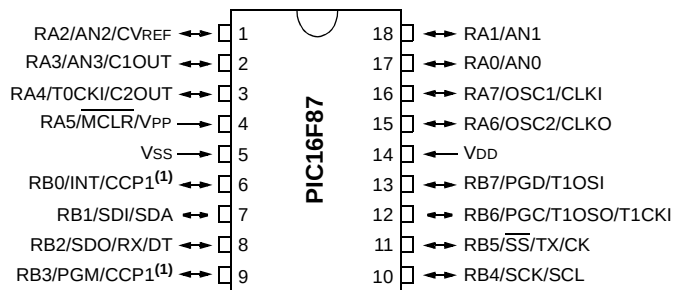


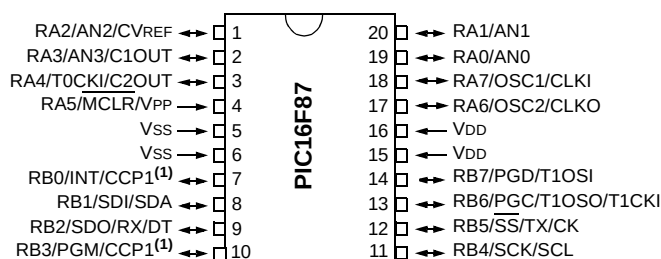
PIC16F87/88

Pin Diagrams

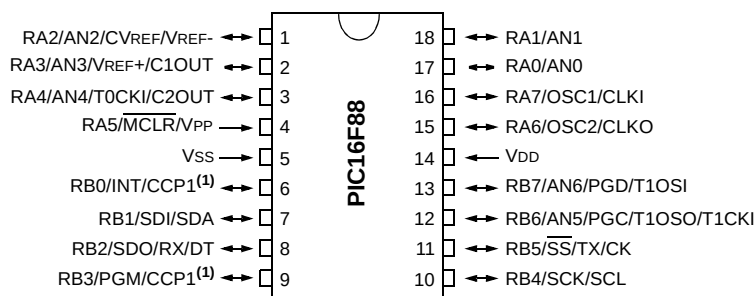
18-Pin PDIP, SOIC



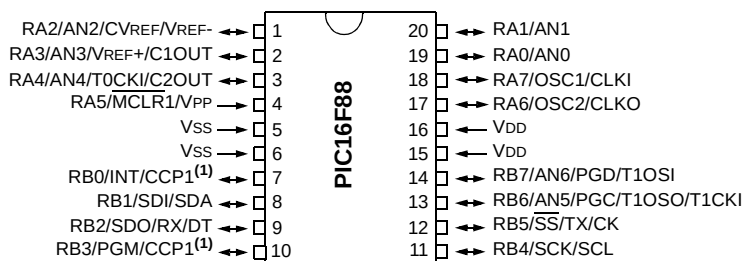
20-Pin SSOP



18-Pin PDIP, SOIC



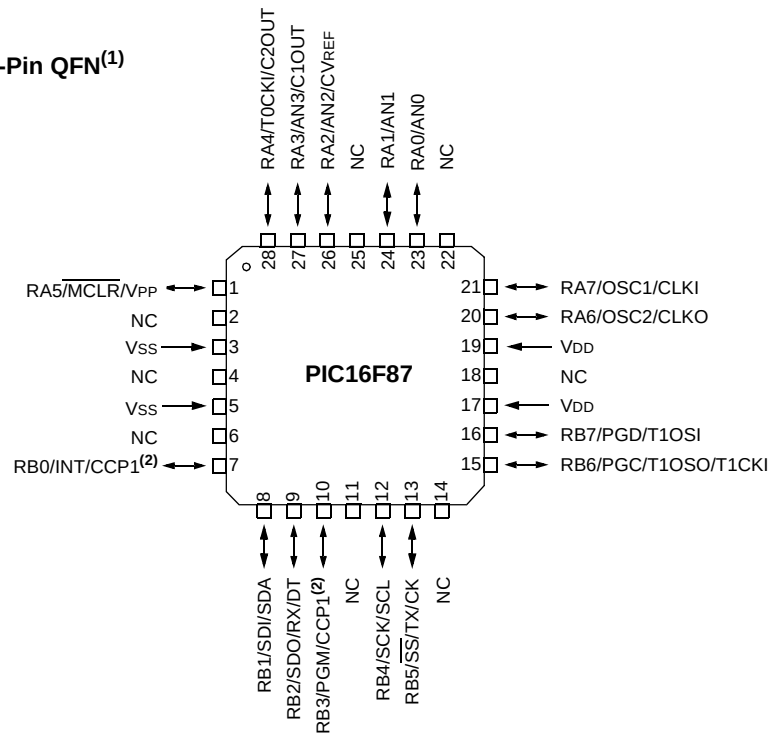
20-Pin SSOP



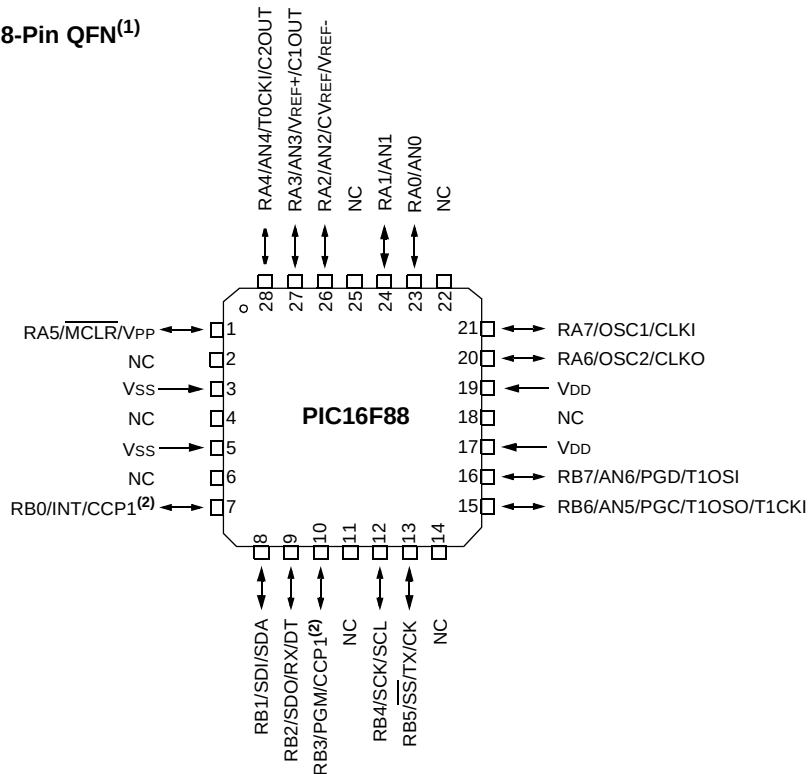
Note 1: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

Pin Diagrams (Cont'd)

28-Pin QFN⁽¹⁾



28-Pin QFN⁽¹⁾



Note 1: For the QFN package, it is recommended that the bottom pad be connected to Vss.

2: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

PIC16F87/88

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1.0 DEVICE OVERVIEW

This document contains device specific information for the operation of the PIC16F87/88 devices. Additional information may be found in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023) which may be downloaded from the Microchip web site. This Reference Manual should be considered a complementary document to this data sheet and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC16F87/88 belongs to the Mid-Range family of the PIC® devices. Block diagrams of the devices are shown in Figure 1-1 and Figure 1-2. These devices contain features that are new to the PIC16 product line:

- Low-power modes: RC_RUN allows the core and peripherals to be clocked from the INTRC, while SEC_RUN allows the core and peripherals to be clocked from the low-power Timer1. Refer to **Section 4.7 “Power-Managed Modes”** for further details.
- Internal RC oscillator with eight selectable frequencies, including 31.25 kHz, 125 kHz, 250 kHz, 500 kHz, 1 MHz, 2 MHz, 4 MHz and 8 MHz. The INTRC can be configured as a primary or secondary clock source. Refer to **Section 4.5 “Internal Oscillator Block”** for further details.
- The Timer1 module current consumption has been greatly reduced from 20 µA (previous PIC16 devices) to 1.8 µA typical (32 kHz at 2V), which is ideal for real-time clock applications. Refer to **Section 7.0 “Timer1 Module”** for further details.
- Extended Watchdog Timer (WDT) that can have a programmable period from 1 ms to 268s. The WDT has its own 16-bit prescaler. Refer to **Section 15.12 “Watchdog Timer (WDT)”** for further details.
- Two-Speed Start-up: When the oscillator is configured for LP, XT or HS Oscillator mode, this feature will clock the device from the INTRC while the oscillator is warming up. This, in turn, will enable almost immediate code execution. Refer to **Section 15.12.3 “Two-Speed Clock Start-up Mode”** for further details.
- Fail-Safe Clock Monitor: This feature will allow the device to continue operation if the primary or secondary clock source fails by switching over to the INTRC.
- The A/D module has a new register for PIC16 devices named ANSEL. This register allows easier configuration of analog or digital I/O pins.

TABLE 1-1: AVAILABLE MEMORY IN PIC16F87/88 DEVICES

Device	Program Flash	Data Memory	Data EEPROM
PIC16F87/88	4K x 14	368 x 8	256 x 8

There are 16 I/O pins that are user configurable on a pin-to-pin basis. Some pins are multiplexed with other device functions. These functions include:

- External Interrupt
- Change on PORTB Interrupt
- Timer0 Clock Input
- Low-Power Timer1 Clock/Oscillator
- Capture/Compare/PWM
- 10-bit, 7-channel A/D Converter (PIC16F88 only)
- SPI/I²C™
- Two Analog Comparators
- AUSART
- MCLR (RA5) can be configured as an input

Table 1-2 details the pinout of the devices with descriptions and details for each pin.

PIC16F87/88

FIGURE 1-1: PIC16F87 DEVICE BLOCK DIAGRAM

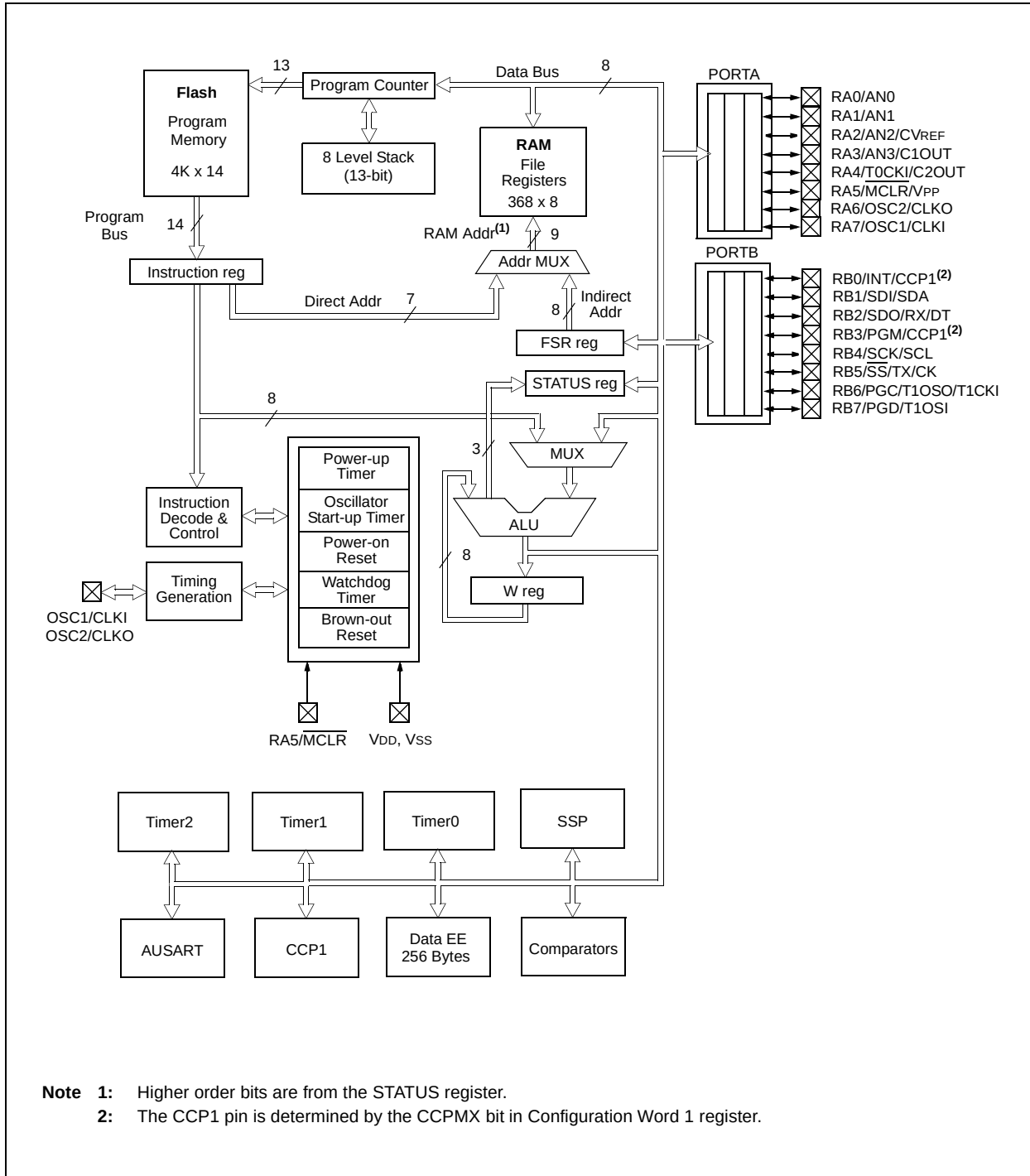
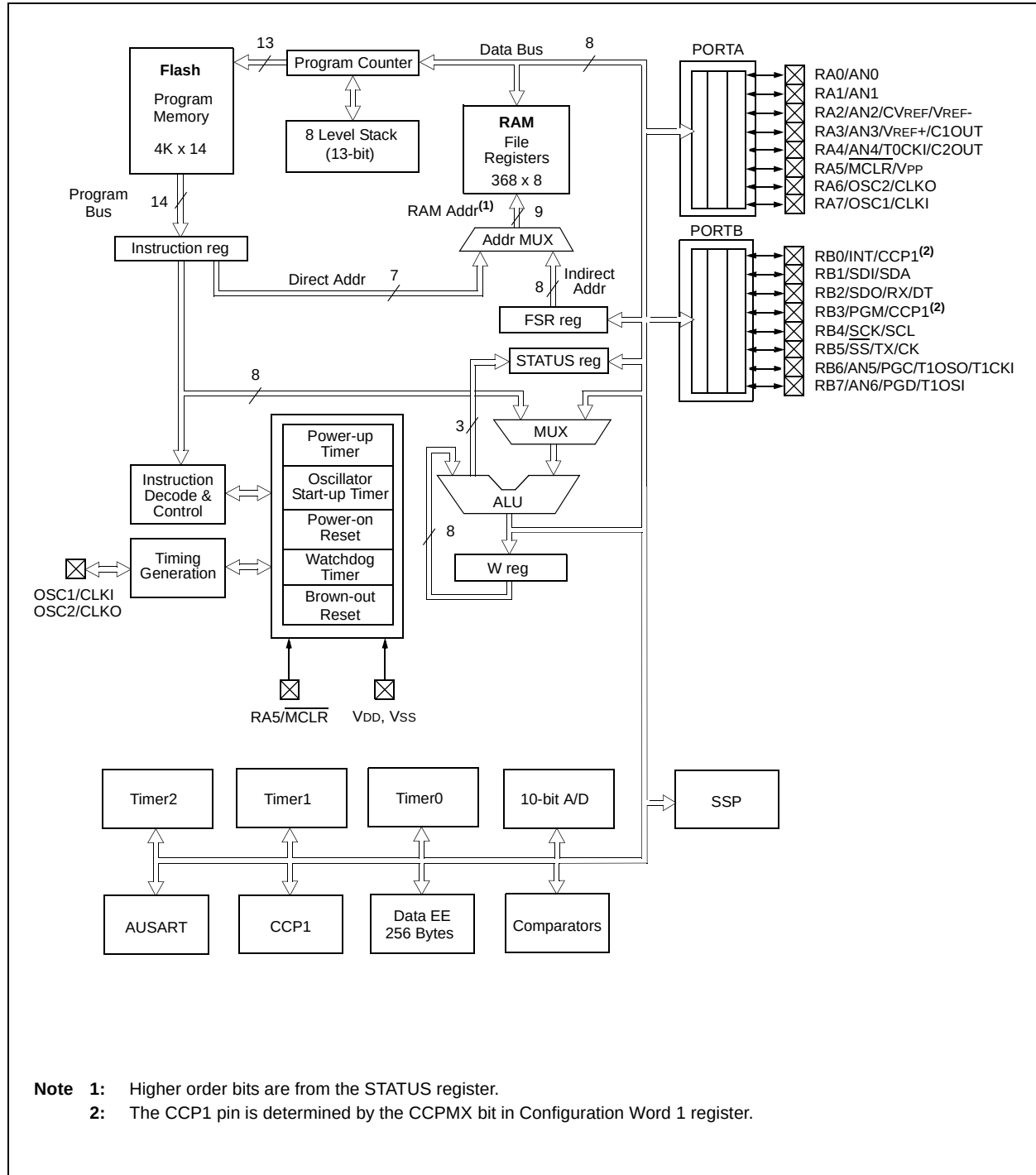


FIGURE 1-2: PIC16F88 DEVICE BLOCK DIAGRAM



PIC16F87/88

TABLE 1-2: PIC16F87/88 PINOUT DESCRIPTION

Pin Name	PDIP/ SOIC Pin#	SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
RA0/AN0 RA0 AN0	17	19	23	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Bidirectional I/O pin. Analog input channel 0.
RA1/AN1 RA1 AN1	18	20	24	I/O I	TTL Analog	Bidirectional I/O pin. Analog input channel 1.
RA2/AN2/CVREF/VREF- RA2 AN2 CVREF VREF-(4)	1	1	26	I/O I O I	TTL Analog Analog	Bidirectional I/O pin. Analog input channel 2. Comparator VREF output. A/D reference voltage (Low) input.
RA3/AN3/VREF+/C1OUT RA3 AN3 VREF+(4) C1OUT	2	2	27	I/O I I O	TTL Analog Analog	Bidirectional I/O pin. Analog input channel 3. A/D reference voltage (High) input. Comparator 1 output.
RA4/AN4/T0CKI/C2OUT RA4 AN4(4) T0CKI C2OUT	3	3	28	I/O I I O	ST Analog ST	Bidirectional I/O pin. Analog input channel 4. Clock input to the TMR0 timer/counter. Comparator 2 output.
RA5/MCLR/VPP RA5 MCLR VPP	4	4	1	I I P	ST ST –	Input pin. Master Clear (Reset). Input/programming voltage input. This pin is an active-low Reset to the device. Programming voltage input.
RA6/OSC2/CLKO RA6 OSC2 CLKO	15	17	20	I/O O O	ST – –	Bidirectional I/O pin. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, this pin outputs CLKO signal which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA7/OSC1/CLKI RA7 OSC1 CLKI	16	18	21	I/O I I	ST ST/CMOS(3) –	Bidirectional I/O pin. Oscillator crystal input. External clock source input.

Legend: I = Input O = Output I/O = Input/Output P = Power
– = Not used TTL = TTL Input ST = Schmitt Trigger Input

- Note** 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: PIC16F88 devices only.
5: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

TABLE 1-2: PIC16F87/88 PINOUT DESCRIPTION (CONTINUED)

Pin Name	PDIP/ SOIC Pin#	SSOP Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
RB0/INT/CCP1 ⁽⁵⁾ RB0 INT CCP1	6	7	7	I/O I I/O	TTL ST ⁽¹⁾ ST	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs. Bidirectional I/O pin. External interrupt pin. Capture input, Compare output, PWM output.
RB1/SDI/SDA RB1 SDI SDA	7	8	8	I/O I I/O	TTL ST ST	Bidirectional I/O pin. SPI data in. I ² C™ data.
RB2/SDO/RX/DT RB2 SDO RX DT	8	9	9	I/O O I I/O	TTL ST ST	Bidirectional I/O pin. SPI data out. AUSART asynchronous receive. AUSART synchronous detect.
RB3/PGM/CCP1 ⁽⁵⁾ RB3 PGM CCP1	9	10	10	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Low-Voltage ICSP™ Programming enable pin. Capture input, Compare output, PWM output.
RB4/SCK/SCL RB4 SCK SCL	10	11	12	I/O I/O I	TTL ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Synchronous serial clock input/output for SPI. Synchronous serial clock Input for I ² C.
RB5/ $\overline{SS}$ /TX/CK RB5 $\overline{SS}$ TX CK	11	12	13	I/O I O I/O	TTL TTL ST	Bidirectional I/O pin. Interrupt-on-change pin. Slave select for SPI in Slave mode. AUSART asynchronous transmit. AUSART synchronous clock.
RB6/AN5/PGC/T1OSO/ T1CKI RB6 AN5 ⁽⁴⁾ PGC T1OSO T1CKI	12	13	15	I/O I I/O O I	TTL ST ⁽²⁾ ST ST	Bidirectional I/O pin. Interrupt-on-change pin. Analog input channel 5. In-Circuit Debugger and programming clock pin. Timer1 oscillator output. Timer1 external clock input.
RB7/AN6/PGD/T1OSI RB7 AN6 ⁽⁴⁾ PGD T1OSI	13	14	16	I/O I I I	TTL ST ⁽²⁾ ST	Bidirectional I/O pin. Interrupt-on-change pin. Analog input channel 6. In-Circuit Debugger and ICSP programming data pin. Timer1 oscillator input.
VSS	5	5, 6	3, 5	P	—	Ground reference for logic and I/O pins.
VDD	14	15, 16	17, 19	P	—	Positive supply for logic and I/O pins.

Legend: I = Input O = Output I/O = Input/Output P = Power
— = Not used TTL = TTL Input ST = Schmitt Trigger Input

- Note 1:** This buffer is a Schmitt Trigger input when configured as the external interrupt.
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.
4: PIC16F88 devices only.
5: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

PIC16F87/88

NOTES:

2.0 MEMORY ORGANIZATION

There are two memory blocks in the PIC16F87/88 devices. These are the program memory and the data memory. Each block has its own bus, so access to each block can occur during the same oscillator cycle.

The data memory can be further broken down into the general purpose RAM and the Special Function Registers (SFRs). The operation of the SFRs that control the “core” are described here. The SFRs used to control the peripheral modules are described in the section discussing each individual peripheral module.

The data memory area also contains the data EEPROM memory. This memory is not directly mapped into the data memory but is indirectly mapped. That is, an indirect address pointer specifies the address of the data EEPROM memory to read/write. The PIC16F87/88 device's 256 bytes of data EEPROM memory have the address range of 00h-FFh. More details on the EEPROM memory can be found in **Section 3.0 “Data EEPROM and Flash Program Memory”**.

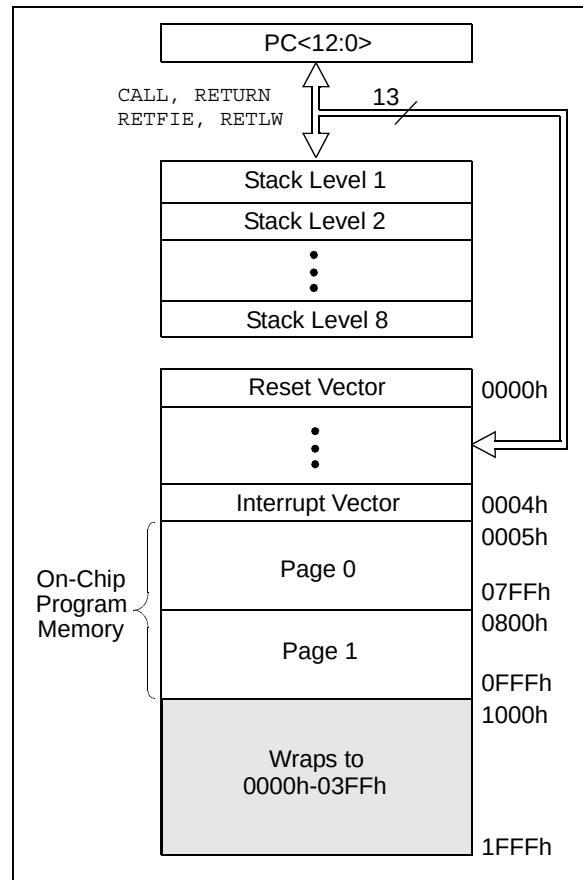
Additional information on device memory may be found in the “*PIC® Mid-Range MCU Family Reference Manual*” (DS33023).

2.1 Program Memory Organization

The PIC16F87/88 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. For the PIC16F87/88, the first 4K x 14 (0000h-0FFFh) is physically implemented (see Figure 2-1). Accessing a location above the physically implemented address will cause a wraparound. For example, the same instruction will be accessed at locations 020h, 420h, 820h, C20h, 1020h, 1420h, 1820h and 1C20h.

The Reset vector is at 0000h and the interrupt vector is at 0004h.

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK: PIC16F87/88



2.2 Data Memory Organization

The data memory is partitioned into multiple banks that contain the General Purpose Registers and the Special Function Registers. Bits RP1 (STATUS<6>) and RP0 (STATUS<5>) are the bank select bits.

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Each bank extends up to 7Fh (128 bytes). The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers, implemented as static RAM. All implemented banks contain SFRs. Some “high use” SFRs from one bank may be mirrored in another bank for code reduction and quicker access (e.g., the STATUS register is in Banks 0-3).

Note: EEPROM data memory description can be found in **Section 3.0 “Data EEPROM and Flash Program Memory”** of this data sheet.

The register file can be accessed either directly, or indirectly, through the File Select Register (FSR).

File Address		File Address		File Address		File Address	
Indirect addr. ^(*)	00h	Indirect addr. ^(*)	80h	Indirect addr. ^(*)	100h	Indirect addr. ^(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽¹⁾	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved ⁽¹⁾	18Fh
T1CON	10h	OSCTUNE	90h	General Purpose Register 16 Bytes	110h	General Purpose Register 16 Bytes	190h
TMR2	11h		91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADDD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h		95h				
CCPR1H	16h		96h				
CCP1CON	17h		97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah		9Ah				
	1Bh		9Bh				
	1Ch	CMCON	9Ch				
	1Dh	CVRCON	9Dh				
	1Eh		9Eh				
	1Fh		9Fh				
General Purpose Register 96 Bytes	20h	General Purpose Register 80 Bytes	A0h	General Purpose Register 80 Bytes	11Fh 120h	General Purpose Register 80 Bytes	19Fh 1A0h
			EFh F0h		16Fh 170h		1EFh 1F0h
	7Fh	accesses 70h-7Fh	FFh	accesses 70h-7Fh	17Fh		1FFh

Bank 0
Bank 1
Bank 2
Bank 3

Unimplemented data memory locations, read as '0'.

* Not a physical register.

Note 1: This register is reserved, maintain this register clear.

FIGURE 2-3: PIC16F88 REGISTER FILE MAP

File Address		File Address		File Address		File Address	
Indirect addr. ^(*)	00h	Indirect addr. ^(*)	80h	Indirect addr. ^(*)	100h	Indirect addr. ^(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h	WDTCON	105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
	07h		87h		107h		187h
	08h		88h		108h		188h
	09h		89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved ⁽¹⁾	18Eh
TMR1H	0Fh	OSCCON	8Fh	EEADRH	10Fh	Reserved ⁽¹⁾	18Fh
T1CON	10h	OSCTUNE	90h		110h		190h
TMR2	11h		91h				
T2CON	12h	PR2	92h				
SSPBUF	13h	SSPADD	93h				
SSPCON	14h	SSPSTAT	94h				
CCPR1L	15h		95h				
CCPR1H	16h		96h				
CCP1CON	17h		97h				
RCSTA	18h	TXSTA	98h				
TXREG	19h	SPBRG	99h				
RCREG	1Ah		9Ah				
	1Bh	ANSEL	9Bh				
	1Ch	CMCON	9Ch				
	1Dh	CVRCON	9Dh				
ADRESH	1Eh	ADRESL	9Eh				
ADCON0	1Fh	ADCON1	9Fh				
	20h		A0h				
		General Purpose Register 80 Bytes					
			EFh				
		accesses 70h-7Fh	F0h				
			FFh				
Bank 0	7Fh	Bank 1	FFh	Bank 2	17Fh	Bank 3	1FFh

Unimplemented data memory locations, read as '0'.

Not a physical register.

Note 1: This register is reserved, maintain this register clear.

PIC16F87/88

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 2-1.

The Special Function Registers can be classified into two sets: core (CPU) and peripheral. Those registers associated with the core functions are described in detail in this section. Those related to the operation of the peripheral features are described in detail in the peripheral feature section.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 0											
00h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
01h	TMR0	Timer0 Module Register								xxxx xxxx	69
02h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	
03h ⁽²⁾	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
04h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
05h	PORTA	PORTA Data Latch when written; PORTA pins when read (PIC16F87) PORTA Data Latch when written; PORTA pins when read (PIC16F88)								xxxx 0000 xxx0 0000	52
06h	PORTB	PORTB Data Latch when written; PORTB pins when read (PIC16F87) PORTB Data Latch when written; PORTB pins when read (PIC16F88)								xxxx xxxx 00xx xxxx	58
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					---0 0000	135
0Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
0Ch	PIR1	—	ADIF ⁽⁴⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	21, 77
0Dh	PIR2	OSFIF	CMIF	—	EEIF	—	—	—	—	00-0 ----	23, 34
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	77, 83
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	77, 83
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYNC}$	TMR1CS	TMR1ON	-000 0000	72, 83
11h	TMR2	Timer2 Module Register								0000 0000	80, 85
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	80, 85
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	90, 95
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	89, 95
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	83, 85
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	83, 85
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	81, 83
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	98, 99
19h	TXREG	AUSART Transmit Data Register								0000 0000	103
1Ah	RCREG	AUSART Receive Data Register								0000 0000	105
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH ⁽⁴⁾	A/D Result Register High Byte								xxxx xxxx	120
1Fh	ADCON0 ⁽⁴⁾	ADCS1	ADCS0	CHS2	CHS1	CHS0	$\overline{GO/DONE}$	—	ADON	0000 00-0	114, 120

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** These registers can be addressed from any bank.
- 3:** RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.
- 4:** PIC16F88 device only.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 1											
80h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
81h	OPTION_REG	RBP $\overline{\text{U}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18, 69
82h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	135
83h ⁽²⁾	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	17
84h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xx $\overline{\text{xx}}$	135
85h	TRISA	TRISA7	TRISA6	TRISA5 ⁽³⁾	PORTA Data Direction Register (TRISA<4:0>)					1111 1111	52, 126
86h	TRISB	PORTB Data Direction Register								1111 1111	58, 85
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter					--0 0000	135
8Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
8Ch	PIE1	—	ADIE ⁽⁴⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	20, 80
8Dh	PIE2	OSFIE	CMIE	—	EEIE	—	—	—	—	00-0 ----	22, 34
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --0q	24
8Fh	OSCCON	—	IRCF2	IRCF1	IRCF0	OSTS	IOFS	SCS1	SCS0	-000 0000	40
90h	OSCTUNE	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0	--00 0000	38
91h	—	Unimplemented								—	—
92h	PR2	Timer2 Period Register								1111 1111	80, 85
93h	SSPAD	Synchronous Serial Port (I ² C™ mode) Address Register								0000 0000	95
94h	SSPSTAT	SMP	CKE	D/ $\overline{\text{A}}$	P	S	R/ $\overline{\text{W}}$	UA	BF	0000 0000	88, 95
95h	—	Unimplemented								—	—
96h	—	Unimplemented								—	—
97h	—	Unimplemented								—	—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	97, 99
99h	SPBRG	Baud Rate Generator Register								0000 0000	99, 103
9Ah	—	Unimplemented								—	—
9Bh	ANSEL ⁽⁴⁾	—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	-111 1111	120
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	121, 126, 128
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	126, 128
9Eh	ADRESL ⁽⁴⁾	A/D Result Register Low Byte								xxxx xxxx	120
9Fh	ADCON1 ⁽⁴⁾	ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—	0000 ----	52, 115, 120

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.

2: These registers can be addressed from any bank.

3: RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

4: PIC16F88 device only.

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TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Details on page
Bank 2											
100h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	26, 135
101h	TMR0	Timer0 Module Register								xxxx xxxx	69
102h ⁽²⁾	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	135
103h ⁽²⁾	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
104h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
105h	WDTCON	—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	---0 1000	142
106h	PORTB	PORTB Data Latch when written; PORTB pins when read (PIC16F87) PORTB Data Latch when written; PORTB pins when read (PIC16F88)								xxxx xxxxx 00xx xxxxx	58
107h	—	Unimplemented								—	—
108h	—	Unimplemented								—	—
109h	—	Unimplemented								—	—
10Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter				---0 0000	135	
10Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
10Ch	EEDATA	EEPROM/Flash Data Register Low Byte								xxxx xxxxx	34
10Dh	EEADR	EEPROM/Flash Address Register Low Byte								xxxx xxxxx	34
10Eh	EEDATH	—	—	EEPROM/Flash Data Register High Byte				--xx xxxxx		34	
10Fh	EEADRH	—	—	—	—	EEPROM/Flash Address Register High Byte				---- xxxxx	34
Bank 3											
180h ⁽²⁾	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000	135
181h	OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	18, 69
182h ⁽²⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	135
183h ⁽²⁾	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	17
184h ⁽²⁾	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	135
185h	—	Unimplemented								—	—
186h	TRISB	PORTB Data Direction Register								1111 1111	58, 83
187h	—	Unimplemented								—	—
188h	—	Unimplemented								—	—
189h	—	Unimplemented								—	—
18Ah ^(1,2)	PCLATH	—	—	—	Write Buffer for the Upper 5 bits of the Program Counter				---0 0000	135	
18Bh ⁽²⁾	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	19, 69, 77
18Ch	EECON1	EEPGD	—	—	FREE	WRERR	WREN	WR	RD	x--x x000	28, 34
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- --	34
18Eh	—	Reserved, maintain clear								0000 0000	—
18Fh	—	Reserved, maintain clear								0000 0000	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note 1:** The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<12:8>, whose contents are transferred to the upper byte of the program counter.
- 2:** These registers can be addressed from any bank.
- 3:** RA5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.
- 4:** PIC16F88 device only.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains the arithmetic status of the ALU, the Reset status and the bank select bits for data memory.

The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u u1uu' (where u = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions are used to alter the STATUS register because these instructions do not affect the Z, C or DC bits from the STATUS register. For other instructions not affecting any Status bits, see **Section 16.0 "Instruction Set Summary"**.

Note: The C and DC bits operate as a borrow and digit borrow bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

REGISTER 2-1: STATUS: ARITHMETIC STATUS REGISTER (ADDRESS 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C
bit 7							bit 0

- bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
 1 = Bank 2, 3 (100h-1FFh)
 0 = Bank 0, 1 (00h-FFh)
- bit 6-5 **RP<1:0>:** Register Bank Select bits (used for direct addressing)
 11 = Bank 3 (180h-1FFh)
 10 = Bank 2 (100h-17Fh)
 01 = Bank 1 (80h-FFh)
 00 = Bank 0 (00h-7Fh)
 Each bank is 128 bytes.
- bit 4 **$\overline{\text{TO}}$:** Time-out bit
 1 = After power-up, `CLRWDT` instruction or `SLEEP` instruction
 0 = A WDT time-out occurred
- bit 3 **$\overline{\text{PD}}$:** Power-Down bit
 1 = After power-up or by the `CLRWDT` instruction
 0 = By execution of the `SLEEP` instruction
- bit 2 **Z:** Zero bit
 1 = The result of an arithmetic or logic operation is zero
 0 = The result of an arithmetic or logic operation is not zero
- bit 1 **DC:** Digit carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions)⁽¹⁾
 1 = A carry-out from the 4th low-order bit of the result occurred
 0 = No carry-out from the 4th low-order bit of the result
- bit 0 **C:** Carry/borrow bit (`ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions)^(1,2)
 1 = A carry-out from the Most Significant bit of the result occurred
 0 = No carry-out from the Most Significant bit of the result occurred

- Note 1:** For borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand.
- 2:** For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low-order bit of the source register.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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2.2.2.2 OPTION_REG Register

The OPTION_REG register is a readable and writable register that contains various control bits to configure the TMR0 prescaler/WDT postscaler (single assignable register known also as the prescaler), the external INT interrupt, TMR0 and the weak pull-ups on PORTB.

Note: To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer. Although the prescaler can be assigned to either the WDT or Timer0, but not both, a new divide counter is implemented in the WDT circuit to give multiple WDT time-out selections. This allows TMR0 and WDT to each have their own scaler. Refer to **Section 15.12 “Watchdog Timer (WDT)”** for further details.

REGISTER 2-2: OPTION_REG: OPTION CONTROL REGISTER (ADDRESS 81h, 181h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS0
	bit 7						bit 0
bit 7	RBPU: PORTB Pull-up Enable bit 1 = PORTB pull-ups are disabled 0 = PORTB pull-ups are enabled by individual port latch values						
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of RB0/INT pin 0 = Interrupt on falling edge of RB0/INT pin						
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on RA4/T0CKI/C2OUT pin 0 = Internal instruction cycle clock (CLKO)						
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on RA4/T0CKI/C2OUT pin 0 = Increment on low-to-high transition on RA4/T0CKI/C2OUT pin						
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the Timer0 module						
bit 2-0	PS<2:0>: Prescaler Rate Select bits						

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register that contains various enable and flag bits for the TMR0 register overflow, RB Port change and External RB0/INT pin interrupts.

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON: INTERRUPT CONTROL REGISTER (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF

bit 7

bit 0

- bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt
- bit 4 **INT0IE:** RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt
- bit 3 **RBIE:** RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt
- bit 2 **TMR0IF:** TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow
- bit 1 **INT0IF:** RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur
- bit 0 **RBIF:** RB Port Change Interrupt Flag bit
A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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2.2.2.4 PIE1 Register

This register contains the individual enable bits for the peripheral interrupts.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS 8Ch)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIE:** A/D Converter Interrupt Enable bit⁽¹⁾

1 = Enabled

0 = Disabled

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

bit 5 **RCIE:** AUSART Receive Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 4 **TXIE:** AUSART Transmit Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 3 **SSPIE:** Synchronous Serial Port (SSP) Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit

1 = Enabled

0 = Disabled

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

2.2.2.5 PIR1 Register

This register contains the individual flag bits for the peripheral interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (ADDRESS 0Ch)

U-0	R/W-0	R-0	R-0	R-0	R/W-0	R/W-0	R/W-0
—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **ADIF:** A/D Converter Interrupt Flag bit⁽¹⁾

1 = The A/D conversion completed (must be cleared in software)

0 = The A/D conversion is not complete

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

bit 5 **RCIF:** AUSART Receive Interrupt Flag bit

1 = The AUSART receive buffer is full (cleared by reading RCREG)

0 = The AUSART receive buffer is not full

bit 4 **TXIF:** AUSART Transmit Interrupt Flag bit

1 = The AUSART transmit buffer is empty (cleared by writing to TXREG)

0 = The AUSART transmit buffer is full

bit 3 **SSPIF:** Synchronous Serial Port (SSP) Interrupt Flag bit

1 = The transmission/reception is complete (must be cleared in software)

0 = Waiting to transmit/receive

bit 2 **CCP1IF:** CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode.

bit 1 **TMR2IF:** TMR2 to PR2 Interrupt Flag bit

1 = A TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit

1 = The TMR1 register overflowed (must be cleared in software)

0 = The TMR1 register did not overflow

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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2.2.2.6 PIE2 Register

The PIE2 register contains the individual enable bit for the EEPROM write operation interrupt.

REGISTER 2-6: PIE2: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (ADDRESS 8Dh)

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
OSFIE	CMIE	—	EEIE	—	—	—	—
bit 7			bit 0				

bit 7 **OSFIE:** Oscillator Fail Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 6 **CMIE:** Comparator Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **EEIE:** EEPROM Write Operation Interrupt Enable bit

1 = Enabled

0 = Disabled

bit 3-0 **Unimplemented:** Read as '0'

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

2.2.2.7 PIR2 Register

The PIR2 register contains the flag bit for the EEPROM write operation interrupt.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-7: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2 (ADDRESS 0Dh)

R/W-0	R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0
OSFIF	CMIF	—	EEIF	—	—	—	—
bit 7				bit 0			

- bit 7 **OSFIF:** Oscillator Fail Interrupt Flag bit
 1 = System oscillator failed, clock input has changed to INTRC (must be cleared in software)
 0 = System clock operating
- bit 6 **CMIF:** Comparator Interrupt Flag bit
 1 = Comparator input has changed (must be cleared in software)
 0 = Comparator input has not changed
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **EEIF:** EEPROM Write Operation Interrupt Flag bit
 1 = The write operation completed (must be cleared in software)
 0 = The write operation is not complete or has not been started
- bit 3-0 **Unimplemented:** Read as '0'

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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2.2.2.8 PCON Register

Note: Interrupt flag bits get set when an interrupt condition occurs, regardless of the state of its corresponding enable bit, or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

The Power Control (PCON) register contains a flag bit to allow differentiation between a Power-on Reset (POR), a Brown-out Reset, an external MCLR Reset and WDT Reset.

Note: $\overline{\text{BOR}}$ is unknown on Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if $\overline{\text{BOR}}$ is clear, indicating a brown-out has occurred. The BOR status bit is a 'don't care' and is not necessarily predictable if the brown-out circuit is disabled (by clearing the BOREN bit in the Configuration Word register).

REGISTER 2-8: PCON: POWER CONTROL REGISTER (ADDRESS 8Eh)

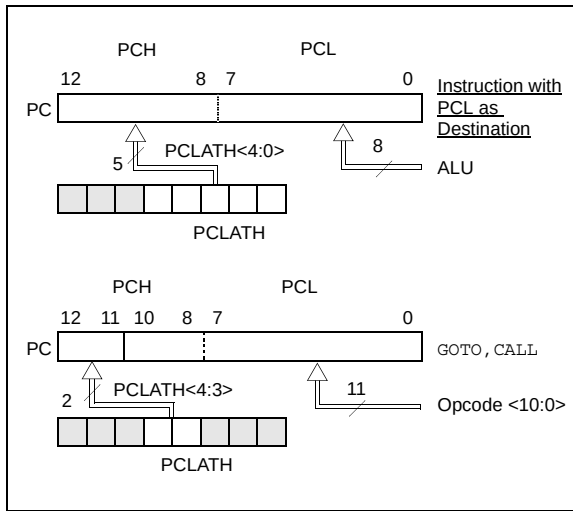
	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-x
	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$
	bit 7						bit 0	
bit 7-2	Unimplemented: Read as '0'							
bit 1	POR: Power-on Reset Status bit							
	1 = No Power-on Reset occurred							
	0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)							
bit 0	BOR: Brown-out Reset Status bit							
	1 = No Brown-out Reset occurred							
	0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

2.3 PCL and PCLATH

The Program Counter (PC) is 13 bits wide. The low byte comes from the PCL register which is a readable and writable register. The upper bits (PC<12:8>) are not readable but are indirectly writable through the PCLATH register. On any Reset, the upper bits of the PC will be cleared. Figure 2-4 shows the two situations for the loading of the PC. The upper example in the figure shows how the PC is loaded on a write to PCL (PCLATH<4:0> → PCH). The lower example in the figure shows how the PC is loaded during a CALL or GOTO instruction (PCLATH<4:3> → PCH).

FIGURE 2-4: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When doing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the application note, AN556, "Implementing a Table Read".

2.3.2 STACK

The PIC16F87/88 family has an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space and the Stack Pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed or an interrupt causes a branch. The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

Note 1: There are no status bits to indicate stack overflow or stack underflow conditions.

2: There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

2.4 Program Memory Paging

All PIC16F87/88 devices are capable of addressing a continuous 8K word block of program memory. The CALL and GOTO instructions provide only 11 bits of address to allow branching within any 2K program memory page. When doing a CALL or GOTO instruction, the upper 2 bits of the address are provided by PCLATH<4:3>. When doing a CALL or GOTO instruction, the user must ensure that the page select bits are programmed so that the desired program memory page is addressed. If a return from a CALL instruction (or interrupt) is executed, the entire 13-bit PC is popped off the stack. Therefore, manipulation of the PCLATH<4:3> bits is not required for the RETURN instructions (which POPs the address from the stack).

Note: The contents of the PCLATH register are unchanged after a RETURN or RETFIE instruction is executed. The user must rewrite the contents of the PCLATH register for any subsequent subroutine calls or GOTO instructions.

Example 2-1 shows the calling of a subroutine in page 1 of the program memory. This example assumes that PCLATH is saved and restored by the Interrupt Service Routine (if interrupts are used).

EXAMPLE 2-1: CALL OF A SUBROUTINE IN PAGE 1 FROM PAGE 0

```

ORG 0x500
BCF PCLATH, 4
BSF PCLATH, 3 ;Select page 1
                ; (800h-FFFh)
CALL SUB1_P1 ;Call subroutine in
:                ;page 1 (800h-FFFh)
:
ORG 0x900 ;page 1 (800h-FFFh)
SUB1_P1
:                ;called subroutine
                ;page 1 (800h-FFFh)
:
RETURN ;return to
        ;Call subroutine
        ;in page 0
        ; (000h-7FFh)
    
```

2.5 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

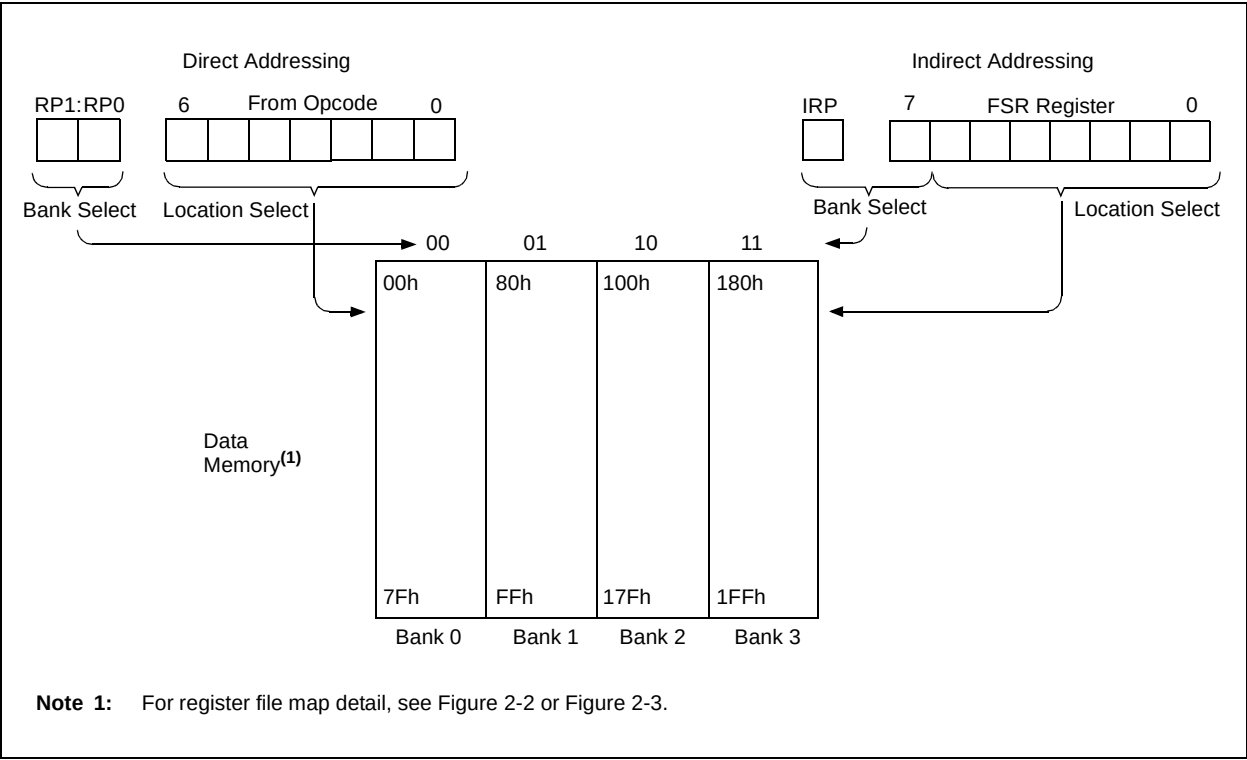
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself, indirectly (FSR = 0) will read 00h. Writing to the INDF register indirectly results in a no operation (although status bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-5.

A simple program to clear RAM locations 20h-2Fh using indirect addressing is shown in Example 2-2.

EXAMPLE 2-2: INDIRECT ADDRESSING

```
MOVW 0x20      ;initialize pointer
MOVWF FSR      ;to RAM
NEXT  CLRF INDF ;clear INDF register
      INCF FSR, F ;inc pointer
      BTFSS FSR, 4 ;all done?
      GOTO NEXT  ;no clear next
CONTINUE
      :          ;yes continue
```

FIGURE 2-5: DIRECT/INDIRECT ADDRESSING



3.0 DATA EEPROM AND FLASH PROGRAM MEMORY

The data EEPROM and Flash program memory are readable and writable during normal operation (over the full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are six SFRs used to read and write this memory:

- EECON1
- EECON2
- EEDATA
- EEDATH
- EEADR
- EEADRH

This section focuses on reading and writing data EEPROM and Flash program memory during normal operation. Refer to the appropriate device programming specification document for serial programming information.

When interfacing the data memory block, EEDATA holds the 8-bit data for read/write and EEADR holds the address of the EEPROM location being accessed. The PIC16F87/88 devices have 256 bytes of data EEPROM with an address range from 00h to 0FFh. When writing to unimplemented locations, the charge pump will be turned off.

When interfacing the program memory block, the EEDATA and EEDATH registers form a two-byte word that holds the 14-bit data for read/write and the EEADR and EEADRH registers form a two-byte word that holds the 13-bit address of the EEPROM location being accessed. The PIC16F87/88 devices have 4K words of program Flash with an address range from 0000h to 0FFFh. Addresses above the range of the respective device will wraparound to the beginning of program memory.

The EEPROM data memory allows single byte read and write. The Flash program memory allows single-word reads and four-word block writes. Program memory writes must first start with a 32-word block erase, then write in 4-word blocks. A byte write in data EEPROM memory automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

When the device is code-protected, the CPU may continue to read and write the data EEPROM memory. Depending on the settings of the write-protect bits, the device may or may not be able to write certain blocks of the program memory; however, reads of the program memory are allowed. When code-protected, the device programmer can no longer access data or program memory; this does NOT inhibit internal reads or writes.

3.1 EEADR and EEADRH

The EEADRH:EEADR register pair can address up to a maximum of 256 bytes of data EEPROM, or up to a maximum of 8K words of program EEPROM. When selecting a data address value, only the LSB of the address is written to the EEADR register. When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADR register.

If the device contains less memory than the full address reach of the address register pair, the Most Significant bits of the registers are not implemented. For example, if the device has 128 bytes of data EEPROM, the Most Significant bit of EEADR is not implemented on access to data EEPROM.

3.2 EECON1 and EECON2 Registers

EECON1 is the control register for memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, as it is when reset, any subsequent operations will operate on the data memory. When set, any subsequent operations will operate on the program memory.

Control bits, RD and WR, initiate read and write, respectively. These bits cannot be cleared, only set in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write or erase operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write (or erase) operation is interrupted by a MCLR, or a WDT Time-out Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and rewrite the location. The data and address will be unchanged in the EEDATA and EEADR registers.

Interrupt flag bit, EEIF in the PIR2 register, is set when the write is complete. It must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the EEPROM write sequence.

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REGISTER 3-1: EECON1: EEPROM ACCESS CONTROL REGISTER 1 (ADDRESS 18Ch)

R/W-x	U-0	U-0	R/W-x	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	—	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

- bit 7 **EEPGD:** Program/Data EEPROM Select bit
 1 = Accesses program memory
 0 = Accesses data memory
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **FREE:** EEPROM Forced Row Erase bit
 1 = Erase the program memory row addressed by EEADRH:EEADR on the next WR command
 0 = Perform write only
- bit 3 **WRERR:** EEPROM Error Flag bit
 1 = A write operation is prematurely terminated (any $\overline{\text{MCLR}}$ or any WDT Reset during normal operation)
 0 = The write operation completed
- bit 2 **WREN:** EEPROM Write Enable bit
 1 = Allows write cycles
 0 = Inhibits write to the EEPROM
- bit 1 **WR:** Write Control bit
 1 = Initiates a write cycle. The bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.
 0 = Write cycle to the EEPROM is complete
- bit 0 **RD:** Read Control bit
 1 = Initiates an EEPROM read, RD is cleared in hardware. The RD bit can only be set (not cleared) in software.
 0 = Does not initiate an EEPROM read

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0' S = Set only
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

3.3 Reading Data EEPROM Memory

To read a data memory location, the user must write the address to the EEADR register, clear the EEPGD control bit (EECON1<7>) and then set control bit RD (EECON1<0>). The data is available in the very next cycle in the EEDATA register; therefore, it can be read in the next instruction (see Example 3-1). EEDATA will hold this value until another read or until it is written to by the user (during a write operation).

The steps to reading the EEPROM data memory are:

1. Write the address to EEADR. Make sure that the address is not larger than the memory size of the device.
2. Clear the EEPGD bit to point to EEPROM data memory.
3. Set the RD bit to start the read operation.
4. Read the data from the EEDATA register.

EXAMPLE 3-1: DATA EEPROM READ

```
BANKSEL EEADR      ; Select Bank of EEADR
MOVF  ADDR, W      ;
MOVWF  EEADR       ; Data Memory Address
                ; to read
BANKSEL EECON1     ; Select Bank of EECON1
BCF    EECON1, EEPGD; Point to Data memory
BSF    EECON1, RD   ; EE Read
BANKSEL EEDATA     ; Select Bank of EEDATA
MOVF   EEDATA, W    ; W = EEDATA
```

3.4 Writing to Data EEPROM Memory

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then, the user must follow a specific write sequence to initiate the write for each byte.

The write will not initiate if the write sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment (see Example 3-2).

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times except when updating EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set. At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. EEIF must be cleared by software.

The steps to write to EEPROM data memory are:

1. If step 10 is not implemented, check the WR bit to see if a write is in progress.
2. Write the address to EEADR. Make sure that the address is not larger than the memory size of the device.
3. Write the 8-bit data value to be programmed in the EEDATA register.
4. Clear the EEPGD bit to point to EEPROM data memory.
5. Set the WREN bit to enable program operations.
6. Disable interrupts (if enabled).
7. Execute the special five instruction sequence:
Write 55h to EECON2 in two steps (first to W, then to EECON2).
Write AAh to EECON2 in two steps (first to W, then to EECON2).
Set the WR bit.
8. Enable interrupts (if using interrupts).
9. Clear the WREN bit to disable program operations.
10. At the completion of the write cycle, the WR bit is cleared and the EEIF interrupt flag bit is set (EEIF must be cleared by firmware). If step 1 is not implemented, then firmware should check for EEIF to be set, or WR to clear, to indicate the end of the program cycle.

EXAMPLE 3-2: DATA EEPROM WRITE

```
BANKSEL EECON1     ; Select Bank of
                ; EECON1
BTFSC  EECON1, WR   ; Wait for write
GOTO   $-1          ; to complete
BANKSEL EEADR       ; Select Bank of
                ; EEADR
MOVF   ADDR, W      ;
MOVWF  EEADR        ; Data Memory
                ; Address to write
MOVF   VALUE, W     ;
MOVWF  EEDATA       ; Data Memory Value
                ; to write
BANKSEL EECON1     ; Select Bank of
                ; EECON1
BCF    EECON1, EEPGD; Point to DATA
                ; memory
BSF    EECON1, WREN ; Enable writes

BCF    INTCON, GIE  ; Disable INTs.
MOVLW  55h          ;
MOVWF  EECON2       ; Write 55h
MOVLW  AAh          ;
MOVWF  EECON2       ; Write AAh
BSF    EECON1, WR   ; Set WR bit to
                ; begin write
BSF    INTCON, GIE  ; Enable INTs.
BCF    EECON1, WREN ; Disable writes
```

3.5 Reading Flash Program Memory

To read a program memory location, the user must write two bytes of the address to the EEADR and EEADRH registers, set the EEPGD control bit (EECON1<7>) and then set control bit RD (EECON1<0>). Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1,RD" instruction to be ignored. The data is available in the very next cycle in the EEDATA and EEDATH registers; therefore, it can be read as two bytes in the following instructions. EEDATA and EEDATH registers will hold this value until another read or until it is written to by the user (during a write operation).

EXAMPLE 3-3: FLASH PROGRAM READ

```
BANKSEL EEADRH      ; Select Bank of EEADRH
MOVF  ADDRHL, W      ;
MOVWF  EEADRH        ; MS Byte of Program
                        ; Address to read
MOVF  ADDRLL, W      ;
MOVWF  EEADR         ; LS Byte of Program
                        ; Address to read
BANKSEL EECON1       ; Select Bank of EECON1
BSF    EECON1, EEPGD ; Point to PROGRAM
                        ; memory
BSF    EECON1, RD    ; EE Read
                        ;
NOP                        ; Any instructions
                        ; here are ignored as
NOP                        ; program memory is
                        ; read in second cycle
                        ; after BSF EECON1,RD
BANKSEL EEDATA       ; Select Bank of EEDATA
MOVF  EEDATA, W      ; DATAL = EEDATA
MOVWF  DATAL         ;
MOVF  EEDATH, W      ; DATAH = EEDATH
MOVWF  DATAH        ;
```

3.6 Erasing Flash Program Memory

The minimum erase block is 32 words. Only through the use of an external programmer, or through ICSP control, can larger blocks of program memory be bulk erased. Word erase in the Flash array is not supported.

When initiating an erase sequence from the microcontroller itself, a block of 32 words of program memory is erased. The Most Significant 11 bits of the EEADRH:EEADR point to the block being erased. EEADR<4:0> are ignored.

The EECON1 register commands the erase operation. The EEPGD bit must be set to point to the Flash program memory. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

For protection, the write initiate sequence for EECON2 must be used.

After the "BSF EECON1,WR" instruction, the processor requires two cycles to setup the erase operation. The user must place two NOP instructions after the WR bit is set. The processor will halt internal operations for the typical 2 ms, only during the cycle in which the erase takes place. This is not Sleep mode, as the clocks and peripherals will continue to run. After the erase cycle, the processor will resume operation with the third instruction after the EECON1 write instruction.

3.6.1 FLASH PROGRAM MEMORY ERASE SEQUENCE

The sequence of events for erasing a block of internal program memory location is:

1. Load EEADRH:EEADR with address of row being erased.
2. Set EEPGD bit to point to program memory, set WREN bit to enable writes and set FREE bit to enable the erase.
3. Disable interrupts.
4. Write 55h to EECON2.
5. Write AAh to EECON2.
6. Set the WR bit. This will begin the row erase cycle.
7. The CPU will stall for duration of the erase.

EXAMPLE 3-4: ERASING A FLASH PROGRAM MEMORY ROW

```

        BANKSEL    EEADRH        ; Select Bank of EEADRH
        MOVF       ADDRH, W      ;
        MOVWF      EEADRH        ; MS Byte of Program Address to Erase
        MOVF       ADDRHL, W     ;
        MOVWF      EEADR         ; LS Byte of Program Address to Erase
ERASE_ROW
        BANKSEL    EECON1        ; Select Bank of EECON1
        BSF        EECON1, EEPGD  ; Point to PROGRAM memory
        BSF        EECON1, WREN   ; Enable Write to memory
        BSF        EECON1, FREE   ; Enable Row Erase operation
;
        BCF        INTCON, GIE    ; Disable interrupts (if using)
        MOVLW      55h            ;
        MOVWF      EECON2         ; Write 55h
        MOVLW      AAh            ;
        MOVWF      EECON2         ; Write AAh
        BSF        EECON1, WR     ; Start Erase (CPU stall)
        NOP                     ; Any instructions here are ignored as processor
                                ; halts to begin Erase sequence
        NOP                     ; processor will stop here and wait for Erase complete
                                ; after Erase processor continues with 3rd instruction
        BCF        EECON1, FREE   ; Disable Row Erase operation
        BCF        EECON1, WREN   ; Disable writes
        BSF        INTCON, GIE    ; Enable interrupts (if using)

```

3.7 Writing to Flash Program Memory

Flash program memory may only be written to if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT1:WRT0 of the device Configuration Word (Register 15-1). Flash program memory must be written in four-word blocks. A block consists of four words with sequential addresses, with a lower boundary defined by an address, where $EEADR<1:0> = 00$. At the same time, all block writes to program memory are done as write-only operations. The program memory must first be erased. The write operation is edge-aligned and cannot occur across boundaries.

To write to the program memory, the data must first be loaded into the buffer registers. There are four 14-bit buffer registers and they are addressed by the low 2 bits of $EEADR$.

The following sequence of events illustrate how to perform a write to program memory:

- Set the $EEP GD$ and $WREN$ bits in the $EECON1$ register
- Clear the $FREE$ bit in $EECON1$
- Write address to $EEADRH:EEADR$
- Write data to $EEDATH:EEDATA$
- Write 55 to $EECON2$
- Write AA to $EECON2$
- Set WR bit in $EECON1$

The user must follow the same specific sequence to initiate the write for each word in the program block by writing each program word in sequence (00, 01, 10, 11).

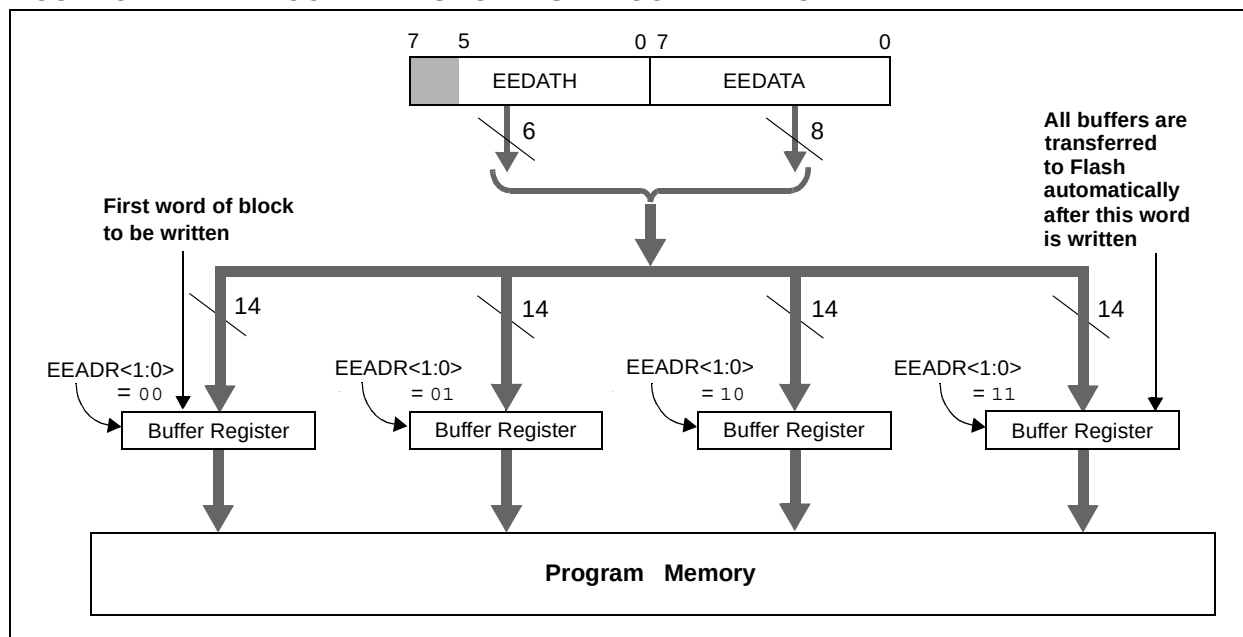
There are 4 buffer register words and all four locations **MUST** be written to with correct data.

After the “BSF $EECON1$, WR ” instruction, if $EEADR \neq \text{xxxxxx}11$, then a short write will occur. This short write only transfers the data to the buffer register. The WR bit will be cleared in hardware after 1 cycle.

After the “BSF $EECON1$, WR ” instruction, if $EEADR = \text{xxxxxx}11$, then a long write will occur. This will simultaneously transfer the data from $EEDATH:EEDATA$ to the buffer registers and begin the write of all four words. The processor will execute the next instruction and then ignore the subsequent instruction. The user should place NOP instructions into the second words. The processor will then halt internal operations for typically 2 msec in which the write takes place. This is not Sleep mode, as the clocks and peripherals will continue to run. After the write cycle, the processor will resume operation with the 3rd instruction after the $EECON1$ write instruction.

After each long write, the 4 buffer registers will be reset to 3FFF.

FIGURE 3-1: BLOCK WRITES TO FLASH PROGRAM MEMORY



An example of the complete four-word write sequence is shown in Example 3-5. The initial address is loaded into the EEADRH:EEADR register pair; the four words of data are loaded using indirect addressing, assuming that a row erase sequence has already been performed.

EXAMPLE 3-5: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:

; 1. The 32 words in the erase block have already been erased.
; 2. A valid starting address (the least significant bits = '00') is loaded into EEADRH:EEADR
; 3. This example is starting at 0x100, this is an application dependent setting.
; 4. The 8 bytes (4 words) of data are loaded, starting at an address in RAM called ARRAY.
; 5. This is an example only, location of data to program is application dependent.
; 6. word_block is located in data memory.

        BANKSEL    EECON1           ;prepare for WRITE procedure
        BSF         EECON1, EEPGD    ;point to program memory
        BSF         EECON1, WREN     ;allow write cycles
        BCF         EECON1, FREE     ;perform write only

        BANKSEL    word_block
        MOVLW       .4
        MOVWF       word_block       ;prepare for 4 words to be written

        BANKSEL    EEADRH           ;Start writing at 0x100
        MOVLW       0x01
        MOVWF       EEADRH          ;load HIGH address
        MOVLW       0x00
        MOVWF       EEADR           ;load LOW address
        BANKSEL    ARRAY
        MOVLW       ARRAY           ;initialize FSR to start of data
        MOVWF       FSR

LOOP
        BANKSEL    EEDATA
        MOVF        INDF, W          ;indirectly load EEDATA
        MOVWF       EEDATA
        INCF        FSR, F           ;increment data pointer
        MOVF        INDF, W          ;indirectly load EEDATH
        MOVWF       EEDATH
        INCF        FSR, F           ;increment data pointer

        BANKSEL    EECON1
        MOVLW       0x55             ;required sequence
        MOVWF       EECON2
        MOVLW       0xAA
        MOVWF       EECON2
        BSF         EECON1, WR       ;set WR bit to begin write
        NOP         ;instructions here are ignored as processor
        NOP

        BANKSEL    EEADR
        INCF        EEADR, f         ;load next word address
        BANKSEL    word_block
        DECFSZ      word_block, f    ;have 4 words been written?
        GOTO        loop            ;NO, continue with writing

        BANKSEL    EECON1
        BCF         EECON1, WREN     ;YES, 4 words complete, disable writes
        BSF         INTCON, GIE      ;enable interrupts
```

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3.8 Protection Against Spurious Write

There are conditions when the device should not write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents an EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch or software malfunction.

3.9 Operation During Code-Protect

When the data EEPROM is code-protected, the microcontroller can read and write to the EEPROM normally. However, all external access to the EEPROM is disabled. External write access to the program memory is also disabled.

When program memory is code-protected, the microcontroller can read and write to program memory normally, as well as execute instructions. Writes by the device may be selectively inhibited to regions of the memory depending on the setting of bits WRT1:WRT0 of the Configuration Word (see **Section 15.1 “Configuration Bits”** for additional information). External access to the memory is also disabled.

TABLE 3-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM AND FLASH PROGRAM MEMORIES

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on all other Resets
10Ch	EEDATA	EEPROM/Flash Data Register Low Byte								xxxx xxxx	uuuu uuuu
10Dh	EEADR	EEPROM/Flash Address Register Low Byte								xxxx xxxx	uuuu uuuu
10Eh	EEDATH	—	—	EEPROM/Flash Data Register High Byte						--xx xxxx	--uu uuuu
10Fh	EEADRH	—	—	—	—	EEPROM/Flash Address Register High Byte				---- xxxx	---- uuuu
18Ch	EECON1	EEPGD	—	—	FREE	WRERR	WREN	WR	RD	x--x x000	x--x q000
18Dh	EECON2	EEPROM Control Register 2 (not a physical register)								---- ----	---- ----
0Dh	PIR2	OSFIF	CMIF	—	EEIF	—	—	—	—	00-0 ----	00-0 ----
8Dh	PIE2	OSFIE	CMIE	—	EEIE	—	—	—	—	00-0 ----	00-0 ----

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends upon condition.
Shaded cells are not used by data EEPROM or Flash program memory.

4.0 OSCILLATOR CONFIGURATIONS

4.1 Oscillator Types

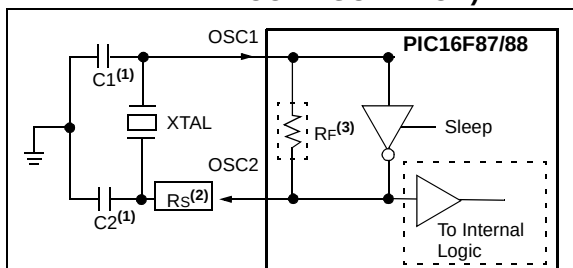
The PIC16F87/88 can be operated in eight different oscillator modes. The user can program three configuration bits (FOSC2:FOSC0) to select one of these eight modes (modes 5-8 are new PIC16 oscillator configurations):

1. LP Low-Power Crystal
2. XT Crystal/Resonator
3. HS High-Speed Crystal/Resonator
4. RC External Resistor/Capacitor with Fosc/4 output on RA6
5. RCIO External Resistor/Capacitor with I/O on RA6
6. INTIO1 Internal Oscillator with Fosc/4 output on RA6 and I/O on RA7
7. INTIO2 Internal Oscillator with I/O on RA6 and RA7
8. ECIO External Clock with I/O on RA6

4.2 Crystal Oscillator/Ceramic Resonators

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKI and OSC2/CLKO pins to establish oscillation (see Figure 4-1 and Figure 4-2). The PIC16F87/88 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturer's specifications.

FIGURE 4-1: CRYSTAL OPERATION (HS, XT, OR LP OSCILLATOR CONFIGURATION)



Note1: See Table 4-1 for typical values of C1 and C2.

- 2: A series resistor (R_s) may be required for AT strip cut crystals.
- 3: R_f varies with the crystal chosen (typically between 2 M Ω to 10 M Ω).

TABLE 4-1: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR (FOR DESIGN GUIDANCE ONLY)

Osc Type	Crystal Freq	Typical Capacitor Values Tested:	
		C1	C2
LP	32 kHz	33 pF	33 pF
XT	200 kHz	56 pF	56 pF
	1 MHz	15 pF	15 pF
	4 MHz	15 pF	15 pF
HS	4 MHz	15 pF	15 pF
	8 MHz	15 pF	15 pF
	20 MHz	15 pF	15 pF

Capacitor values are for design guidance only.

These capacitors were tested with the crystals listed below for basic start-up and operation. These values were not optimized.

Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected V_{DD} and temperature range for the application.

See the notes following this table for additional information.

- Note 1:** Higher capacitance increases the stability of oscillator but also increases the start-up time.
- 2:** Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.
- 3:** R_s may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
- 4:** Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.

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FIGURE 4-2: CERAMIC RESONATOR OPERATION (HS OR XT OSC CONFIGURATION)

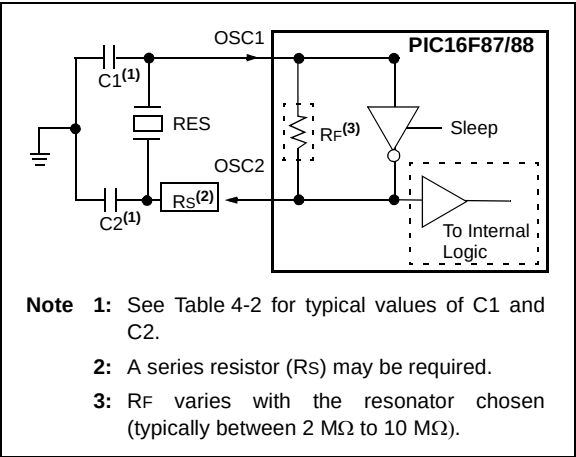


TABLE 4-2: CERAMIC RESONATORS (FOR DESIGN GUIDANCE ONLY)

Typical Capacitor Values Used:			
Mode	Freq	OSC1	OSC2
XT	455 kHz	56 pF	56 pF
	2.0 MHz	47 pF	47 pF
	4.0 MHz	33 pF	33 pF
HS	8.0 MHz	27 pF	27 pF
	16.0 MHz	22 pF	22 pF

Capacitor values are for design guidance only.
These capacitors were tested with the resonators listed below for basic start-up and operation. These values were not optimized.
Different capacitor values may be required to produce acceptable oscillator operation. The user should test the performance of the oscillator over the expected VDD and temperature range for the application.
See the notes following this table for additional information.

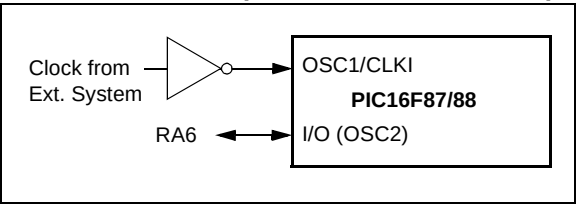
Note: When using resonators with frequencies above 3.5 MHz, the use of HS mode, rather than XT mode, is recommended. HS mode may be used at any VDD for which the controller is rated. If HS is selected, it is possible that the gain of the oscillator will overdrive the resonator. Therefore, a series resistor should be placed between the OSC2 pin and the resonator. As a good starting point, the recommended value of Rs is 330Ω.

4.3 External Clock Input

The ECIO Oscillator mode requires an external clock source to be connected to the OSC1 pin. There is no oscillator start-up time required after a Power-on Reset, or after an exit from Sleep mode.

In the ECIO Oscillator mode, the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 4-3 shows the pin connections for the ECIO Oscillator mode.

FIGURE 4-3: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)

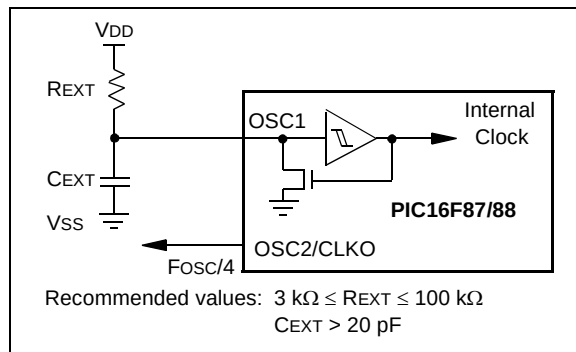


4.4 RC Oscillator

For timing insensitive applications, the “RC” and “RCIO” device options offer additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal manufacturing variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 4-4 shows how the R/C combination is connected.

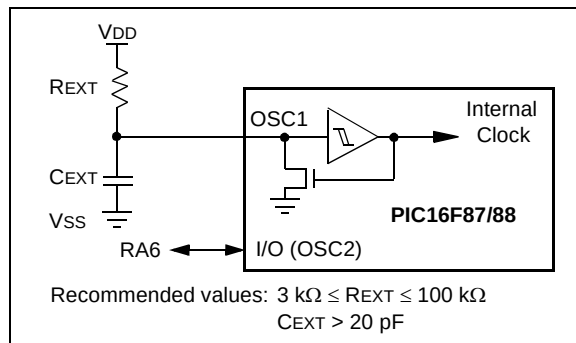
In the RC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic.

FIGURE 4-4: RC OSCILLATOR MODE



The RCIO Oscillator mode (Figure 4-5) functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

FIGURE 4-5: RCIO OSCILLATOR MODE



4.5 Internal Oscillator Block

The PIC16F87/88 devices include an internal oscillator block which generates two different clock signals; either can be used as the system's clock source. This can eliminate the need for external oscillator circuits on the OSC1 and/or OSC2 pins.

The main output (INTOSC) is an 8 MHz clock source which can be used to directly drive the system clock. It also drives the INTOSC postscaler which can provide a range of six clock frequencies from 125 kHz to 4 MHz.

The other clock source is the internal RC oscillator (INTRC) which provides a 31.25 kHz (32 μ s nominal period) output. The INTRC oscillator is enabled by selecting the INTRC as the system clock source or when any of the following are enabled:

- Power-up Timer
- Watchdog Timer
- Two-Speed Start-up
- Fail-Safe Clock Monitor

These features are discussed in greater detail in **Section 15.0 “Special Features of the CPU”**.

The clock source frequency (INTOSC direct, INTRC direct or INTOSC postscaler) is selected by configuring the IRCF bits of the OSCCON register (page 40).

Note: Throughout this data sheet, when referring *specifically* to a generic clock source, the term “INTRC” may also be used to refer to the clock modes using the internal oscillator block. This is regardless of whether the actual frequency used is INTOSC (8 MHz), the INTOSC postscaler or INTRC (31.25 kHz).

4.5.1 INTRC MODES

Using the internal oscillator as the clock source can eliminate the need for up to two external oscillator pins, after which it can be used for digital I/O. Two distinct configurations are available:

- In INTIO1 mode, the OSC2 pin outputs Fosc/4, while OSC1 functions as RA7 for digital input and output.
- In INTIO2 mode, OSC1 functions as RA7 and OSC2 functions as RA6, both for digital input and output.

4.5.2 OSCTUNE REGISTER

The internal oscillator's output has been calibrated at the factory but can be adjusted in the application. This is done by writing to the OSCTUNE register (Register 4-1). The tuning sensitivity is constant throughout the tuning range. The OSCTUNE register has a tuning range of $\pm 12.5\%$.

When the OSCTUNE register is modified, the INTOSC and INTRC frequencies will begin shifting to the new frequency. The INTRC clock will reach the new frequency within 8 clock cycles (approximately $8 * 32 \mu s = 256 \mu s$); the INTOSC clock will stabilize within 1 ms. Code execution continues during this shift. There is no indication that the shift has occurred. Operation of features that depend on the 31.25 kHz INTRC clock source frequency, such as the WDT, Fail-Safe Clock Monitor and peripherals, will also be affected by the change in frequency.

REGISTER 4-1: OSCTUNE: OSCILLATOR TUNING REGISTER (ADDRESS 90h)

	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7								bit 0
bit 7-6	Unimplemented: Read as '0'							
bit 5-0	TUN<5:0>: Frequency Tuning bits							
	011111 = Maximum frequency							
	011110 =							
	•							
	•							
	•							
	000001 =							
	000000 = Center frequency. Oscillator module is running at the calibrated frequency.							
	111111 =							
	•							
	•							
	•							
	100000 = Minimum frequency							

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

4.6 Clock Sources and Oscillator Switching

The PIC16F87/88 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low-frequency clock source. PIC16F87/88 devices offer three alternate clock sources. When enabled, these give additional options for switching to the various power-managed operating modes.

Essentially, there are three clock sources for these devices:

- Primary oscillators
- Secondary oscillators
- Internal oscillator block (INTRC)

The **primary oscillators** include the External Crystal and Resonator modes, the External RC modes, the External Clock mode and the internal oscillator block. The particular mode is defined on POR by the contents of Configuration Word 1. The details of these modes are covered earlier in this chapter.

The **secondary oscillators** are those external sources not connected to the OSC1 or OSC2 pins. These sources may continue to operate even after the controller is placed in a power-managed mode.

PIC16F87/88 devices offer the Timer1 oscillator as a secondary oscillator. This oscillator continues to run when a **SLEEP** instruction is executed and is often the time base for functions such as a real-time clock.

Most often, a 32.768 kHz watch crystal is connected between the RB6/T1OSO and RB7/T1OSI pins. Like the LP mode oscillator circuit, loading capacitors are also connected from each pin to ground. The Timer1 oscillator is discussed in greater detail in **Section 7.6 “Timer1 Oscillator”**.

In addition to being a primary clock source, the **internal oscillator block** is available as a power-managed mode clock source. The 31.25 kHz INTRC source is also used as the clock source for several special features, such as the WDT, Fail-Safe Clock Monitor, Power-up Timer and Two-Speed Start-up.

The clock sources for the PIC16F87/88 devices are shown in Figure 4-6. See **Section 7.0 “Timer1 Module”** for further details of the Timer1 oscillator. See **Section 15.1 “Configuration Bits”** for Configuration register details.

4.6.1 OSCCON REGISTER

The OSCCON register (Register 4-2) controls several aspects of the system clock's operation, both in full power operation and in power-managed modes.

The System Clock Select bits, SCS1:SCS0, select the clock source that is used when the device is operating in power-managed modes. When the bits are cleared (SCS<1:0> = 00), the system clock source comes from the main oscillator that is selected by the

FOSC2:FOSC0 configuration bits in Configuration Word 1 register. When the bits are set in any other manner, the system clock source is provided by the Timer1 oscillator (SCS1:SCS0 = 01) or from the internal oscillator block (SCS1:SCS0 = 10). After a Reset, SCS<1:0> are always set to '00'.

Note: The instruction to immediately follow the modification of SCS<1:0> will have an instruction time (Tcy) based on the previous clock source. This should be taken into consideration when developing time dependant code.

The Internal Oscillator Select bits, IRCF2:IRCF0, select the frequency output of the internal oscillator block that is used to drive the system clock. The choices are the INTRC source (31.25 kHz), the INTOSC source (8 MHz) or one of the six frequencies derived from the INTOSC postscaler (125 kHz to 4 MHz). Changing the configuration of these bits has an immediate change on the multiplexor's frequency output.

The OSTS and IOFS bits indicate the status of the primary oscillator and INTOSC source; these bits are set when their respective oscillators are stable. In particular, OSTS indicates that the Oscillator Start-up Timer has timed out.

4.6.2 CLOCK SWITCHING

Clock switching will occur for the following reasons:

- The FCMEN (CONFIG2<0>) bit is set, the device is running from the primary oscillator and the primary oscillator fails. The clock source will be the internal RC oscillator.
- The FCMEN bit is set, the device is running from the T1OSC and T1OSC fails. The clock source will be the internal RC oscillator.
- Following a wake-up due to a Reset or a POR, when the device is configured for Two-Speed Start-up mode, switching will occur between the INTRC and the system clock defined by the FOSC<2:0> bits.
- A wake-up from Sleep occurs due to an interrupt or WDT wake-up and Two-Speed Start-up is enabled. If the primary clock is XT, HS or LP, the clock will switch between the INTRC and the primary system clock after 1024 clocks (OST) and 8 clocks of the primary oscillator. This is conditional upon the SCS bits being set equal to '00'.
- SCS bits are modified from their original value.
- IRCF bits are modified from their original value.

Note: Because the SCS bits are cleared on any Reset, no clock switching will occur on a Reset unless the Two-Speed Start-up is enabled and the primary clock is XT, HS or LP. The device will wait for the primary clock to become stable before execution begins (Two-Speed Start-up disabled).

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4.6.3 CLOCK TRANSITION AND WDT

When clock switching is performed, the Watchdog Timer is disabled because the Watchdog ripple counter is used as the Oscillator Start-up Timer.

Note: The OST is only used when switching to XT, HS and LP Oscillator modes.

Once the clock transition is complete (i.e., new oscillator selection switch has occurred), the Watchdog counter is re-enabled with the counter reset. This allows the user to synchronize the Watchdog Timer to the start of execution at the new clock frequency.

REGISTER 4-2: OSCCON: OSCILLATOR CONTROL REGISTER (ADDRESS 8Fh)

U-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
—	IRCF2	IRCF1	IRCF0	OSTS ⁽¹⁾	IOFS	SCS1	SCS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **IRCF<2:0>:** Internal RC Oscillator Frequency Select bits

000 = 31.25 kHz

001 = 125 kHz

010 = 250 kHz

011 = 500 kHz

100 = 1 MHz

101 = 2 MHz

110 = 4 MHz

111 = 8 MHz

bit 3 **OSTS:** Oscillator Start-up Time-out Status bit⁽¹⁾

1 = Device is running from the primary system clock

0 = Device is running from T1OSC or INTRC as a secondary system clock

Note 1: Bit resets to '0' with Two-Speed Start-up mode and LP, XT or HS selected as the oscillator mode.

bit 2 **IOFS:** INTOSC Frequency Stable bit

1 = Frequency is stable

0 = Frequency is not stable

bit 1-0 **SCS<1:0>:** Oscillator Mode Select bits

00 = Oscillator mode defined by FOSC<2:0>

01 = T1OSC is used for system clock

10 = Internal RC is used for system clock

11 = Reserved

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

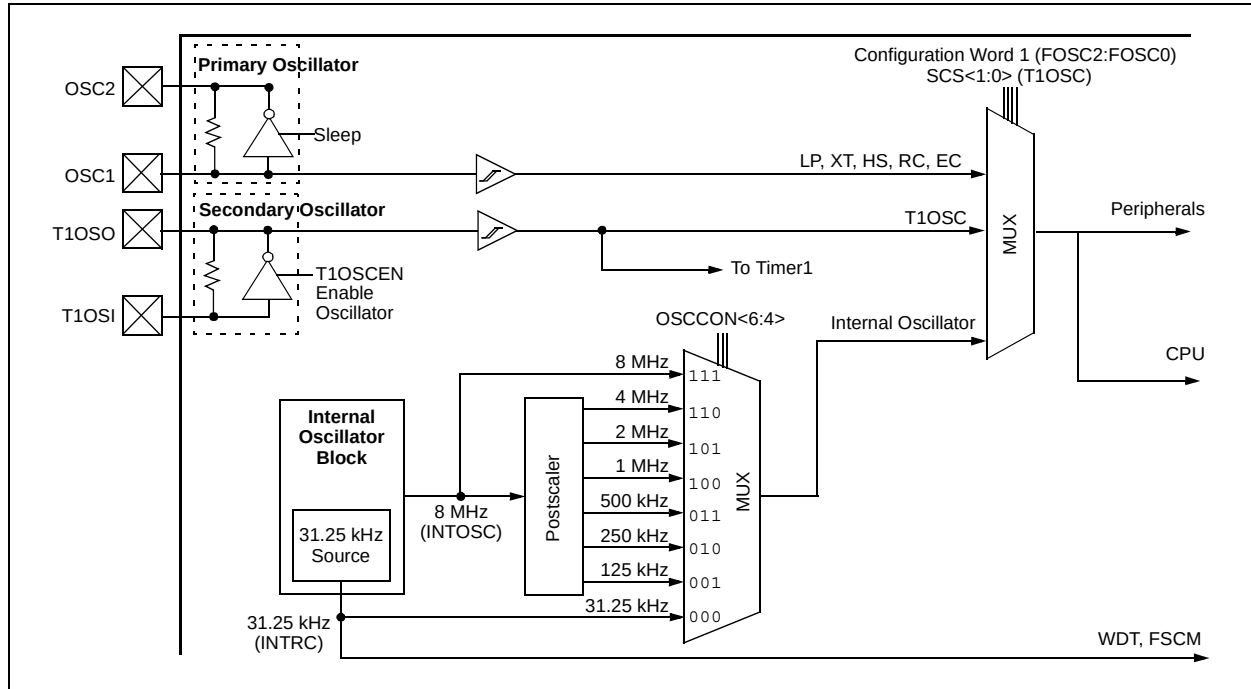
-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

FIGURE 4-6: PIC16F87/88 CLOCK DIAGRAM



4.6.4 MODIFYING THE IRCF BITS

The IRCF bits can be modified at any time regardless of which clock source is currently being used as the system clock. The internal oscillator allows users to change the frequency during run time. This is achieved by modifying the IRCF bits in the OSCCON register. The sequence of events that occur after the IRCF bits are modified is dependent upon the initial value of the IRCF bits before they are modified. If the INTRC (31.25 kHz, IRCF<2:0> = 000) is running and the IRCF bits are modified to any other value than '000', a 4 ms (approx.) clock switch delay is turned on. Code execution continues at a higher than expected frequency while the new frequency stabilizes. Time sensitive code should wait for the IOFS bit in the OSCCON register to become set before continuing. This bit can be monitored to ensure that the frequency is stable before using the system clock in time critical applications.

If the IRCF bits are modified while the internal oscillator is running at any other frequency than INTRC (31.25 kHz, IRCF<2:0> ≠ 000), there is no need for a 4 ms (approx.) clock switch delay. The new INTOSC frequency will be stable immediately after the **eight** falling edges. The IOFS bit will remain set after clock switching occurs.

Note: Caution must be taken when modifying the IRCF bits using BCF or BSF instructions. It is possible to modify the IRCF bits to a frequency that may be out of the VDD specification range; for example, VDD = 2.0V and IRCF = 111 (8 MHz).

4.6.5 CLOCK TRANSITION SEQUENCE

Following are three different sequences for switching the internal RC oscillator frequency.

- Clock before switch: 31.25 kHz (IRCF<2:0> = 000)
 1. IRCF bits are modified to an INTOSC/INTOSC postscaler frequency.
 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
 4. The IOFS bit is clear to indicate that the clock is unstable and a 4 ms (approx.) delay is started. Time dependent code should wait for IOFS to become set.
 5. Switchover is complete.
- Clock before switch: One of INTOSC/INTOSC postscaler (IRCF<2:0> ≠ 000)
 1. IRCF bits are modified to INTRC (IRCF<2:0> = 000).
 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
 4. Oscillator switchover is complete.

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- Clock before switch: One of INTOSC/INTOSC postscaler (IRCF<2:0> $\neq$ 000)
- 1. IRCF bits are modified to a different INTOSC/INTOSC postscaler frequency.
- 2. The clock switching circuitry waits for a falling edge of the current clock, at which point CLKO is held low.
- 3. The clock switching circuitry then waits for eight falling edges of requested clock, after which it switches CLKO to this new clock source.
- 4. The IOFS bit is set.
- 5. Oscillator switchover is complete.

4.6.6 OSCILLATOR DELAY UPON POWER-UP, WAKE-UP AND CLOCK SWITCHING

Table 4-3 shows the different delays invoked for various clock switching sequences. It also shows the delays invoked for POR and wake-up.

TABLE 4-3: OSCILLATOR DELAY EXAMPLES

Clock Switch		Frequency	Oscillator Delay	Comments
From	To			
Sleep/POR	INTRC T1OSC	31.25 kHz 32.768 kHz	CPU Start-up ⁽¹⁾	Following a wake-up from Sleep mode or POR, CPU start-up is invoked to allow the CPU to become ready for code execution.
	INTOSC/ INTOSC Postscaler	125 kHz-8 MHz	4 ms (approx.) and CPU Start-up ⁽¹⁾	
INTRC/Sleep	EC, RC	DC – 20 MHz		
INTRC (31.25 kHz)	EC, RC	DC – 20 MHz		
Sleep	LP, XT, HS	32.768 kHz-20 MHz	1024 Clock Cycles (OST)	Following a change from INTRC, an OST of 1024 cycles must occur.
INTRC (31.25 kHz)	INTOSC/ INTOSC Postscaler	125 kHz-8 MHz	4 ms (approx.)	Refer to Section 4.6.4 “Modifying the IRCF Bits” for further details.

Note 1: The 5-10 μ s start-up delay is based on a 1 MHz system clock.

4.7 Power-Managed Modes

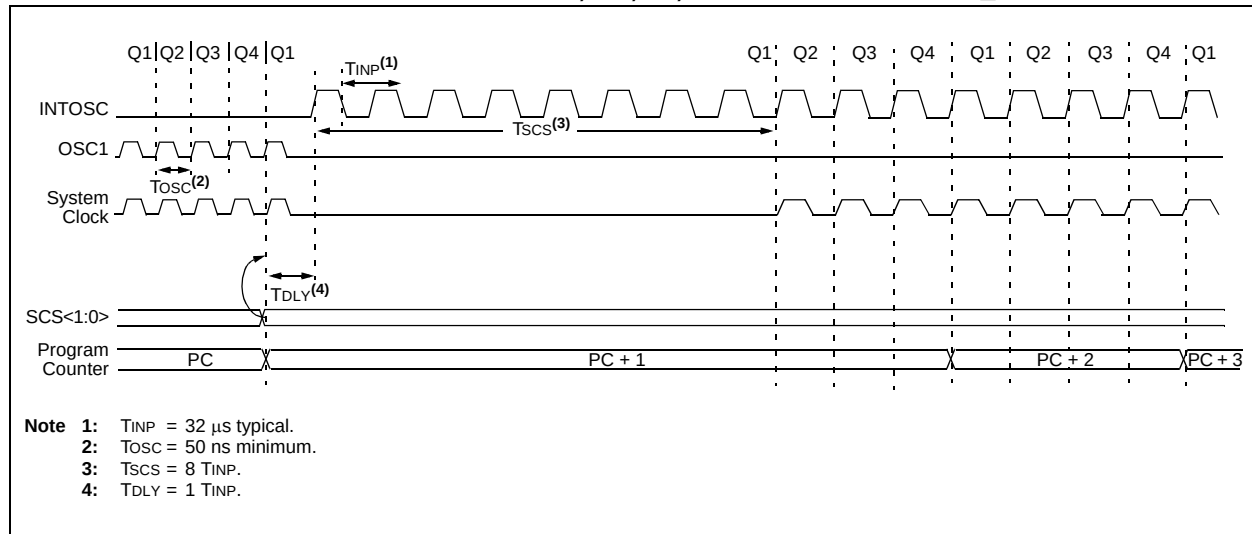
4.7.1 RC_RUN MODE

When SCS bits are configured to run from the INTRC, a clock transition is generated if the system clock is not already using the INTRC. The event will clear the OSTS bit, switch the system clock from the primary system clock (if $SCS<1:0> = 00$) determined by the value contained in the configuration bits, or from the T1OSC (if $SCS<1:0> = 01$) to the INTRC clock option and shut down the primary system clock to conserve power. Clock switching will not occur if the primary system clock is already configured as INTRC.

If the system clock does not come from the INTRC (31.25 kHz) when the SCS bits are changed and the IRCF bits in the OSCCON register are configured for a frequency other than INTRC, the frequency may not be stable immediately. The IOFS bit (OSCCON<2>) will be set when the INTOSC or postscaler frequency is stable, after 4 ms (approx.).

After a clock switch has been executed, the OSTS bit is cleared, indicating a low-power mode and the device does not run from the primary system clock. The internal Q clocks are held in the Q1 state until eight falling edge clocks are counted on the INTRC oscillator. After the eight clock periods have transpired, the clock input to the Q clocks is released and operation resumes (see Figure 4-7).

FIGURE 4-7: TIMING DIAGRAM FOR XT, HS, LP, EC AND EXTRC TO RC_RUN MODE



4.7.2 SEC_RUN MODE

The core and peripherals can be configured to be clocked by T1OSC using a 32.768 kHz crystal. The crystal must be connected to the T1OSO and T1OSI pins. This is the same configuration as the low-power timer circuit (see **Section 7.6 “Timer1 Oscillator”**). When SCS bits are configured to run from T1OSC, a clock transition is generated. It will clear the OSTS bit, switch the system clock from either the primary system clock or INTRC, depending on the value of SCS<1:0> and FOSC<2:0>, to the external low-power Timer1 oscillator input (T1OSC) and shut down the primary system clock to conserve power.

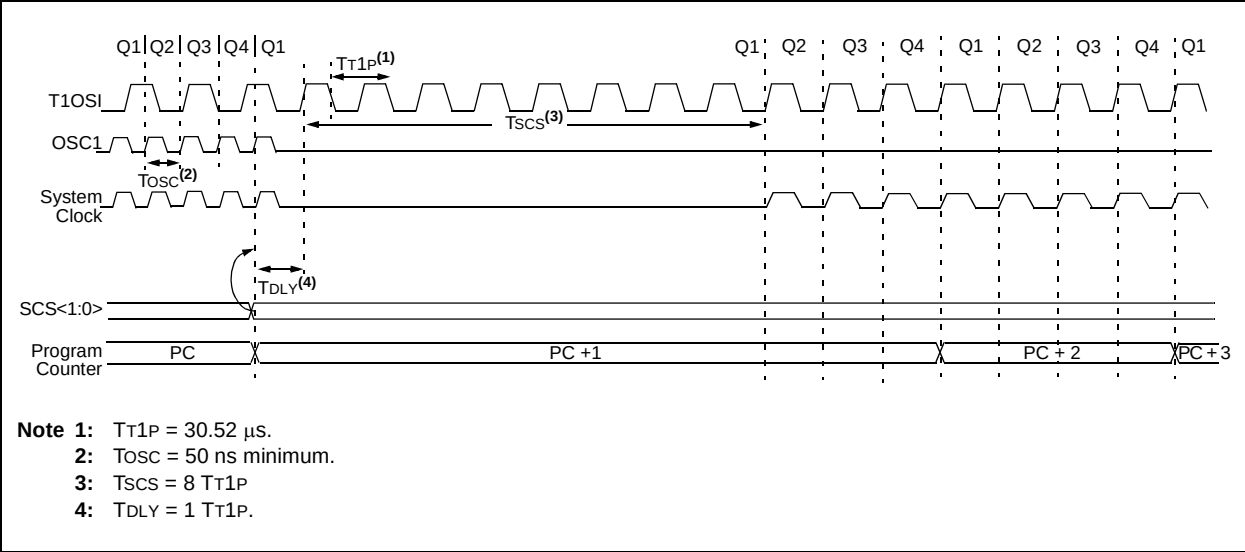
After a clock switch has been executed, the internal Q clocks are held in the Q1 state until eight falling edge clocks are counted on the T1OSC. After the eight clock periods have transpired, the clock input to the Q clocks is released and operation resumes (see Figure 4-8). In addition, T1RUN (In T1CON) is set to indicate that T1OSC is being used as the system clock.

- Note 1: The T1OSCEN bit must be enabled and it is the user's responsibility to ensure T1OSC is stable before clock switching to the T1OSC input clock can occur.
- 2: When T1OSCEN = 0, the following possible effects result.

Original SCS<1:0>	Modified SCS<1:0>	Final SCS<1:0>
00	01	00 – no change
00	11	10 – INTRC
10	11	10 – no change
10	01	00 – Oscillator defined by FOSC<2:0>

A clock switching event will occur if the final state of the SCS bits is different from the original.

FIGURE 4-8: TIMING DIAGRAM FOR SWITCHING TO SEC_RUN MODE



4.7.3 SEC_RUN/RC_RUN TO PRIMARY CLOCK SOURCE

When switching from a SEC_RUN or RC_RUN mode back to the primary system clock, following a change of SCS<1:0> to '00', the sequence of events that takes place will depend upon the value of the FOSC bits in the Configuration register. If the primary clock source is configured as a crystal (HS, XT or LP), then the transition will take place after 1024 clock cycles. This is necessary because the crystal oscillator has been powered down until the time of the transition. In order to provide the system with a reliable clock when the changeover has occurred, the clock will not be released to the changeover circuit until the 1024 count has expired.

During the oscillator start-up time, the system clock comes from the current system clock. Instruction execution and/or peripheral operation continues using the currently selected oscillator as the CPU clock source, until the necessary clock count has expired, to ensure that the primary system clock is stable.

To know when the OST has expired, the OSTS bit should be monitored. OSTS = 1 indicates that the Oscillator Start-up Timer has timed out and the system clock comes from the primary clock source.

Following the oscillator start-up time, the internal Q clocks are held in the Q1 state until eight falling edge clocks are counted from the primary system clock. The clock input to the Q clocks is then released and operation resumes with the primary system clock determined by the FOSC bits (see Figure 4-10).

When in SEC_RUN mode, the act of clearing the T1OSCEN bit in the T1CON register will cause SCS<0> to be cleared, which causes the SCS<1:0> bits to revert to '00' or '10' depending on what SCS<1> is. Although the T1OSCEN bit was cleared, T1OSC will be enabled and instruction execution will continue until the OST time-out for the main system clock is complete. At that time, the system clock will switch from the T1OSC to the primary clock or the INTRC. Following this, the T1 oscillator will be shut down.

Note: If the primary system clock is either RC or EC, an internal delay timer (5-10 μ s) will suspend operation after exiting Secondary Clock mode to allow the CPU to become ready for code execution.

4.7.3.1 Returning to Primary Clock Source Sequence

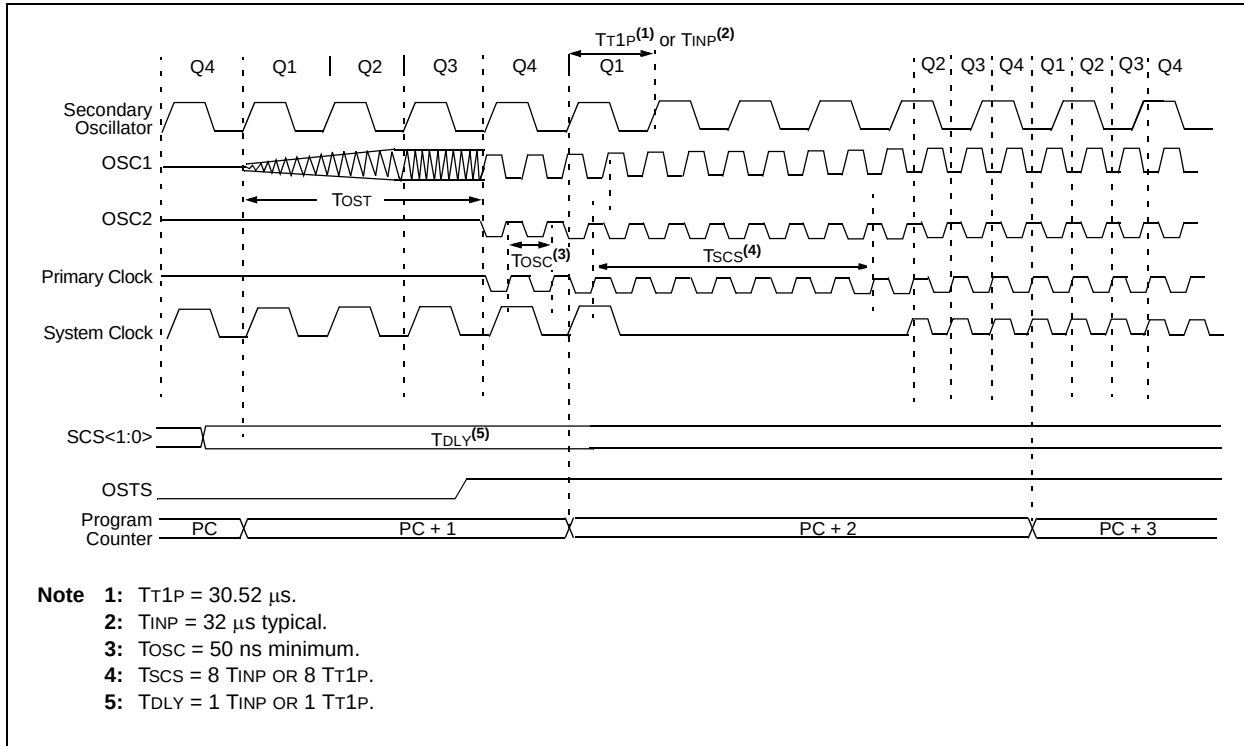
Changing back to the primary oscillator from SEC_RUN or RC_RUN can be accomplished by either changing SCS<1:0> to '00', or clearing the T1OSCEN bit in the T1CON register (if T1OSC was the secondary clock).

The sequence of events that follows is the same for both modes:

1. If the primary system clock is configured as EC, RC or INTRC, then the OST time-out is skipped. Skip to step 3.
2. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active, waiting for 1024 clocks of the primary system clock.
3. On the following Q1, the device holds the system clock in Q1.
4. The device stays in Q1 while eight falling edges of the primary system clock are counted.
5. Once the eight counts transpire, the device begins to run from the primary oscillator.
6. If the secondary clock was INTRC and the primary is not INTRC, the INTRC will be shut down to save current providing that the INTRC is not being used for any other function, such as WDT or Fail-Safe Clock monitoring.
7. If the secondary clock was T1OSC, the T1OSC will continue to run if T1OSCEN is still set; otherwise, the T1 oscillator will be shut down.

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FIGURE 4-9: TIMING FOR TRANSITION BETWEEN SEC_RUN/RC_RUN AND PRIMARY CLOCK



4.7.3.2 Returning to Primary Oscillator with a Reset

A Reset will clear SCS<1:0> back to '00'. The sequence for starting the primary oscillator following a Reset is the same for all forms of Reset, including POR. There is no transition sequence from the alternate system clock to the primary system clock on a Reset condition. Instead, the device will reset the state of the OSCCON register and default to the primary system clock. The sequence of events that takes place after this will depend upon the value of the FOSC bits in the Configuration register. If the external oscillator is configured as a crystal (HS, XT or LP), the CPU will be held in the Q1 state until 1024 clock cycles have transpired on the primary clock. This is necessary because the crystal oscillator has been powered down until the time of the transition.

During the oscillator start-up time, instruction execution and/or peripheral operation is suspended.

Note: If Two-Speed Clock Start-up mode is enabled, the INTRC will act as the system clock until the OST timer has timed out.

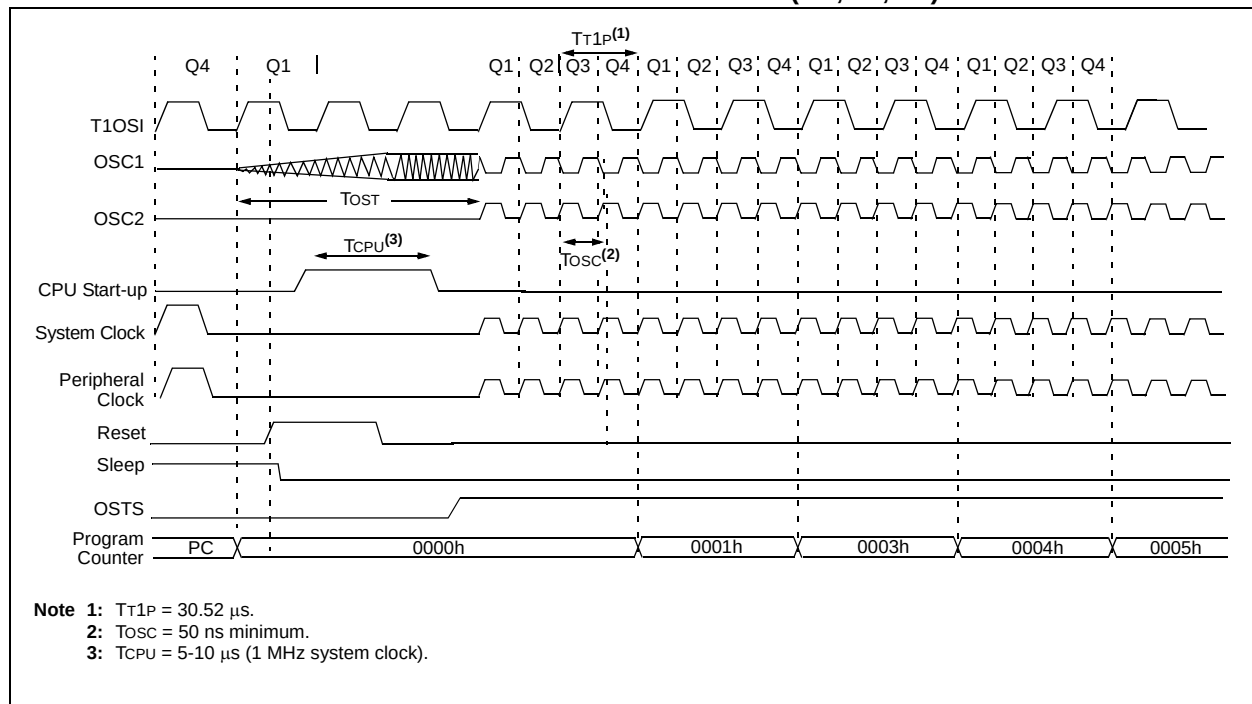
If the primary system clock is either RC, EC or INTRC, the CPU will begin operating on the first Q1 cycle following the wake-up event. This means that there is

no oscillator start-up time required because the primary clock is already stable; however, there is a delay between the wake-up event and the following Q2. An internal delay timer of 5-10 μ s will suspend operation after the Reset to allow the CPU to become ready for code execution. The CPU and peripheral clock will be held in the first Q1.

The sequence of events is as follows:

1. A device Reset is asserted from one of many sources (WDT, BOR, MCLR, etc.).
2. The device resets and the CPU start-up timer is enabled if in Sleep mode. The device is held in Reset until the CPU start-up time-out is complete.
3. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active waiting for 1024 clocks of the primary system clock. While waiting for the OST, the device will be held in Reset. The OST and CPU start-up timers run in parallel.
4. After both the CPU start-up and OST timers have timed out, the device will wait for one additional clock cycle and instruction execution will begin.

FIGURE 4-10: PRIMARY SYSTEM CLOCK AFTER RESET (HS, XT, LP)



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FIGURE 4-11: PRIMARY SYSTEM CLOCK AFTER RESET (EC, RC, INTRC)

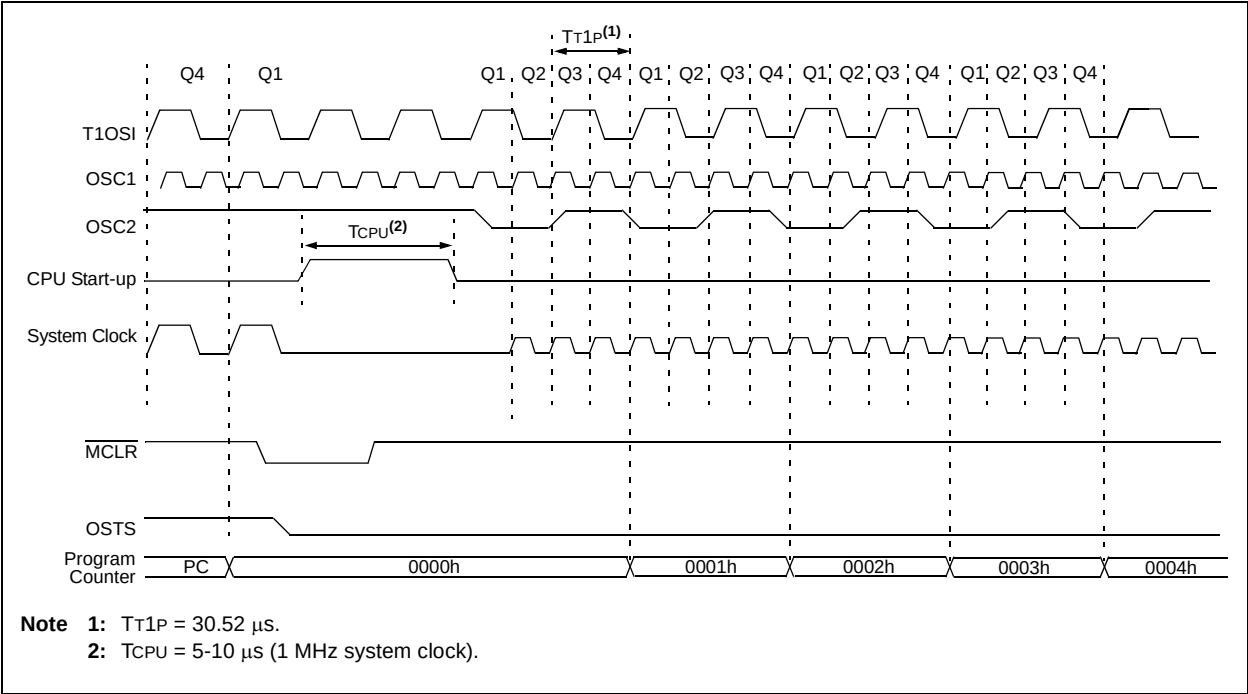


TABLE 4-4: CLOCK SWITCHING MODES

Current System Clock	SCS Bits <1:0> Modified to:	Delay	OSTS Bit	IOFS Bit	T1RUN Bit	New System Clock	Comments
LP, XT, HS, T1OSC, EC, RC	10 (INTRC) FOSC<2:0> = LP, XT or HS	8 Clocks of INTRC	0	1 ⁽¹⁾	0	INTRC or INTOSC or INTOSC Postscaler	The internal RC oscillator frequency is dependant upon the IRCF bits.
LP, XT, HS, INTRC, EC, RC	01 (T1OSC) FOSC<2:0> = LP, XT or HS	8 Clocks of T1OSC	0	N/A	1	T1OSC	T1OSCEN bit must be enabled.
INTRC T1OSC	00 FOSC<2:0> = EC or FOSC<2:0> = RC	8 Clocks of EC or RC	1	N/A	0	EC or RC	
INTRC T1OSC	00 FOSC<2:0> = LP, XT, HS	1024 Clocks (OST) + 8 Clocks of LP, XT, HS	1	N/A	0	LP, XT, HS	During the 1024 clocks, program execution is clocked from the secondary oscillator until the primary oscillator becomes stable.
LP, XT, HS	00 (Due to Reset) LP, XT, HS	1024 Clocks (OST)	1	N/A	0	LP, XT, HS	When a Reset occurs, there is no clock transition sequence. Instruction execution and/or peripheral operation is suspended unless Two-Speed Start-up mode is enabled, after which the INTRC will act as the system clock until the OST timer has expired.

Note 1: If the new clock source is the INTOSC or INTOSC postscaler, then the IOFS bit will be set 4 ms (approx.) after the clock change.

4.7.4 EXITING SLEEP WITH AN INTERRUPT

Any interrupt, such as WDT or INT0, will cause the part to leave the Sleep mode.

The SCS bits are unaffected by a `SLEEP` command and are the same before and after entering and leaving Sleep. The clock source used after an exit from Sleep is determined by the SCS bits.

4.7.4.1 Sequence of Events

If $SCS<1:0> = 00$:

1. The device is held in Sleep until the CPU start-up time-out is complete.
2. If the primary system clock is configured as an external oscillator (HS, XT, LP), then the OST will be active waiting for 1024 clocks of the primary system clock. While waiting for the OST, the device will be held in Sleep unless Two-Speed Start-up is enabled. The OST and CPU start-up timers run in parallel. Refer to **Section 15.12.3 “Two-Speed Clock Start-up Mode”** for details on Two-Speed Start-up.
3. After both the CPU start-up and OST timers have timed out, the device will exit Sleep and begin instruction execution with the primary clock defined by the FOSC bits.

If $SCS<1:0> = 01$ or 10 :

1. The device is held in Sleep until the CPU start-up time-out is complete.
2. After the CPU start-up timer has timed out, the device will exit Sleep and begin instruction execution with the selected oscillator mode.

Note: If a user changes $SCS<1:0>$ just before entering Sleep mode, the system clock used when exiting Sleep mode could be different than the system clock used when entering Sleep mode.

As an example, if $SCS<1:0> = 01$ and T1OSC is the system clock and the following instructions are executed:

```
BCF      OSCCON, SCS0
SLEEP
```

then a clock change event is executed. If the primary oscillator is XT, LP or HS, the core will continue to run off T1OSC and execute the `SLEEP` command.

When Sleep is exited, the part will resume operation with the primary oscillator after the OST has expired.

5.0 I/O PORTS

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

Additional information on I/O ports may be found in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

5.1 PORTA and the TRISA Register

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Note: On a Power-on Reset, the pins PORTA<4:0> are configured as analog inputs and read as '0'.

Reading the PORTA register, reads the status of the pins, whereas writing to it, will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the port data latch.

Pin RA4 is multiplexed with the Timer0 module clock input. On PIC16F88 devices, it is also multiplexed with an analog input to become the RA4/AN4/T0CKI/C2OUT pin. The RA4/AN4/T0CKI/C2OUT pin is a Schmitt Trigger input and full CMOS output driver.

Pin RA5 is multiplexed with the Master Clear module input. The RA5/MCLR/VPP pin is a Schmitt Trigger input.

Pin RA6 is multiplexed with the oscillator module input and external oscillator output. Pin RA7 is multiplexed with the oscillator module input and external oscillator input. Pin RA6/OSC2/CLKO and pin RA7/OSC1/CLKI are Schmitt Trigger inputs and full CMOS output drivers.

Pins RA<1:0> are multiplexed with analog inputs. Pins RA<3:2> are multiplexed with analog inputs and comparator outputs. On PIC16F88 devices, pins RA<3:2> are also multiplexed with the VREF inputs. Pins RA<3:0> have TTL inputs and full CMOS output drivers.

EXAMPLE 5-1: INITIALIZING PORTA

```
BANKSEL PORTA    ; select bank of PORTA
CLRF   PORTA     ; Initialize PORTA by
                  ; clearing output
                  ; data latches
BANKSEL ANSEL     ; Select Bank of ANSEL
MOVLW   0x00      ; Configure all pins
MOVWF   ANSEL     ; as digital inputs

MOVLW   0xFF      ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISA     ; Set RA<7:0> as inputs
```

TABLE 5-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit 0	TTL	Input/output or analog input.
RA1/AN1	bit 1	TTL	Input/output or analog input.
RA2/AN2/CVREF/VREF ⁽²⁾	bit 2	TTL	Input/output, analog input, VREF- or comparator VREF output.
RA3/AN3/VREF+ ⁽²⁾ /C1OUT	bit 3	TTL	Input/output, analog input, VREF+ or comparator output.
RA4/AN4 ⁽²⁾ /T0CKI/C2OUT	bit 4	ST	Input/output, analog input, TMR0 external input or comparator output.
RA5/MCLR/VPP	bit 5	ST	Input, Master Clear (Reset) or programming voltage input.
RA6/OSC2/CLKO	bit 6	ST	Input/output, connects to crystal or resonator, oscillator output or 1/4 the frequency of OSC1 and denotes the instruction cycle in RC mode.
RA7/OSC1/CLKI	bit 7	ST/CMOS ⁽¹⁾	Input/output, connects to crystal or resonator or oscillator input.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

2: PIC16F88 only.

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TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
05h	PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000 ⁽¹⁾ xxx0 0000 ⁽²⁾	uuuu 0000 ⁽¹⁾ uuu0 0000 ⁽²⁾
85h	TRISA	TRISA7	TRISA6	TRISA5 ⁽³⁾	PORTA Data Direction Register					1111 1111	1111 1111
9Fh	ADCON1	ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—	0000 ----	0000 ----
9Bh	ANSEL ⁽⁴⁾	—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	-111 1111	-111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTA.

Note 1: This value applies only to the PIC16F87.

Note 2: This value applies only to the PIC16F88.

Note 3: Pin 5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

Note 4: PIC16F88 device only.

FIGURE 5-1: BLOCK DIAGRAM OF RA0/AN0:RA1/AN1 PINS

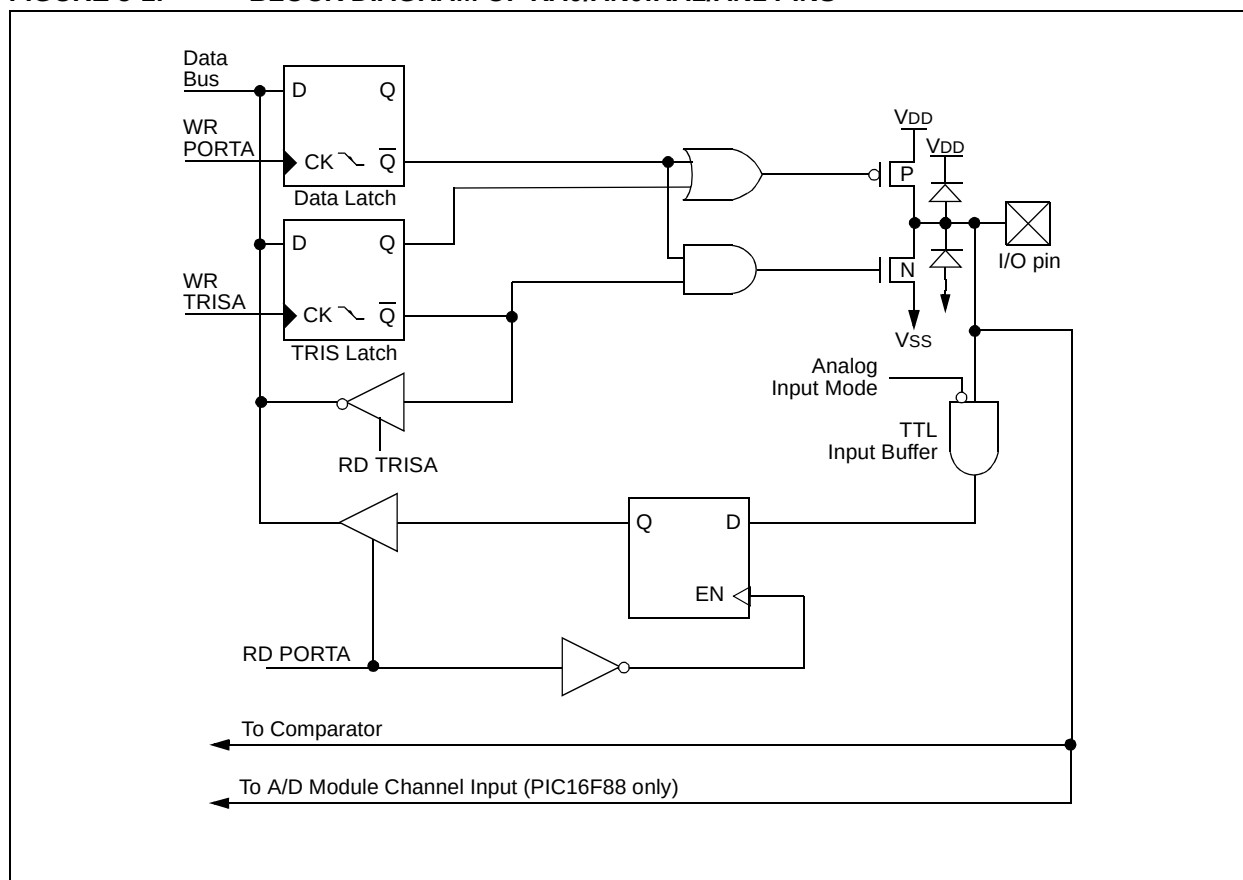


FIGURE 5-2: BLOCK DIAGRAM OF RA3/AN3/VREF+/C1OUT PIN

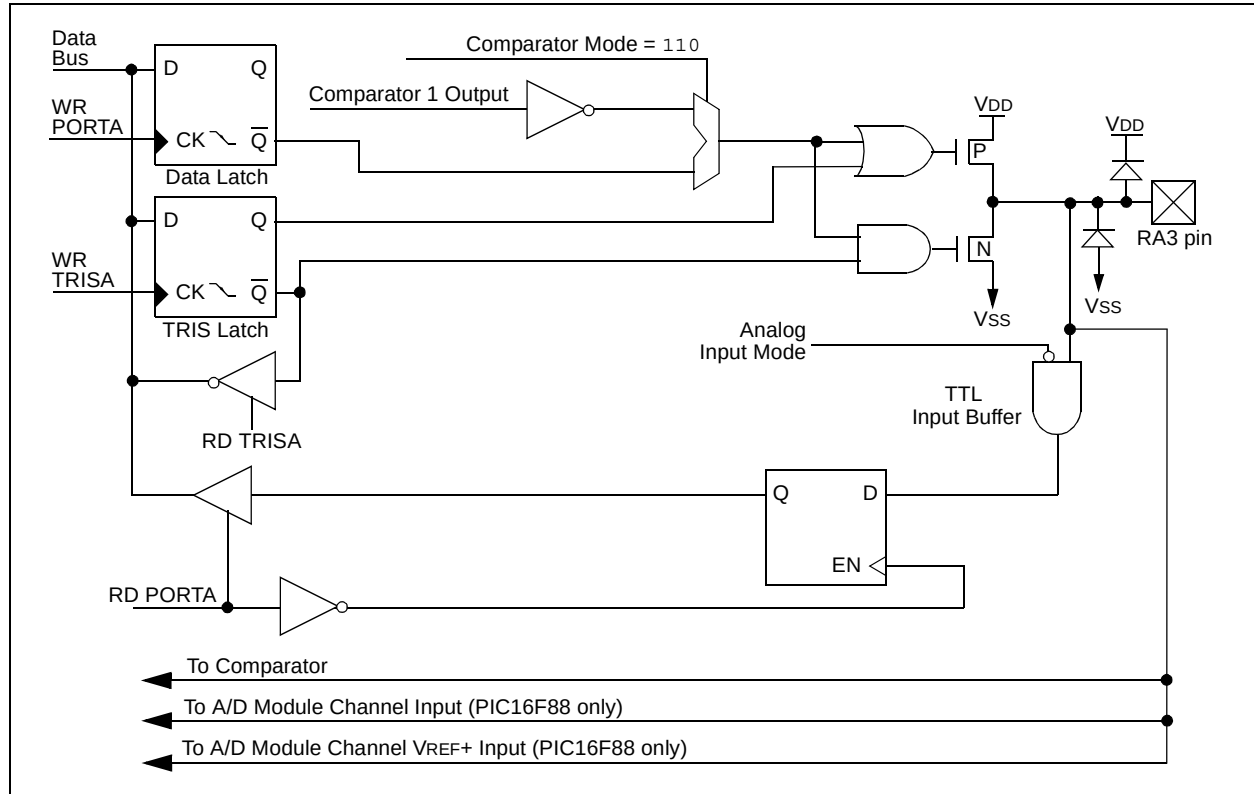
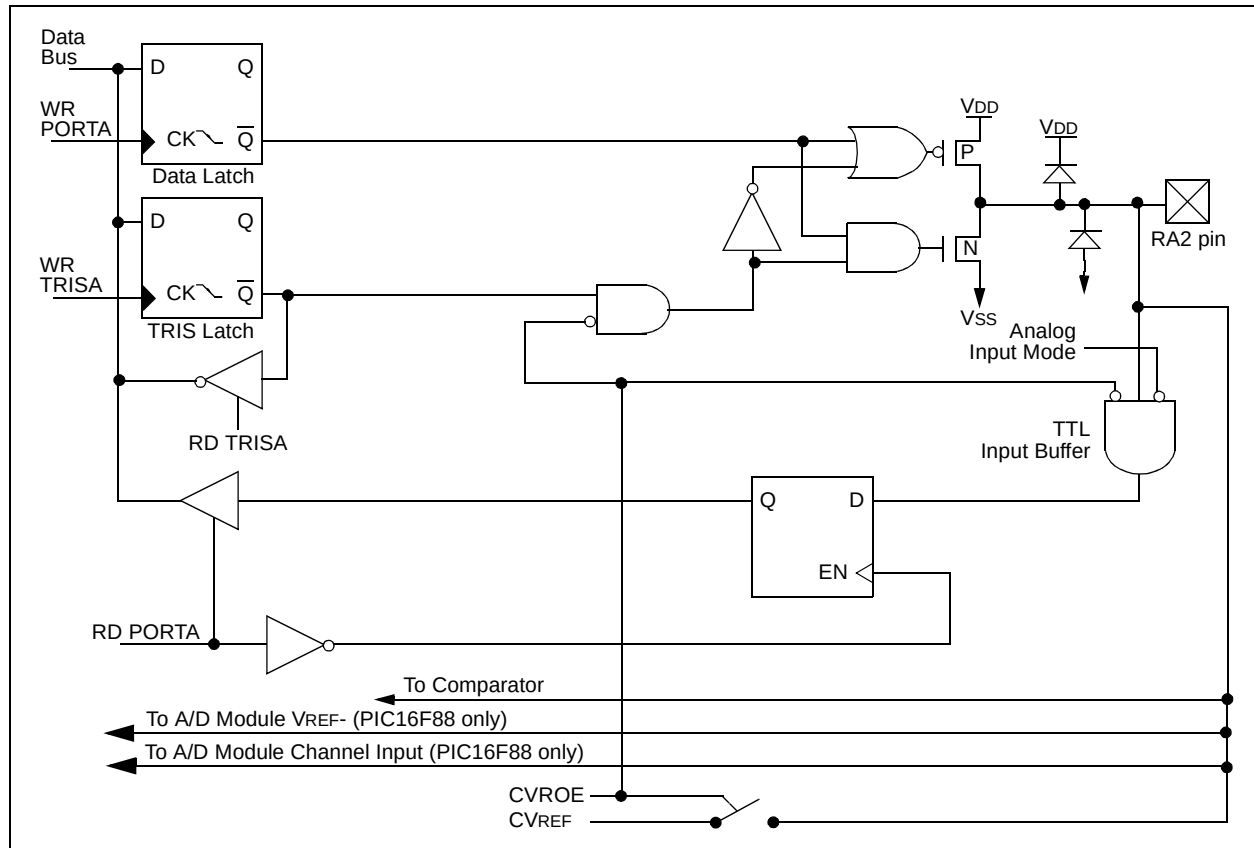


FIGURE 5-3: BLOCK DIAGRAM OF RA2/AN2/CVREF/VREF- PIN



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FIGURE 5-4: BLOCK DIAGRAM OF RA4/AN4/T0CKI/C2OUT PIN

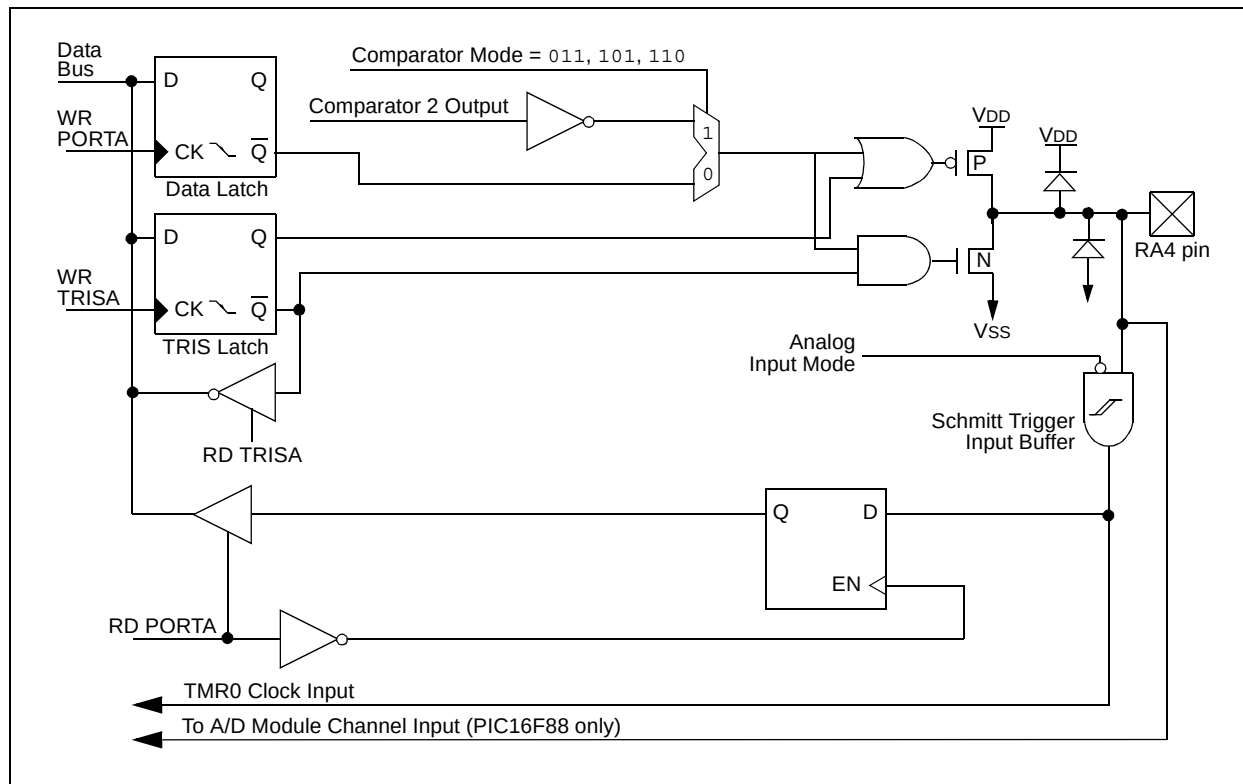


FIGURE 5-5: BLOCK DIAGRAM OF RA5/MCLR/VPP PIN

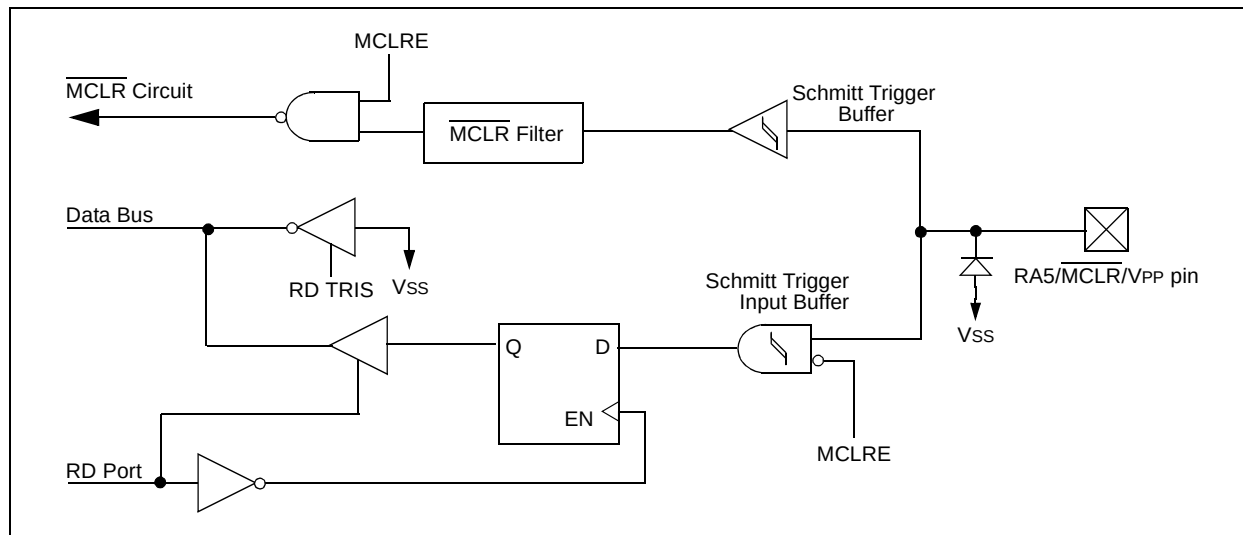
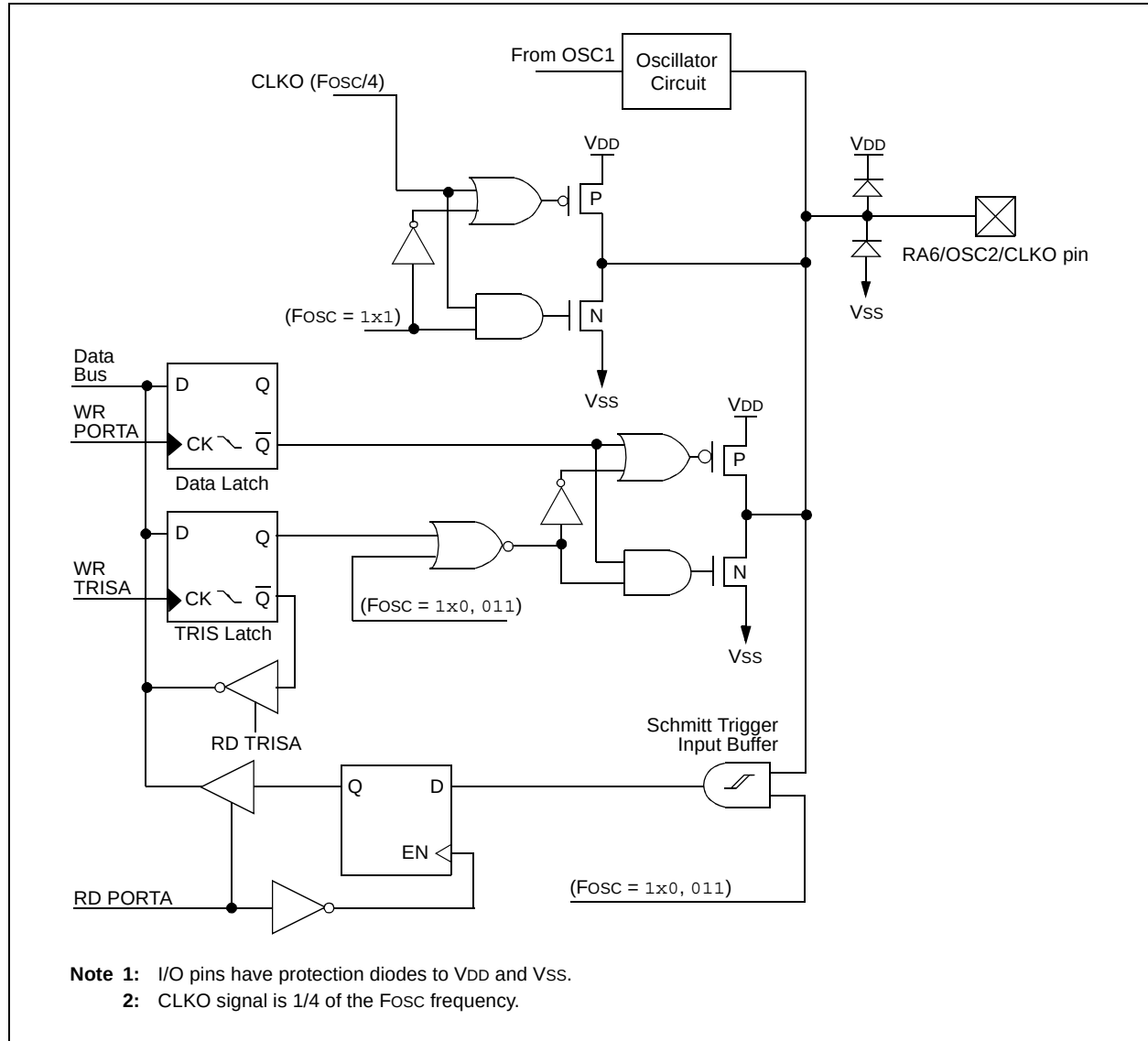
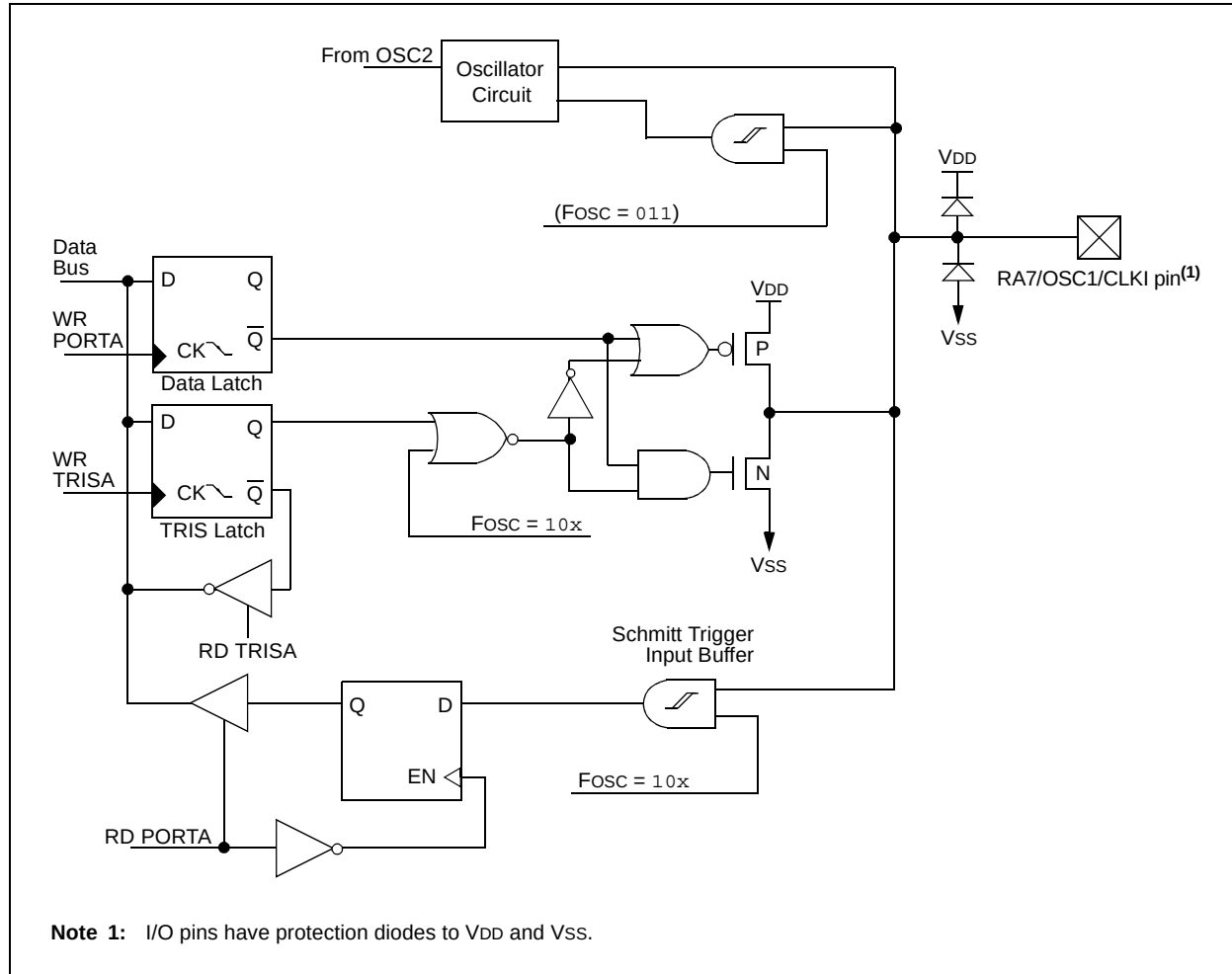


FIGURE 5-6: BLOCK DIAGRAM OF RA6/OSC2/CLKO PIN



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FIGURE 5-7: BLOCK DIAGRAM OF RA7/OSC1/CLKI PIN



5.2 PORTB and the TRISB Register

PORTB is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTION_REG<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of PORTB's pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with Flag bit RBIF (INTCON<0>).

This interrupt can wake the device from Sleep. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB. This will end the mismatch condition.
- b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

RB0/INT is an external interrupt input pin and is configured using the INTEDG bit (OPTION_REG<6>).

PORTB is multiplexed with several peripheral functions (see Table 5-3). PORTB pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTB pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. Since the TRIS bit override is in effect while the peripheral is enabled, read-modify-write instructions (BSF, BCF, XORWF) with TRISB as the destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

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TABLE 5-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT/CCP1 ⁽⁷⁾	bit 0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input. Capture input/Compare output/PWM output pin. Internal software programmable weak pull-up.
RB1/SDI/SDA	bit 1	TTL/ST ⁽⁵⁾	Input/output pin, SPI data input pin or I ² C™ data I/O pin. Internal software programmable weak pull-up.
RB2/SDO/RX/DT	bit 2	TTL/ST ⁽⁴⁾	Input/output pin, SPI data output pin. AUSART asynchronous receive or synchronous data. Internal software programmable weak pull-up.
RB3/PGM/CCP1 ^(3,7)	bit 3	TTL/ST ⁽²⁾	Input/output pin, programming in LVP mode or Capture input/Compare output/PWM output pin. Internal software programmable weak pull-up.
RB4/SCK/SCL	bit 4	TTL/ST ⁽⁵⁾	Input/output pin or SPI and I ² C clock pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5/SS/TX/CK	bit 5	TTL	Input/output pin or SPI slave select pin (with interrupt-on-change). AUSART asynchronous transmit or synchronous clock. Internal software programmable weak pull-up.
RB6/AN5 ⁽⁶⁾ /PGC/ T1OSO/T1CKI	bit 6	TTL/ST ⁽²⁾	Input/output pin, analog input ⁽⁶⁾ , serial programming clock (with interrupt-on-change), Timer1 oscillator output pin or Timer1 clock input pin. Internal software programmable weak pull-up.
RB7/AN6 ⁽⁶⁾ /PGD/ T1OSI	bit 7	TTL/ST ⁽²⁾	Input/output pin, analog input ⁽⁶⁾ , serial programming data (with interrupt-on-change) or Timer1 oscillator input pin. Internal software programmable weak pull-up.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: Low-Voltage ICSP™ Programming (LVP) is enabled by default, which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 18-pin mid-range devices.

4: This buffer is a Schmitt Trigger input when configured for CCP or SSP mode.

5: This buffer is a Schmitt Trigger input when configured for SPI or I²C mode.

6: PIC16F88 only.

7: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

TABLE 5-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

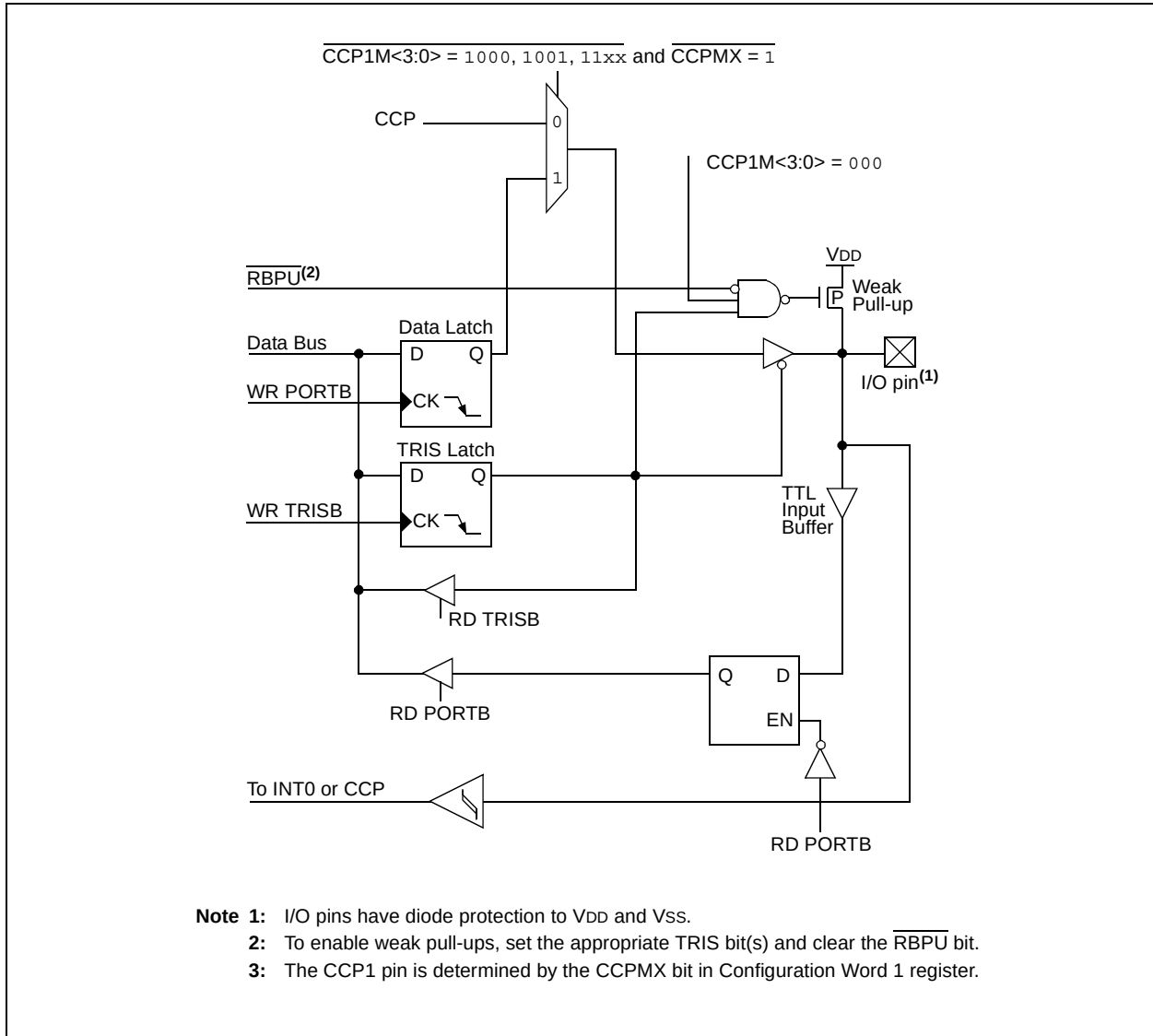
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx ⁽¹⁾ 00xx xxxx ⁽²⁾	uuuu uuuu ⁽¹⁾ 00uu uuuu ⁽²⁾
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBP	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
9Bh	ANSEL ⁽²⁾	—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	-111 1111	-111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTB.

Note 1: This value applies only to the PIC16F87.

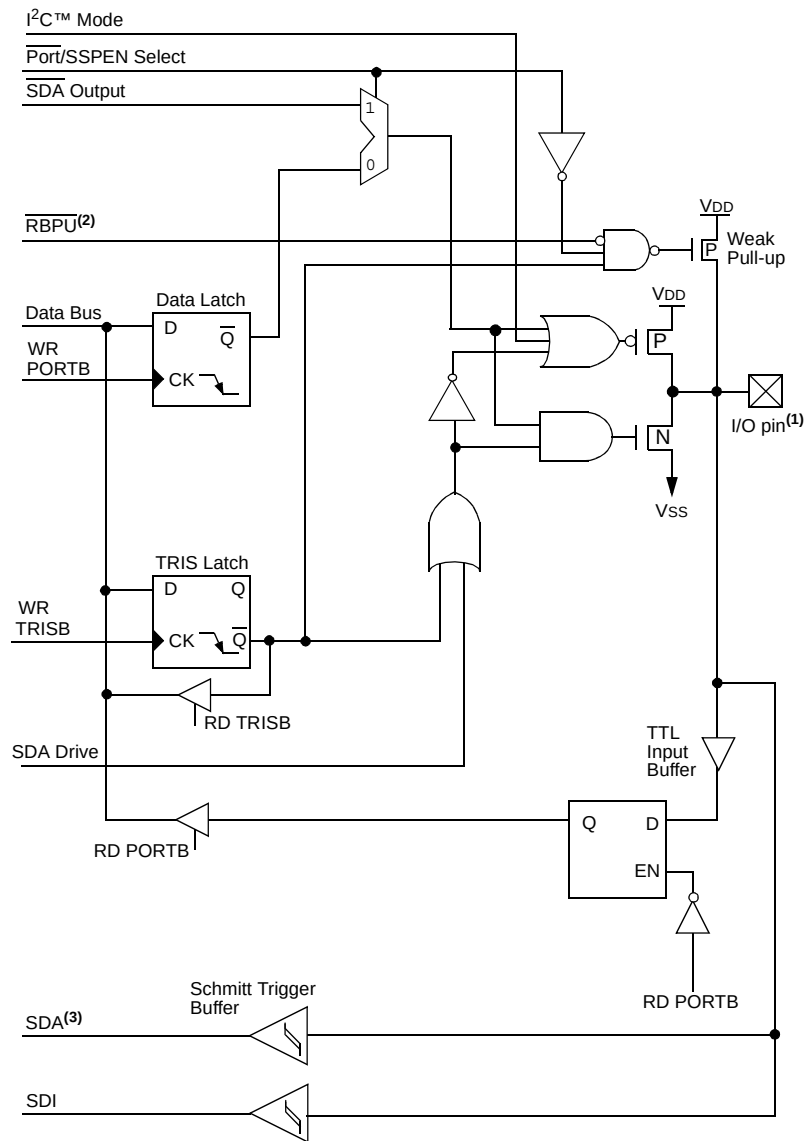
2: This value applies only to the PIC16F88.

FIGURE 5-8: BLOCK DIAGRAM OF RB0/INT/CCP1⁽³⁾ PIN



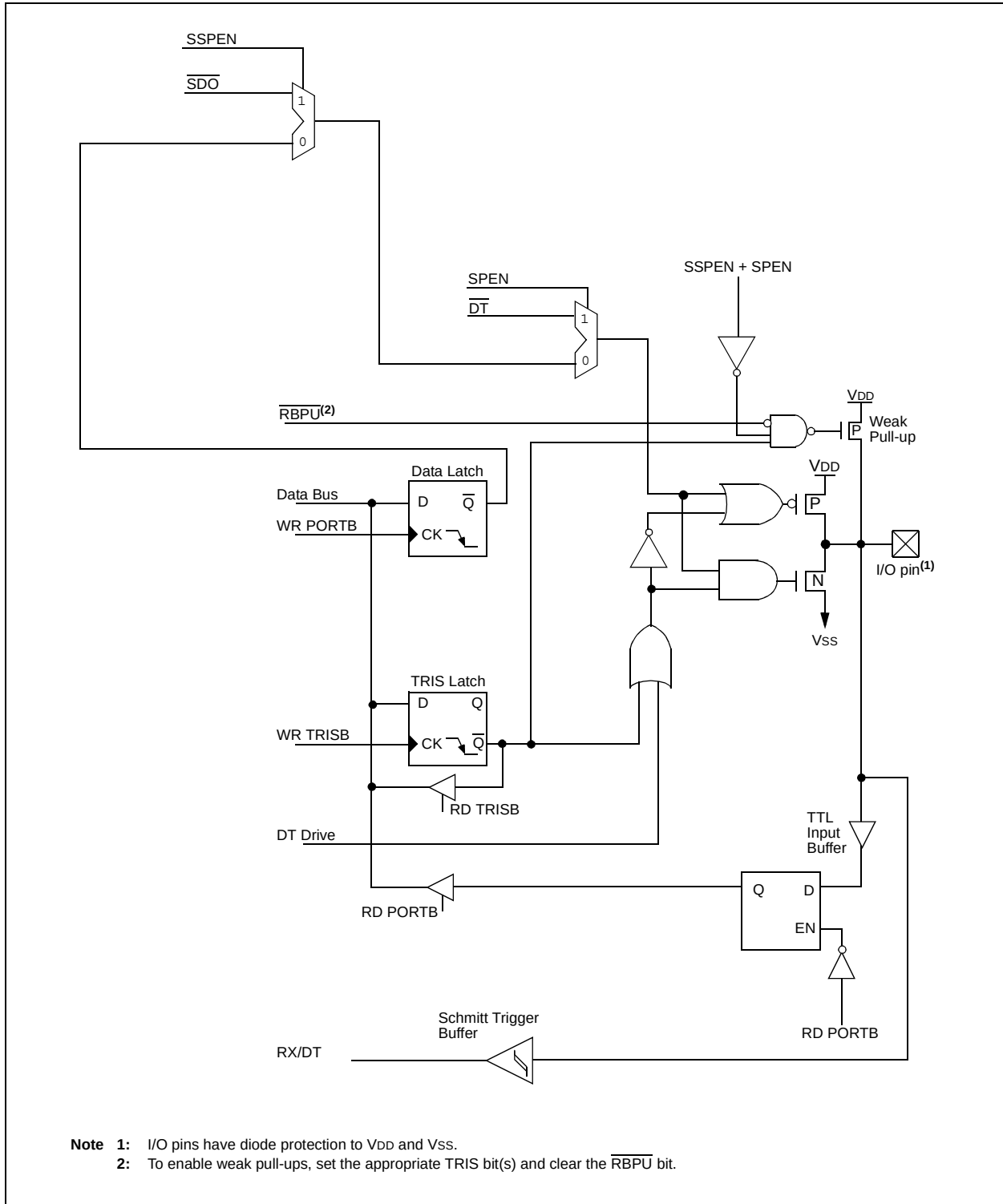
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FIGURE 5-9: BLOCK DIAGRAM OF RB1/SDI/SDA PIN



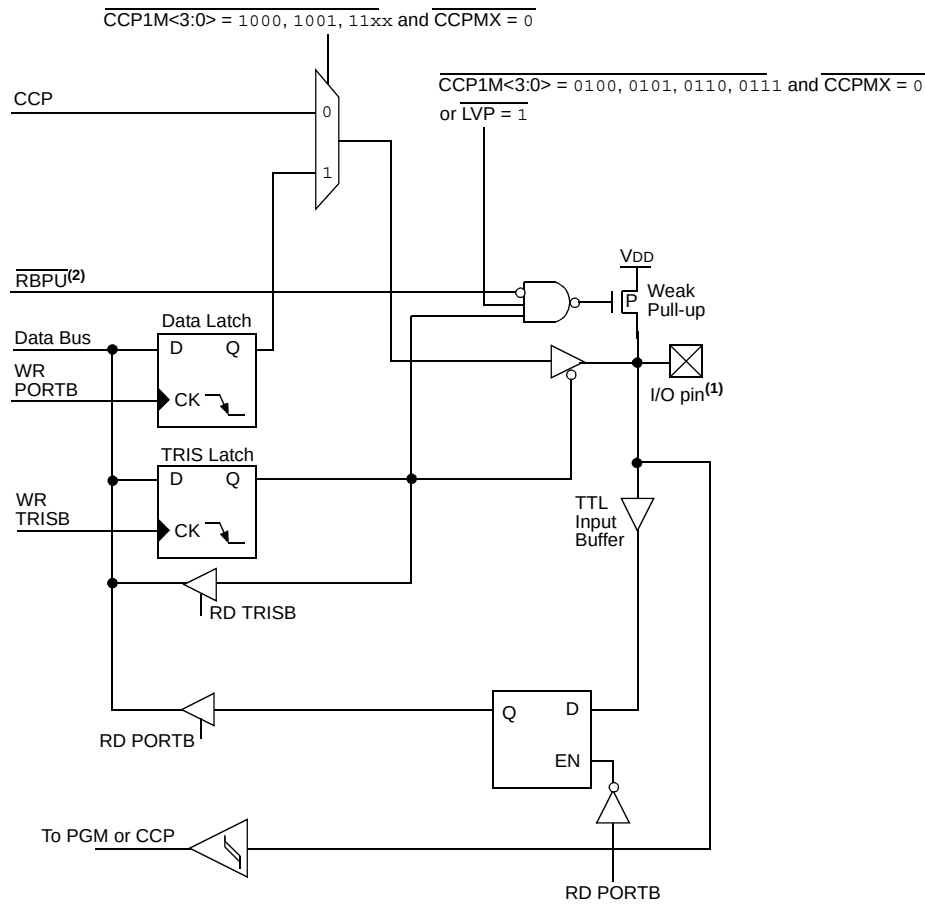
- Note**
- 1: I/O pins have diode protection to VDD and VSS.
 - 2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBP1}}$ bit.
 - 3: The SDA Schmitt conforms to the I²C specification.

FIGURE 5-10: BLOCK DIAGRAM OF RB2/SDO/RX/DT PIN



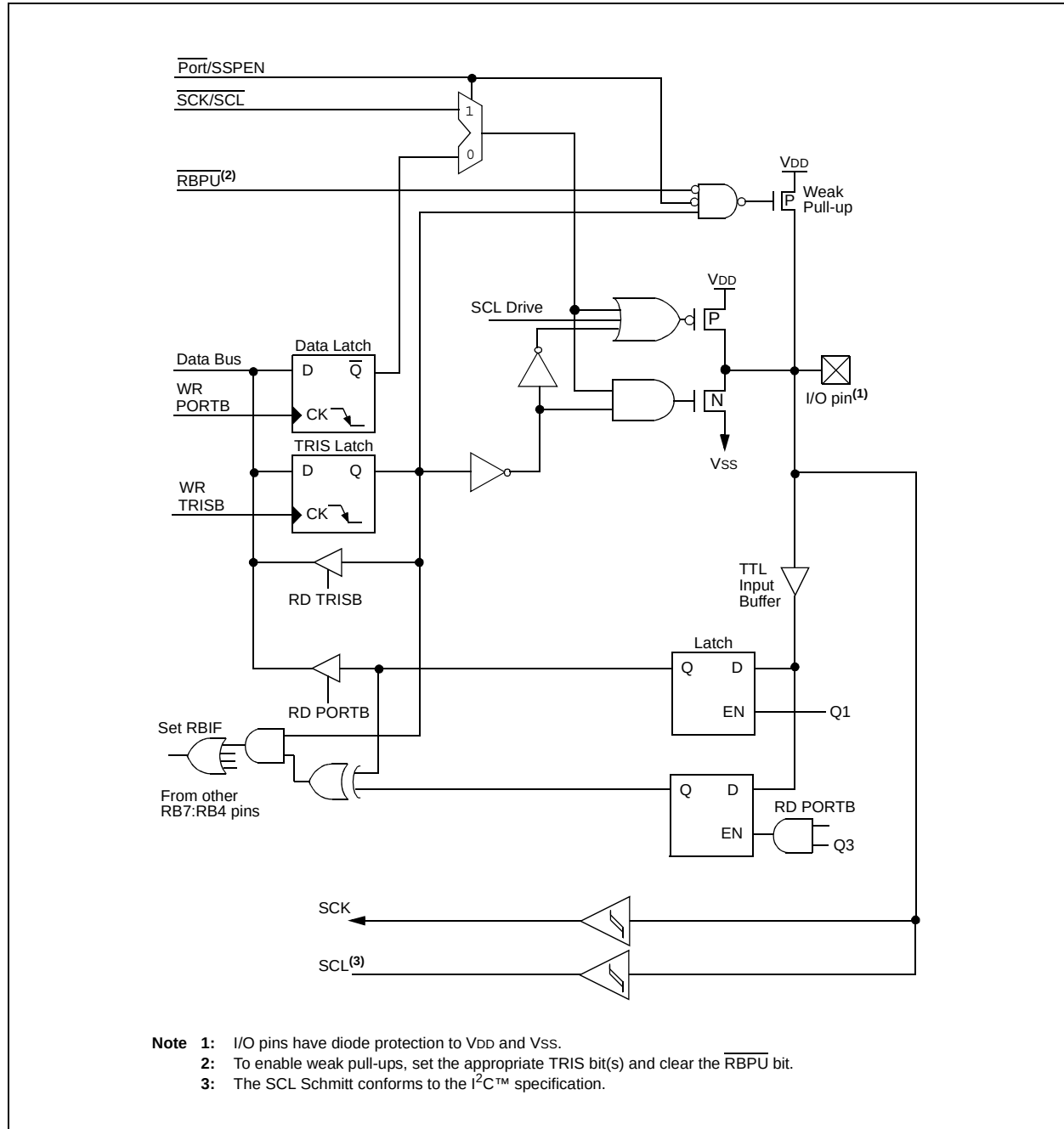
PIC16F87/88

FIGURE 5-11: BLOCK DIAGRAM OF RB3/PGM/CCP1⁽³⁾ PIN



- Note**
- 1: I/O pins have diode protection to VDD and VSS.
 - 2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the $\overline{\text{RBP}}$ bit.
 - 3: The CCP1 pin is determined by the CCPMX bit in Configuration Word 1 register.

FIGURE 5-12: BLOCK DIAGRAM OF RB4/SCK/SCL PIN



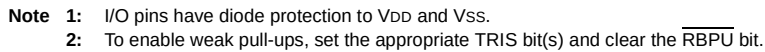
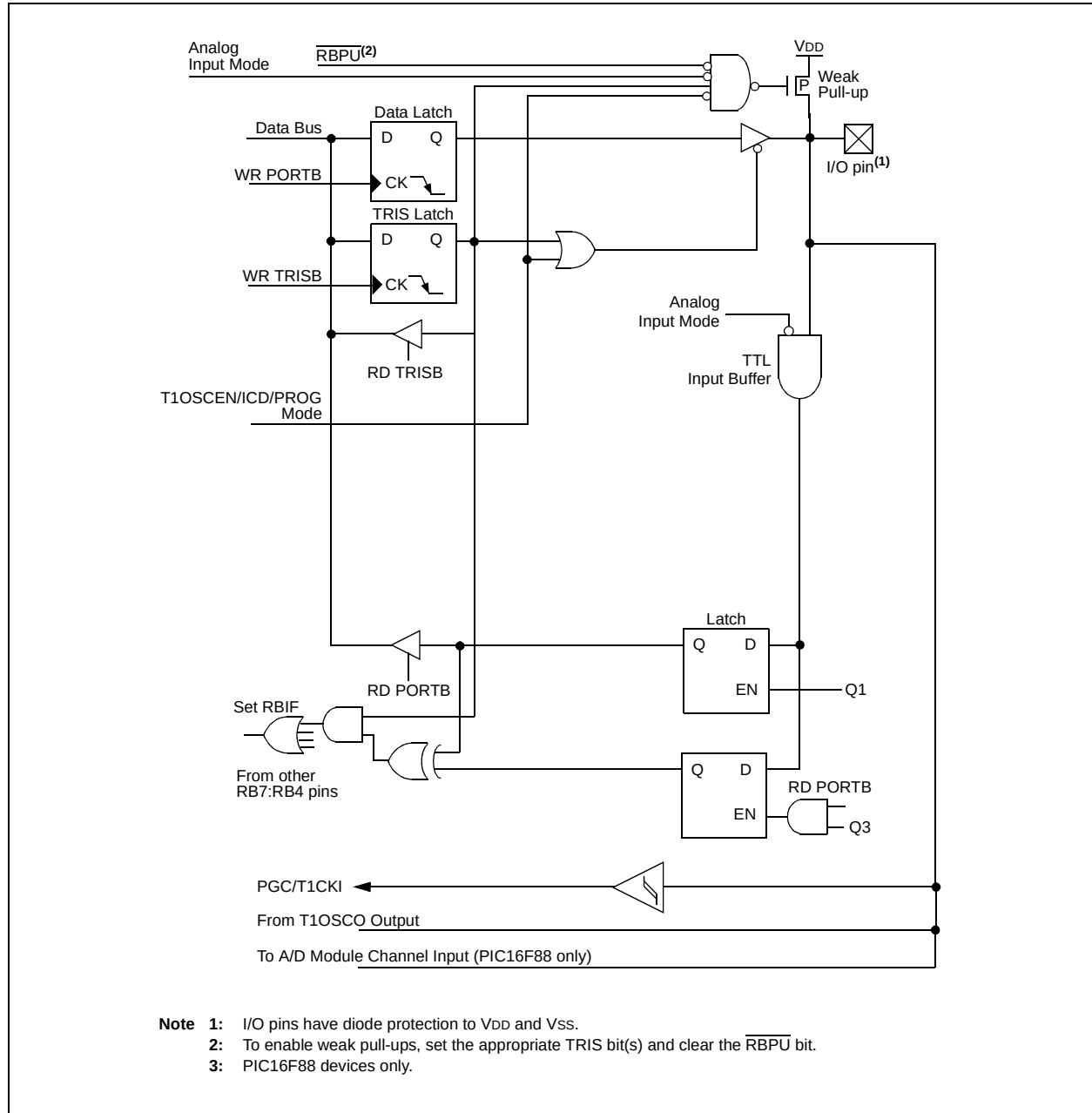
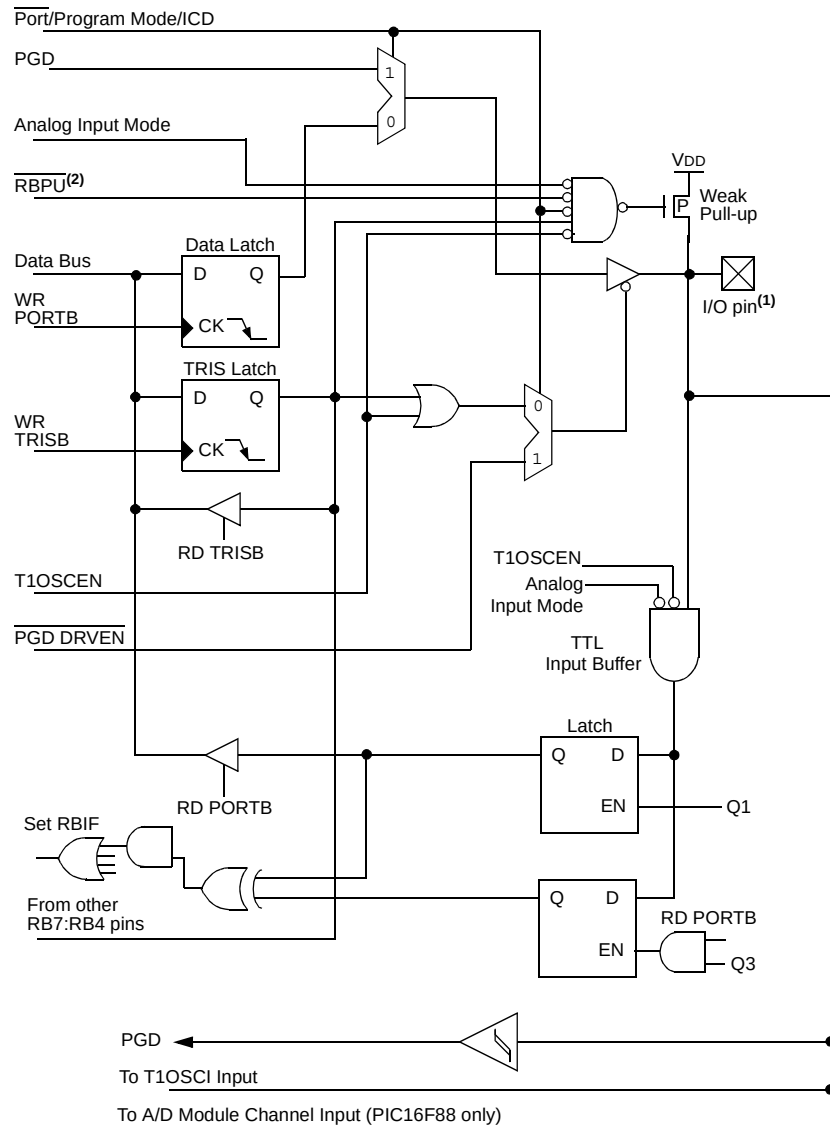


FIGURE 5-14: BLOCK DIAGRAM OF RB6/AN5⁽³⁾/PGC/T1OSO/T1CKI PIN



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FIGURE 5-15: BLOCK DIAGRAM OF RB7/AN6⁽³⁾/PGD/T1OSI PIN



- Note** 1: I/O pins have diode protection to VDD and VSS.
 2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit.
 3: PIC16F88 devices only.

6.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt-on-overflow from FFh to 00h
- Edge select for external clock

Additional information on the Timer0 module is available in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

Figure 6-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

6.1 Timer0 Operation

Timer0 operation is controlled through the OPTION_REG register (see Register 2-2). Timer mode is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

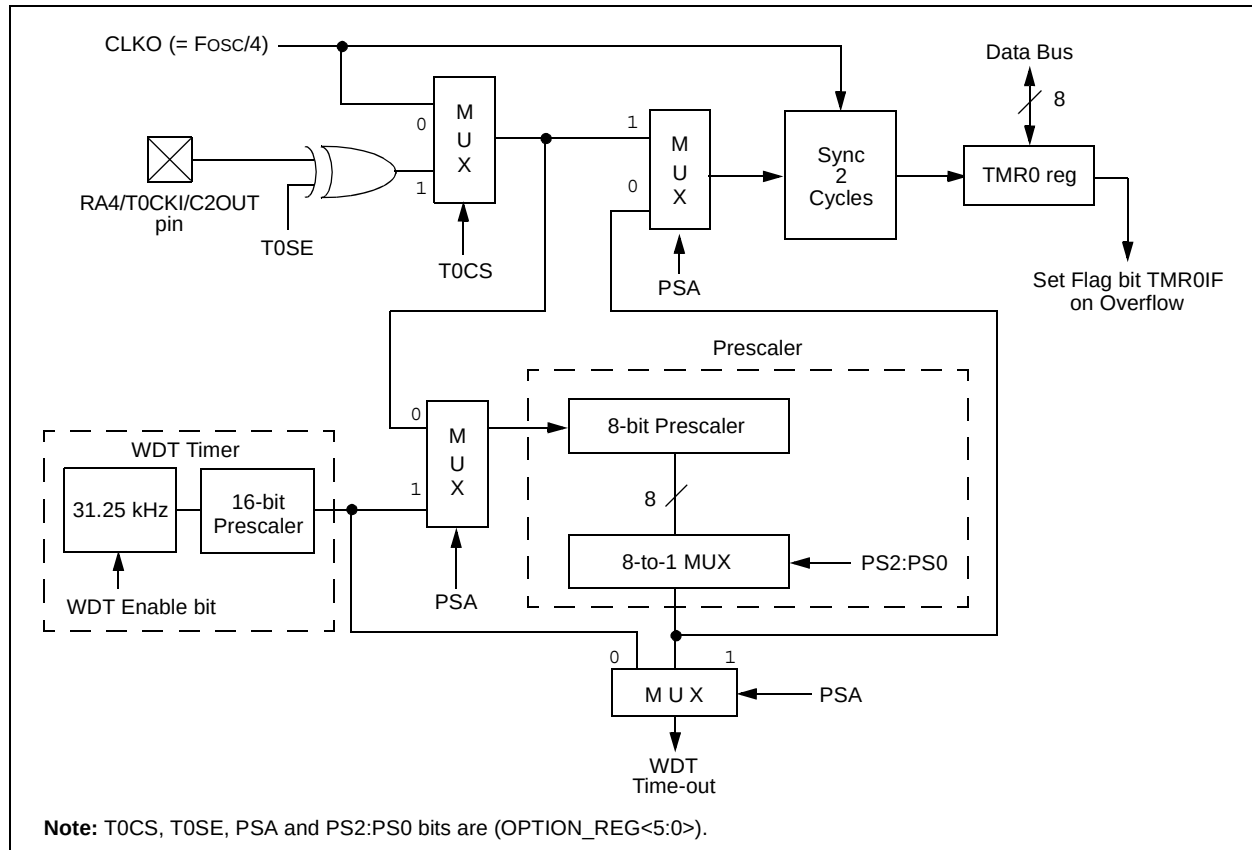
Counter mode is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI/C2OUT. The incrementing edge is determined by the Timer0 Source Edge Select bit, T0SE (OPTION_REG<4>). Clearing bit T0SE selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 6.3 “Using Timer0 with an External Clock”**.

The prescaler is mutually, exclusively shared between the Timer0 module and the Watchdog Timer. The prescaler is not readable or writable. **Section 6.4 “Prescaler”** details the operation of the prescaler.

6.2 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h. This overflow sets bit TMR0IF (INTCON<2>). The interrupt can be masked by clearing bit TMR0IE (INTCON<5>). Bit TMR0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from Sleep, since the timer is shut off during Sleep.

FIGURE 6-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



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6.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 T_{osc} (and a small RC delay of 20 ns) and low for at least 2 T_{osc} (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

6.4 Prescaler

There is only one prescaler available, which is mutually exclusively shared between the Timer0 module and the Watchdog Timer. A prescaler assignment for the Timer0 module means that the prescaler cannot be used by the Watchdog Timer and vice versa. This prescaler is not readable or writable (see Figure 6-1).

Note: Although the prescaler can be assigned to either the WDT or Timer0, but not both, a new divide counter is implemented in the WDT circuit to give multiple WDT time-out selections. This allows TMR0 and WDT to each have their own scaler. Refer to **Section 15.12 “Watchdog Timer (WDT)”** for further details.

The PSA and PS2:PS0 bits (OPTION_REG<3:0>) determine the prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, x,...etc.) will clear the prescaler. When assigned to WDT, a CLRWD instruction will clear the prescaler along with the Watchdog Timer. The prescaler is not readable or writable.

Note: Writing to TMR0, when the prescaler is assigned to Timer0, will clear the prescaler count but will not change the prescaler assignment.

REGISTER 6-1: OPTION_REG: OPTION CONTROL REGISTER (ADDRESS 81h, 181h)

	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
	bit 7							bit 0
bit 7	RBPU: PORTB Pull-up Enable bit							
bit 6	INTEDG: Interrupt Edge Select bit							
bit 5	T0CS: TMR0 Clock Source Select bit							
	1 = Transition on T0CKI pin							
	0 = Internal instruction cycle clock (CLKO)							
bit 4	T0SE: TMR0 Source Edge Select bit							
	1 = Increment on high-to-low transition on T0CKI pin							
	0 = Increment on low-to-high transition on T0CKI pin							
bit 3	PSA: Prescaler Assignment bit							
	1 = Prescaler is assigned to the WDT							
	0 = Prescaler is assigned to the Timer0 module							
bit 2-0	PS<2:0>: Prescaler Rate Select bits							
	Bit Value	TMR0 Rate	WDT Rate					
	000	1 : 2	1 : 1					
	001	1 : 4	1 : 2					
	010	1 : 8	1 : 4					
	011	1 : 16	1 : 8					
	100	1 : 32	1 : 16					
	101	1 : 64	1 : 32					
	110	1 : 128	1 : 64					
	111	1 : 256	1 : 128					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

Note: To avoid an unintended device Reset, the instruction sequence shown in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023) must be executed when changing the prescaler assignment from Timer0 to the WDT. This sequence must be followed even if the WDT is disabled.

EXAMPLE 6-1: CHANGING THE PRESCALER ASSIGNMENT FROM WDT TO TIMER0

```
CLRWDT          ; Clear WDT and prescaler
BANKSEL OPTION_REG ; Select Bank of OPTION_REG
MOVLW  b'xxxx0xxx' ; Select TMR0, new prescale
MOVWF  OPTION_REG  ; value and clock source
```

TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
01h,101h	TMR0	Timer0 Module Register								xxxx xxxx	uuuu uuuu
0Bh,8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
81h,181h	OPTION_REG	RBP $\overline{U}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged. Shaded cells are not used by Timer0.

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NOTES:

7.0 TIMER1 MODULE

The Timer1 module is a 16-bit timer/counter consisting of two 8-bit registers (TMR1H and TMR1L) which are readable and writable. The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit, TMR1IE (PIE1<0>).

The Timer1 oscillator can be used as a secondary clock source in low-power modes. When the T1RUN bit is set along with SCS<1:0> = 01, the Timer1 oscillator is providing the system clock. If the Fail-Safe Clock Monitor is enabled and the Timer1 oscillator fails while providing the system clock, polling the T1RUN bit will indicate whether the clock is being provided by the Timer1 oscillator or another source.

Timer1 can also be used to provide Real-Time Clock (RTC) functionality to applications with only a minimal addition of external components and code overhead.

7.1 Timer1 Operation

Timer1 can operate in one of three modes:

- as a Timer
- as a Synchronous Counter
- as an Asynchronous Counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

In Timer mode, Timer1 increments every instruction cycle. In Counter mode, it increments on every rising edge of the external clock input.

Timer1 can be enabled/disabled by setting/clearing control bit, TMR1ON (T1CON<0>).

Timer1 also has an internal "Reset input". This Reset can be generated by the CCP1 module as the special event trigger (see **Section 9.1 "Capture Mode"**). Register 7-1 shows the Timer1 Control register.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RB6/PGC/T1OSO/T1CKI and RB7/PGD/T1OSI pins become inputs. That is, the TRISB<7:6> value is ignored and these pins read as '0'.

Additional information on timer modules is available in the "*PIC® Mid-Range MCU Family Reference Manual*" (DS33023).

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REGISTER 7-1: T1CON: TIMER1 CONTROL REGISTER (ADDRESS 10h)

U-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **T1RUN:** Timer1 System Clock Status bit
 1 = System clock is derived from Timer1 oscillator
 0 = System clock is derived from another source

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits
 11 = 1:8 Prescale value
 10 = 1:4 Prescale value
 01 = 1:2 Prescale value
 00 = 1:1 Prescale value

bit 3 **T1OSCEN:** Timer1 Oscillator Enable Control bit
 1 = Oscillator is enabled
 0 = Oscillator is shut off (the oscillator inverter is turned off to eliminate power drain)

bit 2 **T1SYNC:** Timer1 External Clock Input Synchronization Control bit
TMR1CS = 1:
 1 = Do not synchronize external clock input
 0 = Synchronize external clock input
TMR1CS = 0:
 This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0.

bit 1 **TMR1CS:** Timer1 Clock Source Select bit
 1 = External clock from pin RB6/AN5⁽¹⁾/PGC/T1OSO/T1CKI (on the rising edge)
 0 = Internal clock (Fosc/4)

Note 1: Available on PIC16F88 devices only.

bit 0 **TMR1ON:** Timer1 On bit
 1 = Enables Timer1
 0 = Stops Timer1

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

7.2 Timer1 Operation in Timer Mode

Timer mode is selected by clearing the TMR1CS (T1CON<1>) bit. In this mode, the input clock to the timer is $F_{osc}/4$. The synchronize control bit, T1SYNC (T1CON<2>), has no effect since the internal clock is always in sync.

7.3 Timer1 Counter Operation

Timer1 may operate in Asynchronous or Synchronous mode, depending on the setting of the TMR1CS bit.

When Timer1 is being incremented via an external source, increments occur on a rising edge. After Timer1 is enabled in Counter mode, the module must first have a falling edge before the counter begins to increment.

7.4 Timer1 Operation in Synchronized Counter Mode

Counter mode is selected by setting bit TMR1CS. In this mode, the timer increments on every rising edge of clock input on pin RB7/PGD/T1OSI when bit T1OSCEN is set, or on pin RB6/PGC/T1OSO/T1CKI when bit T1OSCEN is cleared.

If T1SYNC is cleared, then the external clock input is synchronized with internal phase clocks. The synchronization is done after the prescaler stage. The prescaler stage is an asynchronous ripple counter.

In this configuration, during Sleep mode, Timer1 will not increment even if the external clock is present since the synchronization circuit is shut off. The prescaler, however, will continue to increment.

FIGURE 7-1: TIMER1 INCREMENTING EDGE

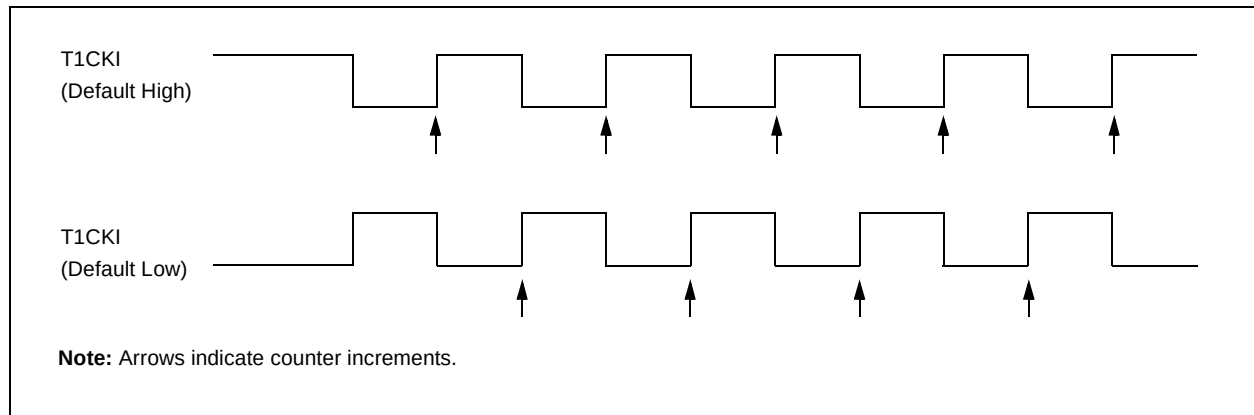
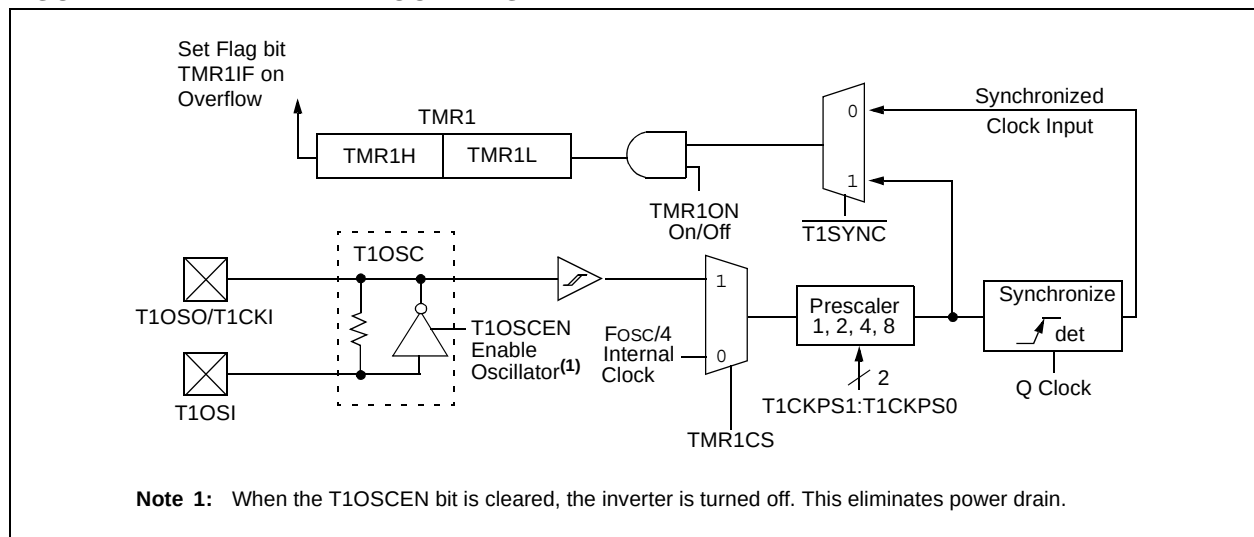


FIGURE 7-2: TIMER1 BLOCK DIAGRAM



7.5 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronously to the internal phase clocks. The timer will continue to run during Sleep and can generate an interrupt-on-overflow that will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section 7.5.1 “Reading and Writing Timer1 in Asynchronous Counter Mode”**).

In Asynchronous Counter mode, Timer1 cannot be used as a time base for capture or compare operations.

7.5.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. The example codes provided in Example 7-1 and Example 7-2 demonstrate how to write to and read Timer1 while it is running in Asynchronous mode.

EXAMPLE 7-1: WRITING A 16-BIT FREE RUNNING TIMER

```
; All interrupts are disabled
CLRF      TMR1L      ; Clear Low byte, Ensures no rollover into TMR1H
MOVLW     HI_BYTE    ; Value to load into TMR1H
MOVWF     TMR1H, F   ; Write High byte
MOVLW     LO_BYTE    ; Value to load into TMR1L
MOVWF     TMR1L, F   ; Write Low byte
; Re-enable the Interrupt (if required)
CONTINUE      ; Continue with your code
```

EXAMPLE 7-2: READING A 16-BIT FREE RUNNING TIMER

```
; All interrupts are disabled
MOVF      TMR1H, W    ; Read high byte
MOVWF     TMPH
MOVF      TMR1L, W    ; Read low byte
MOVWF     TMPL
MOVF      TMR1H, W    ; Read high byte
SUBWF     TMPH, W     ; Sub 1st read with 2nd read
BTFSC     STATUS, Z   ; Is result = 0
GOTO      CONTINUE    ; Good 16-bit read
; TMR1L may have rolled over between the read of the high and low bytes.
; Reading the high and low bytes now will read a good value.
MOVF      TMR1H, W    ; Read high byte
MOVWF     TMPH
MOVF      TMR1L, W    ; Read low byte
MOVWF     TMPL
; Re-enable the Interrupt (if required)
CONTINUE      ; Continue with your code
```

7.6 Timer1 Oscillator

A crystal oscillator circuit is built between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator, rated up to 32.768 kHz. It will continue to run during all power-managed modes. It is primarily intended for a 32 kHz crystal. The circuit for a typical LP oscillator is shown in Figure 7-3. Table 7-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper oscillator start-up.

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming™ (ICSP™) may not function correctly (high voltage or low voltage), or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead) or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

FIGURE 7-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR

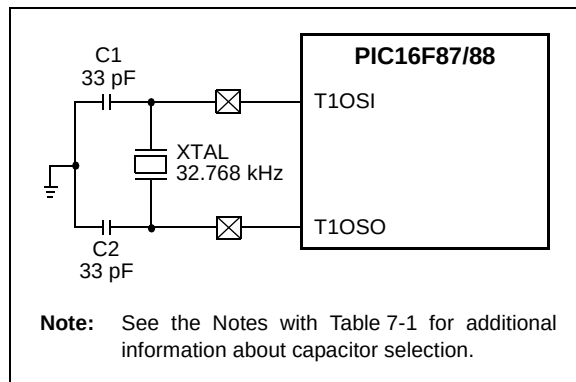


TABLE 7-1: CAPACITOR SELECTION FOR THE TIMER1 OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	33 pF	33 pF

Note 1: Microchip suggests this value as a starting point in validating the oscillator circuit.

2: Higher capacitance increases the stability of the oscillator but also increases the start-up time.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Capacitor values are for design guidance only.

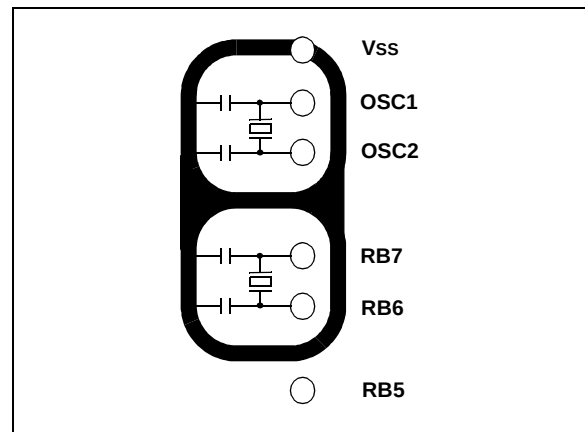
7.7 Timer1 Oscillator Layout Considerations

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 7-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD.

If a high-speed circuit must be located near the oscillator, a grounded guard ring around the oscillator circuit, as shown in Figure 7-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.

FIGURE 7-4: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



7.8 Resetting Timer1 Using a CCP Trigger Output

If the CCP1 module is configured in Compare mode to generate a “special event trigger” signal (CCP1M3:CCP1M0 = 1011), the signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note: The special event triggers from the CCP1 module will not set interrupt flag bit, TMR1IF (PIR1<0>).

Timer1 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this Reset operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCPR1H:CCPR1L register pair effectively becomes the period register for Timer1.

7.9 Resetting Timer1 Register Pair (TMR1H, TMR1L)

TMR1H and TMR1L registers are not reset to 00h on a POR, or any other Reset, except by the CCP1 special event triggers.

T1CON register is reset to 00h on a Power-on Reset or a Brown-out Reset, which shuts off the timer and leaves a 1:1 prescale. In all other Resets, the register is unaffected.

7.10 Timer1 Prescaler

The prescaler counter is cleared on writes to the TMR1H or TMR1L registers.

7.11 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 7.6 “Timer1 Oscillator”**) gives users the option to include RTC functionality to their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, *RTCisr*, shown in Example 7-3, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow triggers the interrupt and calls the routine, which increments the seconds counter by one; additional counters for minutes and hours are incremented as the previous counter overflows.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it; the simplest method is to set the MSb of TMR1H with a BSF instruction. Note that the TMR1L register is never preloaded or altered; doing so may introduce cumulative error over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = 1), as shown in the routine, *RTCinit*. The Timer1 oscillator must also be enabled and running at all times.

EXAMPLE 7-3: IMPLEMENTING A REAL-TIME CLOCK USING A TIMER1 INTERRUPT SERVICE

RTCinit	BANKSEL	TMR1H		
	MOVLW	0x80		; Preload TMR1 register pair
	MOVWF	TMR1H		; for 1 second overflow
	CLRF	TMR1L		
	MOVLW	b'00001111'		; Configure for external clock,
	MOVWF	T1CON		; Asynchronous operation, external oscillator
	CLRF	secs		; Initialize timekeeping registers
	CLRF	mins		
	MOVLW	.12		
	MOVWF	hours		
	BANKSEL	PIE1		
	BSF	PIE1, TMR1IE		; Enable Timer1 interrupt
	RETURN			
RTCisr	BANKSEL	TMR1H		
	BSF	TMR1H, 7		; Preload for 1 sec overflow
	BCF	PIR1, TMR1IF		; Clear interrupt flag
	INCF	secs, F		; Increment seconds
	MOVF	secs, w		
	SUBLW	.60		
	BTFS	STATUS, Z		; 60 seconds elapsed?
	RETURN			; No, done
	CLRF	seconds		; Clear seconds
	INCF	mins, f		; Increment minutes
	MOVF	mins, w		
	SUBLW	.60		
	BTFS	STATUS, Z		; 60 seconds elapsed?
	RETURN			; No, done
	CLRF	mins		; Clear minutes
	INCF	hours, f		; Increment hours
	MOVF	hours, w		
	SUBLW	.24		
	BTFS	STATUS, Z		; 24 hours elapsed?
	RETURN			; No, done
	CLRF	hours		; Clear hours
	RETURN			; Done

TABLE 7-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000	-uuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

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NOTES:

8.0 TIMER2 MODULE

Timer2 is an 8-bit timer with a prescaler and a postscaler. It can be used as the PWM time base for the PWM mode of the CCP1 module. The TMR2 register is readable and writable and is cleared on any device Reset.

The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T2CKPS1:T2CKPS0 (T2CON<1:0>).

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon Reset.

The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit TMR2IF (PIR1<1>)).

Timer2 can be shut off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption.

Register 8-1 shows the Timer2 Control register.

Additional information on timer modules is available in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

8.1 Timer2 Prescaler and Postscaler

The prescaler and postscaler counters are cleared when any of the following occurs:

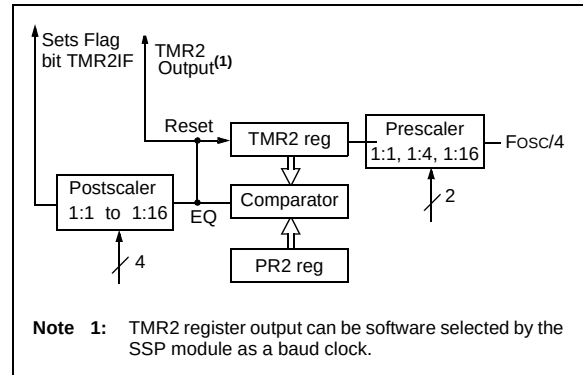
- A write to the TMR2 register
- A write to the T2CON register
- Any device Reset (Power-on Reset, $\overline{\text{MCLR}}$, WDT Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

8.2 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module (SSP) which optionally uses it to generate a shift clock.

FIGURE 8-1: TIMER2 BLOCK DIAGRAM



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REGISTER 8-1: T2CON: TIMER2 CONTROL REGISTER (ADDRESS 12h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **TOUTPS<3:0>:** Timer2 Output Postscale Select bits
 0000 = 1:1 Postscale
 0001 = 1:2 Postscale
 0010 = 1:3 Postscale
 •
 •
 •
 1111 = 1:16 Postscale
- bit 2 **TMR2ON:** Timer2 On bit
 1 = Timer2 is on
 0 = Timer2 is off
- bit 1-0 **T2CKPS<1:0>:** Timer2 Clock Prescale Select bits
 00 = Prescaler is 1
 01 = Prescaler is 4
 1x = Prescaler is 16

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

TABLE 8-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

9.0 CAPTURE/COMPARE/PWM (CCP) MODULE

The Capture/Compare/PWM (CCP) module contains a 16-bit register that can operate as a:

- 16-bit Capture register
- 16-bit Compare register
- PWM Master/Slave Duty Cycle register.

Table 9-1 shows the timer resources of the CCP module modes.

Capture/Compare/PWM Register 1 (CCPR1) is comprised of two 8-bit registers: CCPR1L (low byte) and CCPR1H (high byte). The CCP1CON register controls the operation of CCP1. The special event trigger is generated by a compare match which will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

The CCP module's input/output pin (CCP1) can be configured as RB0 or RB3. This selection is set in bit 12 (CCPMX) of the Configuration Word.

Additional information on the CCP module is available in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023) and in Application Note AN594, "Using the CCP Module(s)" (DS00594).

TABLE 9-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1
Compare	Timer1
PWM	Timer2

REGISTER 9-1: CCP1CON: CAPTURE/COMPARE/PWM CONTROL REGISTER 1 (ADDRESS 17h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **CCP1X:CCP1Y:** PWM Least Significant bits

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPR1L.

bit 3-0 **CCP1M<3:0>:** CCP1 Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCP1 module)

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, set output on match (CCP1IF bit is set)

1001 = Compare mode, clear output on match (CCP1IF bit is set)

1010 = Compare mode, generate software interrupt on match (CCP1IF bit is set, CCP1 pin is unaffected)

1011 = Compare mode, trigger special event (CCP1IF bit is set, CCP1 pin is unaffected); CCP1 resets TMR1 and starts an A/D conversion (if A/D module is enabled)

11xx = PWM mode

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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9.1 Capture Mode

In Capture mode, CCP1H:CCP1L captures the 16-bit value of the TMR1 register when an event occurs on the CCP1 pin. An event is defined as:

- Every falling edge
- Every rising edge
- Every 4th rising edge
- Every 16th rising edge

An event is selected by control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF (PIR1<2>), is set. It must be cleared in software. If another capture occurs before the value in register CCP1 is read, the old captured value is overwritten by the new captured value.

9.1.1 CCP PIN CONFIGURATION

In Capture mode, the CCP1 pin should be configured as an input by setting the TRISB<x> bit.

- Note 1:** If the CCP1 pin is configured as an output, a write to the port can cause a capture condition.
- 2:** The TRISB bit (0 or 3) is dependent upon the setting of configuration bit 12 (CCPMX).

9.1.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode for the CCP module to use the capture feature. In Asynchronous Counter mode, the capture operation may not work.

9.1.3 SOFTWARE INTERRUPT

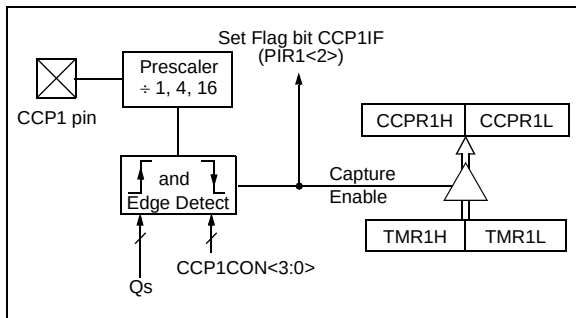
When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit, CCP1IF, following any such change in operating mode.

9.1.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off, or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 9-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

FIGURE 9-1: CAPTURE MODE OPERATION BLOCK DIAGRAM



EXAMPLE 9-1: CHANGING BETWEEN CAPTURE PRESCALERS

```
CLRF    CCP1CON    ;Turn CCP module off
MOVLW   NEW_CAPT_PS ;Load the W reg with
                        ;the new prescaler
                        ;move value and CCP ON
MOVWF    CCP1CON    ;Load CCP1CON with this
                        ;value
```

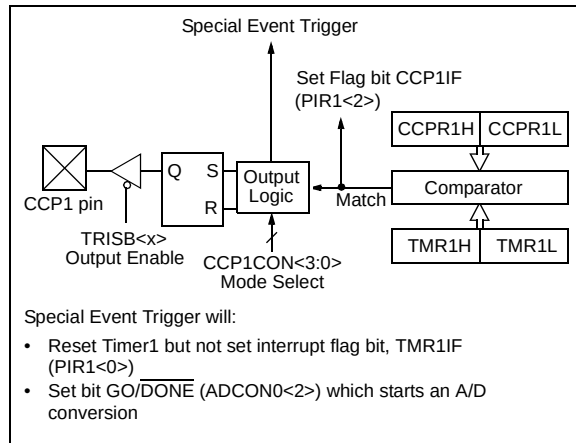
9.2 Compare Mode

In Compare mode, the 16-bit CCPR1 register value is constantly compared against the TMR1 register pair value. When a match occurs, the CCP1 pin is:

- Driven high
- Driven low
- Remains unchanged

The action on the pin is based on the value of control bits CCP1M3:CCP1M0 (CCP1CON<3:0>). At the same time, interrupt flag bit, CCP1IF, is set.

FIGURE 9-2: COMPARE MODE OPERATION BLOCK DIAGRAM



9.2.1 CCP PIN CONFIGURATION

The user must configure the CCP1 pin as an output by clearing the TRISB<x> bit.

- Note 1:** Clearing the CCP1CON register will force the CCP1 compare output latch to the default low level. This is not the data latch.
- 2:** The TRISB bit (0 or 3) is dependent upon the setting of configuration bit 12 (CCPMX).

9.2.2 TIMER1 MODE SELECTION

Timer1 must be running in Timer mode or Synchronized Counter mode if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

9.2.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

9.2.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated that may be used to initiate an action.

The special event trigger output of CCP1 resets the TMR1 register pair and starts an A/D conversion (if the A/D module is enabled). This allows the CCPR1 register to effectively be a 16-bit programmable period register for Timer1.

- Note:** The special event trigger from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

TABLE 9-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh 10BH,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	T1SYN	TMR1CS	TMR1ON	-000 0000	-uuu uuuu
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	-00 0000	-00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

9.3 PWM Mode

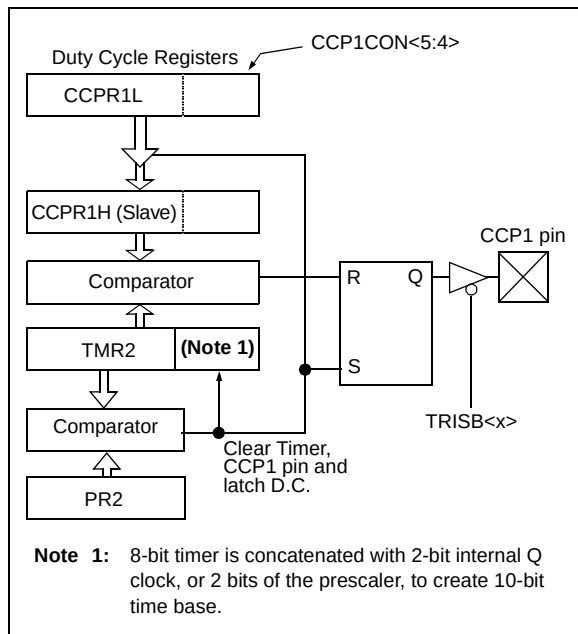
In Pulse-Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTB data latch, the TRISB<x> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTB I/O data latch.

Figure 9-3 shows a simplified block diagram of the CCP module in PWM mode.

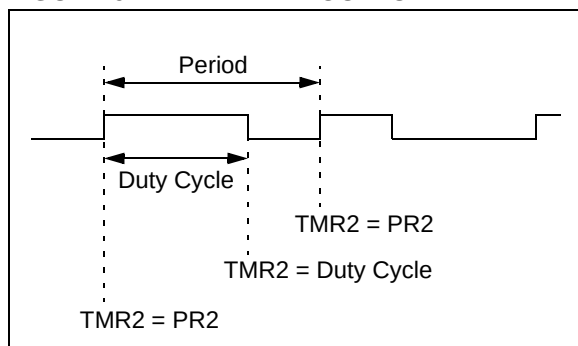
For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 9.3.3 “Setup for PWM Operation”**.

FIGURE 9-3: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 9-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 9-4: PWM OUTPUT



9.3.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula.

EQUATION 9-1:

$$\text{PWM Period} = [(PR2) + 1] \cdot 4 \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as $1/[\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 postscaler (see **Section 8.0 “Timer2 Module”**) is not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

9.3.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSBs and the CCP1CON<5:4> bits contain the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time.

EQUATION 9-2:

$$\text{PWM Duty Cycle} = (\text{CCPR1L:CCP1CON<5:4>}) \cdot T_{OSC} \cdot (\text{TMR2 Prescale Value})$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read-only register.

The CCPR1H register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2, concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the following formula.

EQUATION 9-3:

$$\text{Resolution} = \frac{\log\left(\frac{F_{\text{OSC}}}{F_{\text{PWM}}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

9.3.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISB<x> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

Note: The TRISB bit (0 or 3) is dependant upon the setting of configuration bit 12 (CCPMX).

TABLE 9-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 20 MHz

PWM Frequency	1.22 kHz	4.88 kHz	19.53 kHz	78.12 kHz	156.3 kHz	208.3 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	0xFF	0xFF	0xFF	0x3F	0x1F	0x17
Maximum Resolution (bits)	10	10	10	8	7	6.6

TABLE 9-4: REGISTERS ASSOCIATED WITH PWM AND TIMER2

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
11h	TMR2	Timer2 Module Register								0000 0000	0000 0000
92h	PR2	Timer2 Period Register								1111 1111	1111 1111
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
15h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
16h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM and Timer2.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

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NOTES:

10.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

10.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I²C™)

An overview of I²C operations and additional information on the SSP module can be found in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

Refer to Application Note AN578, “Use of the SSP Module in the I²C™ Multi-Master Environment” (DS00578).

10.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module.

SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO) RB2/SDO/RX/DT
- Serial Data In (SDI) RB1/SDI/SDA
- Serial Clock (SCK) RB4/SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$) RB5/ $\overline{SS}$ /TX/CK

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON register (SSPCON<5:0>) and the SSPSTAT register (SSPSTAT<7:6>). These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

Note: Before enabling the module in SPI Slave mode, the state of the clock line (SCK) must match the polarity selected for the Idle state. The clock line can be observed by reading the SCK pin. The polarity of the Idle state is determined by the CKP bit (SSPCON<4>).

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REGISTER 10-1: SSPSTAT: SYNCHRONOUS SERIAL PORT STATUS REGISTER (ADDRESS 94h)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	P ⁽¹⁾	S ⁽¹⁾	R/W	UA	BF
bit 7							bit 0

- bit 7 **SMP:** SPI Data Input Sample Phase bit
SPI Master mode:
 1 = Input data sampled at end of data output time
 0 = Input data sampled at middle of data output time (Microwire)
SPI Slave mode:
 This bit must be cleared when SPI is used in Slave mode.
I²C mode:
 This bit must be maintained clear.
- bit 6 **CKE:** SPI Clock Edge Select bit
 1 = Transmit occurs on transition from active to Idle clock state
 0 = Transmit occurs on transition from Idle to active clock state
Note: Polarity of clock state is set by the CKP bit (SSPCON<4>).
- bit 5 **D/A:** Data/Address bit (I²C mode only)
In I²C Slave mode:
 1 = Indicates that the last byte received was data
 0 = Indicates that the last byte received was address
- bit 4 **P:** Stop bit⁽¹⁾ (I²C mode only)
 1 = Indicates that a Stop bit has been detected last
 0 = Stop bit was not detected last
- bit 3 **S:** Start bit⁽¹⁾ (I²C mode only)
 1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
 0 = Start bit was not detected last
- bit 2 **R/W:** Read/Write Information bit (I²C mode only)
 Holds the R/W bit information following the last address match and is only valid from address match to the next Start bit, Stop bit or ACK bit.
 1 = Read
 0 = Write
- bit 1 **UA:** Update Address bit (10-bit I²C mode only)
 1 = Indicates that the user needs to update the address in the SSPADD register
 0 = Address does not need to be updated
- bit 0 **BF:** Buffer Full Status bit
Receive (SPI and I²C modes):
 1 = Receive complete, SSPBUF is full
 0 = Receive not complete, SSPBUF is empty
Transmit (in I²C mode only):
 1 = Transmit in progress, SSPBUF is full (8 bits)
 0 = Transmit complete, SSPBUF is empty
Note 1: This bit is cleared when the SSP module is disabled (i.e., the SSPEN bit is cleared).

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 10-2: SSPCON: SYNCHRONOUS SERIAL PORT CONTROL REGISTER (ADDRESS 14h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN ⁽¹⁾	CKP	SSPM3	SSPM2	SSPM1	SSPM0
bit 7							bit 0

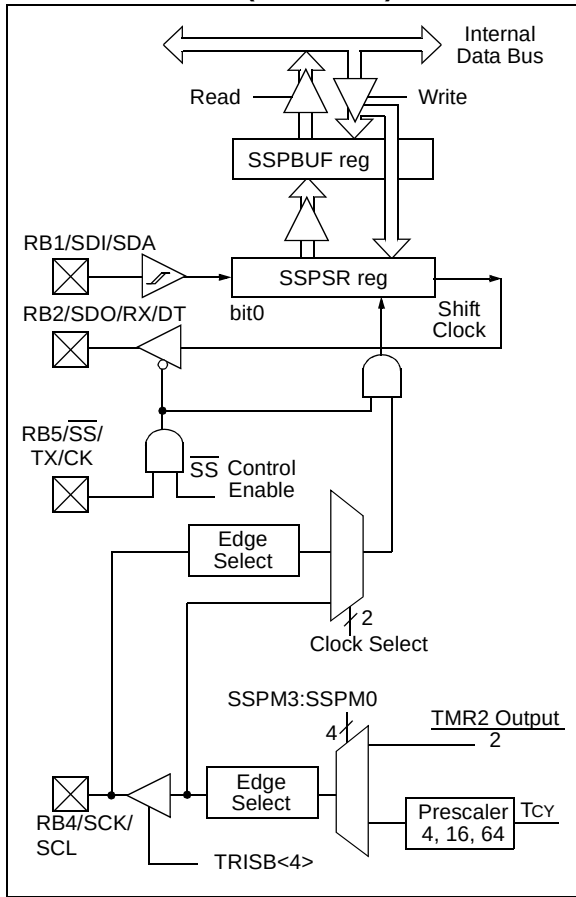
- bit 7 **WCOL:** Write Collision Detect bit
 1 = An attempt to write the SSPBUF register failed because the SSP module is busy (must be cleared in software)
 0 = No collision
- bit 6 **SSPOV:** Receive Overflow Indicator bit
In SPI mode:
 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
 0 = No overflow
In I²C mode:
 1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. SSPOV must be cleared in software in either mode.
 0 = No overflow
- bit 5 **SSPEN:** Synchronous Serial Port Enable bit⁽¹⁾
In SPI mode:
 1 = Enables serial port and configures SCK, SDO and SDI as serial port pins
 0 = Disables serial port and configures these pins as I/O port pins
In I²C mode:
 1 = Enables the serial port and configures the SDA and SCL pins as serial port pins
 0 = Disables serial port and configures these pins as I/O port pins
Note 1: In both modes, when enabled, these pins must be properly configured as input or output.
- bit 4 **CKP:** Clock Polarity Select bit
In SPI mode:
 1 = Transmit happens on falling edge, receive on rising edge. Idle state for clock is a high level.
 0 = Transmit happens on rising edge, receive on falling edge. Idle state for clock is a low level.
In I²C Slave mode:
 SCK release control
 1 = Enable clock
 0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
- bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits
 0000 = SPI Master mode, clock = OSC/4
 0001 = SPI Master mode, clock = OSC/16
 0010 = SPI Master mode, clock = OSC/64
 0011 = SPI Master mode, clock = TMR2 output/2
 0100 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control enabled.
 0101 = SPI Slave mode, clock = SCK pin. $\overline{SS}$ pin control disabled. $\overline{SS}$ can be used as I/O pin.
 0110 = I²C Slave mode, 7-bit address
 0111 = I²C Slave mode, 10-bit address
 1011 = I²C Firmware Controlled Master mode (Slave Idle)
 1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
 1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled
 1000, 1001, 1010, 1100, 1101 = Reserved

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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FIGURE 10-1: SSP BLOCK DIAGRAM (SPI MODE)



To enable the serial port, SSP Enable bit, SSPEN (SSPCON<5>), must be set. To reset or reconfigure SPI mode, clear bit SSPEN, reinitialize the SSPCON register and then set bit SSPEN. This configures the SDI, SDO, SCK and SS pins as serial port pins. For the pins to behave as the serial port function, they must have their data direction bits (in the TRISB register) appropriately programmed. That is:

- SDI must have TRISB<1> set
- SDO must have TRISB<2> cleared
- SCK (Master mode) must have TRISB<4> cleared
- SCK (Slave mode) must have TRISB<4> set
- SS must have TRISB<5> set

Note 1: When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

2: If the SPI is used in Slave mode with CKE = 1, then the SS pin control must be enabled.

TABLE 10-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh,8Bh 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

FIGURE 10-2: SPI MODE TIMING (MASTER MODE)

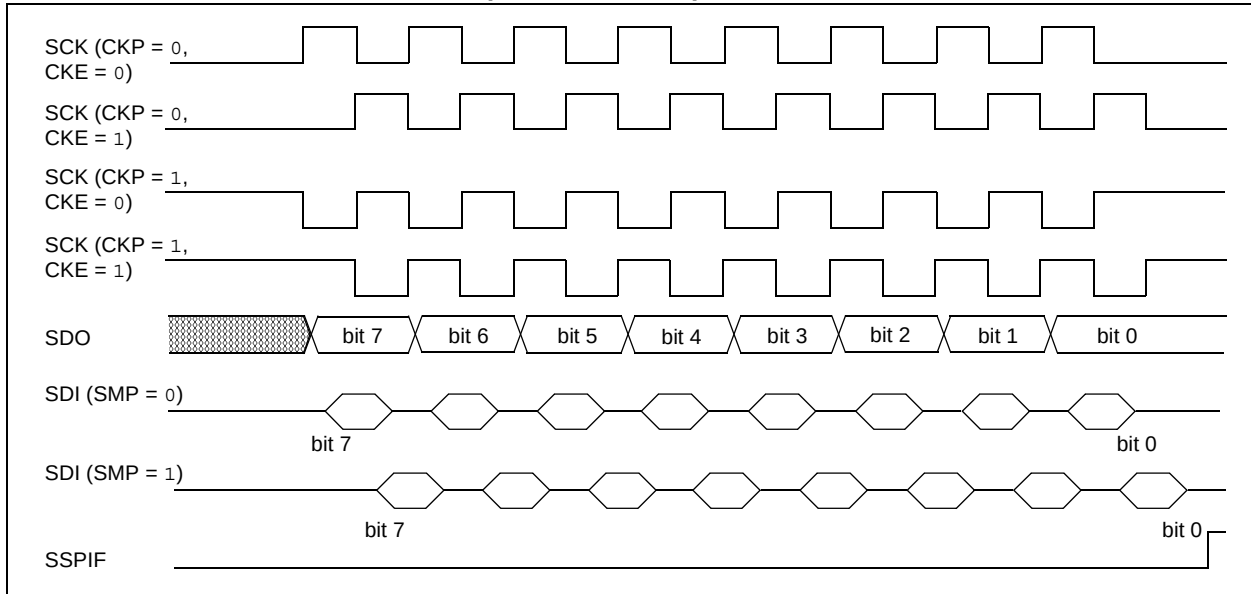


FIGURE 10-3: SPI MODE TIMING (SLAVE MODE WITH CKE = 0)

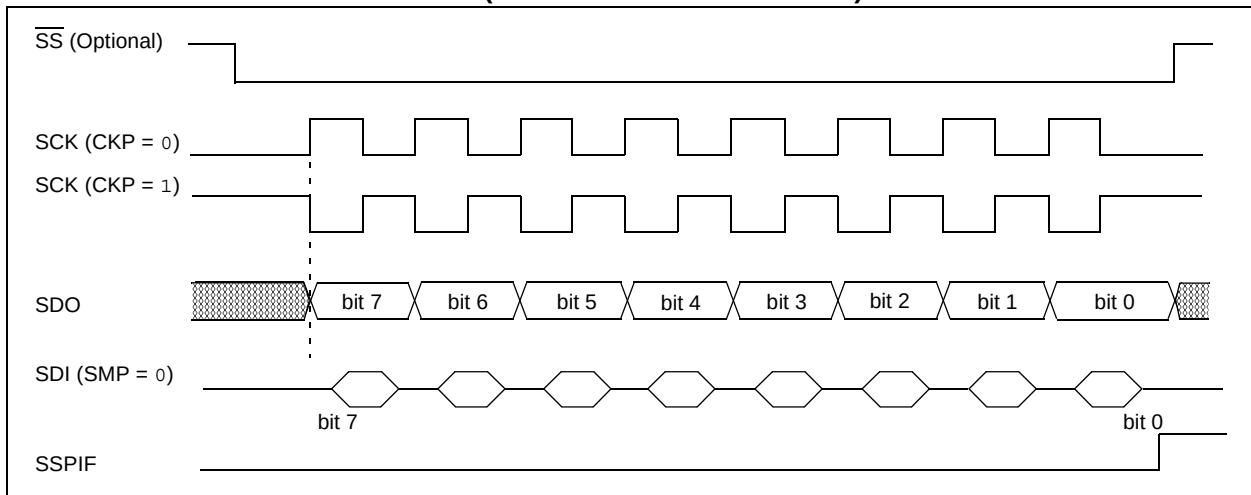
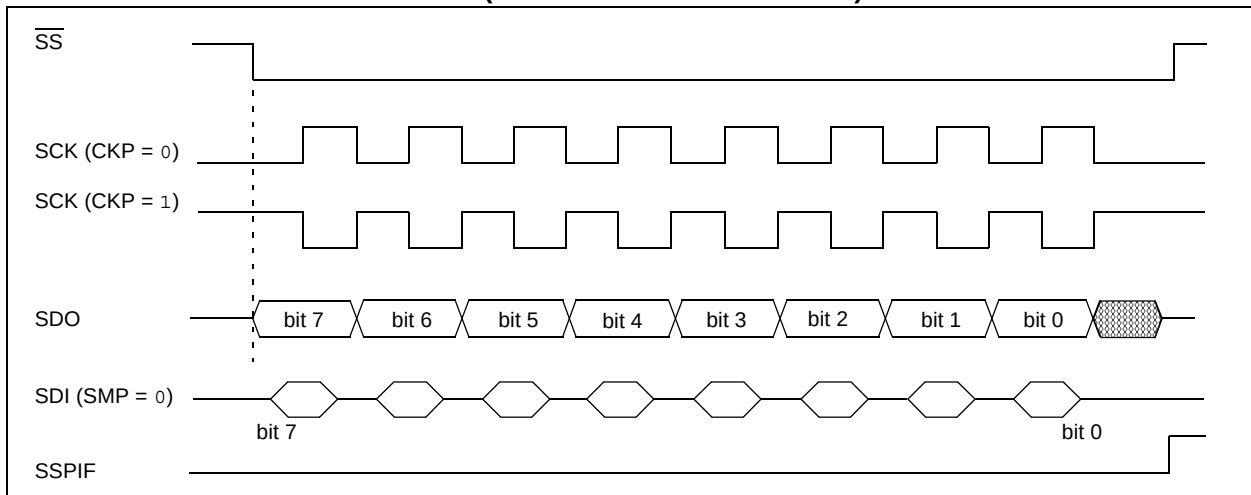


FIGURE 10-4: SPI MODE TIMING (SLAVE MODE WITH CKE = 1)



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10.3 SSP I²C Mode Operation

The SSP module in I²C mode fully implements all slave functions, except general call support and provides interrupts on Start and Stop bits in hardware to facilitate firmware implementations of the master functions. The SSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer. These are the RB4/SCK/SCL pin, which is the clock (SCL) and the RB1/SDI/SDA pin, which is the data (SDA). The user must configure these pins as inputs or outputs through the TRISB<4,1> bits.

To ensure proper communication of the I²C Slave mode, the TRIS bits (TRISx [SDA, SCL]) corresponding to the I²C pins must be set to '1'. If any TRIS bits (TRISx<7:0>) of the port containing the I²C pins (PORTx [SDA, SCL]) are changed in software during I²C communication using a Read-Modify-Write instruction (BSF, BCF), then the I²C mode may stop functioning properly and I²C communication may suspend. Do not change any of the TRISx bits (TRIS bits of the port containing the I²C pins) using the instruction BSF or BCF during I²C communication. If it is absolutely necessary to change the TRISx bits during communication, the following method can be used:

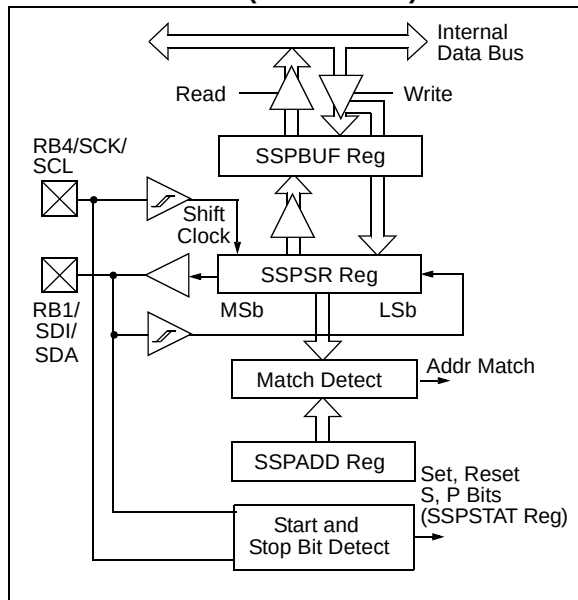
EXAMPLE 10-1:

```
MOVWF    TRISC, W      ; Example for an 18-pin part such as the PIC16F818/819
IORLW    0x18           ; Ensures <4:3> bits are '11'
ANDLW    B'11111001'   ; Sets <2:1> as output, but will not alter other bits
                                ; User can use their own logic here, such as IORLW, XORLW and ANDLW

MOVWF    TRISC
```

The SSP module functions are enabled by setting SSP Enable bit, SSPEN (SSPCON<5>).

FIGURE 10-5: SSP BLOCK DIAGRAM (I²C™ MODE)



The SSP module has five registers for I²C operation:

- SSP Control register (SSPCON)
- SSP Status register (SSPSTAT)
- Serial Receive/Transmit Buffer register (SSPBUF)
- SSP Shift register (SSPSR) – Not directly accessible
- SSP Address register (SSPADD)

The SSPCON register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address) with Start and Stop bit interrupts enabled to support Firmware Controlled Master mode
- I²C Slave mode (10-bit address) with Start and Stop bit interrupts enabled to support Firmware Controlled Master mode
- I²C Firmware Controlled Master mode operation with Start and Stop bit interrupts enabled; slave is Idle

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open-drain, provided these pins are programmed to inputs by setting the appropriate TRISB bits. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

Additional information on SSP I²C operation may be found in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

10.3.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISB<4,1> set). The SSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched, or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (ACK) pulse and then load the SSPBUF register with the received value currently in the SSPSR register.

Either or both of the following conditions will cause the SSP module not to give this ACK pulse:

- The Buffer Full bit, BF (SSPSTAT<0>), was set before the transfer was received.
- The Overflow bit, SSPOV (SSPCON<6>), was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. Table 10-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit, BF, is cleared by reading the SSPBUF register while bit, SSPOV, is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I²C specification, as well as the requirement of the SSP module, are shown in timing parameter #100 and parameter #101.

10.3.1.1 Addressing

Once the SSP module has been enabled, it waits for a Start condition to occur. Following the Start condition, the eight bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register.
- The Buffer Full bit, BF, is set.
- An ACK pulse is generated.
- SSP Interrupt Flag bit, SSPIF (PIR1<3>), is set (interrupt is generated if enabled) – on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave device. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address.

The sequence of events for 10-bit Address mode is as follows, with steps 7-9 for slave transmitter:

- Receive first (high) byte of address (bits SSPIF, BF and UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of address (clears bit UA and releases the SCL line).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive second (low) byte of address (bits SSPIF, BF and UA are set).
- Update the SSPADD register with the first (high) byte of address; if match releases SCL line, this will clear bit UA.
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive Repeated Start condition.
- Receive first (high) byte of address (bits SSPIF and BF are set).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

10.3.1.2 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then a no Acknowledge (ACK) pulse is given. An overflow condition is indicated if either bit, BF (SSPSTAT<0>), is set or bit, SSPOV (SSPCON<6>), is set.

An SSP interrupt is generated for each data transfer byte. Flag bit, SSPIF (PIR1<3>), must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

10.3.1.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and pin RB4/SCK/SCL is held low. The transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then, pin RB4/SCK/SCL should be enabled by setting bit CKP (SSPCON<4>). The master device must monitor the SCL pin prior to asserting another clock pulse. The slave devices may be holding off the master device by stretching the clock. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 10-7).

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An SSP interrupt is generated for each data transfer byte. Flag bit, SSPIF, must be cleared in software and the SSPSTAT register is used to determine the status of the byte. Flag bit, SSPIF, is set on the falling edge of the ninth clock pulse.

As a slave transmitter, the $\overline{\text{ACK}}$ pulse from the master receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line was high (not ACK), then

the data transfer is complete. When the $\overline{\text{ACK}}$ is latched by the slave device, the slave logic is reset (resets SSPSTAT register) and the slave device then monitors for another occurrence of the Start bit. If the SDA line was low (ACK), the transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then, pin RB4/SCK/SCL should be enabled by setting bit CKP.

TABLE 10-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{\text{ACK}}$ Pulse	Set SSPIF Bit (SSP Interrupt Occurs if Enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	No	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

FIGURE 10-6: I²C™ WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)

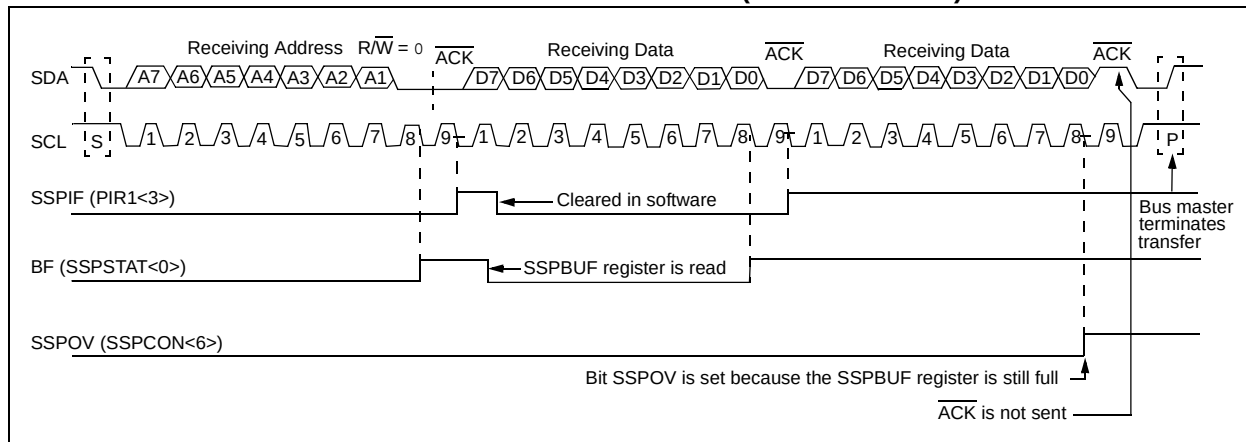
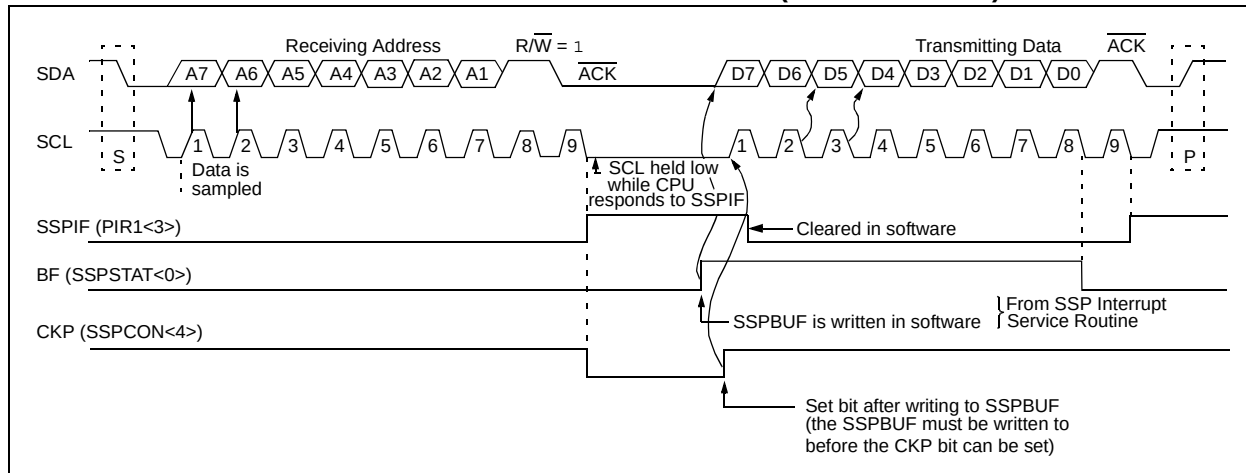


FIGURE 10-7: I²C™ WAVEFORMS FOR TRANSMISSION (7-BIT ADDRESS)



10.3.2 MASTER MODE OPERATION

Master mode operation is supported in firmware using interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset, or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when the P bit is set, or the bus is Idle and both the S and P bits are clear.

In Master mode operation, the SCL and SDA lines are manipulated in firmware by clearing the corresponding TRISB<4,1> bit(s). The output level is always low, irrespective of the value(s) in PORTB<4,1>. So, when transmitting data, a '1' data bit must have the TRISB<1> bit set (input) and a '0' data bit must have the TRISB<1> bit cleared (output). The same scenario is true for the SCL line with the TRISB<4> bit. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I²C module.

The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP Interrupt if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received

Master mode operation can be done with either the Slave mode Idle (SSPM3:SSPM0 = 1011), or with the Slave mode active. When both Master mode operation and Slave modes are used, the software needs to differentiate the source(s) of the interrupt.

For more information on Master mode operation, see Application Note AN554, "Software Implementation of I²C™ Bus Master".

10.3.3 MULTI-MASTER MODE OPERATION

In Multi-Master mode operation, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset, or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I²C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is Idle and both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In Multi-Master mode operation, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISB<4,1>). There are two stages where this arbitration can be lost:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave device continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an ACK pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to retransfer the data at a later time.

For more information on Multi-Master mode operation, see Application Note AN578, "Use of the SSP Module in the of I²C™ Multi-Master Environment".

TABLE 10-3: REGISTERS ASSOCIATED WITH I²C™ OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxxx xxxxx	uuuu uuuu
93h	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
94h	SSPSTAT	SMP ⁽²⁾	CKE ⁽²⁾	D/Ā	P	S	R/Ā	UA	BF	0000 0000	0000 0000
86h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.
Shaded cells are not used by SSP module in SPI mode.

- Note 1:** This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.
2: Maintain these bits clear in I²C™ mode.

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NOTES:

11.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (AUSART)

The Addressable Universal Synchronous Asynchronous Receiver Transmitter (AUSART) module is one of the two serial I/O modules. (AUSART is also known as a Serial Communications Interface or SCI.) The AUSART can be configured as a full-duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers, or it can be configured as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

The AUSART can be configured in the following modes:

- Asynchronous (full-duplex)
- Synchronous – Master (half-duplex)
- Synchronous – Slave (half-duplex)

Bit SPEN (RCSTA<7>) and bits TRISB<5,2> have to be set in order to configure pins, RB5/ $\overline{SS}$ /TX/CK and RB2/SDO/RX/DT, as the Addressable Universal Synchronous Asynchronous Receiver Transmitter.

The AUSART module also has a multi-processor communication capability, using 9-bit address detection.

REGISTER 11-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D

bit 7

bit 0

- bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
 Don't care.
Synchronous mode:
 1 = Master mode (clock generated internally from BRG)
 0 = Slave mode (clock from external source)
- bit 6 **TX9:** 9-bit Transmit Enable bit
 1 = Selects 9-bit transmission
 0 = Selects 8-bit transmission
- bit 5 **TXEN:** Transmit Enable bit
 1 = Transmit enabled
 0 = Transmit disabled
Note: SREN/CREN overrides TXEN in Sync mode.
- bit 4 **SYNC:** AUSART Mode Select bit
 1 = Synchronous mode
 0 = Asynchronous mode
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
 1 = High speed
 0 = Low speed
Synchronous mode:
 Unused in this mode.
- bit 1 **TRMT:** Transmit Shift Register Status bit
 1 = TSR empty
 0 = TSR full
- bit 0 **TX9D:** 9th bit of Transmit Data, can be Parity bit

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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REGISTER 11-2: RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

- bit 7 **SPEN:** Serial Port Enable bit
 1 = Serial port enabled (configures RB2/SDO/RX/DT and RB5/ $\overline{SS}$ /TX/CK pins as serial port pins)
 0 = Serial port disabled
- bit 6 **RX9:** 9-bit Receive Enable bit
 1 = Selects 9-bit reception
 0 = Selects 8-bit reception
- bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
 Don't care.
Synchronous mode – Master:
 1 = Enables single receive
 0 = Disables single receive
 This bit is cleared after reception is complete.
Synchronous mode – Slave:
 Don't care.
- bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
 1 = Enables continuous receive
 0 = Disables continuous receive
Synchronous mode:
 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
 0 = Disables continuous receive
- bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
 1 = Enables address detection, enables interrupt and load of the receive buffer when RSR<8> is set
 0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit
- bit 2 **FERR:** Framing Error bit
 1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
 0 = No framing error
- bit 1 **OERR:** Overrun Error bit
 1 = Overrun error (can be cleared by clearing bit CREN)
 0 = No overrun error
- bit 0 **RX9D:** 9th bit of Received Data (can be Parity bit, but must be calculated by user firmware)

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

11.1 AUSART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the AUSART. It is a dedicated 8-bit Baud Rate Generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 11-1 shows the formula for computation of the baud rate for different AUSART modes which only apply in Master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRG register can be calculated using the formula in Table 11-1. From this, the error in baud rate can be determined.

It may be advantageous to use the high baud rate (BRGH = 1) even for slower baud clocks. This is because the $F_{osc}/(16(X + 1))$ equation can reduce the baud rate error in some cases.

Writing a new value to the SPBRG register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

11.1.1 AUSART AND INTRC OPERATION

The PIC16F87/88 has an 8 MHz INTRC that can be used as the system clock, thereby eliminating the need for external components to provide the clock source. When the INTRC provides the system clock, the AUSART module will also use the INTRC as its system clock. Table 11-1 shows some of the INTRC frequencies that can be used to generate the AUSART module's baud rate.

11.1.2 LOW-POWER MODE OPERATION

The system clock is used to generate the desired baud rate; however, when a low-power mode is entered, the low-power clock source may be operating at a different frequency than in full power execution. In Sleep mode, no clocks are present. This may require the value in SPBRG to be adjusted.

11.1.3 SAMPLING

The data on the RB2/SDO/RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX pin.

TABLE 11-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = $F_{osc}/(64(X + 1))$	Baud Rate = $F_{osc}/(16(X + 1))$
1	(Synchronous) Baud Rate = $F_{osc}/(4(X + 1))$	N/A

Legend: X = value in SPBRG (0 to 255)

TABLE 11-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

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TABLE 11-3: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—
1.2	1.221	+1.75	255	1.202	+0.17	207	1.202	+0.17	129
2.4	2.404	+0.17	129	2.404	+0.17	103	2.404	+0.17	64
9.6	9.766	+1.73	31	9.615	+0.16	25	9.766	+1.73	15
19.2	19.531	+1.72	15	19.231	+0.16	12	19.531	+1.72	7
28.8	31.250	+8.51	9	27.778	-3.55	8	31.250	+8.51	4
33.6	34.722	+3.34	8	35.714	+6.29	6	31.250	-6.99	4
57.6	62.500	+8.51	4	62.500	+8.51	3	52.083	-9.58	2
HIGH	1.221	—	255	0.977	—	255	0.610	—	255
LOW	312.500	—	0	250.000	—	0	156.250	—	0

BAUD RATE (K)	Fosc = 4 MHz			Fosc = 3.6864 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	0.300	0	207	0.3	0	191
1.2	1.202	+0.17	51	1.2	0	47
2.4	2.404	+0.17	25	2.4	0	23
9.6	8.929	+6.99	6	9.6	0	5
19.2	20.833	+8.51	2	19.2	0	2
28.8	31.250	+8.51	1	28.8	0	1
33.6	—	—	—	—	—	—
57.6	62.500	+8.51	0	57.6	0	0
HIGH	0.244	—	255	0.225	—	255
LOW	62.500	—	0	57.6	—	0

TABLE 11-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	—	—	—	—	—	—	—	—	—
1.2	—	—	—	—	—	—	—	—	—
2.4	—	—	—	—	—	—	2.441	+1.71	255
9.6	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64
19.2	19.231	+0.16	64	19.231	+0.16	51	19.531	+1.72	31
28.8	29.070	+0.94	42	29.412	+2.13	33	28.409	-1.36	21
33.6	33.784	+0.55	36	33.333	-0.79	29	32.895	-2.10	18
57.6	59.524	+3.34	20	58.824	+2.13	16	56.818	-1.36	10
HIGH	4.883	—	255	3.906	—	255	2.441	—	255
LOW	1250.000	—	0	1000.000	—	0	625.000	—	0

BAUD RATE (K)	Fosc = 4 MHz			Fosc = 3.6864 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	—	—	—	—	—	—
1.2	1.202	+0.17	207	1.2	0	191
2.4	2.404	+0.17	103	2.4	0	95
9.6	9.615	+0.16	25	9.6	0	23
19.2	19.231	+0.16	12	19.2	0	11
28.8	27.798	-3.55	8	28.8	0	7
33.6	35.714	+6.29	6	32.9	-2.04	6
57.6	62.500	+8.51	3	57.6	0	3
HIGH	0.977	—	255	0.9	—	255
LOW	250.000	—	0	230.4	—	0

TABLE 11-5: INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	Fosc = 8 MHz			Fosc = 4 MHz			Fosc = 2 MHz			Fosc = 1 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	—	—	0.300	0	207	0.300	0	103	0.300	0	51
1.2	1.202	+0.16	103	1.202	+0.16	51	1.202	+0.16	25	1.202	+0.16	12
2.4	2.404	+0.16	51	2.404	+0.16	25	2.404	+0.16	12	2.232	-6.99	6
9.6	9.615	+0.16	12	8.929	-6.99	6	10.417	+8.51	2	NA	—	—
19.2	17.857	-6.99	6	20.833	+8.51	2	NA	—	—	NA	—	—
28.8	31.250	+8.51	3	31.250	+8.51	1	31.250	+8.51	0	NA	—	—
38.4	41.667	+8.51	2	NA	—	—	NA	—	—	NA	—	—
57.6	62.500	+8.51	1	62.500	8.51	0	NA	—	—	NA	—	—

TABLE 11-6: INTRC BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	Fosc = 8 MHz			Fosc = 4 MHz			Fosc = 2 MHz			Fosc = 1 MHz		
	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)	KBAUD	% ERROR	SPBRG value (decimal)
0.3	NA	—	—	NA	—	—	NA	—	—	0.300	0	207
1.2	NA	—	—	1.202	+0.16	207	1.202	+0.16	103	1.202	+0.16	51
2.4	2.404	+0.16	207	2.404	+0.16	103	2.404	+0.16	51	2.404	+0.16	25
9.6	9.615	+0.16	51	9.615	+0.16	25	9.615	+0.16	12	8.929	-6.99	6
19.2	19.231	+0.16	25	19.231	+0.16	12	17.857	-6.99	6	20.833	+8.51	2
28.8	29.412	+2.12	16	27.778	-3.55	8	31.250	+8.51	3	31.250	+8.51	1
38.4	38.462	+0.16	12	35.714	-6.99	6	41.667	+8.51	2	NA	—	—
57.6	55.556	-3.55	8	62.500	+8.51	3	62.500	+8.51	1	62.500	+8.51	0

11.2 AUSART Asynchronous Mode

In this mode, the AUSART uses standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip, dedicated, 8-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator. The AUSART transmits and receives the LSb first. The transmitter and receiver are functionally independent, but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during Sleep.

Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

The AUSART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

11.2.1 AUSART ASYNCHRONOUS TRANSMITTER

The AUSART transmitter block diagram is shown in Figure 11-1. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available). Once the TXREG register transfers the data to the TSR register (occurs in one Tcy), the TXREG register is empty and flag bit, TXIF (PIR1<4>), is set. This

interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

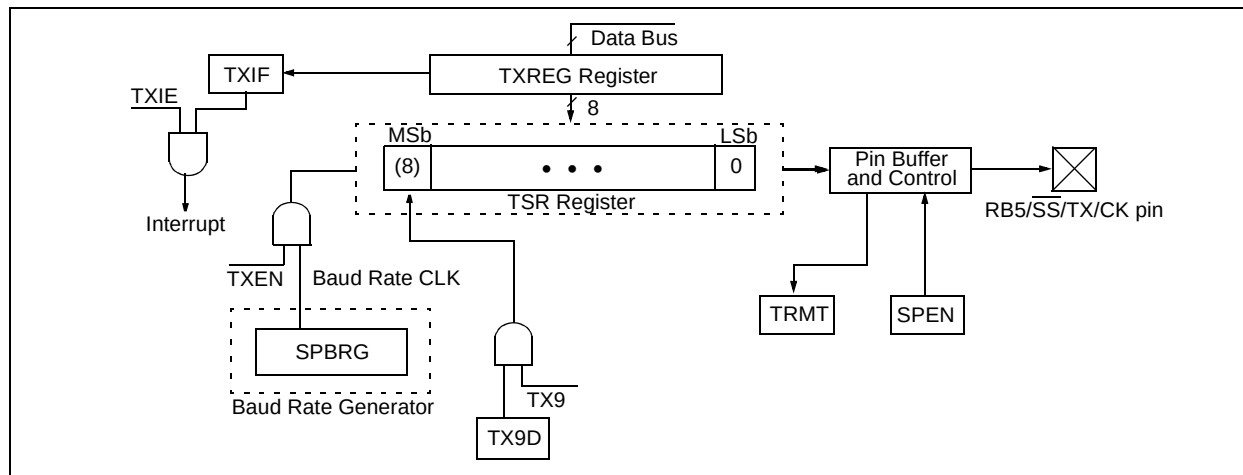
Note 1: The TSR register is not mapped in data memory, so it is not available to the user.

2: Flag bit TXIF is set when enable bit TXEN is set. TXIF is cleared by loading TXREG.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data and the Baud Rate Generator (BRG) has produced a shift clock (Figure 11-2). The transmission can also be started by first loading the TXREG register and then setting enable bit TXEN. Normally, when transmission is first started, the TSR register is empty. At that point, transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 11-3). Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. As a result, the RB5/SS/TX/CK pin will revert to high-impedance.

In order to select 9-bit transmission, transmit bit, TX9 (TXSTA<6>), should be set and the ninth bit should be written to TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG register can result in an immediate transfer of the data to the TSR register (if the TSR is empty). In such a case, an incorrect ninth data bit may be loaded in the TSR register.

FIGURE 11-1: AUSART TRANSMIT BLOCK DIAGRAM



When setting up an asynchronous transmission, follow these steps:

1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH (Section 11.1 “AUSART Baud Rate Generator (BRG)”).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).
8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

FIGURE 11-2: ASYNCHRONOUS MASTER TRANSMISSION

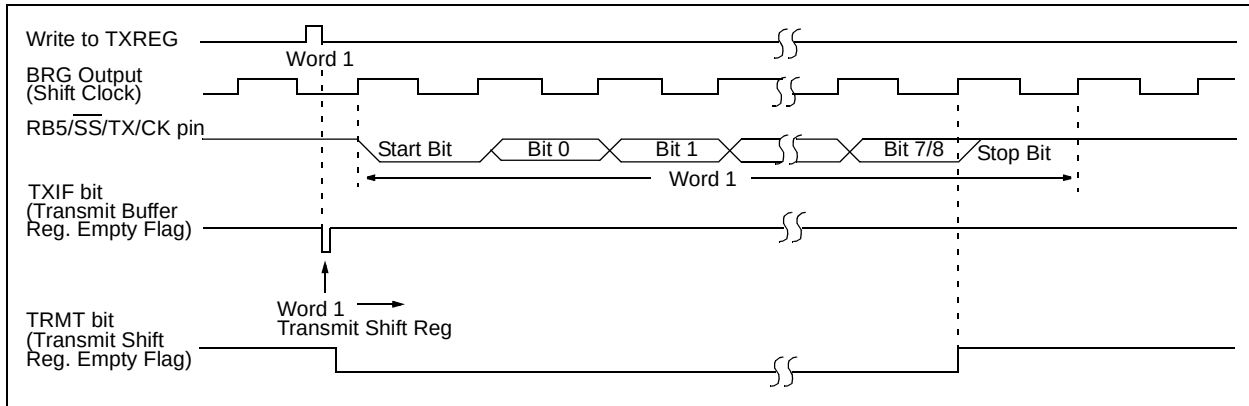


FIGURE 11-3: ASYNCHRONOUS MASTER TRANSMISSION (BACK TO BACK)

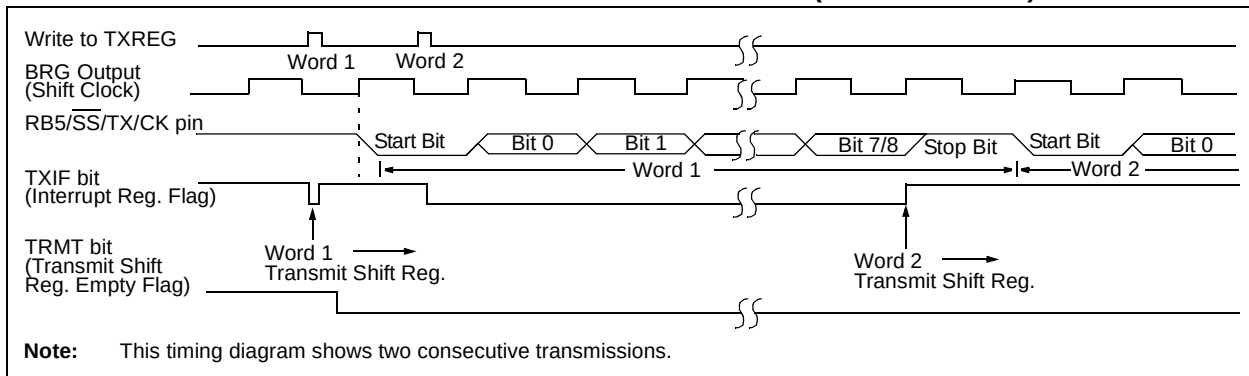


TABLE 11-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous transmission.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

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11.2.2 AUSART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 11-4. The data is received on the RB2/SDO/RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter, operating at x16 times the baud rate; whereas, the main receive serial shifter operates at the bit rate or at F_{osc} .

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the Receive (Serial) Shift Register (RSR). After sampling the Stop bit, the received data in the RSR is transferred to the RCREG register (if it is empty). If the transfer is complete, flag bit, RCIF (PIR1<5>), is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>). Flag bit RCIF is a read-only bit which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty. The RCREG is a double-buffered register (i.e., it is a two-deep FIFO). It

is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the Stop bit of the third byte, if the RCREG register is still full, the Overrun Error bit, OERR (RCSTA<1>), will be set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Overrun bit OERR has to be cleared in software. This is done by resetting the receive logic (CREN is cleared and then set). If bit OERR is set, transfers from the RSR register to the RCREG register are inhibited and no further data will be received. It is, therefore, essential to clear error bit OERR if it is set. Framing Error bit, FERR (RCSTA<2>), is set if a Stop bit is detected as clear. Bit FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG will load bits RX9D and FERR with new values; therefore, it is essential for the user to read the RCSTA register, before reading the RCREG register, in order not to lose the old FERR and RX9D information.

FIGURE 11-4: AUSART RECEIVE BLOCK DIAGRAM

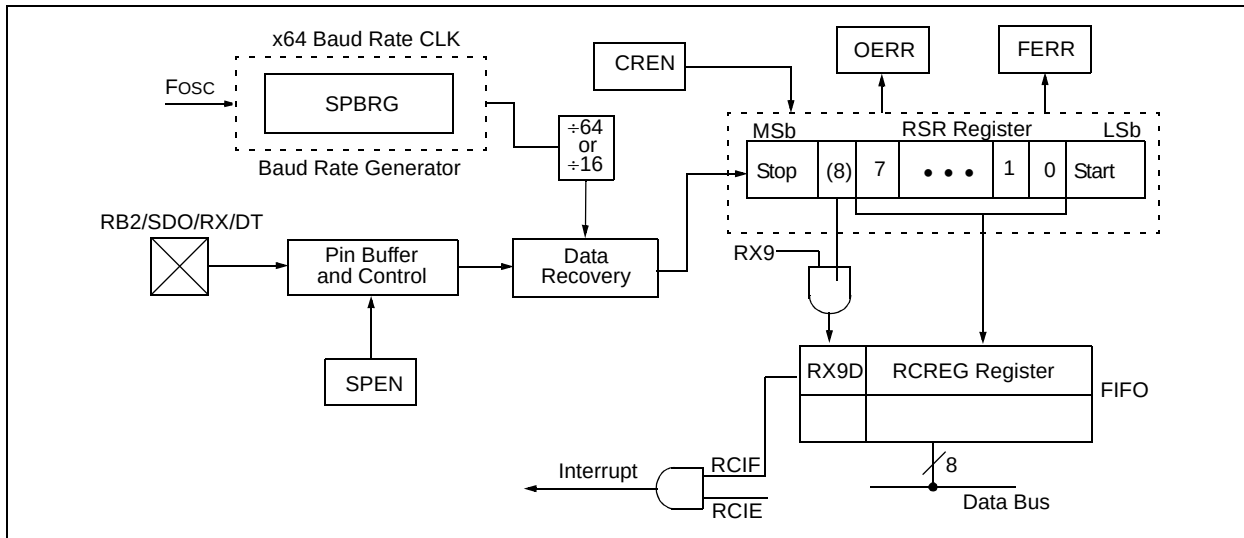
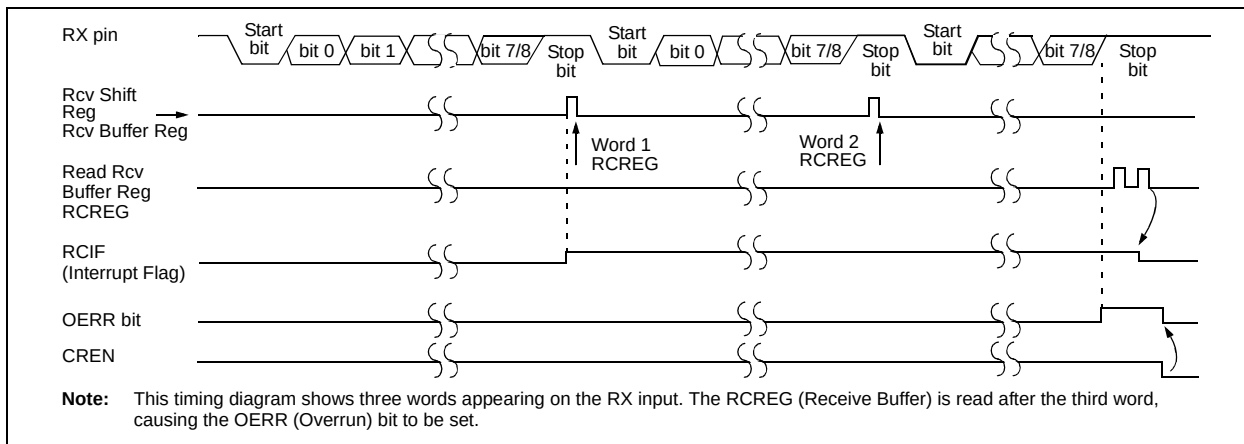


FIGURE 11-5: ASYNCHRONOUS RECEPTION



When setting up an asynchronous reception, follow these steps:

1. Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH (Section 11.1 “AUSART Baud Rate Generator (BRG)”).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit RCIE.
4. If 9-bit reception is desired, then set bit RX9.
5. Enable the reception by setting bit CREN.
6. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE is set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.
10. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-8: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	AUSART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

When setting up an asynchronous reception with address detect enabled:

- Initialize the SPBRG register for the appropriate baud rate. If a high-speed baud rate is desired, set bit BRGH.
- Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
- If interrupts are desired, then set enable bit RCIE.
- Set bit RX9 to enable 9-bit reception.
- Set ADDEN to enable address detect.
- Enable the reception by setting enable bit CREN.

- Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
- Read the RSTA register to get the ninth bit and determine if any error occurred during reception.
- Read the 8-bit received data by reading the RCREG register to determine if the device is being addressed.
- If any error occurred, clear the error by clearing enable bit CREN.
- If the device has been addressed, clear the ADDEN bit to allow data bytes and address bytes to be read into the receive buffer and interrupt the CPU.

The diagram illustrates the SPI module architecture. It starts with the **FOSC** input to the **Baud Rate Generator** (containing **SPBRG** and a divider of $\div 64$ or $\div 16$). The **Baud Rate Generator** is clocked by **x64 Baud Rate CLK**. The output of the divider goes to the **RSR Register** (bits 0-7) and the **MSb** (bit 8). The **RSR Register** is also clocked by **CREN**. The **MSb** output is ANDed with **RX9** to produce the **Enable Load of Receive Buffer** signal. The **RSR Register** output (bits 0-7) is ANDed with **RX9** to produce the **Receive Buffer** signal. The **Receive Buffer** signal is then loaded into the **RX9D** register. The **RX9D** register is part of the **RCREG Register** (FIFO). The **RCREG Register** output (bits 0-7) is connected to the **Data Bus**. The **RCIF** (Receive Complete Interrupt Flag) is set when the **RCREG Register** is full, and it is ANDed with **RCIE** (Receive Complete Interrupt Enable) to produce the **Interrupt** signal.

FIGURE 11-7: ASYNCHRONOUS RECEPTION WITH ADDRESS DETECT

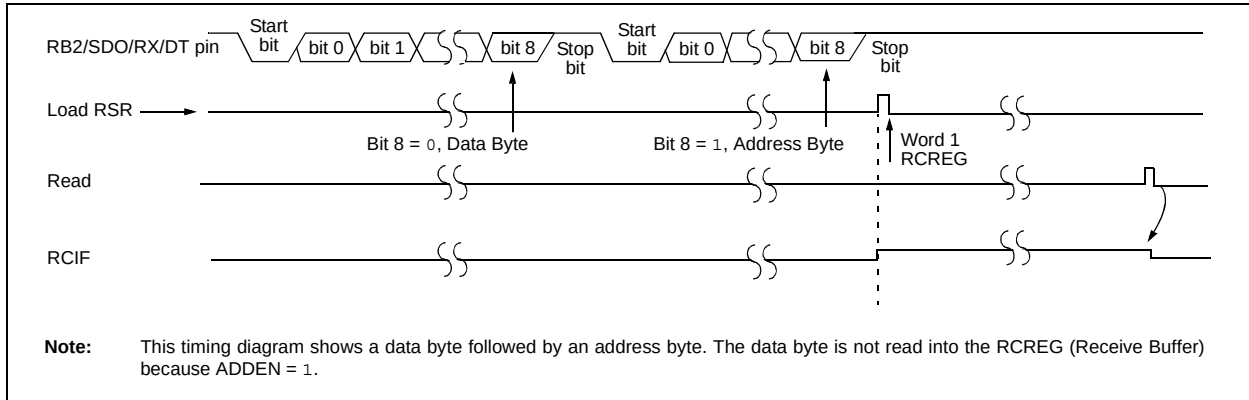


FIGURE 11-8: ASYNCHRONOUS RECEPTION WITH ADDRESS BYTE FIRST

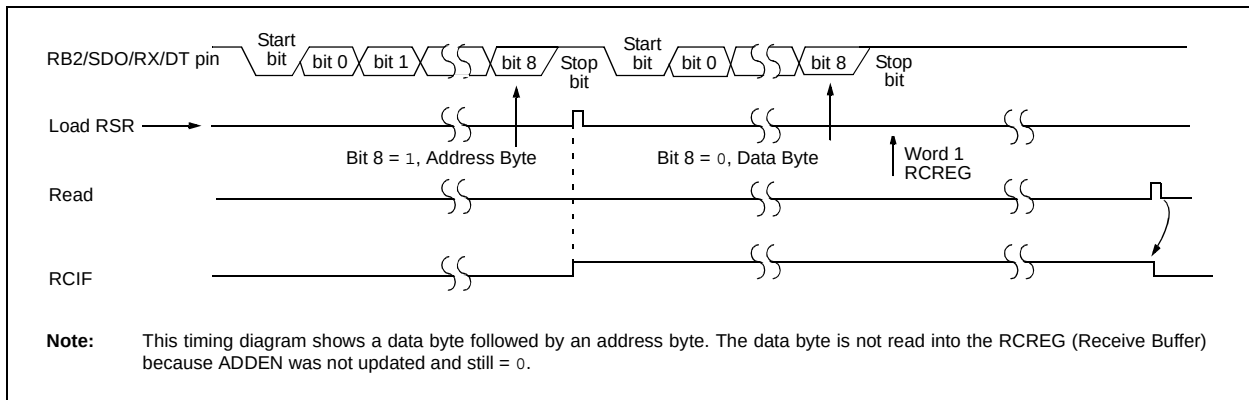


TABLE 11-9: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	AUSART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for asynchronous reception.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

11.3 AUSART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RB5/SS/TX/CK and RB2/SDO/RX/DT I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTA<7>).

11.3.1 AUSART SYNCHRONOUS MASTER TRANSMISSION

The AUSART transmitter block diagram is shown in Figure 11-6. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once the TXREG register transfers the data to the TSR register (occurs in one T_{CYCLE}), the TXREG is empty and interrupt bit TXIF (PIR1<4>) is set. The interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>). Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register. While flag bit TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

Transmission is enabled by setting enable bit TXEN (TXSTA<5>). The actual transmission will not occur until the TXREG register has been loaded with data. The first data bit will be shifted out on the next available rising edge of the clock on the CK line. Data out is stable around the falling edge of the synchronous clock (Figure 11-9). The transmission can also be started by first loading the TXREG register and then setting bit TXEN (Figure 11-10). This is advantageous when slow baud rates are selected, since the BRG is kept in Reset when bits TXEN, CREN and SREN are clear. Setting enable bit TXEN will start the BRG, creating a shift clock immediately. Normally, when transmission is first started, the TSR register is empty, so a transfer to the TXREG register will result in an immediate transfer to TSR, resulting in an empty TXREG. Back-to-back transfers are possible.

Clearing enable bit TXEN during a transmission will cause the transmission to be aborted and will reset the transmitter. The DT and CK pins will revert to high-impedance. If either bit CREN or bit SREN is set during a transmission, the transmission is aborted and the DT pin reverts to a high-impedance state (for a reception). The CK pin will remain an output if bit CSRC is set (internal clock). The transmitter logic, however, is not reset, although it is disconnected from the pins. In order to reset the transmitter, the user has to clear bit TXEN. If bit SREN is set (to interrupt an on-going transmission and receive a single word), then after the single word is received, bit SREN will be cleared and the serial port will revert back to transmitting, since bit TXEN is still set. The DT line will immediately switch from High-Impedance Receive mode to transmit and start driving. To avoid this, bit TXEN should be cleared.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit should be written to bit TX9D (TXSTA<0>). The ninth bit must be written before writing the 8-bit data to the TXREG register. This is because a data write to the TXREG can result in an immediate transfer of the data to the TSR register (if the TSR is empty). If the TSR was empty and the TXREG was written before writing the “new” TX9D, the “present” value of bit TX9D is loaded.

Steps to follow when setting up a synchronous master transmission:

1. Initialize the SPBRG register for the appropriate baud rate (**Section 11.1 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. If interrupts are desired, set enable bit TXIE.
4. If 9-bit transmission is desired, set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous master transmission.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

FIGURE 11-9: SYNCHRONOUS TRANSMISSION

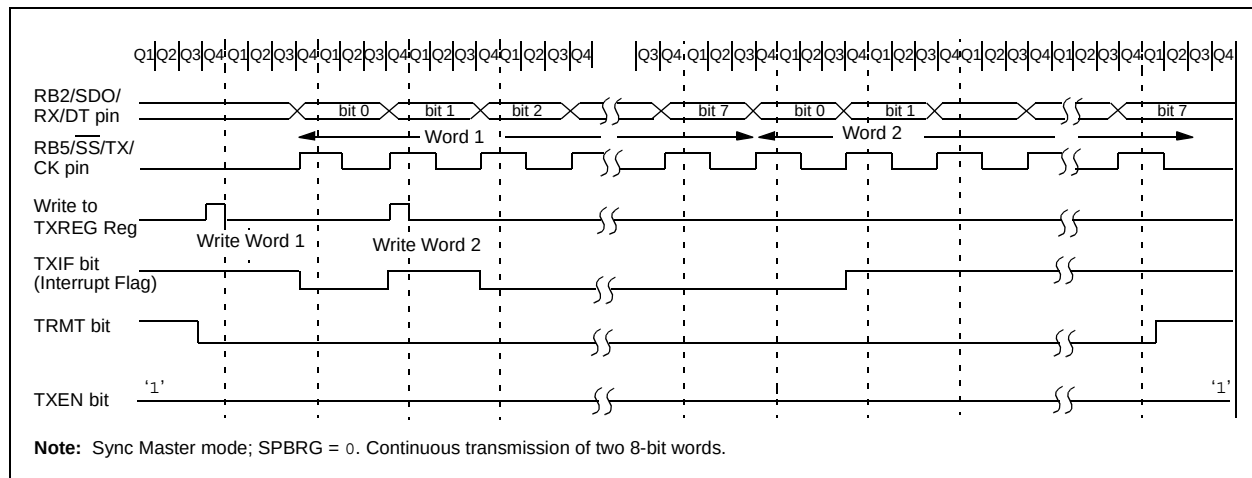
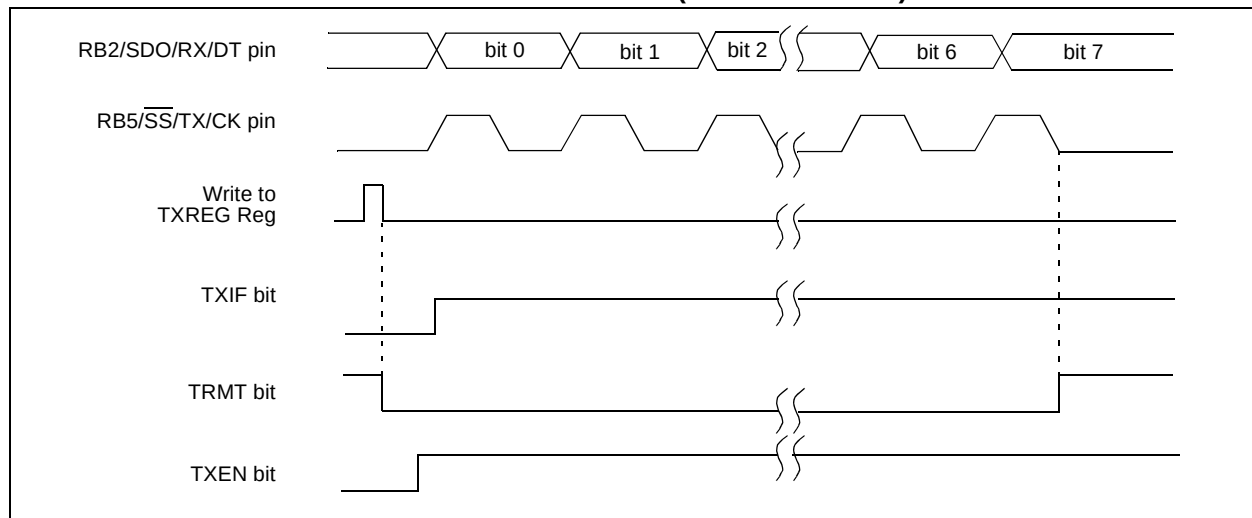


FIGURE 11-10: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



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11.3.2 AUSART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either enable bit SREN (RCSTA<5>), or enable bit CREN (RCSTA<4>). Data is sampled on the RB2/SDO/RX/DT pin on the falling edge of the clock. If enable bit SREN is set, then only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, CREN takes precedence.

After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to the RCREG register (if it is empty). When the transfer is complete, interrupt flag bit, RCIF (PIR1<5>), is set. The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>).

Flag bit RCIF is a read-only bit which is reset by the hardware. In this case, it is reset when the RCREG register has been read and is empty. The RCREG is a double-buffered register (i.e., it is a two-deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR register. On the clocking of the last bit of the third byte, if the RCREG register is still full, then Overrun Error bit, OERR (RCSTA<1>), is set. The word in the RSR will be lost. The RCREG register can be read twice to retrieve the two bytes in the FIFO. Bit OERR has to be cleared in software (by clearing bit CREN). If bit OERR is set, transfers from the RSR to the RCREG are inhibited, so it is essential to clear bit OERR if it is set. The ninth receive bit is buffered the same way as the

receive data. Reading the RCREG register will load bit RX9D with a new value, therefore, it is essential for the user to read the RCSTA register, before reading RCREG, in order not to lose the old RX9D information.

When setting up a synchronous master reception:

1. Initialize the SPBRG register for the appropriate baud rate (**Section 11.1 “AUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Ensure bits CREN and SREN are clear.
4. If interrupts are desired, then set enable bit RCIE.
5. If 9-bit reception is desired, then set bit RX9.
6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
7. Interrupt flag bit, RCIF, will be set when reception is complete and an interrupt will be generated if enable bit, RCIE, was set.
8. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREG register.
10. If any error occurred, clear the error by clearing bit CREN.
11. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

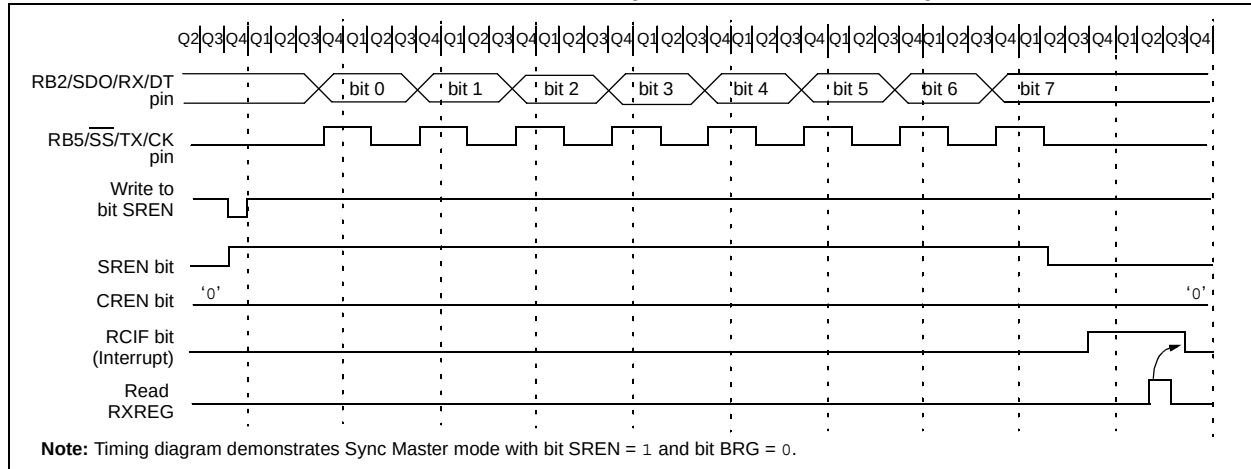
TABLE 11-11: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	AUSART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous master reception.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

FIGURE 11-11: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



11.4 AUSART Synchronous Slave Mode

Synchronous Slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the RB5/SS/TX/CK pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in Sleep mode. Slave mode is entered by clearing bit CSRC (TXSTA<7>).

11.4.1 AUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes is identical, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- The second word will remain in the TXREG register.
- Flag bit TXIF will not be set.
- When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit TXIF will now be set.

- If enable bit TXIE is set, the interrupt will wake the chip from Sleep and if the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

When setting up a synchronous slave transmission, follow these steps:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- Clear bits CREN and SREN.
- If interrupts are desired, then set enable bit TXIE.
- If 9-bit transmission is desired, then set bit TX9.
- Enable the transmission by setting enable bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREG register.
- If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-12: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
19h	TXREG	AUSART Transmit Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

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11.4.2 AUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the Sleep mode. Bit SREN is a “don’t care” in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during Sleep. On completely receiving the word, the RSR register will transfer the data to the RCREG register and if enable bit RCIE bit is set, the interrupt generated will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector (0004h).

When setting up a synchronous slave reception, follow these steps:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. If interrupts are desired, set enable bit RCIE.
3. If 9-bit reception is desired, set bit RX9.
4. To enable reception, set enable bit CREN.
5. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE was set.
6. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREG register.
8. If any error occurred, clear the error by clearing bit CREN.
9. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

TABLE 11-13: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
1Ah	RCREG	AUSART Receive Data Register								0000 0000	0000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception.

Note 1: This bit is only implemented on the PIC16F88. The bit will read '0' on the PIC16F87.

12.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The Analog-to-Digital (A/D) converter module has seven inputs for 18/20 pin devices (PIC16F88 devices only).

The conversion of an analog input signal results in a corresponding 10-bit digital number. The A/D module has a high and low-voltage reference input that is software selectable to some combination of VDD, VSS, VREF- (RA2) or VREF+ (RA3).

The A/D converter has a unique feature of being able to operate while the device is in Sleep mode. To operate in Sleep, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The A/D module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- Analog Select Register (ANSEL)

The ADCON0 register, shown in Register 12-2, controls the operation of the A/D module. The ANSEL register, shown in Register 12-1 and the ADCON1 register, shown in Register 12-3, configure the functions of the port pins. The port pins can be configured as analog inputs (RA3/RA2 can also be voltage references) or as digital I/O.

Additional information on using the A/D module can be found in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

REGISTER 12-1: ANSEL: ANALOG SELECT REGISTER (ADDRESS 9Bh) PIC16F88 DEVICES ONLY

U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ANS<6:0>:** Analog Input Select bits

Bits select input function on corresponding AN<6:0> pins.

1 = Analog I/O^(1,2)

0 = Digital I/O

Note 1: Setting a pin to an analog input disables the digital input buffer. The corresponding TRIS bit should be set to input mode when using pins as analog inputs. Only AN2 is an analog I/O, all other ANx pins are analog inputs.

2: See the block diagrams for the analog I/O pins to see how ANSEL interacts with the CHS bits of the ADCON0 register.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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REGISTER 12-2: ADCON0: A/D CONTROL REGISTER (ADDRESS 1Fh) PIC16F88 DEVICES ONLY

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON
bit 7							bit 0

bit 7-6 **ADCS<1:0>**: A/D Conversion Clock Select bits

If ADCS2 = 0:

00 = Fosc/2

01 = Fosc/8

10 = Fosc/32

11 = FRC (clock derived from the internal A/D module RC oscillator)

If ADCS2 = 1:

00 = Fosc/4

01 = Fosc/16

10 = Fosc/64

11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 **CHS<2:0>**: Analog Channel Select bits

000 = Channel 0 (RA0/AN0)

001 = Channel 1 (RA1/AN1)

010 = Channel 2 (RA2/AN2)

011 = Channel 3 (RA3/AN3)

100 = Channel 4 (RA4/AN4)

101 = Channel 5 (RB6/AN5)

110 = Channel 6 (RB7/AN6)

bit 2 **GO/DONE**: A/D Conversion Status bit

If ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion)

0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

1 = A/D converter module is operating

0 = A/D converter module is shut off and consumes no operating current

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 12-3: ADCON1: A/D CONTROL REGISTER 1 (ADDRESS 9Fh) PIC16F88 DEVICES ONLY

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Clock Divide by 2 Select bit

1 = A/D clock source is divided by 2 when system clock is used

0 = Disabled

bit 5-4 **VCFG<1:0>:** A/D Voltage Reference Configuration bits

Logic State	VREF+	VREF-
00	AVDD	AVSS
01	AVDD	VREF-
10	VREF+	AVSS
11	VREF+	VREF-

Note: The ANSEL bits for AN3 and AN2 inputs must be configured as analog inputs for the VREF+ and VREF- external pins to be used.

bit 3-0 **Unimplemented:** Read as '0'

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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The ADRESH:ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the A/D Result register pair, the GO/DONE bit (ADCON0<2>) is cleared and A/D Interrupt Flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 12-1.

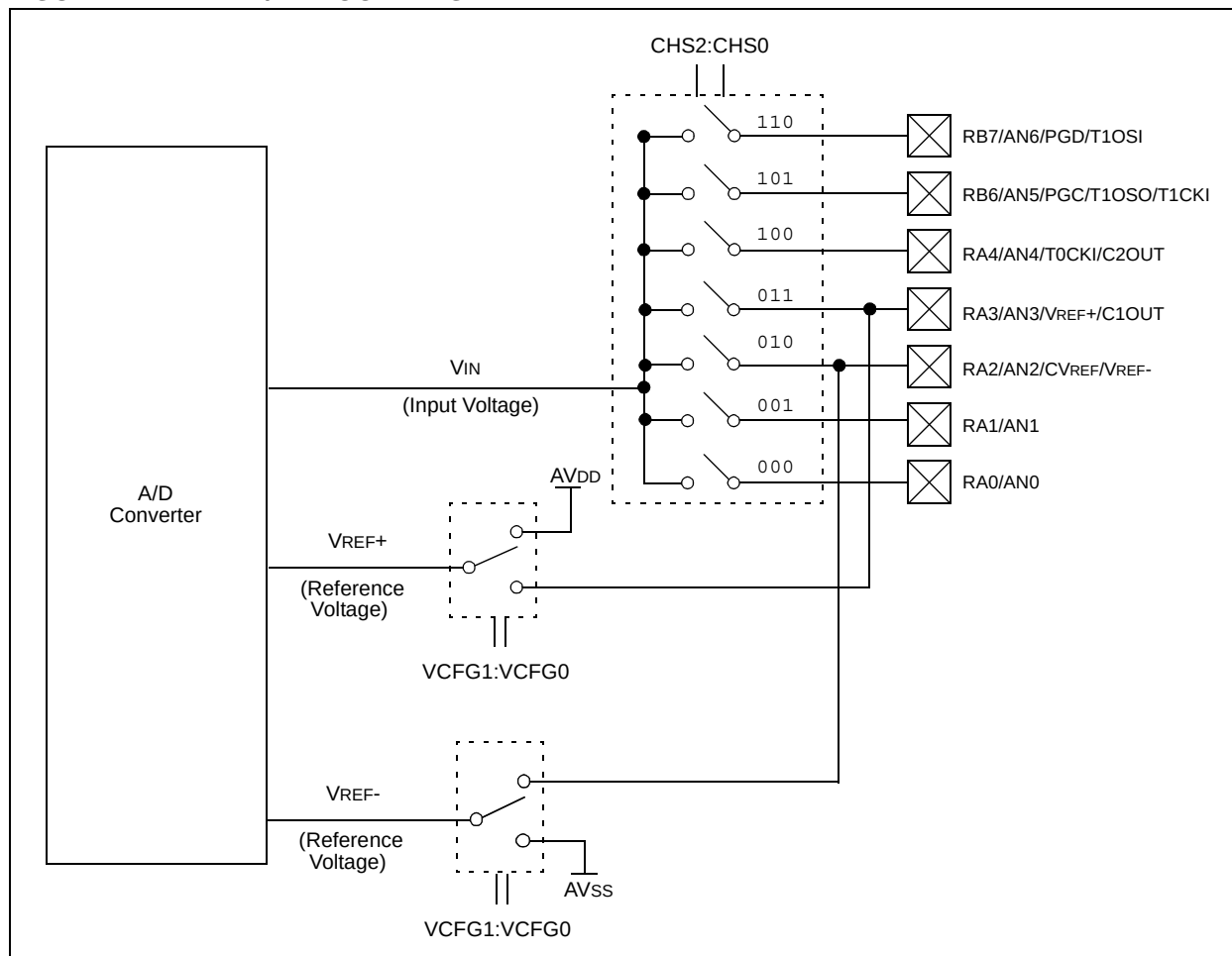
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as inputs.

To determine sample time, see **Section 12.1 “A/D Acquisition Requirements”**. After this sample time has elapsed, the A/D conversion can be started.

These steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
 - Configure analog/digital I/O (ANSEL)
 - Configure voltage reference (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON0)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - SET PEIE bit
 - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
 - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared (with interrupts disabled); OR
 - Waiting for the A/D interrupt
6. Read A/D Result register pair (ADRESH:ADRESL), clear bit ADIF if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as T_{AD} . A minimum wait of 2 T_{AD} is required before the next acquisition starts.

FIGURE 12-1: A/D BLOCK DIAGRAM



12.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 12-2. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 12-2. **The maximum recommended impedance for analog sources is 10 kΩ.** As the impedance is decreased, the

acquisition time may be decreased. After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 12-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, TACQ, see the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

EQUATION 12-1: ACQUISITION TIME

$$\begin{aligned}
 T_{ACQ} &= \text{Amplifier Settling Time} + \text{Hold Capacitor Charging Time} + \text{Temperature Coefficient} \\
 &= T_{AMP} + T_C + T_{COFF} \\
 &= 2 \mu s + T_C + [(\text{Temperature} - 25^\circ C)(0.05 \mu s / ^\circ C)] \\
 T_C &= CHOLD (R_{IC} + R_{SS} + R_S) \ln(1/2047) \\
 &= -120 \text{ pF} (1 \text{ k}\Omega + 7 \text{ k}\Omega + 10 \text{ k}\Omega) \ln(0.0004885) \\
 &= 16.47 \mu s \\
 T_{ACQ} &= 2 \mu s + 16.47 \mu s + [(50^\circ C - 25^\circ C)(0.05 \mu s / ^\circ C)] \\
 &= 19.72 \mu s
 \end{aligned}$$

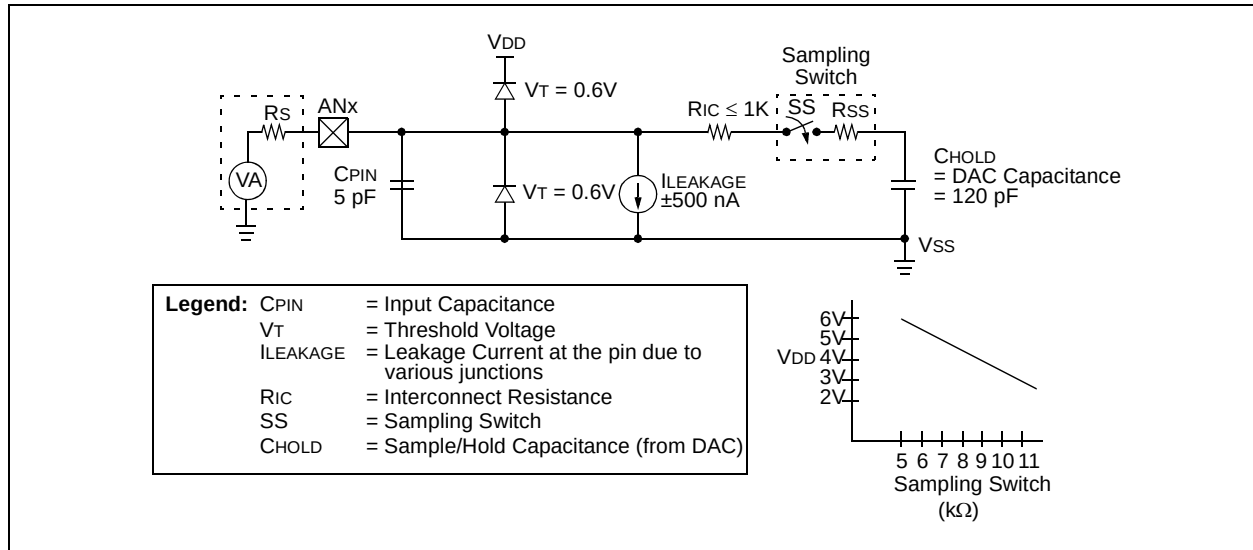
Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

4: After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.

FIGURE 12-2: ANALOG INPUT MODEL



12.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as T_{AD} . The A/D conversion requires 9.0 T_{AD} per 10-bit conversion. The source of the A/D conversion clock is software selectable. The seven possible options for T_{AD} are:

- 2 T_{OSC}
- 4 T_{OSC}
- 8 T_{OSC}
- 16 T_{OSC}
- 32 T_{OSC}
- 64 T_{OSC}
- Internal A/D module RC oscillator (2-6 μs)

For correct A/D conversions, the A/D conversion clock (T_{AD}) must be selected to ensure a minimum T_{AD} time as small as possible, but no less than 1.6 μs and not greater than 6.4 μs .

Table 12-1 shows the resultant T_{AD} times derived from the device operating frequencies and the A/D clock source selected.

12.3 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the $ADCS2:ADCS0$ bits in $ADCON0$ and $ADCON1$ should be updated in accordance with the power-managed mode clock that will be used. After the power-managed mode is entered (either of the power-managed Run modes), an A/D acquisition or conversion may be started. Once an acquisition or conversion is started, the device should continue to be clocked by the same power-managed mode clock source until the conversion has been completed.

If the power-managed mode clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

TABLE 12-1: T_{AD} vs. MAXIMUM DEVICE OPERATING FREQUENCIES – STANDARD DEVICES (C)

AD Clock Source (T_{AD})			Maximum Device Frequency
Operation	$ADCS<2>$	$ADCS<1:0>$	Max.
2 T_{OSC}	0	00	1.25 MHz
4 T_{OSC}	1	00	2.5 MHz
8 T_{OSC}	0	01	5 MHz
16 T_{OSC}	1	01	10 MHz
32 T_{OSC}	0	10	20 MHz
64 T_{OSC}	1	10	20 MHz
RC ^(1,2,3)	x	11	(Note 1)

- Note 1:** The RC source has a typical T_{AD} time of 4 μs , but can vary between 2-6 μs .
- 2:** When the device frequencies are greater than 1 MHz, the RC A/D conversion clock source is only recommended for Sleep operation.
- 3:** For extended voltage devices (LF), please refer to **Section 18.0 “Electrical Characteristics”**.

12.4 Configuring Analog Port Pins

The ADCON1, ANSEL, TRISA and TRISB registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<2:0> bits and the TRIS bits.

Note 1: When reading the Port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

2: Analog levels on any pin that is defined as a digital input (including the RA4:RA0 and RB7:RB6 pins), may cause the input buffer to consume current out of the device specification.

12.5 A/D Conversions

Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D Result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2 TAD wait is required before the next acquisition is started. After this 2 TAD wait, acquisition on the selected channel is automatically started. The GO/DONE bit can then be set to start the conversion.

In Figure 12-3, after the GO/DONE bit is set, the first time segment has a minimum of Tcy and a maximum of TAD.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

12.5.1 A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16 bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. Figure 12-4 shows the operation of the A/D result justification. The extra bits are loaded with '0's. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

FIGURE 12-3: A/D CONVERSION TAD CYCLES

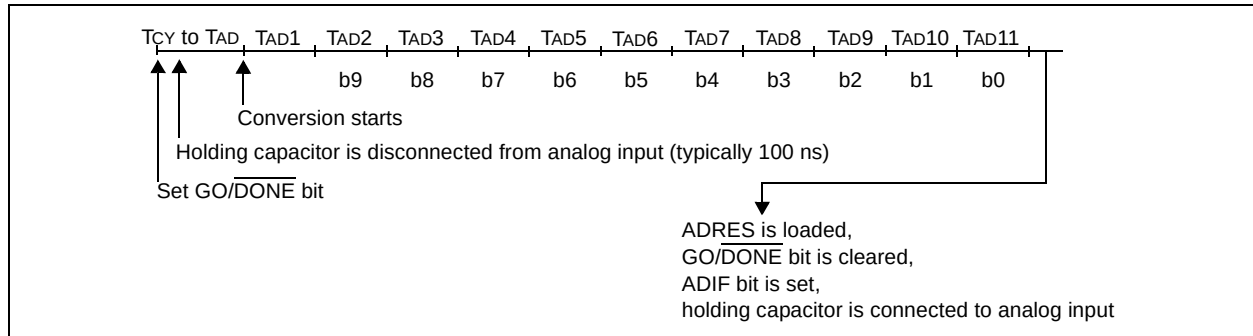
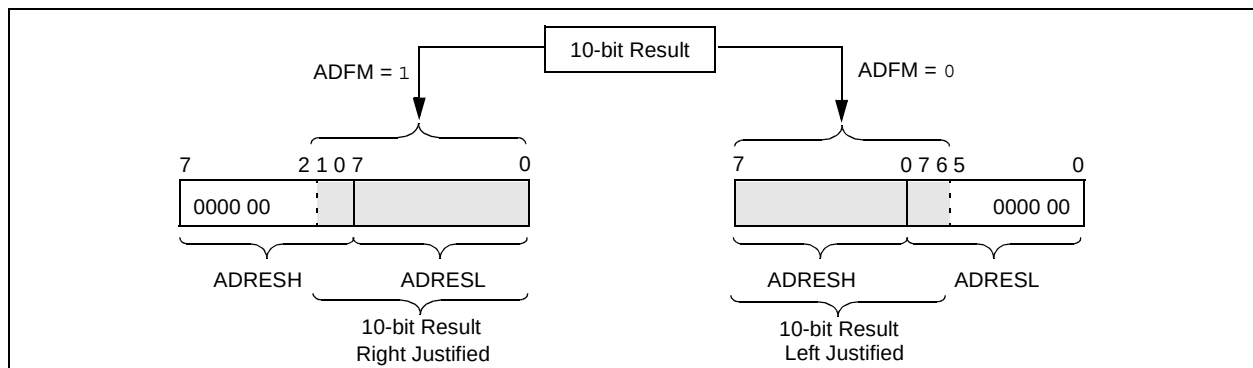


FIGURE 12-4: A/D RESULT JUSTIFICATION



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12.6 A/D Operation During Sleep

The A/D module can operate during Sleep mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the *SLEEP* instruction to be executed which eliminates all digital switching noise from the conversion. When the conversion is completed, the *GO/DONE* bit will be cleared and the result loaded into the ADRES registers. If the A/D interrupt is enabled, the device will wake-up from Sleep. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a *SLEEP* instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note: For the A/D module to operate in Sleep, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in Sleep, ensure the *SLEEP* instruction immediately follows the instruction that sets the *GO/DONE* bit.

12.7 Effects of a Reset

A device Reset forces all registers to their Reset state. The A/D module is disabled and any conversion in progress is aborted. All A/D input pins are configured as analog inputs.

The value that is in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

12.8 Use of the CCP Trigger

An A/D conversion can be started by the “special event trigger” of the CCP module. This requires that the CCP1M3:CCP1M0 bits (CCP1CON<3:0>) be programmed as ‘1011’ and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the *GO/DONE* bit will be set, starting the A/D conversion and the Timer1 counter will be reset to zero. Timer1 is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving the ADRESH:ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the “special event trigger” sets the *GO/DONE* bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), then the “special event trigger” will be ignored by the A/D module, but will still reset the Timer1 counter.

TABLE 12-2: REGISTERS/BITS ASSOCIATED WITH A/D

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Ch	PIR1	—	ADIF ⁽¹⁾	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	-000 0000	-000 0000
8Ch	PIE1	—	ADIE ⁽¹⁾	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	-000 0000	-000 0000
1Eh	ADRESH ⁽²⁾	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
9Eh	ADRESL ⁽²⁾	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
1Fh	ADCON0 ⁽²⁾	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	—	ADON	0000 00-0	0000 00-0
9Fh	ADCON1 ⁽²⁾	ADFM	ADCS2	VCFG1	VCFG0	—	—	—	—	0000 ----	0000 ----
9Bh	ANSEL ⁽²⁾	—	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	-111 1111	-111 1111
05h	PORTA (PIC16F87) (PIC16F88)	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000 xxx0 0000	uuuu 0000 uuu0 0000
05h, 106h	PORTB (PIC16F87) (PIC16F88)	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx 00xx xxxx	uuuu uuuu 00uu uuuu
85h	TRISA	TRISA7	TRISA6	TRISA5 ⁽³⁾	PORTA Data Direction Register (TRISA<4:0>)					1111 1111	1111 1111
86h, 186h	TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as ‘0’. Shaded cells are not used for A/D conversion.

Note 1: This bit is only implemented on the PIC16F88. The bit will read ‘0’ on the PIC16F87.

2: PIC16F88 only.

3: Pin 5 is an input only; the state of the TRISA5 bit has no effect and will always read ‘1’.

13.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with I/O port pins RA0 through RA3, while the outputs are multiplexed to pins RA3 and RA4. The on-chip Voltage Reference (**Section 14.0 “Comparator Voltage Reference Module”**) can also be an input to the comparators.

The CMCON register (Register 13-1) controls the comparator input and output multiplexors. A block diagram of the various comparator configurations is shown in Figure 13-1.

REGISTER 13-1: CMCON: COMPARATOR MODULE CONTROL REGISTER (ADDRESS 9Ch)

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							bit 0

bit 7 **C2OUT:** Comparator 2 Output bit

When C2INV = 0:

1 = C2 VIN+ > C2 VIN-

0 = C2 VIN+ < C2 VIN-

When C2INV = 1:

1 = C2 VIN+ < C2 VIN-

0 = C2 VIN+ > C2 VIN-

bit 6 **C1OUT:** Comparator 1 Output bit

When C1INV = 0:

1 = C1 VIN+ > C1 VIN-

0 = C1 VIN+ < C1 VIN-

When C1INV = 1:

1 = C1 VIN+ < C1 VIN-

0 = C1 VIN+ > C1 VIN-

bit 5 **C2INV:** Comparator 2 Output Inversion bit

1 = C2 output inverted

0 = C2 output not inverted

bit 4 **C1INV:** Comparator 1 Output Inversion bit

1 = C1 output inverted

0 = C1 output not inverted

bit 3 **CIS:** Comparator Input Switch bit

When CM2:CM0 = 001:

1 = C1 VIN- connects to RA3

0 = C1 VIN- connects to RA0

When CM2:CM0 = 010:

1 = C1 VIN- connects to RA3

C2 VIN- connects to RA2

0 = C1 VIN- connects to RA0

C2 VIN- connects to RA1

bit 2-0 **CM<2:0>:** Comparator Mode bits

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

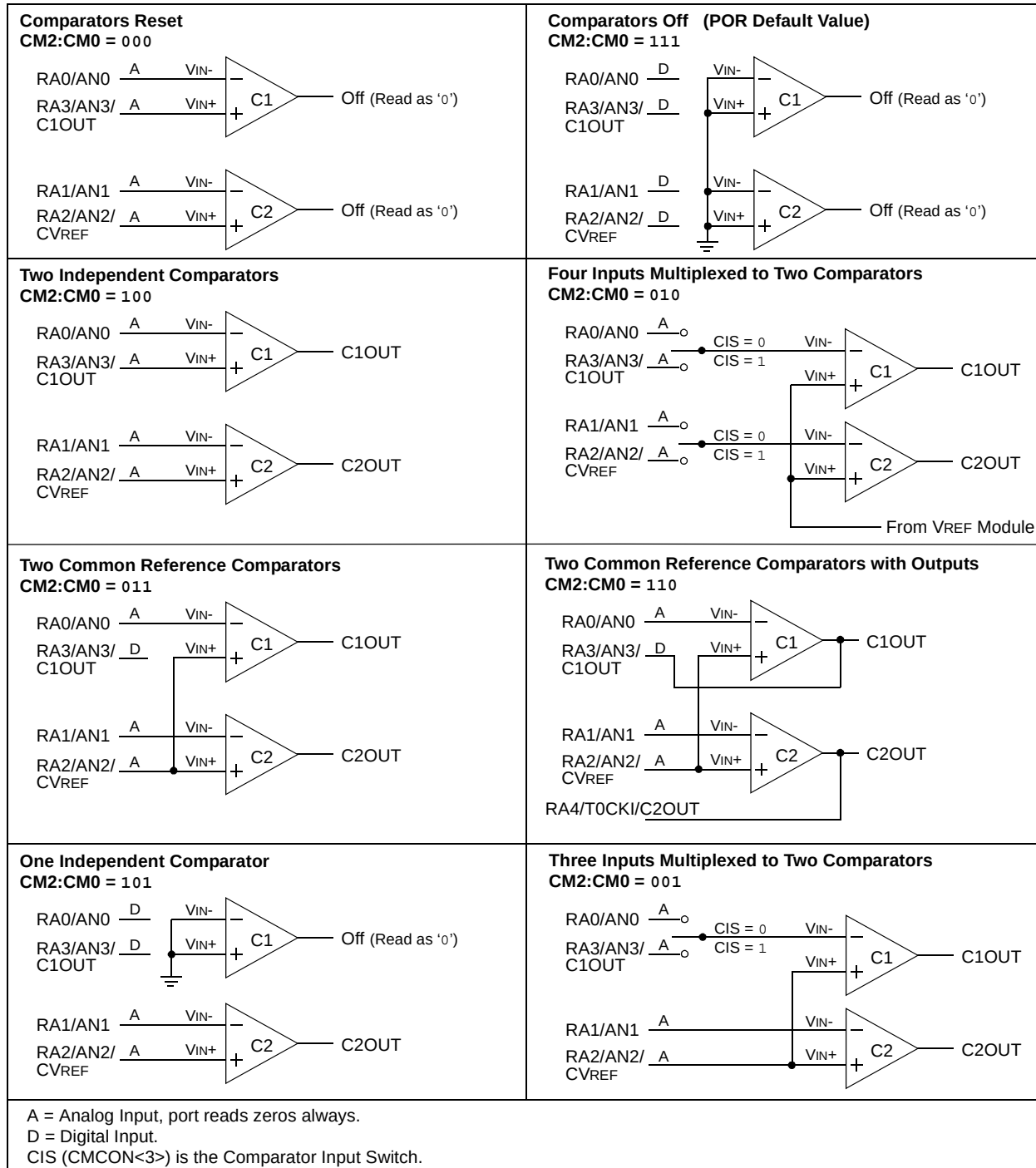
x = Bit is unknown

13.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select these modes. Figure 13-1 shows the eight possible modes. The TRISA register controls the data direction of the comparator pins for each mode. If the Comparator mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Section 18.0 "Electrical Characteristics".

Note: Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may occur.

FIGURE 13-1: COMPARATOR I/O OPERATING MODES



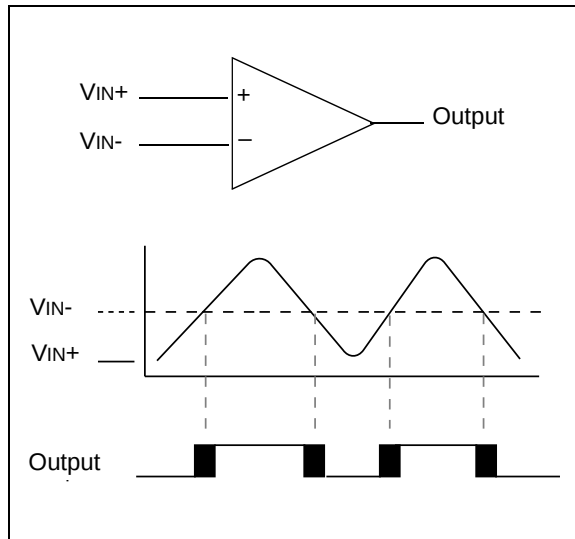
13.2 Comparator Operation

A single comparator is shown in Figure 13-2, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 13-2 represent the uncertainty due to input offsets and response time.

13.3 Comparator Reference

An external or internal reference signal may be used depending on the comparator operating mode. The analog signal present at V_{IN-} is compared to the signal at V_{IN+} and the digital output of the comparator is adjusted accordingly (Figure 13-2).

FIGURE 13-2: SINGLE COMPARATOR



13.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same, or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between V_{SS} and V_{DD} and can be applied to either pin of the comparator(s).

13.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. **Section 14.0 "Comparator Voltage Reference Module"** contains a detailed description of the Comparator Voltage Reference module that provides this signal. The internal reference signal is used when comparators are in mode $CM<2:0> = 010$ (Figure 13-1). In this mode, the internal voltage reference is applied to the V_{IN+} pin of both comparators.

13.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (**Section 18.0 "Electrical Characteristics"**).

13.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RA3 and RA4 I/O pins. When enabled, multiplexors in the output path of the RA3 and RA4 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 13-3 shows the comparator output block diagram.

The TRISA bits will still function as an output enable/disable for the RA3 and RA4 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<5:4>).

- Note 1:** When reading the Port register, all pins configured as analog inputs will read as '0'. Pins configured as digital inputs will convert an analog input, according to the Schmitt Trigger input specification.
- 2:** Analog levels, on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265	266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284	285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322	323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341	342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360	361	362	363	364	365	366	367	368	369	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	388	389	390	391	392	393	394	395	396	397	398	399	400	401	402	403	404	405	406	407	408	409	410	411	412	413	414	415	416	417	418	419	420	421	422	423	424	425	426	427	428	429	430	431	432	433	434	435	436	437	438	439	440	441	442	443	444	445	446	447	448	449	450	451	452	453	454	455	456	457	458	459	460	461	462	463	464	465	466	467	468	469	470	471	472	473	474	475	476	477	478	479	480	481	482	483	484	485	486	487	488	489	490	491	492	493	494	495	496	497	498	499	500	501	502	503	504	505	506	507	508	509	510	511	512	513	514	515	516	517	518	519	520	521	522	523	52
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b) Clear flag bit CMIF.

13.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from Sleep mode when enabled. While the comparator is powered up, higher Sleep currents than shown in the power-down current specification will occur. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in Sleep mode, turn off the comparators, $CM<2:0> = 111$, before entering Sleep. If the device wakes up from Sleep, the contents of the CMCON register are not affected.

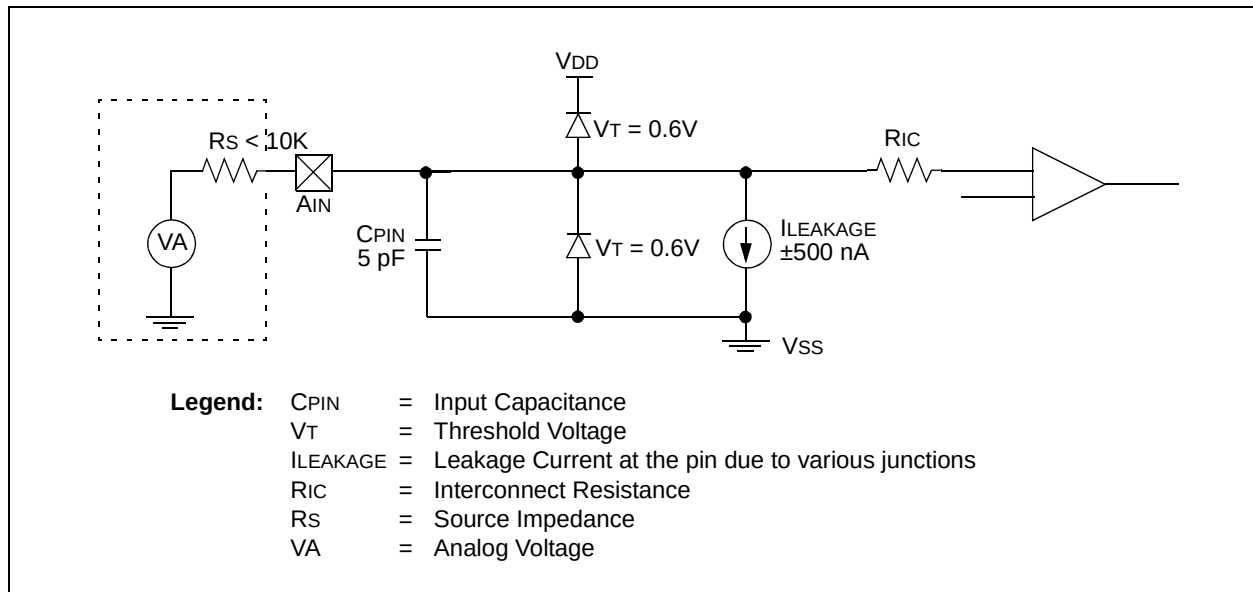
13.8 Effects of a Reset

A device Reset forces the CMCON register to its Reset state, causing the comparator module to be in the Comparator Off mode, $CM<2:0> = 111$.

13.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 13-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to V_{DD} and V_{SS} . The analog input, therefore, must be between V_{SS} and V_{DD} . If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up condition may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 13-4: ANALOG INPUT MODEL



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TABLE 13-1: REGISTERS ASSOCIATED WITH THE COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
0Bh, 8Bh, 10Bh, 18Bh	INTCON	GIE	PEIE	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 000x	0000 000u
0Dh	PIR2	OSFIF	CMIF	—	EEIF	—	—	—	—	00-0 ----	00-0 ----
8Dh	PIE2	OSFIE	CMIE	—	EEIE	—	—	—	—	00-0 ----	00-0 ----
05h	PORTA (PIC16F87) (PIC16F88)	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	xxxx 0000 xxx0 0000	uuuu 0000 uuu0 0000
85h	TRISA	TRISA7	TRISA6	TRISA5 ⁽¹⁾	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the comparator module.

Note 1: Pin 5 is an input only; the state of the TRISA5 bit has no effect and will always read '1'.

14.0 COMPARATOR VOLTAGE REFERENCE MODULE

The comparator voltage reference generator is a 16-tap resistor ladder network that provides a fixed voltage reference when the comparators are in mode '010'. A programmable register controls the function of the reference generator. Register 14-1 lists the bit functions of the CVRCON register.

As shown in Figure 14-1, the resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The comparator reference

supply voltage (also referred to as CVRSRC) comes directly from VDD. It should be noted, however, that the voltage at the top of the ladder is $CVRSRC - VSAT$, where VSAT is the saturation voltage of the power switch transistor. This reference will only be as accurate as the values of CVRSRC and VSAT.

The output of the reference generator may be connected to the RA2/AN2/CVREF/VREF- pin (VREF- is available on the PIC16F88 device only). This can be used as a simple D/A function by the user if a very high-impedance load is used. The primary purpose of this function is to provide a test path for testing the reference generator function.

REGISTER 14-1: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS 9Dh)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0

bit 7

bit 0

- bit 7 **CVREN:** Comparator Voltage Reference Enable bit
 1 = CVREF circuit powered on
 0 = CVREF circuit powered down
- bit 6 **CVROE:** Comparator VREF Output Enable bit
 1 = CVREF voltage level is output on the RA2/AN2/CVREF/VREF- pin⁽¹⁾
 0 = CVREF voltage level is disconnected from the RA2/AN2/CVREF/VREF- pin⁽¹⁾
- bit 5 **CVRR:** Comparator VREF Range Selection bit⁽¹⁾
 1 = 0.00 CVRSRC to 0.625 CVRSRC with CVRSRC/24 step size
 0 = 0.25 CVRSRC to 0.72 CVRSRC with CVRSRC/32 step size
- bit 4 **Unimplemented:** Read as '0'
- bit 3-0 **CVR<3:0>:** Comparator VREF Value Selection $0 \leq VR3:VR0 \leq 15$ bits⁽¹⁾
When CVRR = 1:
 $CVREF = (VR<3:0>/24) \cdot (CVRSRC)$
When CVRR = 0:
 $CVREF = 1/4 \cdot (CVRSRC) + (VR3:VR0/32) \cdot (CVRSRC)$
- Note 1:** VREF is available on the PIC16F88 device only.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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FIGURE 14-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

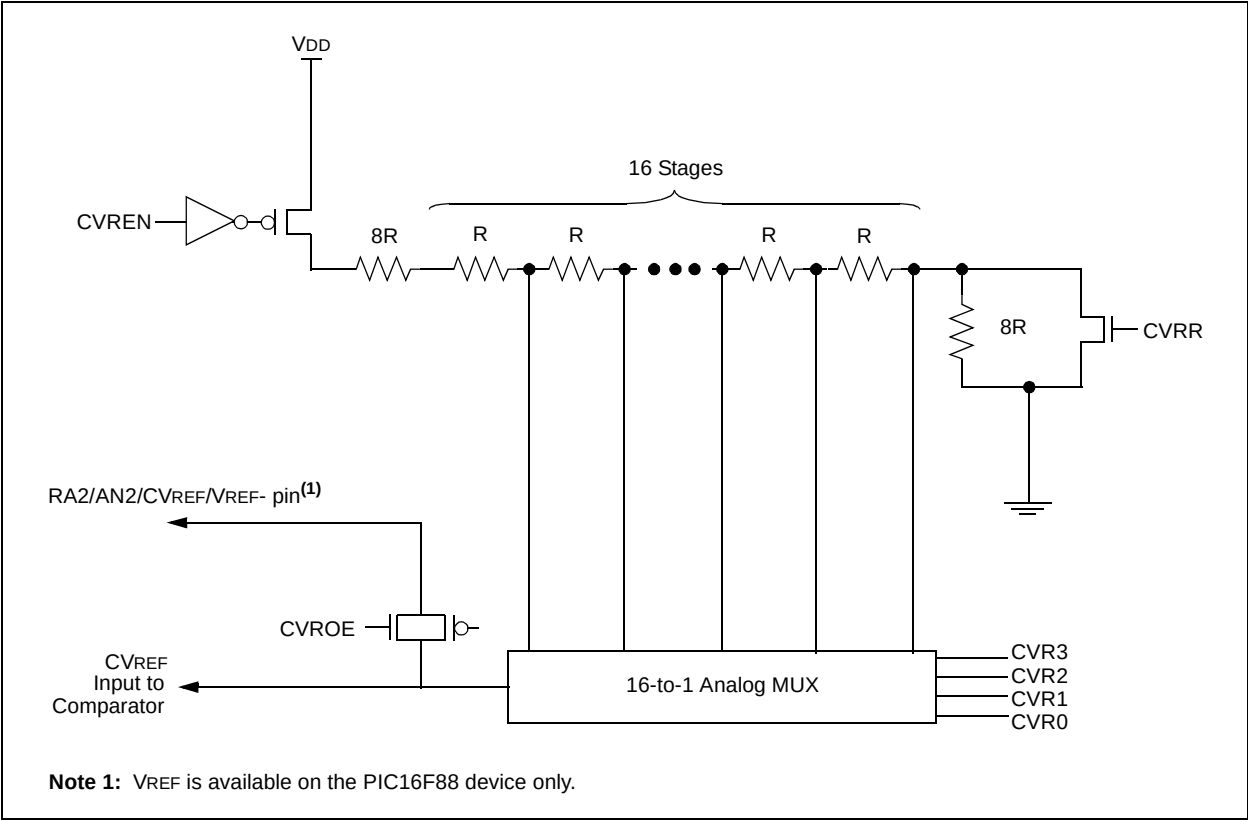


TABLE 14-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other Resets
9Dh	CVRCON	CVREN	CVROE	CVRR	—	CVR3	CVR2	CVR1	CVR0	000- 0000	000- 0000
9Ch	CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0111	0000 0111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used with the comparator voltage reference.

15.0 SPECIAL FEATURES OF THE CPU

These devices have a host of features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection:

- Reset
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- Two-Speed Start-up
- Fail-Safe Clock Monitor
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™ (ICSP™)

There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in Reset until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only. It is designed to keep the part in Reset while the power supply stabilizes and is enabled or disabled using a configuration bit. With these two timers on-chip, most applications need no external Reset circuitry.

Sleep mode is designed to offer a very low-current Power-down mode. The user can wake-up from Sleep through external Reset, Watchdog Timer wake-up or through an interrupt.

Additional information on special features is available in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

15.1 Configuration Bits

The configuration bits can be programmed (read as ‘0’), or left unprogrammed (read as ‘1’), to select various device configurations. These bits are mapped in program memory locations 2007h and 2008h.

The user will note that address 2007h is beyond the user program memory space which can be accessed only during programming.

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REGISTER 15-1: CONFIG1: CONFIGURATION WORD 1 REGISTER (ADDRESS 2007h)

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP	CCPMX	DEBUG	WRT1	WRT0	CPD	LVP	BOREN	MCLR	FOSC2	PWRTEN	WDTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13 **CP:** Flash Program Memory Code Protection bits

1 = Code protection off

0 = 0000h to 0FFFh code-protected (all protected)

bit 12 **CCPMX:** CCP1 Pin Selection bit

1 = CCP1 function on RB0

0 = CCP1 function on RB3

bit 11 **DEBUG:** In-Circuit Debugger Mode bit

1 = In-Circuit Debugger disabled, RB6 and RB7 are general purpose I/O pins

0 = In-Circuit Debugger enabled, RB6 and RB7 are dedicated to the debugger

bit 10-9 **WRT<1:0>:** Flash Program Memory Write Enable bits

11 = Write protection off

10 = 0000h to 00FFh write-protected, 0100h to 0FFFh may be modified by EECON control

01 = 0000h to 07FFh write-protected, 0800h to 0FFFh may be modified by EECON control

00 = 0000h to 0FFFh write-protected

bit 8 **CPD:** Data EE Memory Code Protection bit

1 = Code protection off

0 = Data EE memory code-protected

bit 7 **LVP:** Low-Voltage Programming Enable bit

1 = RB3/PGM pin has PGM function, Low-Voltage Programming enabled

0 = RB3 is digital I/O, HV on MCLR must be used for programming

bit 6 **BOREN:** Brown-out Reset Enable bit

1 = BOR enabled

0 = BOR disabled

bit 5 **MCLR:** RA5/MCLR/VPP Pin Function Select bit

1 = RA5/MCLR/VPP pin function is MCLR

0 = RA5/MCLR/VPP pin function is digital I/O, MCLR internally tied to VDD

bit 3 **PWRTEN:** Power-up Timer Enable bit

1 = PWRT disabled

0 = PWRT enabled

bit 2 **WDTEN:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 4, 1-0 **FOSC<2:0>:** Oscillator Selection bits

111 = EXTRC oscillator; CLKO function on RA6/OSC2/CLKO

110 = EXTRC oscillator; port I/O function on RA6/OSC2/CLKO

101 = INTRC oscillator; CLKO function on RA6/OSC2/CLKO pin and port I/O function on RA7/OSC1/CLKI pin

100 = INTRC oscillator; port I/O function on both RA6/OSC2/CLKO pin and RA7/OSC1/CLKI pin

011 = ECIO; port I/O function on RA6/OSC2/CLKO

010 = HS oscillator

001 = XT oscillator

000 = LP oscillator

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 15-2: CONFIG2: CONFIGURATION WORD 2 REGISTER (ADDRESS 2008h)

U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	—	IESO	FCMEN

bit 13

bit 0

bit 13-2 **Unimplemented:** Read as '1'

bit 1 **IESO:** Internal External Switchover bit

- 1 = Internal External Switchover mode enabled
- 0 = Internal External Switchover mode disabled

bit 0 **FCMEN:** Fail-Safe Clock Monitor Enable bit

- 1 = Fail-Safe Clock Monitor enabled
- 0 = Fail-Safe Clock Monitor disabled

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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15.2 Reset

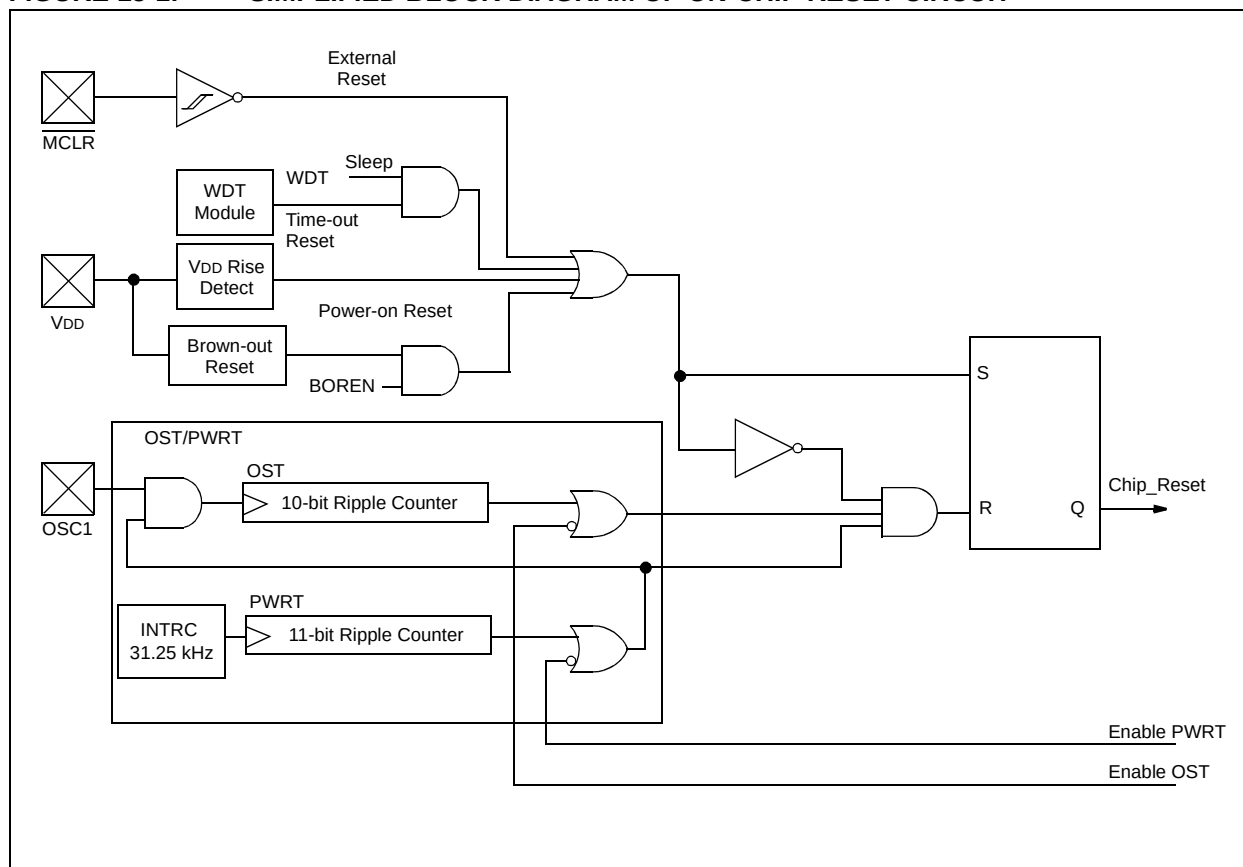
The PIC16F87/88 differentiates between various kinds of Reset:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Reset during normal operation
- WDT wake-up during Sleep
- Brown-out Reset (BOR)

Some registers are not affected in any Reset condition. Their status is unknown on POR and unchanged in any other Reset. Most other registers are reset to a "Reset state" on Power-on Reset (POR), on the $\overline{\text{MCLR}}$ and WDT Reset, on $\overline{\text{MCLR}}$ Reset during Sleep and Brown-out Reset (BOR). They are not affected by a WDT wake-up which is viewed as the resumption of normal operation. The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different Reset situations, as indicated in Table 15-3. These bits are used in software to determine the nature of the Reset. Upon a POR, BOR or wake-up from Sleep, the CPU requires approximately 5-10 μs to become ready for code execution. This delay runs in parallel with any other timers. See Table 15-4 for a full description of Reset states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 15-1.

FIGURE 15-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



15.3 MCLR

PIC16F87/88 devices have a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

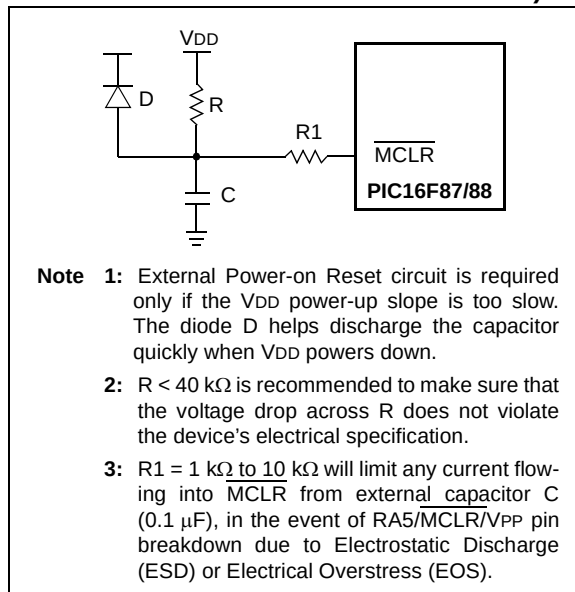
It should be noted that a WDT Reset does not drive $\overline{\text{MCLR}}$ pin low.

The behavior of the ESD protection on the $\overline{\text{MCLR}}$ pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both $\overline{\text{MCLR}}$ and excessive current beyond the device specification during the ESD event. The circuit, as shown in Figure 15-2, is suggested.

Note: For this reason, Microchip recommends that the $\overline{\text{MCLR}}$ pin no longer be tied directly to V_{DD} .

The RA5/ $\overline{\text{MCLR}}$ / V_{PP} pin can be configured for $\overline{\text{MCLR}}$ (default), or as an I/O pin (RA5). This is configured through the MCLRE bit in Configuration Word 1.

FIGURE 15-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW V_{DD} POWER-UP)



15.4 Power-on Reset (POR)

A Power-on Reset pulse is generated on-chip when V_{DD} rise is detected (in the range of 1.2V-1.7V). To take advantage of the POR, tie the $\overline{\text{MCLR}}$ pin to V_{DD} , as described in **Section 15.3 "MCLR"**. A maximum rise time for V_{DD} is specified. See **Section 18.0 "Electrical Characteristics"** for details.

When the device starts normal operation (exits the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. For more information, see Application Note, AN607 "Power-up Trouble Shooting" (DS00607).

15.5 Power-up Timer (PWRT)

The Power-up Timer (PWRT) of the PIC16F87/88 is a counter that uses the INTRC oscillator as the clock input. This yields a count of 72 ms. While the PWRT is counting, the device is held in Reset.

The power-up time delay depends on the INTRC and will vary from chip-to-chip due to temperature and process variation. See DC parameter #33 for details.

The PWRT is enabled by clearing configuration bit PWRTE.

15.6 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (if enabled). This helps to ensure that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from Sleep.

15.7 Brown-out Reset (BOR)

The configuration bit, BOREN, can enable or disable the Brown-out Reset circuit. If V_{DD} falls below V_{BOR} (parameter D005, about 4V) for longer than T_{BOR} (parameter #35, about 100 μs), the brown-out situation will reset the device. If V_{DD} falls below V_{BOR} for less than T_{BOR} , a Reset may not occur.

Once the brown-out occurs, the device will remain in Brown-out Reset until V_{DD} rises above V_{BOR} . The Power-up Timer (if enabled) will keep the device in Reset for T_{PWRT} (parameter #33, about 72 ms). If V_{DD} should fall below V_{BOR} during T_{PWRT} , the Brown-out Reset process will restart when V_{DD} rises above V_{BOR} with the Power-up Timer Reset. Unlike previous PIC16 devices, the PWRT is no longer automatically enabled when the Brown-out Reset circuit is enabled. The PWRTE and BOREN configuration bits are independent of each other.

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15.8 Time-out Sequence

On power-up, the time-out sequence is as follows: the PWRT delay starts (if enabled) when a POR occurs. Then, OST starts counting 1024 oscillator cycles when PWRT ends (LP, XT, HS). When the OST ends, the device comes out of Reset.

If $\overline{\text{MCLR}}$ is kept low long enough, all delays will expire. Bringing $\overline{\text{MCLR}}$ high will begin execution immediately. This is useful for testing purposes, or to synchronize more than one PIC16F87/88 device operating in parallel.

Table 15-3 shows the Reset conditions for the STATUS, PCON and PC registers, while Table 15-4 shows the Reset conditions for all the registers.

15.9 Power Control/Status Register (PCON)

The Power Control/Status Register, PCON, has two bits to indicate the type of Reset that last occurred.

Bit 0 is Brown-out Reset Status bit, $\overline{\text{BOR}}$. Bit $\overline{\text{BOR}}$ is unknown on a Power-on Reset. It must then be set by the user and checked on subsequent Resets to see if bit $\overline{\text{BOR}}$ cleared, indicating a Brown-out Reset occurred. When the Brown-out Reset is disabled, the state of the $\overline{\text{BOR}}$ bit is unpredictable.

Bit 1 is POR (Power-on Reset Status bit). It is cleared on a Power-on Reset and unaffected otherwise. The user must set this bit following a Power-on Reset.

TABLE 15-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Reset		Wake-up from Sleep
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
XT, HS, LP	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$\text{TPWRT} + 1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$	$1024 \cdot \text{TOSC}$
EXTRC, INTRC	TPWRT	$5\text{-}10 \mu\text{s}^{(1)}$	TPWRT	$5\text{-}10 \mu\text{s}^{(1)}$	$5\text{-}10 \mu\text{s}^{(1)}$
T1OSC	—	—	—	—	$5\text{-}10 \mu\text{s}^{(1)}$

Note 1: CPU start-up is always invoked on POR, BOR and wake-up from Sleep. The 5-10 μs delay is based on a 1 MHz system clock.

TABLE 15-2: STATUS BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOR}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	
0	x	1	1	Power-on Reset
0	x	0	x	Illegal, $\overline{\text{TO}}$ is set on $\overline{\text{POR}}$
0	x	x	0	Illegal, $\overline{\text{PD}}$ is set on $\overline{\text{POR}}$
1	0	1	1	Brown-out Reset
1	1	0	1	WDT Reset
1	1	0	0	WDT Wake-up
1	1	u	u	$\overline{\text{MCLR}}$ Reset during Normal Operation
1	1	1	0	$\overline{\text{MCLR}}$ Reset during Sleep or Interrupt Wake-up from Sleep

Legend: u = unchanged, x = unknown

TABLE 15-3: RESET CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	000h	000u uuuu	---- --uu
MCLR Reset during Sleep	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 1uuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Reset	000h	0001 1uuu	---- --u0
Interrupt Wake-up from Sleep	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

TABLE 15-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Power-on Reset, Brown-out Reset	MCLR Reset, WDT Reset	Wake-up via WDT or Interrupt
W	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	N/A	N/A	N/A
TMR0	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	0000h	0000h	PC + 1 ⁽²⁾
STATUS	0001 1xxx	000q quuu ⁽³⁾	uuuq quuu ⁽³⁾
FSR	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA (PIC16F87)	xxxx 0000	uuuu 0000	uuuu uuuu
PORTA (PIC16F88)	xxx0 0000	uuu0 0000	uuuu uuuu
PORTB (PIC16F87)	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB (PIC16F87)	00xx xxxx	00uu uuuu	uuuu uuuu
PCLATH	---0 0000	---0 0000	---u uuuu
INTCON	0000 000x	0000 000u	uuuu uuuu ⁽¹⁾
PIR1	-000 0000	-000 0000	-uuu uuuu ⁽¹⁾
PIR2	00-0 ----	00-0 ----	uu-u ---- ⁽¹⁾
TMR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	-000 0000	-uuu uuuu	-uuu uuuu
TMR2	0000 0000	0000 0000	uuuu uuuu
T2CON	-000 0000	-000 0000	-uuu uuuu
SSPBUF	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPCON	0000 0000	0000 0000	uuuu uuuu
CCPR1L	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1H	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	--00 0000	--00 0000	--uu uuuu
RCSTA	0000 000x	0000 000x	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and PR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 15-3 for Reset value for specific condition.

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TABLE 15-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Power-on Reset, Brown-out Reset	MCLR Reset, WDT Reset	Wake-up via WDT or Interrupt
TXREG	0000 0000	0000 0000	uuuu uuuu
RCREG	0000 0000	0000 0000	uuuu uuuu
ADRESH	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	0000 00-0	0000 00-0	uuuu uu-u
OPTION_REG	1111 1111	1111 1111	uuuu uuuu
TRISA	1111 1111	1111 1111	uuuu uuuu
TRISB	1111 1111	1111 1111	uuuu uuuu
PIE1	-000 0000	-000 0000	-uuu uuuu
PIE2	00-0 ----	00-0 ----	uu-u ----
PCON	---- --0q	---- --uu	---- --uu
OSCCON	-000 0000	-000 0000	-uuu uuuu
OSCTUNE	--00 0000	--00 0000	--uu uuuu
PR2	1111 1111	1111 1111	1111 1111
SSPADD	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	0000 0000	0000 0000	uuuu uuuu
TXSTA	0000 -010	0000 -010	uuuu -u1u
SPBRG	0000 0000	0000 0000	uuuu uuuu
ANSEL	-111 1111	-111 1111	-111 1111
CMCON	0000 0111	0000 0111	uuuu u111
CVRCON	000- 0000	000- 0000	uuu- uuuu
WDTCON	---0 1000	---0 1000	---u uuuu
ADRESL	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON1	0000 ----	0000 ----	uuuu ----
EEDATA	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEADR	xxxx xxxx	uuuu uuuu	uuuu uuuu
EEDATH	--xx xxxx	--uu uuuu	--uu uuuu
EEADRH	---- -xxx	---- -uuu	---- -uuu
EECON1	x--x x000	u--x u000	u--u uuuu
EECON2	---- ----	---- ----	---- ----

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition

Note 1: One or more bits in INTCON, PIR1 and PR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).

3: See Table 15-3 for Reset value for specific condition.

FIGURE 15-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} THROUGH PULL-UP RESISTOR)

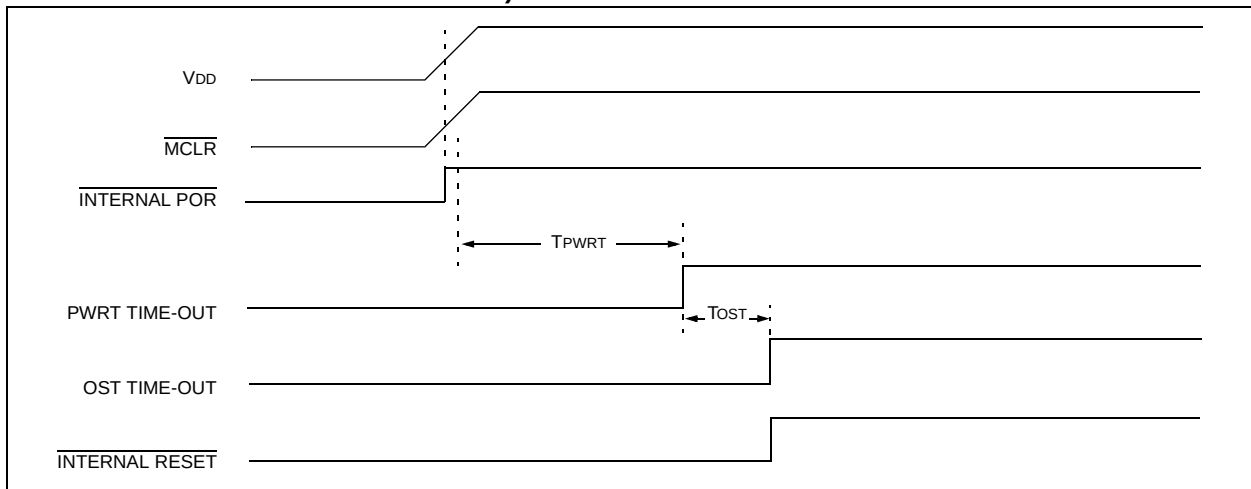


FIGURE 15-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} THROUGH RC NETWORK): CASE 1

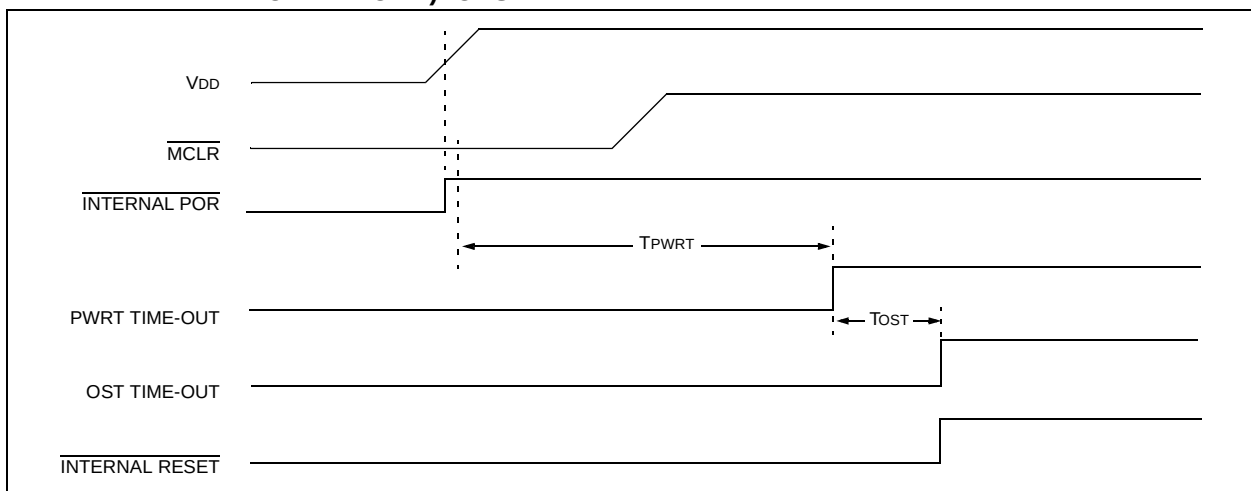
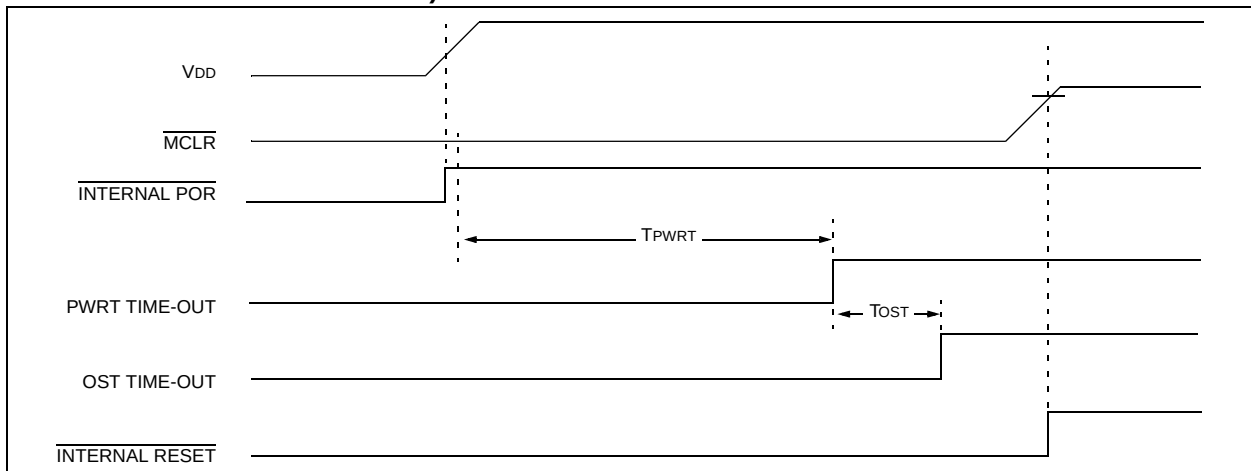
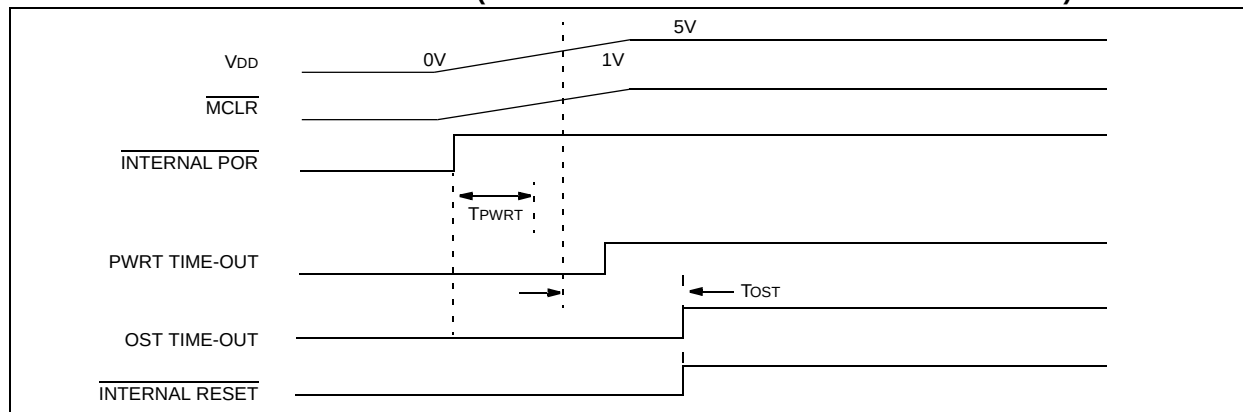


FIGURE 15-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD} THROUGH RC NETWORK): CASE 2



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FIGURE 15-6: SLOW RISE TIME (MCLR TIED TO V_{DD} THROUGH RC NETWORK)



15.10 Interrupts

The PIC16F87/88 has up to 12 sources of interrupt. The Interrupt Control register (INTCON) records individual interrupt requests in flag bits. It also has individual and global interrupt enable bits.

Note: Individual interrupt flag bits are set regardless of the status of their corresponding mask bit or the GIE bit.

A global interrupt enable bit, GIE (INTCON<7>), enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. When bit GIE is enabled and an interrupt's flag bit and mask bit are set, the interrupt will vector immediately. Individual interrupts can be disabled through their corresponding enable bits in various registers. Individual interrupt bits are set regardless of the status of the GIE bit. The GIE bit is cleared on Reset.

The "return from interrupt" instruction, RETFIE, exits the interrupt routine, as well as sets the GIE bit which re-enables interrupts.

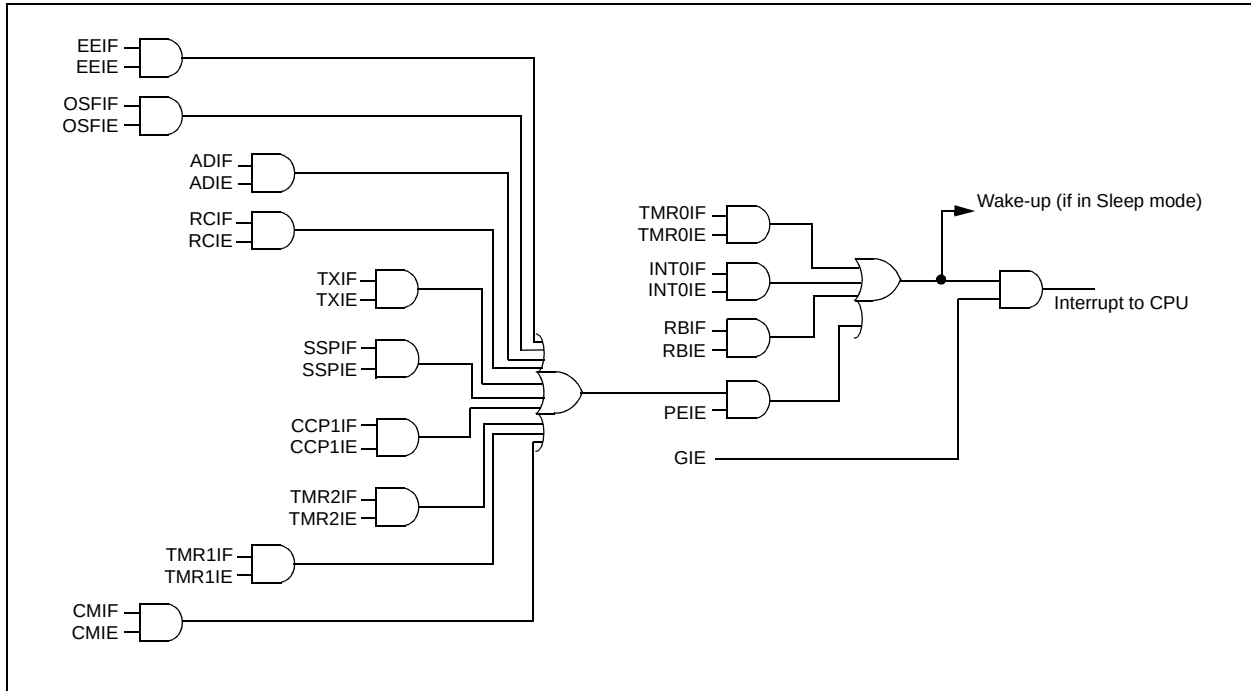
The RB0/INT pin interrupt, the RB port change interrupt and the TMR0 overflow interrupt flags are contained in the INTCON register.

The peripheral interrupt flags are contained in the Special Function Register, PIR1. The corresponding interrupt enable bits are contained in Special Function Register, PIE1 and the peripheral interrupt enable bit is contained in Special Function Register, INTCON.

When an interrupt is serviced, the GIE bit is cleared to disable any further interrupt, the return address is pushed onto the stack and the PC is loaded with 0004h. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

For external interrupt events, such as the INT pin or PORTB change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends on when the interrupt event occurs, relative to the current Q cycle. The latency is the same for one or two cycle instructions. Individual interrupt flag bits are set regardless of the status of their corresponding mask bit, PEIE bit or the GIE bit.

FIGURE 15-7: INTERRUPT LOGIC



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15.10.1 INT INTERRUPT

External interrupt on the RB0/INT pin is edge-triggered, either rising if bit INTEDG (OPTION_REG<6>) is set, or falling if the INTEDG bit is clear. When a valid edge appears on the RB0/INT pin, flag bit, INT0IF (INTCON<1>), is set. This interrupt can be disabled by clearing enable bit INT0IE (INTCON<4>). Flag bit INT0IF must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The INT interrupt can wake-up the processor from Sleep, if bit INT0IE was set prior to going into Sleep. The status of global interrupt enable bit GIE decides whether or not the processor branches to the interrupt vector, following wake-up. See **Section 15.13 “Power-Down Mode (Sleep)”** for details on Sleep mode.

15.10.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set flag bit TMR0IF (INTCON<2>). The interrupt can be enabled/disabled by setting/clearing enable bit TMR0IE (INTCON<5>), see **Section 6.0 “Timer0 Module”**.

15.10.3 PORTB INTCON CHANGE

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit RBIE (INTCON<4>), see **Section 3.2 “EECON1 and EECN2 Registers”**.

15.11 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt (i.e., W, STATUS registers).

Since the upper 16 bytes of each bank are common in the PIC16F87/88 devices, temporary holding registers W_TEMP, STATUS_TEMP and PCLATH_TEMP should be placed in here. These 16 locations don't require banking and therefore, make it easier for context save and restore. The same code shown in Example 15-1 can be used.

EXAMPLE 15-1: SAVING STATUS, W AND PCLATH REGISTERS IN RAM

```
MOVWF    W_TEMP          ;Copy W to TEMP register
SWAPF    STATUS, W       ;Swap status to be saved into W
CLRF     STATUS          ;bank 0, regardless of current bank, Clears IRP,RP1,RP0
MOVWF    STATUS_TEMP     ;Save status to bank zero STATUS_TEMP register
MOVF     PCLATH, W        ;Only required if using page 1
MOVWF    PCLATH_TEMP     ;Save PCLATH into W
CLRF     PCLATH           ;Page zero, regardless of current page
:
: (ISR)                   ; (Insert user code here)
:
MOVF     PCLATH_TEMP, W   ;Restore PCLATH
MOVWF    PCLATH           ;Move W into PCLATH
SWAPF    STATUS_TEMP, W  ;Swap STATUS_TEMP register into W
                        ; (sets bank to original state)
MOVWF    STATUS          ;Move W into STATUS register
SWAPF    W_TEMP, F       ;Swap W_TEMP
SWAPF    W_TEMP, W       ;Swap W_TEMP into W
```

15.12 Watchdog Timer (WDT)

For PIC16F87/88 devices, the WDT has been modified from previous PIC16 devices. The new WDT is code and functionally backward compatible with previous PIC16 WDT modules and allows the user to have a scaler value for the WDT and TMR0 at the same time. In addition, the WDT time-out value can be extended to 268 seconds, using the prescaler with the postscaler when PSA is set to '1'.

15.12.1 WDT OSCILLATOR

The WDT derives its time base from the 31.25 kHz INTRC. The value of WDTCON is '---0 1000' on all Resets. This gives a nominal time base of 16.38 ms, which is compatible with the time base generated with previous PIC16 microcontroller versions.

Note: When the OST is invoked, the WDT is held in Reset because the WDT ripple counter is used by the OST to perform the oscillator delay count. When the OST count has expired, the WDT will begin counting (if enabled).

A new prescaler has been added to the path between the internal RC and the multiplexors used to select the path for the WDT. This prescaler is 16 bits and can be programmed to divide the internal RC by 32 to 65536, giving the time base used for the WDT a nominal range of 1 ms to 2.097s.

15.12.2 WDT CONTROL

The WDTEN bit is located in Configuration Word 1 and when this bit is set, the WDT runs continuously.

The SWDTEN bit is in the WDTCON register. When the WDTEN bit in the Configuration Word 1 register is set, the SWDTEN bit has no effect. If WDTEN is clear, then the SWDTEN bit can be used to enable and disable the WDT. Setting the bit will enable it and clearing the bit will disable it.

The PSA and PS<2:0> bits (OPTION_REG register) have the same function as in previous versions of the PIC16 family of microcontrollers.

FIGURE 15-8: WATCHDOG TIMER BLOCK DIAGRAM

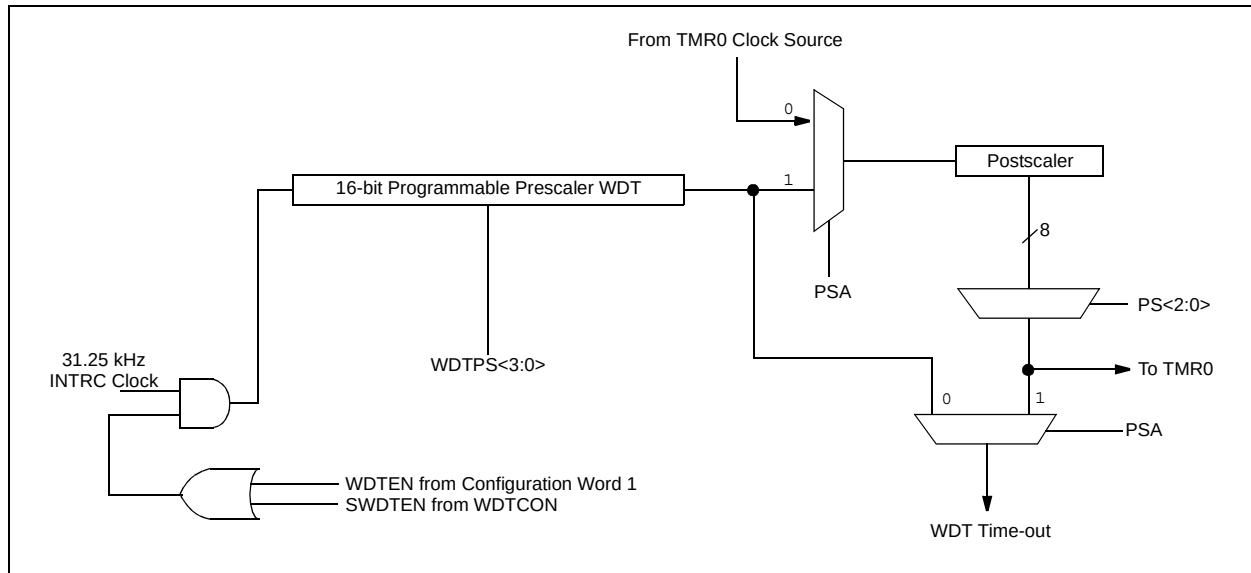


TABLE 15-5: PRESCALER/POSTSCALER BIT STATUS

Conditions	Prescaler	Postscaler (PSA = 1)
WDTEN = 0	Cleared	Cleared
CLRWDT command		
Oscillator fail detected		
Exit Sleep + System Clock = T1OSC, EXTRC, INTRC, ECIO		
Exit Sleep + System Clock = XT, HS, LP	Cleared at end of OST	Cleared at end of OST

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REGISTER 15-3: WDTCON: WATCHDOG CONTROL REGISTER (ADDRESS 105h)

U-0	U-0	U-0	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0
—	—	—	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN ⁽¹⁾
bit 7			bit 0				

bit 7-5 **Unimplemented:** Read as '0'

bit 4-1 **WDTPS<3:0>:** Watchdog Timer Period Select bits

Bit Value	Prescale Rate
0000	= 1:32
0001	= 1:64
0010	= 1:128
0011	= 1:256
0100	= 1:512
0101	= 1:1024
0110	= 1:2048
0111	= 1:4096
1000	= 1:8192
1001	= 1:16394
1010	= 1:32768
1011	= 1:65536

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit⁽¹⁾

1 = WDT is turned on

0 = WDT is turned off

Note 1: If WDTE configuration bit = 1, then WDT is always enabled, irrespective of this control bit. If WDTE configuration bit = 0, then it is possible to turn WDT on/off with this control bit.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

TABLE 15-6: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
81h,181h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
2007h	Configuration bits	LVP	BOREN	MCLRE	FOSC2	$\overline{\text{PWRTE}}\text{N}$	WDTEN	FOSC1	FOSC0
105h	WDTCON	—	—	—	WDTPS3	$\overline{\text{WDTPS}}\text{2}$	WDTPS1	WDTPS0	SWDTEN

Legend: Shaded cells are not used by the Watchdog Timer.

Note 1: See Register 15-1 for operation of these bits.

15.12.3 TWO-SPEED CLOCK START-UP MODE

Two-Speed Start-up mode minimizes the latency between oscillator start-up and code execution that may be selected with the IESO (Internal/External Switchover) bit in Configuration Word 2. This mode is achieved by initially using the INTRC for code execution until the primary oscillator is stable.

If this mode is enabled and any of the following conditions exist, the system will begin execution with the INTRC oscillator. This results in almost immediate code execution with a minimum of delay.

- POR and after the Power-up Timer has expired (if $PWRTEN = 0$);
- or following a wake-up from Sleep;
- or a Reset when running from T1OSC or INTRC (after a Reset, $SCS<1:0>$ are always set to '00').

Note: Following any Reset, the IRCF bits are zeroed and the frequency selection is forced to 31.25 kHz. The user can modify the IRCF bits to select a higher internal oscillator frequency.

If the primary oscillator is configured to be anything other than XT, LP or HS, then Two-Speed Start-up mode is disabled because the primary oscillator will not require any time to become stable after POR, or an exit from Sleep.

If the IRCF bits of the OSCCON register are configured to a non-zero value prior to entering Sleep mode, the system clock frequency will come from the output of the INTOSC. The IOFS bit in the OSCCON register will be clear until the INTOSC is stable. This will allow the user to determine when the internal oscillator can be used for time critical applications.

Checking the state of the OSTS bit will confirm whether the primary clock configuration is engaged. If not, the OSTS bit will remain clear.

When the device is auto-configured in INTRC mode following a POR or wake-up from Sleep, the rules for entering other oscillator modes still apply, meaning the $SCS<1:0>$ bits in OSCCON can be modified before the OST time-out has occurred. This would allow the application to wake-up from Sleep, perform a few instructions using the INTRC as the clock source and go back to Sleep without waiting for the primary oscillator to become stable.

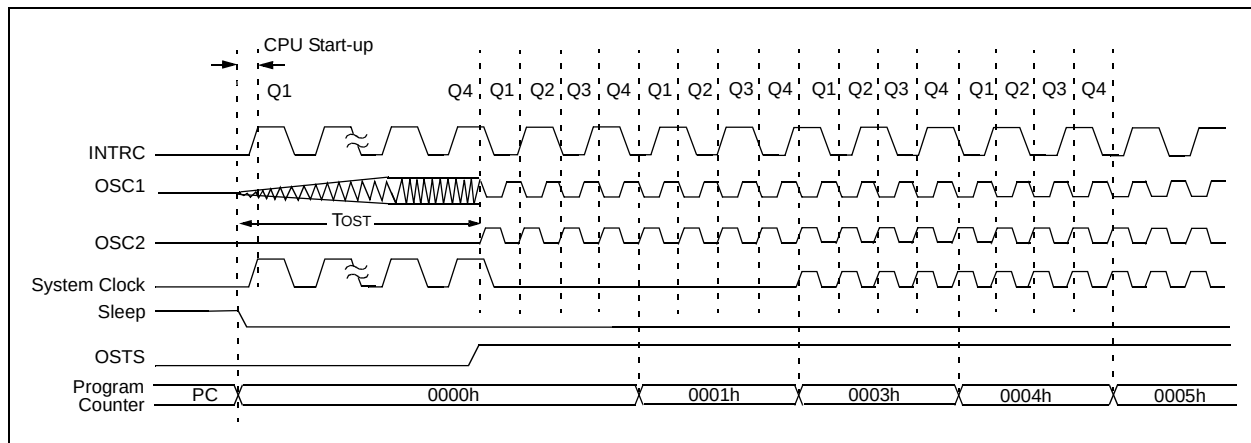
Note: Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit to remain clear.

15.12.3.1 Two-Speed Start-up Mode Sequence

1. Wake-up from Sleep, Reset or POR.
2. OSCCON bits configured to run from INTRC (31.25 kHz).
3. Instructions begin execution by INTRC (31.25 kHz).
4. OST enabled to count 1024 clock cycles.
5. OST timed out, wait for falling edge of INTRC.
6. OSTS is set.
7. System clock held low for eight falling edges of new clock (LP, XT or HS).
8. System clock is switched to primary source (LP, XT or HS).

The software may read the OSTS bit to determine when the switchover takes place so that any software timing edges can be adjusted.

FIGURE 15-9: TWO-SPEED START-UP MODE

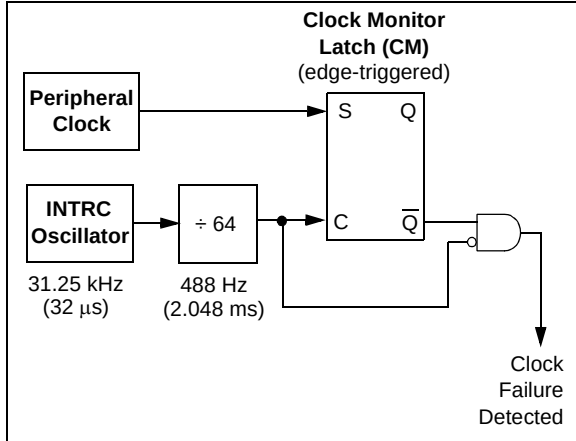


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15.12.4 FAIL-SAFE OPTION

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate even in the event of an oscillator failure.

FIGURE 15-10: FSCM BLOCK DIAGRAM



The FSCM function is enabled by setting the FCMEN bit in Configuration Word 2.

In the event of an oscillator failure, the FSCM will generate an oscillator fail interrupt and will switch the system clock over to the internal oscillator. The system will continue to come from the internal oscillator until the fail-safe condition is exited. The fail-safe condition is exited with either a Reset, the execution of a *SLEEP* instruction or a write to the OSCCON register.

The frequency of the internal oscillator will depend upon the value contained in the IRCF bits. Another clock source can be selected via the IRCF and the SCS bits of the OSCCON register.

The FSCM sample clock is generated by dividing the INTRC clock by 64. This will allow enough time between FSCM sample clocks for a system clock edge to occur.

On the rising edge of the postscaled clock, the monitoring latch (CM = 0) will be cleared. On a falling edge of the primary or secondary system clock, the monitoring latch will be set (CM = 1). In the event that a falling edge of the postscaled clock occurs and the monitoring latch is not set, a clock failure has been detected.

While in Fail-Safe mode, a Reset will exit the fail-safe condition. If the primary clock source is configured for a crystal, the OST timer will wait for the 1024 clock cycles for the OST time-out and the device will continue running from the internal oscillator until the OST is complete. A *SLEEP* instruction, or a write to the SCS bits (where SCS bits do not = 00), can be performed to put the device into a low-power mode.

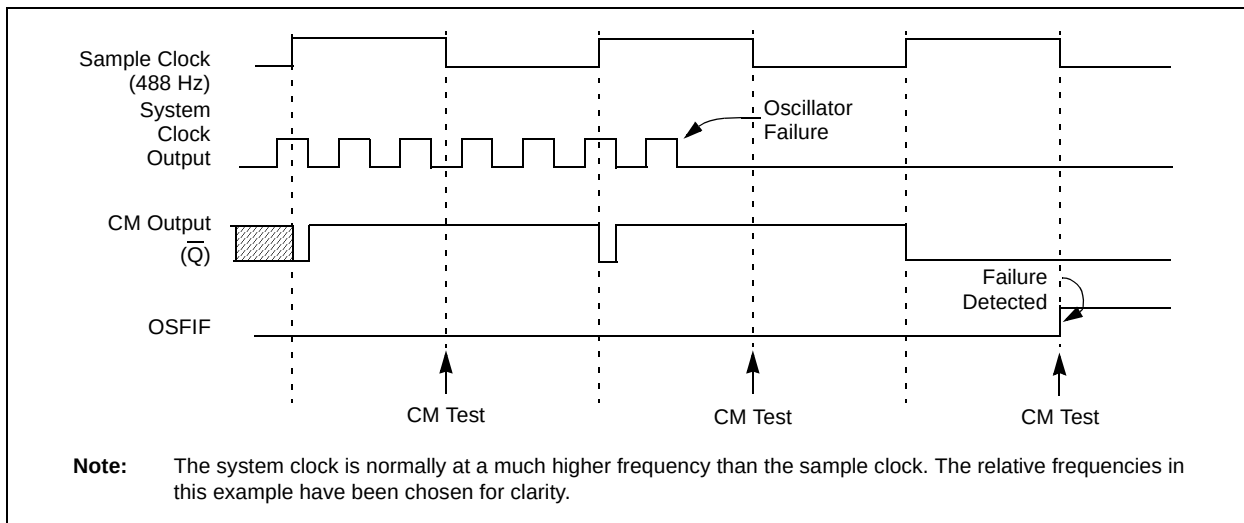
Note: Two-Speed Start-up mode is automatically enabled when the fail-safe option is enabled.

If Reset occurs while in Fail-Safe mode and the primary clock source is EC or RC, then the device will immediately switch back to EC or RC mode.

15.12.4.1 Fail-Safe in Low-Power Mode

A write to the OSCCON register, or *SLEEP* instruction, will end the fail-safe condition. The system clock will default to the source selected by the SCS bits, which is either T1OSC, INTRC or none (Sleep mode). However, the FSCM will continue to monitor the system clock. If the secondary clock fails, the device will immediately switch to the internal oscillator clock. If OSFIE is set, an interrupt will be generated.

FIGURE 15-11: FSCM TIMING DIAGRAM



15.12.4.2 FSCM and the Watchdog Timer

When a clock failure is detected, SCS<1:0> will be forced to '10' which will reset the WDT (if enabled).

15.12.4.3 POR or Wake From Sleep

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary system clock is EC, RC or INTRC modes, monitoring can begin immediately following these events.

For Oscillator modes involving a crystal or resonator (HS, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the system clock and functions until the primary clock is stable (the OST timer has timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on port or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

15.12.4.4 Example Fail-Safe Conditions

1. CONDITIONS:

The device is clocked from a crystal, crystal operation fails and then Sleep mode is entered.

OSTS = 0

SCS = 00

OSFIF = 1

USER ACTION:

Sleep mode will exit the fail-safe condition. Therefore, if the user code did not handle the detected fail-safe prior to the SLEEP command, then upon wake-up, the device will try to start the crystal that failed and a fail-safe condition will not be detected. Monitoring the OSTS bit will determine if the crystal is operating. The user should not enter Sleep mode without handling the fail-safe condition first.

2. CONDITIONS:

After a POR (Power-on Reset), the device is running in Two-Speed Start-up mode. The crystal fails before the OST has expired. If a crystal fails during the OST period, a fail-safe condition will not be detected (OSFIF will not get set).

OSTS = 0

SCS = 00

OSFIF = 0

USER ACTION:

Check the OSTS bit. If it's clear and the OST should have expired at this point, then the user can assume the crystal has failed. The user should change the SCS bit to cause a clock switch which will also release the 10-bit ripple counter for WDT operation (if enabled).

3. CONDITIONS:

The device is clocked from a crystal during normal operation and it fails.

OSTS = 0

SCS = 00

OSFIF = 1

USER ACTION:

Clear the OSFIF bit. Configure the SCS bits for a clock switch and the fail-safe condition will be cleared. Later, if the user decides to, the crystal can be retried for operation. If this is done, the OSTS bit should be monitored to determine if the crystal operates.

15.13 Power-Down Mode (Sleep)

Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ (STATUS<4>) bit is set and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, low or high-impedance).

For lowest current consumption in this mode, place all I/O pins at either VDD or VSS, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are high-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or VSS for lowest current consumption. The contribution from on-chip pull-ups on PORTB should also be considered.

The MCLR pin must be at a logic high level (VIHMC).

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15.14 In-Circuit Debugger

When the DEBUG bit in the Configuration Word is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® ICD. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 15-7 shows which features are consumed by the background debugger.

TABLE 15-7: DEBUGGER RESOURCES

I/O pins	RB6, RB7
Stack	1 level
Program Memory	Address 0000h must be NOP
	Last 100h words
Data Memory	0x070 (0x0F0, 0x170, 0x1F0) 0x1EB-0x1EF

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to RA5/MCLR/VPP, VDD, GND, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip, or one of the third party development tool companies.

15.15 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

15.16 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify. It is recommended that only the four Least Significant bits of the ID location are used.

15.17 In-Circuit Serial Programming

PIC16F87/88 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage (see Figure 15-13 for an example). This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

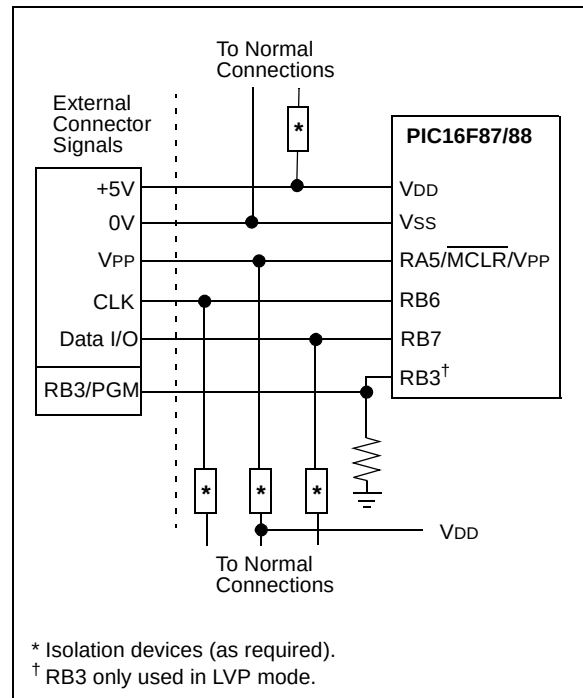
For more information on serial programming, please refer to the "PIC16F87/88 Flash Memory Programming Specification" (DS39607).

Note: The Timer1 oscillator shares the T1OSI and T1OSO pins with the PGD and PGC pins used for programming and debugging.

When using the Timer1 oscillator, In-Circuit Serial Programming™ (ICSP™) may not function correctly (high voltage or low voltage), or the In-Circuit Debugger (ICD) may not communicate with the controller. As a result of using either ICSP or ICD, the Timer1 crystal may be damaged.

If ICSP or ICD operations are required, the crystal should be disconnected from the circuit (disconnect either lead), or installed after programming. The oscillator loading capacitors may remain in-circuit during ICSP or ICD operation.

FIGURE 15-13: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



15.18 Low-Voltage ICSP Programming

The LVP bit of the Configuration Word enables Low-Voltage ICSP Programming. This mode allows the microcontroller to be programmed via ICSP using a VDD source in the operating voltage range. This only means that VPP does not have to be brought to VIH, but can instead be left at the normal operating voltage. In this mode, the RB3/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin.

If Low-Voltage Programming mode is not used, the LVP bit can be programmed to a '0' and RB3/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed when Programming mode is entered with VIH on MCLR. The LVP bit can only be changed when using high voltage on MCLR.

It should be noted that once the LVP bit is programmed to '0', only the High-Voltage Programming mode is available and only this mode can be used to program the device.

When using Low-Voltage ICSP, the part must be supplied at 4.5V to 5.5V if a bulk erase will be executed. This includes reprogramming of the code-protect bits from an ON state to an OFF state. For all other cases of Low-Voltage ICSP, the part may be programmed at the normal operating voltage. This means calibration values, unique user IDs or user code can be reprogrammed or added.

The following LVP steps assume the LVP bit is set in the Configuration register.

1. Apply VDD to the VDD pin.
2. Drive MCLR low.
3. Apply VDD to the RB3/PGM pin.
4. Apply VDD to the MCLR pin.
5. Follow with the associated programming steps.

Note 1: The High-Voltage Programming mode is always available, regardless of the state of the LVP bit, by applying VIH to the MCLR pin.

- 2: While in Low-Voltage ICSP mode (LVP = 1), the RB3 pin can no longer be used as a general purpose I/O pin.
- 3: When using Low-Voltage ICSP Programming (LVP) and the pull-ups on PORTB are enabled, bit 3 in the TRISB register must be cleared to disable the pull-up on RB3 and ensure the proper operation of the device.
- 4: RB3 should not be allowed to float if LVP is enabled. An external pull-down device should be used to default the device to normal operating mode. If RB3 floats high, the PIC16F87/88 devices will enter Programming mode.
- 5: LVP mode is enabled by default on all devices shipped from Microchip. It can be disabled by clearing the LVP bit in the CONFIG1 register.
- 6: Disabling LVP will provide maximum compatibility to other PIC16CXXX devices.

16.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories are presented in Figure 16-1, while the various opcode fields are summarized in Table 16-1.

Table 16-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the “PIC® Mid-Range MCU Family Reference Manual” (DS33023).

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the W register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator, which selects the bit affected by the operation, while ‘f’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an eight or eleven-bit constant or literal value

One instruction cycle consists of four oscillator periods. For an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μs. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note: To maintain upward compatibility with future PIC16F87/88 products, do not use the **OPTION** and **TRIS** instructions.

All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

16.1 Read-Modify-Write Operations

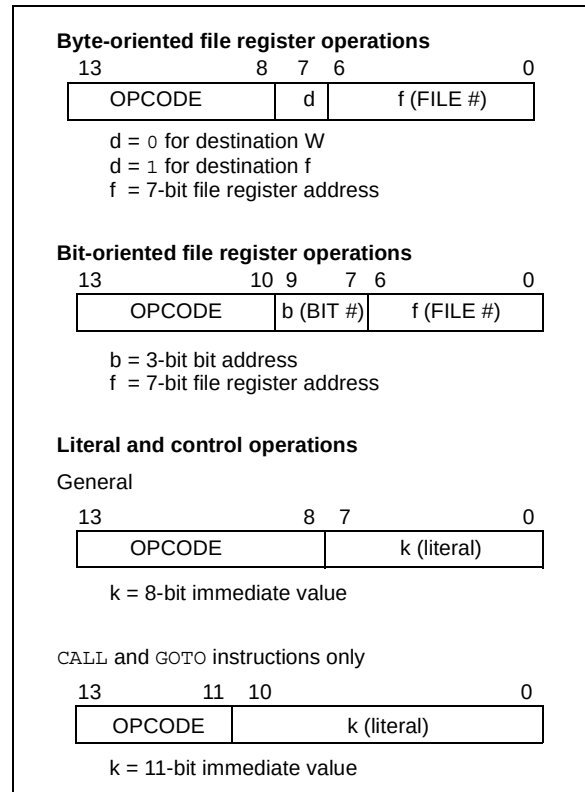
Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (RMW) operation. The register is read, the data is modified and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a “CLRF PORTB” instruction will read PORTB, clear all the data bits, then write the result back to PORTB. This example would have the unintended result that the condition that sets the RBIF flag would be cleared.

TABLE 16-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-Down bit

FIGURE 16-1: GENERAL FORMAT FOR INSTRUCTIONS



PIC16F87/88

TABLE 16-2: PIC16F87/88 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	1fff	ffff	Z	2
CLRWF	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	1fff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDI	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into Standby mode	1	00	0000	0110	0011	$\overline{TO}, \overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., `MOVF PORTB, 1`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a `NOP`.

Note: Additional information on the mid-range instruction set is available in the "PIC® Mid-Range MCU Family Reference Manual" (DS33023).

16.2 Instruction Descriptions

ADDLW **Add Literal and W**

Syntax: [*label*] ADDLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) + k \rightarrow (W)$

Status Affected: C, DC, Z

Description: The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

ANDWF **AND W with f**

Syntax: [*label*] ANDWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .AND. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: AND the W register with register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

ADDWF **Add W and f**

Syntax: [*label*] ADDWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) + (f) \rightarrow (\text{destination})$

Status Affected: C, DC, Z

Description: Add the contents of the W register with register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

BCF **Bit Clear f**

Syntax: [*label*] BCF *f,b*

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: $0 \rightarrow (f)$

Status Affected: None

Description: Bit 'b' in register 'f' is cleared.

ANDLW **AND Literal with W**

Syntax: [*label*] ANDLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) .AND. (k) \rightarrow (W)$

Status Affected: Z

Description: The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BSF **Bit Set f**

Syntax: [*label*] BSF *f,b*

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: $1 \rightarrow (f)$

Status Affected: None

Description: Bit 'b' in register 'f' is set.

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BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \leq f \leq 127$
 $0 \leq b < 7$

Operation: skip if (f) = 1

Status Affected: None

Description: If bit 'b' in register 'f' = 0, the next instruction is executed.
 If bit 'b' = 1, then the next instruction is discarded and a NOP is executed instead, making this a 2 Tcy instruction.

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: $0 \leq f \leq 127$

Operation: 00h $\rightarrow$ (f),
 1 $\rightarrow$ Z

Status Affected: Z

Description: The contents of register 'f' are cleared and the Z bit is set.

BTFSC **Bit Test, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: $0 \leq f \leq 127$
 $0 \leq b \leq 7$

Operation: skip if (f) = 0

Status Affected: None

Description: If bit 'b' in register 'f' = 1, the next instruction is executed.
 If bit 'b', in register 'f', = 0, the next instruction is discarded and a NOP is executed instead, making this a 2 Tcy instruction.

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h $\rightarrow$ (W),
 1 $\rightarrow$ Z

Status Affected: Z

Description: W register is cleared. Zero bit (Z) is set.

CALL **Call Subroutine**

Syntax: [*label*] CALL k

Operands: $0 \leq k \leq 2047$

Operation: (PC) + 1 $\rightarrow$ TOS,
 k $\rightarrow$ PC<10:0>,
 (PCLATH<4:3>) $\rightarrow$ PC<12:11>

Status Affected: None

Description: Call subroutine. First, return address (PC + 1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.

CLRWD T **Clear Watchdog Timer**

Syntax: [*label*] CLRWD T

Operands: None

Operation: 00h $\rightarrow$ WDT,
 0 $\rightarrow$ WDT prescaler,
 1 $\rightarrow$ $\overline{\text{TO}}$,
 1 $\rightarrow$ $\overline{\text{PD}}$

Status Affected: $\overline{\text{TO}}$, $\overline{\text{PD}}$

Description: CLRWD T instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.

COMF	Complement f
Syntax:	[<i>label</i>] COMF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are complemented. If 'd' = 0, the result is stored in W. If 'd' = 1, the result is stored back in register 'f'.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow PC<10:0>$, $PCLATH<4:3> \rightarrow PC<12:11>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

DECf	Decrement f
Syntax:	[<i>label</i>] DECf f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Decrement register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$; skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', then a NOP is executed instead, making it a 2 Tcy instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'. If the result is '1', the next instruction is executed. If the result is '0', a NOP is executed instead, making it a 2 Tcy instruction.

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IORLW	Inclusive OR Literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	(W) .OR. k $\rightarrow$ (W)
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

MOVLW	Move Literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	k $\rightarrow$ (W)
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as '0's.

IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(W) .OR. (f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'.

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	(W) $\rightarrow$ (f)
Status Affected:	None
Description:	Move data from W register to register 'f'.

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	(f) $\rightarrow$ (destination)
Status Affected:	Z
Description:	The contents of register 'f' are moved to a destination dependant upon the status of 'd'. If 'd' = 0, the destination is W register. If 'd' = 1, the destination is file register 'f' itself. 'd' = 1 is useful to test a file register, since status flag Z is affected.

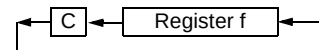
NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE Return from Interrupt

Syntax: `[label] RETFIE`
 Operands: None
 Operation: TOS → PC,
 1 → GIE
 Status Affected: None

RLF Rotate Left f through Carry

Syntax: `[label] RLF f,d`
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: See description below
 Status Affected: C
 Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is stored back in register 'f'.

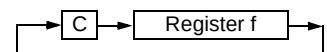


RETLW Return with Literal in W

Syntax: `[label] RETLW k`
 Operands: $0 \leq k \leq 255$
 Operation: $k \rightarrow (W)$;
 TOS → PC
 Status Affected: None
 Description: The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RRF Rotate Right f through Carry

Syntax: `[label] RRF f,d`
 Operands: $0 \leq f \leq 127$
 $d \in [0,1]$
 Operation: See description below
 Status Affected: C
 Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' = 0, the result is placed in the W register. If 'd' = 1, the result is placed back in register 'f'.



RETURN Return from Subroutine

Syntax: `[label] RETURN`
 Operands: None
 Operation: TOS → PC
 Status Affected: None
 Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

SLEEP Sleep

Syntax: `[label] SLEEP`
 Operands: None
 Operation: 00h → WDT,
 0 → WDT prescaler,
 1 → $\overline{TO}$,
 0 → $\overline{PD}$
 Status Affected: $\overline{TO}$, $\overline{PD}$
 Description: The Power-Down status bit, $\overline{PD}$, is cleared. Time-out status bit, $\overline{TO}$, is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

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SUBLW Subtract W from Literal

Syntax: *[label]* SUBLW *k*

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (two's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

XORLW Exclusive OR Literal with W

Syntax: *[label]* XORLW *k*

Operands: $0 \leq k \leq 255$

Operation: $(W) .XOR. k \rightarrow (W)$

Status Affected: Z

Description: The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.

SUBWF Subtract W from f

Syntax: *[label]* SUBWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f) - (W) \rightarrow (\text{destination})$

Status Affected: C, DC, Z

Description: Subtract (two's complement method) W register from register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

XORWF Exclusive OR W with f

Syntax: *[label]* XORWF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(W) .XOR. (f) \rightarrow (\text{destination})$

Status Affected: Z

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' = 0, the result is stored in the W register. If 'd' = 1, the result is stored back in register 'f'.

SWAPF Swap Nibbles in f

Syntax: *[label]* SWAPF *f,d*

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: $(f<3:0>) \rightarrow (\text{destination}<7:4>),$
 $(f<7:4>) \rightarrow (\text{destination}<3:0>)$

Status Affected: None

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' = 0, the result is placed in W register. If 'd' = 1, the result is placed in register 'f'.

17.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers and dsPIC® digital signal controllers are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB C Compiler for Various Device Families
 - HI-TECH C® for Various Device Families
 - MPASM™ Assembler
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers
 - MPLAB ICD 3
 - PICKit™ 3 Debug Express
- Device Programmers
 - PICKit™ 2 Programmer
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits, and Starter Kits

17.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16/32-bit microcontroller market. The MPLAB IDE is a Windows® operating system-based application that contains:

- A single graphical interface to all debugging tools
 - Simulator
 - Programmer (sold separately)
 - In-Circuit Emulator (sold separately)
 - In-Circuit Debugger (sold separately)
- A full-featured editor with color-coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High-level source code debugging
- Mouse over variable inspection
- Drag and drop variables from source to watch windows
- Extensive on-line help
- Integration of select third party tools, such as IAR C Compilers

The MPLAB IDE allows you to:

- Edit your source files (either C or assembly)
- One-touch compile or assemble, and download to emulator and simulator tools (automatically updates all project information)
- Debug using:
 - Source files (C or assembly)
 - Mixed C and assembly
 - Machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost-effective simulators, through low-cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increased flexibility and power.

17.2 MPLAB C Compilers for Various Device Families

The MPLAB C Compiler code development systems are complete ANSI C compilers for Microchip's PIC18, PIC24 and PIC32 families of microcontrollers and the dsPIC30 and dsPIC33 families of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

17.3 HI-TECH C for Various Device Families

The HI-TECH C Compiler code development systems are complete ANSI C compilers for Microchip's PIC family of microcontrollers and the dsPIC family of digital signal controllers. These compilers provide powerful integration capabilities, omniscient code generation and ease of use.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

The compilers include a macro assembler, linker, pre-processor, and one-step driver, and can run on multiple platforms.

17.4 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

17.5 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

17.6 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC devices. MPLAB C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

17.7 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

17.8 MPLAB REAL ICE In-Circuit Emulator System

MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs PIC® Flash MCUs and dsPIC® Flash DSCs with the easy-to-use, powerful graphical user interface of the MPLAB Integrated Development Environment (IDE), included with each kit.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB IDE. In upcoming releases of MPLAB IDE, new devices will be supported, and new features will be added. MPLAB REAL ICE offers significant advantages over competitive emulators including low-cost, full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, a ruggedized probe interface and long (up to three meters) interconnection cables.

17.9 MPLAB ICD 3 In-Circuit Debugger System

MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost effective high-speed hardware debugger/programmer for Microchip Flash Digital Signal Controller (DSC) and microcontroller (MCU) devices. It debugs and programs PIC® Flash microcontrollers and dsPIC® DSCs with the powerful, yet easy-to-use graphical user interface of MPLAB Integrated Development Environment (IDE).

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

17.10 PICkit 3 In-Circuit Debugger/Programmer and PICkit 3 Debug Express

The MPLAB PICkit 3 allows debugging and programming of PIC® and dsPIC® Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB Integrated Development Environment (IDE). The MPLAB PICkit 3 is connected to the design engineer's PC using a full speed USB interface and can be connected to the target via an Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the reset line to implement in-circuit debugging and In-Circuit Serial Programming™.

The PICkit 3 Debug Express include the PICkit 3, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

17.11 PICkit 2 Development Programmer/Debugger and PICkit 2 Debug Express

The PICkit™ 2 Development Programmer/Debugger is a low-cost development tool with an easy to use interface for programming and debugging Microchip's Flash families of microcontrollers. The full featured Windows® programming interface supports baseline (PIC10F, PIC12F5xx, PIC16F5xx), midrange (PIC12F6xx, PIC16F), PIC18F, PIC24, dsPIC30, dsPIC33, and PIC32 families of 8-bit, 16-bit, and 32-bit microcontrollers, and many Microchip Serial EEPROM products. With Microchip's powerful MPLAB Integrated Development Environment (IDE) the PICkit™ 2 enables in-circuit debugging on most PIC® microcontrollers. In-Circuit-Debugging runs, halts and single steps the program while the PIC microcontroller is embedded in the application. When halted at a breakpoint, the file registers can be examined and modified.

The PICkit 2 Debug Express include the PICkit 2, demo board and microcontroller, hookup cables and CDROM with user's guide, lessons, tutorial, compiler and MPLAB IDE software.

17.12 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages and a modular, detachable socket assembly to support various package types. The ICSP™ cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices and incorporates an MMC card for file storage and data applications.

17.13 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

18.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and MCLR)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	-0.3 to +7.5V
Voltage on MCLR with respect to VSS (Note 2)	-0.3 to +14V
Total power dissipation (Note 1)	1W
Maximum current out of VSS pin	200 mA
Maximum current into VDD pin	200 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by PORTA	100 mA
Maximum current sourced by PORTA	100 mA
Maximum current sunk by PORTB	100 mA
Maximum current sourced by PORTB	100 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

2: Voltage spikes at the MCLR pin may cause latch-up. A series resistor of greater than 1 kΩ should be used to pull MCLR to VDD, rather than tying the pin directly to VDD.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PIC16F87/88

FIGURE 18-1: PIC16F87/88 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL, EXTENDED)

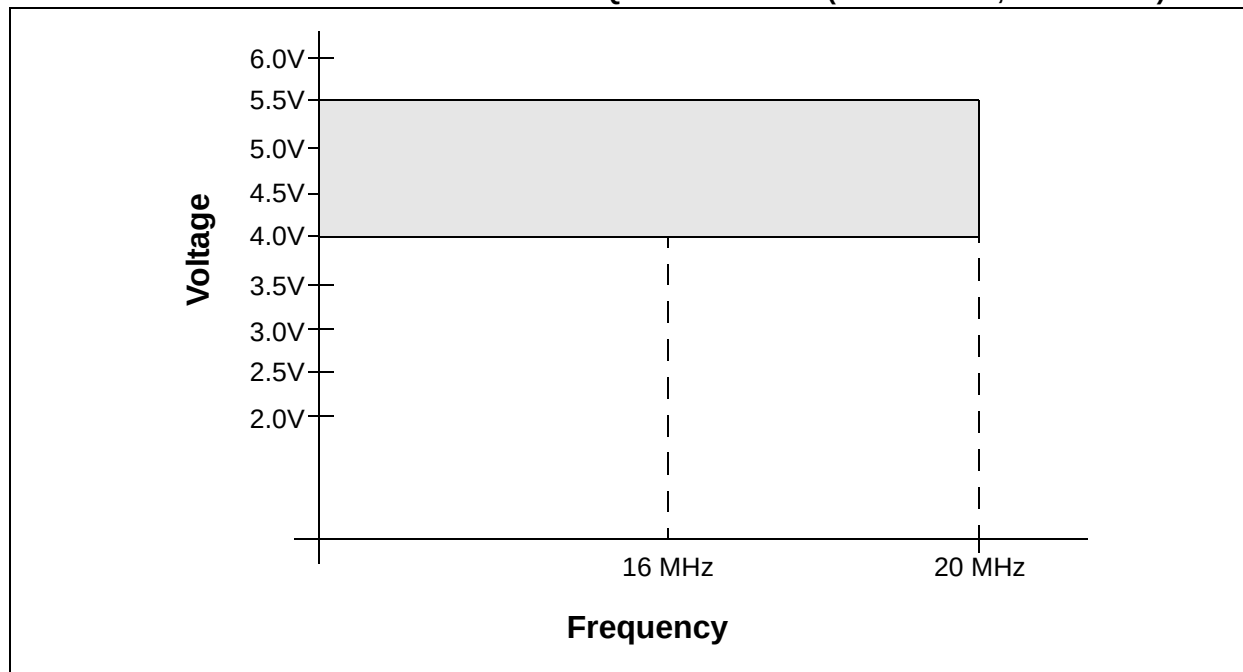
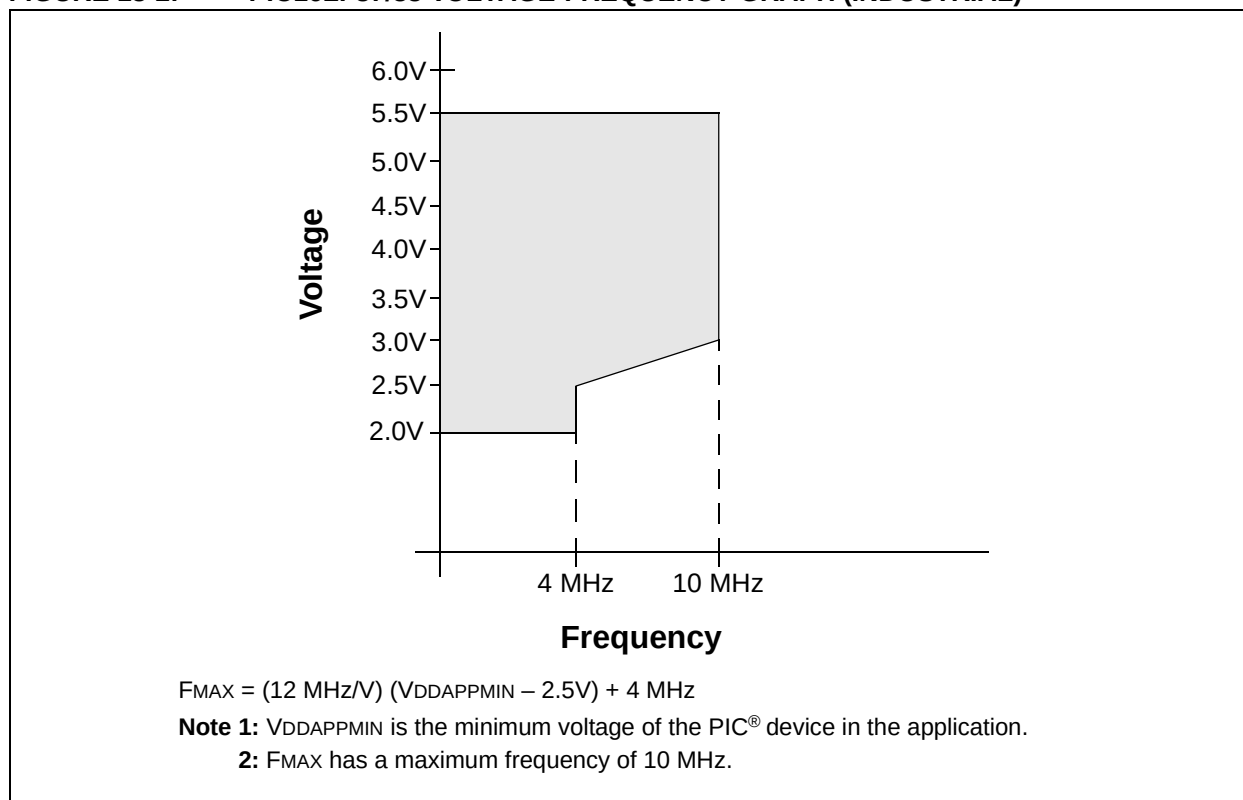


FIGURE 18-2: PIC16LF87/88 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



18.1 DC Characteristics: Supply Voltage

PIC16F87/88 (Industrial, Extended)

PIC16LF87/88 (Industrial)

PIC16LF87/88 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC16F87/88 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC16LF87/88	2.0	—	5.5	V	HS, XT, RC and LP Oscillator mode
		PIC16F87/88	4.0	—	5.5	V	
D002	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	—	0.7	V	See Section 15.4 “Power-on Reset (POR)” for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See Section 15.4 “Power-on Reset (POR)” for details
D005	VBOR	Brown-out Reset Voltage					
		PIC16LF87/88	3.65	—	4.35	V	
		PIC16F87/88	3.65	—	4.35	V	FMAX = 14 MHz ⁽²⁾

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When BOR is enabled, the device will operate correctly until the VBOR voltage trip point is reached.

PIC16F87/88

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Power-Down Current (IPD)⁽¹⁾						
	PIC16LF87/88	0.1	0.4	μA	-40°C	VDD = 2.0V	
		0.1	0.4	μA	+25°C		
		0.4	1.5	μA	+85°C		
	PIC16LF87/88	0.3	0.5	μA	-40°C	VDD = 3.0V	
		0.3	0.5	μA	+25°C		
		0.7	1.7	μA	+85°C		
	All devices	0.6	1.0	μA	-40°C	VDD = 5.0V	
		0.6	1.0	μA	+25°C		
		1.2	5.0	μA	+85°C		
	Extended devices	6	28	μA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{PD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in k Ω .

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (I _{DD}) ^(2,3)						
	PIC16LF87/88	9	20	μA	-40°C	V _{DD} = 2.0V	Fosc = 32 kHz (LP Oscillator)
		7	15	μA	+25°C		
		7	15	μA	+85°C		
	PIC16LF87/88	16	30	μA	-40°C	V _{DD} = 3.0V	
		14	25	μA	+25°C		
		14	25	μA	+85°C		
	All devices	32	40	μA	-40°C	V _{DD} = 5.0V	
		26	35	μA	+25°C		
		26	35	μA	+85°C		
	Extended Devices	35	53	μA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with REXT in kΩ.

PIC16F87/88

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ^(2,3)						
	PIC16LF87/88	72	95	μA	-40°C	VDD = 2.0V	FOSC = 1 MHz (RC Oscillator) ⁽³⁾
		76	90	μA	+25°C		
		76	90	μA	+85°C		
	PIC16LF87/88	138	175	μA	-40°C	VDD = 3.0V	
		136	170	μA	+25°C		
		136	170	μA	+85°C		
	All devices	310	380	μA	-40°C	VDD = 5.0V	
		290	360	μA	+25°C		
		280	360	μA	+85°C		
	Extended devices	330	500	μA	125°C		
	PIC16LF87/88	270	335	μA	-40°C	VDD = 2.0V	FOSC = 4 MHz (RC Oscillator) ⁽³⁾
		280	330	μA	+25°C		
		285	330	μA	+85°C		
	PIC16LF87/88	460	610	μA	-40°C	VDD = 3.0V	
		450	600	μA	+25°C		
		450	600	μA	+85°C		
	All devices	900	1060	μA	-40°C	VDD = 5.0V	
		890	1050	μA	+25°C		
		890	1050	μA	+85°C		
Extended devices	.920	1.5	mA	+125°C			

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all I_{DD} measurements in active operation mode are:

$OSC1$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;

$MCLR$ = V_{DD} ; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD)^(2,3)						
	All devices	1.8	2.3	mA	-40°C	VDD = 4.0V	FOSC = 20 MHz (HS Oscillator)
		1.6	2.2	mA	+25°C		
		1.3	2.2	mA	+85°C		
	All devices	3.0	4.2	mA	-40°C	VDD = 5.0V	
		2.5	4.0	mA	+25°C		
		2.5	4.0	mA	+85°C		
	Extended devices	3.0	5.0	mA	+85°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 $\overline{\text{OSC1}}$ = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
 $\overline{\text{MCLR}}$ = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

PIC16F87/88

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ^(2,3)						
	PIC16LF87/88	8	20	μA	-40°C	VDD = 2.0V	Fosc = 31.25 kHz (RC_RUN mode, Internal RC Oscillator)
		7	15	μA	+25°C		
		7	15	μA	+85°C		
	PIC16LF87/88	16	30	μA	-40°C	VDD = 3.0V	
		14	25	μA	+25°C		
		14	25	μA	+85°C		
	All devices	32	40	μA	-40°C	VDD = 5.0V	
		29	35	μA	+25°C		
		29	35	μA	+85°C		
	Extended devices	35	45	μA	+125°C		
	PIC16LF87/88	132	160	μA	-40°C	VDD = 2.0V	Fosc = 1 MHz (RC_RUN mode, Internal RC Oscillator)
		126	155	μA	+25°C		
		126	155	μA	+85°C		
	PIC16LF87/88	260	310	μA	-40°C	VDD = 3.0V	
		230	300	μA	+25°C		
		230	300	μA	+85°C		
	All devices	560	690	μA	-40°C	VDD = 5.0V	
		500	650	μA	+25°C		
		500	650	μA	+85°C		
Extended devices	570	710	μA	+125°C			

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (I _{DD}) ^(2,3)						
	PIC16LF87/88	310	420	μA	-40°C	V _{DD} = 2.0V	FOSC = 4 MHz (RC_RUN mode, Internal RC Oscillator)
		300	410	μA	+25°C		
		300	410	μA	+85°C		
	PIC16F87/88	550	650	μA	-40°C	V _{DD} = 3.0V	
		530	620	μA	+25°C		
		530	620	μA	+85°C		
	All devices	1.2	1.5	mA	-40°C	V _{DD} = 5.0V	
		1.1	1.4	mA	+25°C		
		1.1	1.4	mA	+85°C		
	Extended devices	1.3	1.6	mA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in $k\Omega$.

PIC16F87/88

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial						
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended						
Param No.	Device	Typ	Max	Units	Conditions			
	Supply Current (IDD) ^(2,3)							
	PIC16LF87/88	.950	1.3	mA	-40°C	VDD = 3.0V	FOSC = 8 MHz (RC_RUN mode, Internal RC Oscillator)	
		.930	1.2	mA	+25°C			
		.930	1.2	mA	+85°C			
	All devices	1.8	3.0	mA	-40°C	VDD = 5.0V		
		1.7	2.8	mA	+25°C			
		1.7	2.8	mA	+85°C			
	Extended devices	2.0	4.0	mA	+125°C			
	PIC16LF87/88	9	13	μA	-10°C	VDD = 2.0V		FOSC = 32 kHz (SEC_RUN mode, Timer1 as clock)
		9	14	μA	+25°C			
		11	16	μA	+70°C			
	PIC16LF87/88	12	34	μA	-10°C	VDD = 3.0V		
		12	31	μA	+25°C			
		14	28	μA	+70°C			
	All devices	20	72	μA	-10°C	VDD = 5.0V		
		20	65	μA	+25°C			
		25	59	μA	+70°C			

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD};
MCLR = V_{DD}; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through R_{EXT} is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in kΩ.

18.2 DC Characteristics: Power-Down and Supply Current PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC16F87/88 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
D022 (ΔI _{WDT})	Module Differential Currents (ΔI _{WDT} , ΔI _{BOR} , ΔI _{LVD} , ΔI _{OSCB} , ΔI _{AD})						
	Watchdog Timer	1.5	3.8	μA	-40°C	V _{DD} = 2.0V	
		2.2	3.8	μA	+25°C		
		2.7	4.0	μA	+85°C		
		2.3	4.6	μA	-40°C	V _{DD} = 3.0V	
		2.7	4.6	μA	+25°C		
		3.1	4.8	μA	+85°C		
		3.0	10.0	μA	-40°C	V _{DD} = 5.0V	
		3.3	10.0	μA	+25°C		
	3.9	13.0	μA	+85°C			
Extended devices	5.0	21.0	μA	+125°C			
D022A (ΔI _{BOR})	Brown-out Reset	40	60	μA	-40°C to +85°C	V _{DD} = 5.0V	
D025 (ΔI _{OSCB})	Timer1 Oscillator	1.7	2.3	μA	-40°C	V _{DD} = 2.0V	32 kHz on Timer1
		1.8	2.3	μA	+25°C		
		2.0	2.3	μA	+85°C		
		2.2	3.8	μA	-40°C	V _{DD} = 3.0V	
		2.6	3.8	μA	+25°C		
		2.9	3.8	μA	+85°C		
		3.0	6.0	μA	-40°C	V _{DD} = 5.0V	
		3.2	6.0	μA	+25°C		
		3.4	7.0	μA	+85°C		
D026 (ΔI _{AD})	A/D Converter	0.001	2.0	μA	-40°C to +85°C	V _{DD} = 2.0V	A/D on, Sleep, not converting
		0.001	2.0	μA	-40°C to +85°C	V _{DD} = 3.0V	
		0.003	2.0	μA	-40°C to +85°C	V _{DD} = 5.0V	
	Extended devices	4.0	8.0	μA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ;
MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = V_{DD}/2R_{EXT}$ (mA) with R_{EXT} in k Ω .

PIC16F87/88

18.3 DC Characteristics: Internal RC Accuracy

PIC16F87/88 (Industrial, Extended)

PIC16LF87/88 (Industrial)

PIC16LF87/88 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature					
-------------------------------------	--	---	--	--	--	--	--

Legend: Shading of rows is to assist in readability of the table.

Note 1: Frequency calibrated at 25°C. OSCTUNE register can be used to compensate for temperature drift.

Note 2: INTRC frequency after calibration.

18.4 DC Characteristics: PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
			Operating voltage V_{DD} range as described in DC Specification, Section 18.1 “DC Characteristics: Supply Voltage”.				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D034	V_{IL}	Input Low Voltage					
		I/O ports:					
		with TTL buffer	V_{SS}	—	$0.15 V_{DD}$	V	For entire V_{DD} range
			V_{SS}	—	0.8V	V	$4.5V \leq V_{DD} \leq 5.5V$
		with Schmitt Trigger buffer	V_{SS}	—	$0.2 V_{DD}$	V	
		MCLR, OSC1 (in RC mode)	V_{SS}	—	$0.2 V_{DD}$	V	(Note 1)
		OSC1 (in XT and LP mode)	V_{SS}	—	0.3V	V	
		OSC1 (in HS mode)	V_{SS}	—	$0.3 V_{DD}$	V	
D040 D040A D041 D042 D042A D043 D044	V_{IH}	Input High Voltage					
		I/O ports:					
		with TTL buffer	2.0	—	V_{DD}	V	$4.5V \leq V_{DD} \leq 5.5V$
			$0.25 V_{DD} + 0.8V$	—	V_{DD}	V	For entire V_{DD} range
		with Schmitt Trigger buffer	$0.8 V_{DD}$	—	V_{DD}	V	For entire V_{DD} range
		MCLR	$0.8 V_{DD}$	—	V_{DD}	V	
		OSC1 (in XT and LP mode)	1.6V	—	V_{DD}	V	
		OSC1 (in HS mode)	$0.7 V_{DD}$	—	V_{DD}	V	
D070	I_{PURB}	PORTB Weak Pull-up Current	50	250	400	μA	$V_{DD} = 5V, V_{PIN} = V_{SS}$
D060 D061 D063	I_{IL}	Input Leakage Current (Notes 2, 3)					
		I/O ports	—	—	± 1	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, pin at high-impedance
		MCLR	—	—	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
		OSC1	—	—	± 5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP oscillator configuration

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F87/88 be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

PIC16F87/88

18.4 DC Characteristics: PIC16F87/88 (Industrial, Extended) PIC16LF87/88 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended Operating voltage V_{DD} range as described in DC Specification, Section 18.1 “DC Characteristics: Supply Voltage”.				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D080	VOL	Output Low Voltage					
		I/O ports	—	—	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D083		OSC2/CLKO (RC oscillator configuration)	—	—	0.6	V	$I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D090	VOH	Output High Voltage					
		I/O ports (Note 3)	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D092		OSC2/CLKO (RC oscillator configuration)	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40°C to $+125^{\circ}\text{C}$
D100	Cosc2	Capacitive Loading Specs on Output Pins					
		OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	—	50	pF	
D102	CB	SCL, SDA in I ² C™ mode	—	—	400	pF	
D120	ED	Data EEPROM Memory					
		Endurance	100K 10K	1M 100K	— —	E/W E/W	-40°C to 85°C $+85^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
	VDRW	V_{DD} for Read/Write	V_{MIN}	—	5.5	V	Using EECON to read/write, V_{MIN} = min. operating voltage
	TDEW	Erase/Write Cycle Time	—	4	8	ms	
D130	EP	Program Flash Memory					
		Endurance	10K 1K	100K 10K	— —	E/W E/W	-40°C to 85°C $+85^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
	VPR	V_{DD} for Read	V_{MIN}	—	5.5	V	Using EECON to read/write, V_{MIN} = min. operating voltage
		V_{DD} for Erase/Write	V_{MIN}	—	5.5	V	
	TPE	Erase Cycle Time	—	2	4	ms	
	D134	TPW	Write Cycle Time	—	2	4	ms

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC16F87/88 be driven with external clock in RC mode.
- 2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.

TABLE 18-1: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < V _{DD} < 5.5V, -40°C < T _A < +85°C, unless otherwise stated							
Param No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D300	V _{IOFF}	Input Offset Voltage	—	±5.0	±10	mV	
D301	V _{ICM}	Input Common Mode Voltage*	0	—	V _{DD} – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio*	55	—	—	dB	
300 300A	T _{RESP}	Response Time ^{(1)*}	—	150	400 600	ns ns	PIC16F87/88 PIC16LF87/88
301	T _{MC2OV}	Comparator Mode Change to Output Valid*	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (V_{DD} – 1.5)/2 while the other input transitions from V_{SS} to V_{DD}.

TABLE 18-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: 3.0V < V _{DD} < 5.5V, -40°C < T _A < +85°C, unless otherwise stated							
Spec No.	Sym	Characteristics	Min	Typ	Max	Units	Comments
D310	V _{RES}	Resolution	V _{DD} /24	—	V _{DD} /32	LSb	
D311	V _{RAA}	Absolute Accuracy	— —	— —	1/2 1/2	LSb LSb	Low Range (CVRR = 1) High Range (CVRR = 0)
D312	V _{RUR}	Unit Resistor Value (R)*	—	2k	—	Ω	
310	T _{SET}	Settling Time ^{(1)*}	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while CVRR = 1 and CVR<3:0> transitions from '0000' to '1111'.

PIC16F87/88

18.5 Timing Parameter Symbology

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS
2. TppS
3. TCC:ST (I²C specifications only)
4. Ts (I²C specifications only)

T			
F	Frequency	T	Time

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKO	rd	$\overline{RD}$
cs	$\overline{CS}$	rw	$\overline{RD}$ or $\overline{WR}$
di	SDI	sc	SCK
do	SDO	ss	$\overline{SS}$
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	$\overline{MCLR}$	wr	$\overline{WR}$

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance
I²C only			
AA	output access	High	High
BUF	Bus free	Low	Low

TCC:ST (I²C specifications only)

CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

FIGURE 18-3: LOAD CONDITIONS

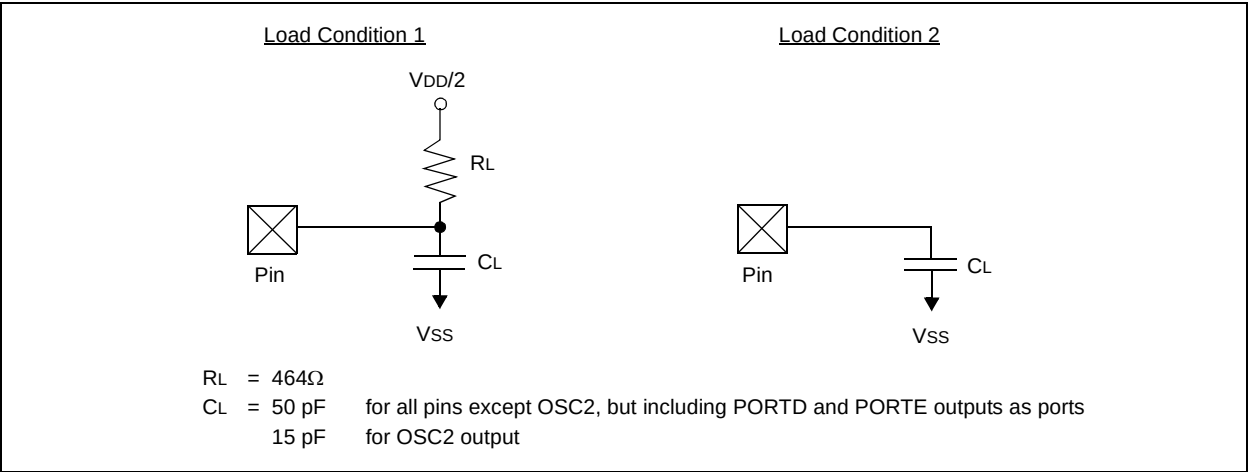


FIGURE 18-4: EXTERNAL CLOCK TIMING

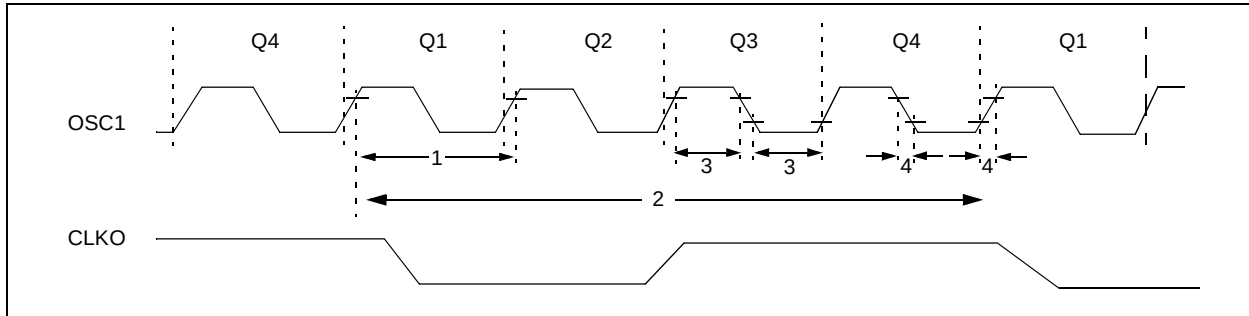


TABLE 18-3: EXTERNAL CLOCK TIMING REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKI Frequency (Note 1)	DC	—	1	MHz	XT and RC Oscillator mode
			DC	—	20	MHz	HS Oscillator mode
			DC	—	32	kHz	LP Oscillator mode
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC Oscillator mode
			0.1	—	4	MHz	XT Oscillator mode
			4	—	20	MHz	HS Oscillator mode
			5	—	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period (Note 1)	1000	—	—	ns	XT and RC Oscillator modes
			50	—	—	ns	HS Oscillator mode
			5	—	—	ms	LP Oscillator mode
		Oscillator Period (Note 1)	250	—	—	ns	RC Oscillator mode
			250	—	10,000	ns	XT Oscillator mode
			50	—	250	ns	HS Oscillator mode
			5	—	—	ms	LP Oscillator mode
2	Tcy	Instruction Cycle Time (Note 1)	200	Tcy	DC	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	500	—	—	ns	XT oscillator
			2.5	—	—	ms	LP oscillator
			15	—	—	ns	HS oscillator
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	—	25	ns	XT oscillator
			—	—	50	ns	LP oscillator
			—	—	15	ns	HS oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

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FIGURE 18-5: CLKO AND I/O TIMING

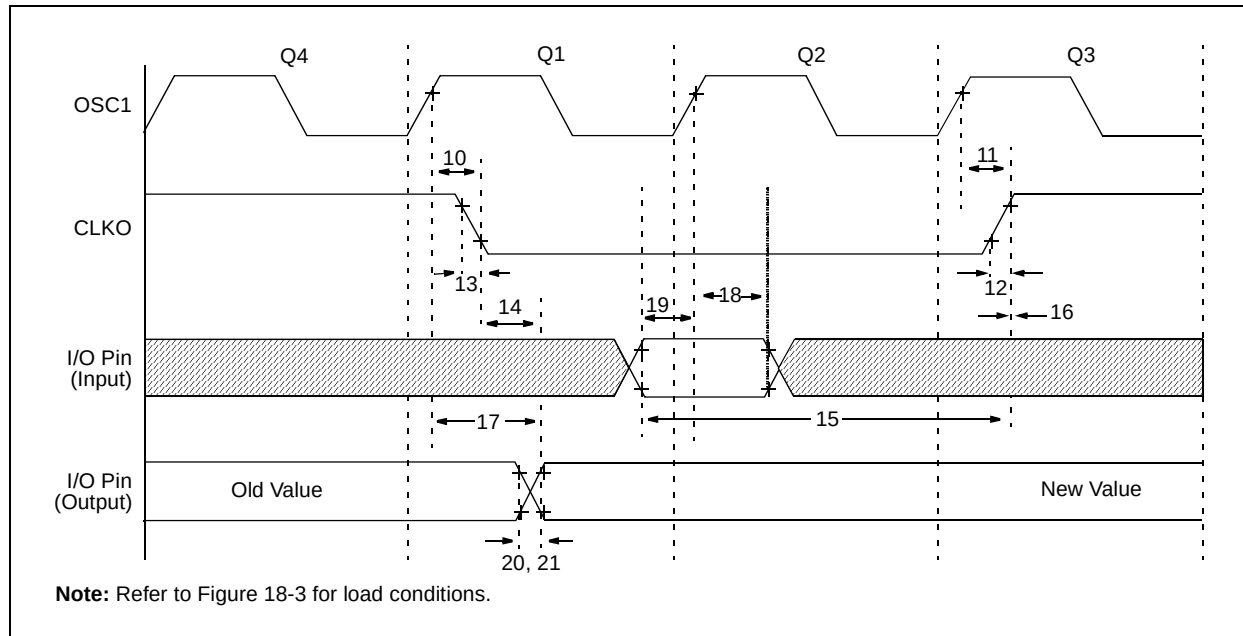


TABLE 18-4: CLKO AND I/O TIMING REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
10*	TosH2ckL	OSC1 ↑ to CLKO ↓	—	75	200	ns	(Note 1)
11*	TosH2ckH	OSC1 ↑ to CLKO ↑	—	75	200	ns	(Note 1)
12*	TckR	CLKO Rise Time	—	35	100	ns	(Note 1)
13*	TckF	CLKO Fall Time	—	35	100	ns	(Note 1)
14*	TckL2ioV	CLKO ↓ to Port Out Valid	—	—	0.5 Tcy + 20	ns	(Note 1)
15*	TioV2ckH	Port In Valid before CLKO ↑	Tosc + 200	—	—	ns	(Note 1)
16*	TckH2ioI	Port In Hold after CLKO ↑	0	—	—	ns	(Note 1)
17*	TosH2ioV	OSC1 ↑ (Q1 cycle) to Port Out Valid	—	100	255	ns	
18*	TosH2ioI	OSC1 ↑ (Q2 cycle) to Port Input Invalid (I/O in hold time)	PIC16F87/88	100	—	—	ns
			PIC16LF87/88	200	—	—	ns
19*	TioV2osH	Port Input Valid to OSC1 ↑ (I/O in setup time)	0	—	—	ns	
20*	TioR	Port Output Rise Time	PIC16F87/88	—	10	40	ns
			PIC16LF87/88	—	—	145	ns
21*	TioF	Port Output Fall Time	PIC16F87/88	—	10	40	ns
			PIC16LF87/88	—	—	145	ns
22††*	TINP	INT Pin High or Low Time	Tcy	—	—	ns	
23††*	TRBP	RB7:RB4 Change INT High or Low Time	Tcy	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode where CLKO output is 4 x TOSC.

FIGURE 18-6: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

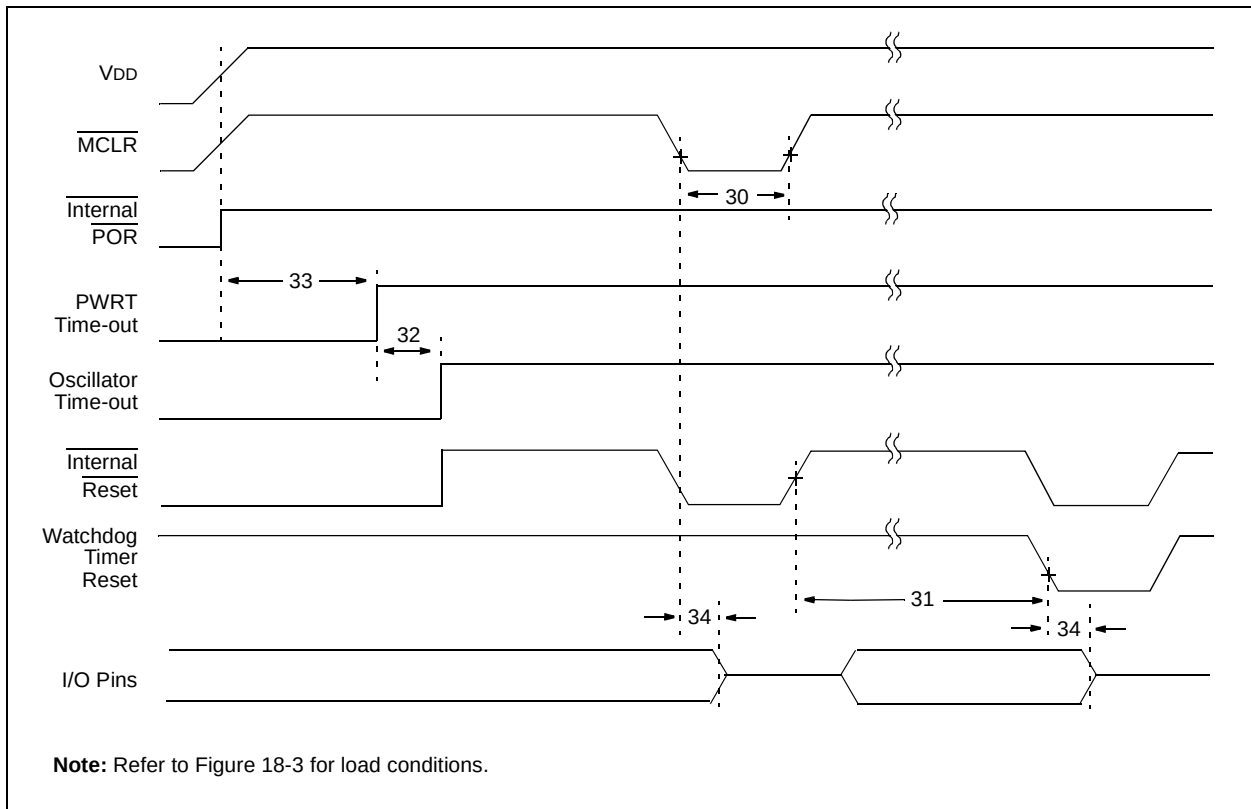


FIGURE 18-7: BROWN-OUT RESET TIMING

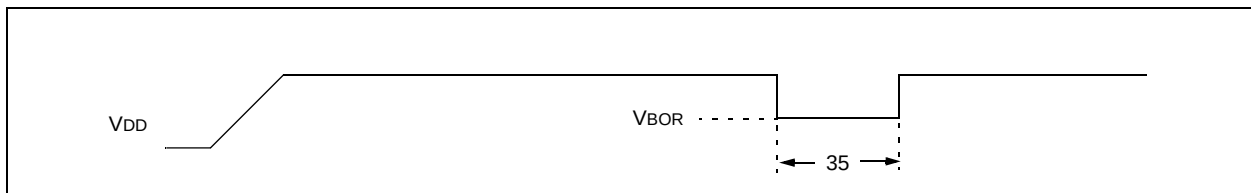


TABLE 18-5: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Parameter No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TmCL	MCLR Pulse Width (Low)	2	—	—	μs	VDD = 5V, -40°C to +85°C
31*	TWDT	Watchdog Timer Time-out Period (16-bit prescaler = 0100 and no postscaler)	13.6	16	18.4	ms	VDD = 5V, -40°C to +85°C
32	TOST	Oscillation Start-up Timer Period	—	1024 TOSC	—	—	TOSC = OSC1 period
33*	TPWRT	Power-up Timer Period	61.2	72	82.8	ms	VDD = 5V, -40°C to +85°C
34	TIOZ	I/O High-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.1	μs	
35	TBOR	Brown-out Reset Pulse Width	100	—	—	μs	VDD ≤ VBOR (D005)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC16F87/88

FIGURE 18-8: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

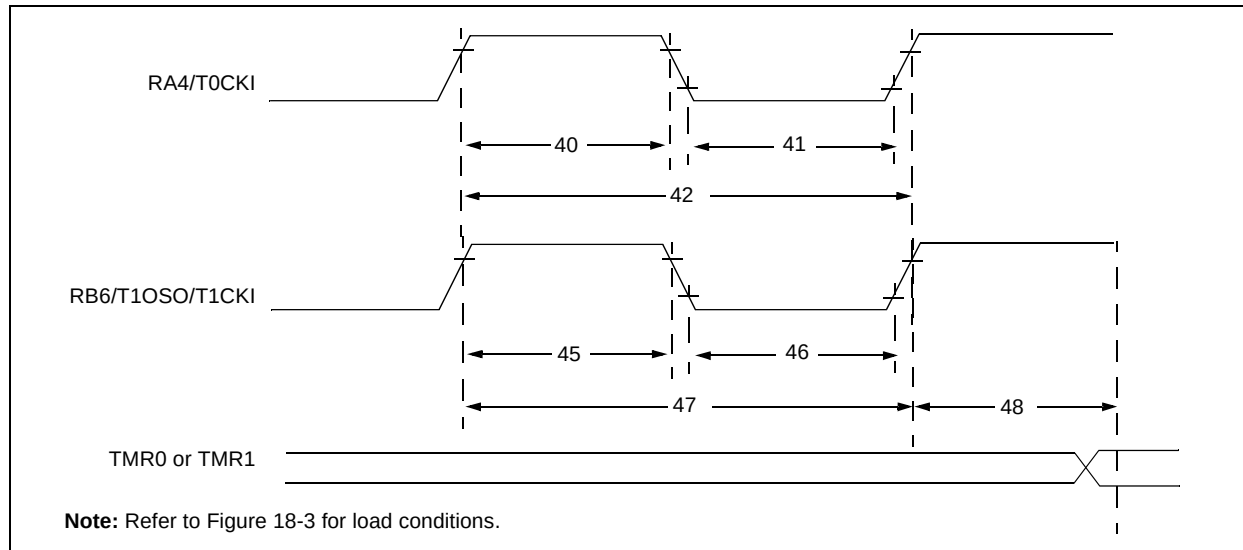


TABLE 18-6: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Symbol	Characteristic			Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width		No Prescaler	0.5 Tcy + 20	—	—	ns	Must also meet parameter 42
	With Prescaler			10	—	—	ns		
41*	Tt0L	T0CKI Low Pulse Width		No Prescaler	0.5 Tcy + 20	—	—	ns	Must also meet parameter 42
	With Prescaler			10	—	—	ns		
42*	Tt0P	T0CKI Period		No Prescaler	Tcy + 40	—	—	ns	N = prescale value (2, 4, ..., 256)
	With Prescaler			Greater of: 20 or $\frac{Tcy + 40}{N}$	—	—	ns		
45*	Tt1H	T1CKI High Time	Synchronous, Prescaler = 1		0.5 Tcy + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2, 4, 8	PIC16F87/88	15	—	—	ns	
				PIC16LF87/88	25	—	—	ns	
			Asynchronous	PIC16F87/88	30	—	—	ns	
				PIC16LF87/88	50	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, Prescaler = 1		0.5 Tcy + 20	—	—	ns	Must also meet parameter 47
			Synchronous, Prescaler = 2, 4, 8	PIC16F87/88	15	—	—	ns	
				PIC16LF87/88	25	—	—	ns	
			Asynchronous	PIC16F87/88	30	—	—	ns	
				PIC16LF87/88	50	—	—	ns	
47*	Tt1P	T1CKI Input Period	Synchronous	PIC16F87/88	Greater of: 30 or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
				PIC16LF87/88	Greater of: 50 or $\frac{Tcy + 40}{N}$				N = prescale value (1, 2, 4, 8)
			Asynchronous	PIC16F87/88	60	—	—	ns	
				PIC16LF87/88	100	—	—	ns	
	Ft1	Timer1 Oscillator Input Frequency Range (Oscillator enabled by setting bit T1OSCEN)			DC	—	32.768	kHz	
48	TCKEZtmr1	Delay from External Clock Edge to Timer Increment			2 Tosc	—	7 Tosc	—	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-9: CAPTURE/COMPARE/PWM TIMINGS (CCP1)

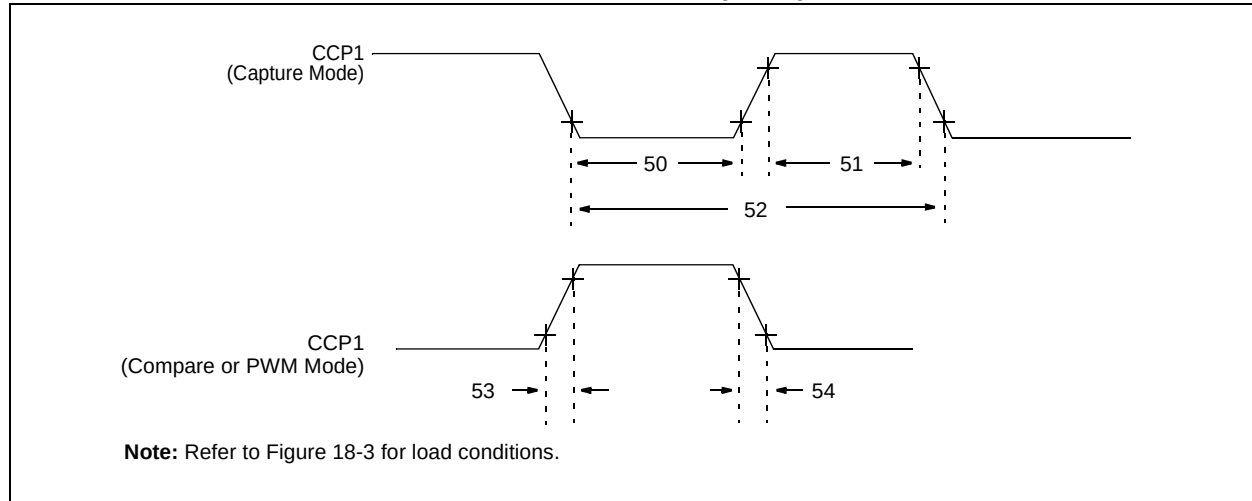


TABLE 18-7: CAPTURE/COMPARE/PWM REQUIREMENTS (CCP1)

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
50*	TccL	CCP1 Input Low Time	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	PIC16F87/88	10	—	—	
				PIC16LF87/88	20	—	—	
51*	TccH	CCP1 Input High Time	No Prescaler	$0.5 T_{CY} + 20$	—	—	ns	
			With Prescaler	PIC16F87/88	10	—	—	
				PIC16LF87/88	20	—	—	
52*	TccP	CCP1 Input Period		$\frac{3 T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 4 or 16)
53*	TccR	CCP1 Output Rise Time	PIC16F87/88	—	10	25	ns	
			PIC16LF87/88	—	25	50	ns	
54*	TccF	CCP1 Output Fall Time	PIC16F87/88	—	10	25	ns	
			PIC16LF87/88	—	25	45	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 18-10: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

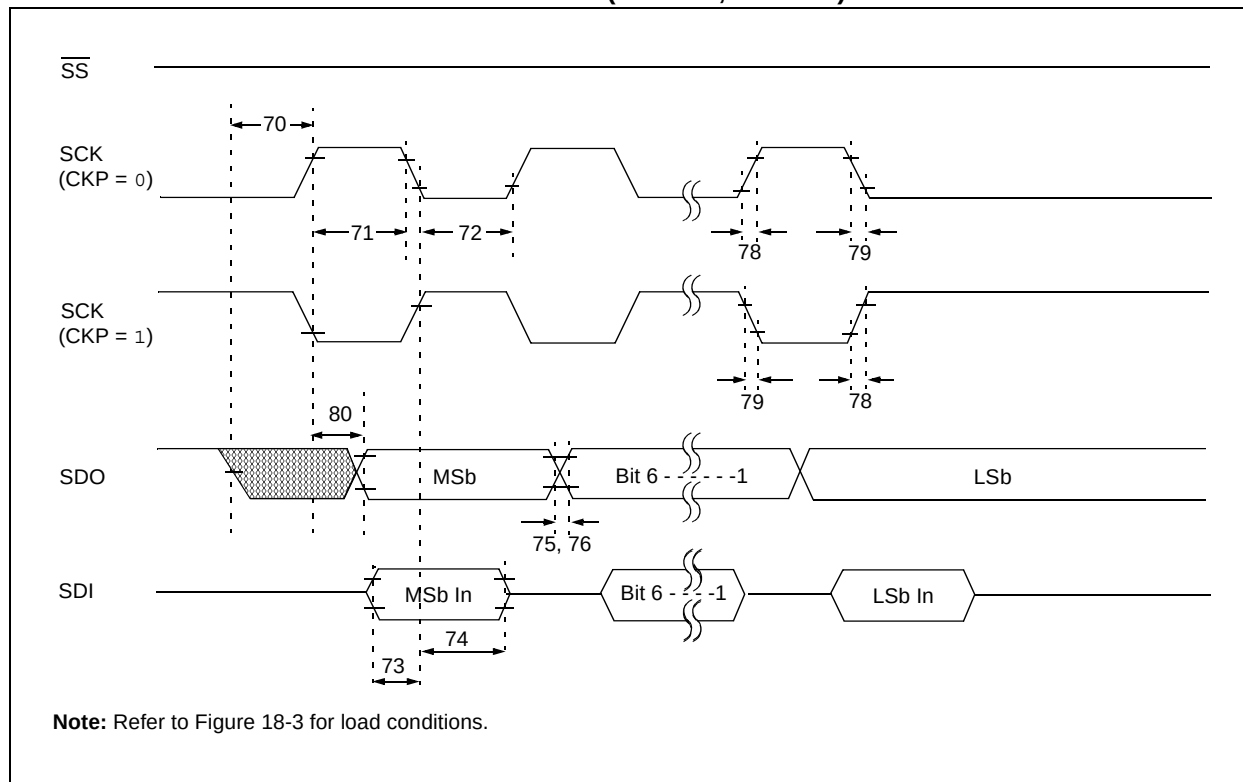


FIGURE 18-11: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)

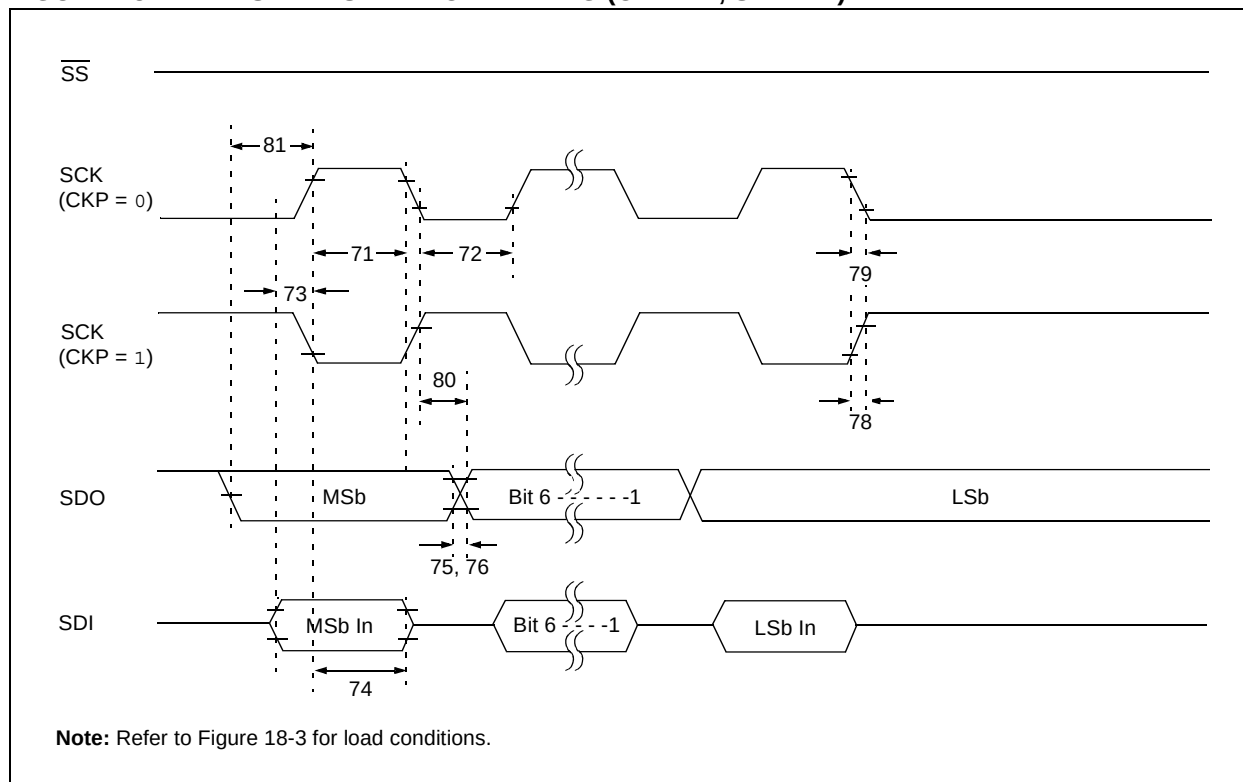


FIGURE 18-12: SPI SLAVE MODE TIMING (CKE = 0)

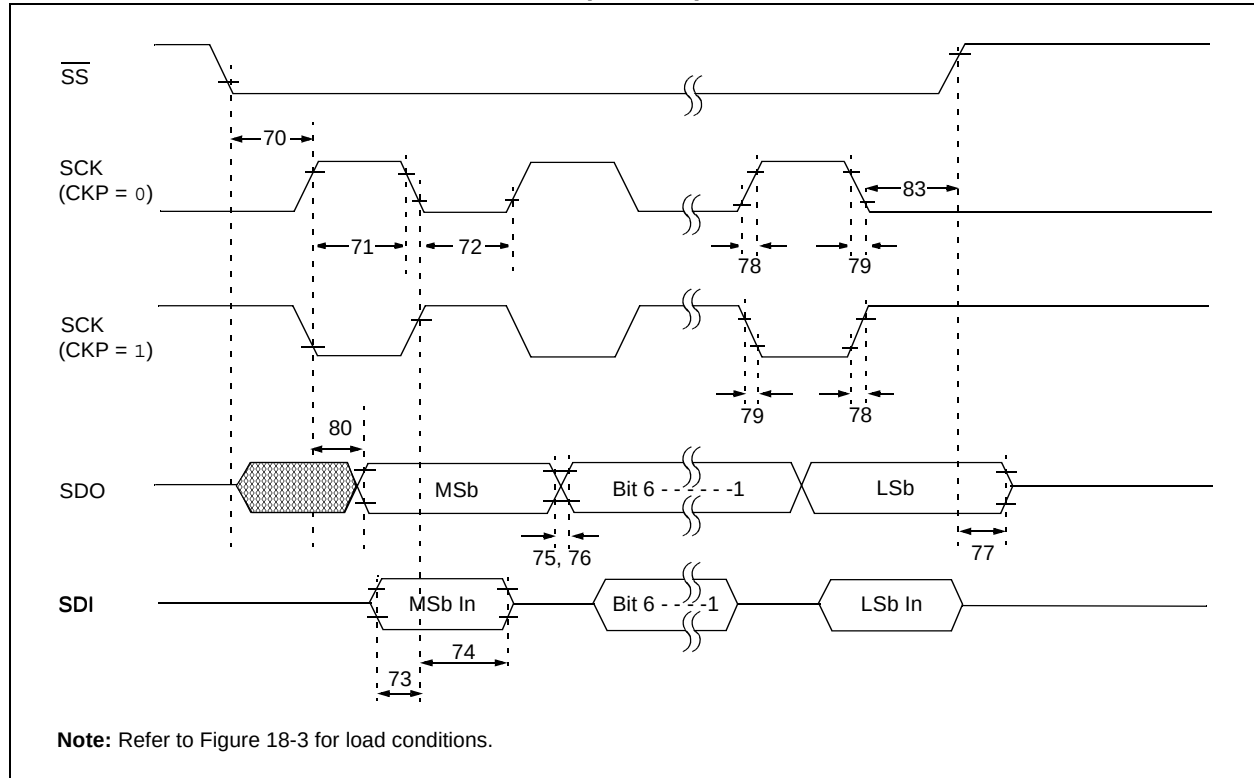
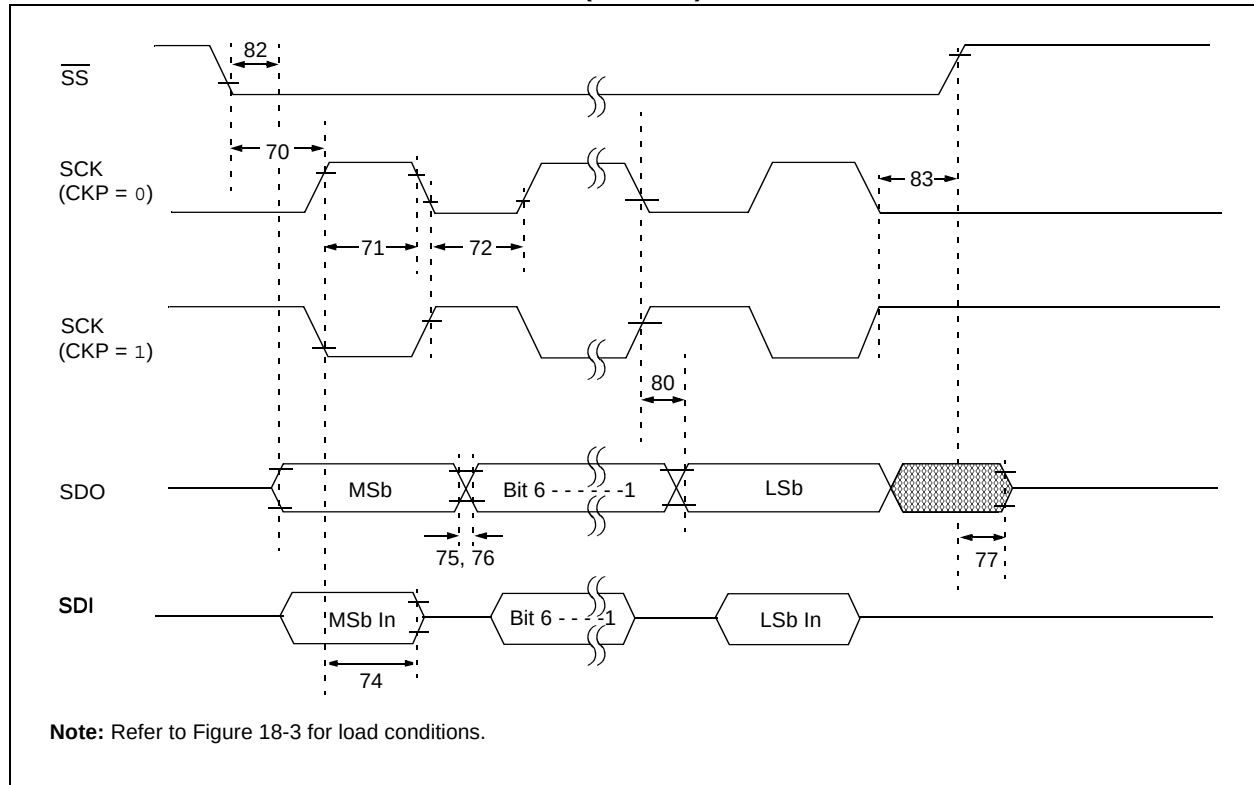


FIGURE 18-13: SPI SLAVE MODE TIMING (CKE = 1)



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TABLE 18-8: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Typ†	Max	Units	Conditions
70*	TssL2scH, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	T _{CY}	—	—	ns	
71*	TscH	SCK Input High Time (Slave mode)	T _{CY} + 20	—	—	ns	
72*	TscL	SCK Input Low Time (Slave mode)	T _{CY} + 20	—	—	ns	
73*	TdiV2scH, TdiV2scL	Setup Time of SDI Data Input to SCK Edge	100	—	—	ns	
74*	Tsch2diL, TscL2diL	Hold Time of SDI Data Input to SCK Edge	100	—	—	ns	
75*	TdoR	SDO Data Output Rise Time	—	10	25	ns	PIC16F87/88 PIC16LF87/88
76*	TdoF	SDO Data Output Fall Time	—	10	25	ns	
77*	TssH2doZ	$\overline{SS}$ ↑ to SDO Output High-Impedance	10	—	50	ns	
78*	TscR	SCK Output Rise Time (Master mode)	—	10	25	ns	PIC16F87/88 PIC16LF87/88
79*	TscF	SCK Output Fall Time (Master mode)	—	10	25	ns	
80*	Tsch2doV, TscL2doV	SDO Data Output Valid after SCK Edge	—	—	50 145	ns	PIC16F87/88 PIC16LF87/88
81*	TdoV2scH, TdoV2scL	SDO Data Output Setup to SCK Edge	T _{CY}	—	—	ns	
82*	TssL2doV	SDO Data Output Valid after $\overline{SS}$ ↓ Edge	—	—	50	ns	
83*	Tsch2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK Edge	1.5 T _{CY} + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-14: I²C™ BUS START/STOP BITS TIMING

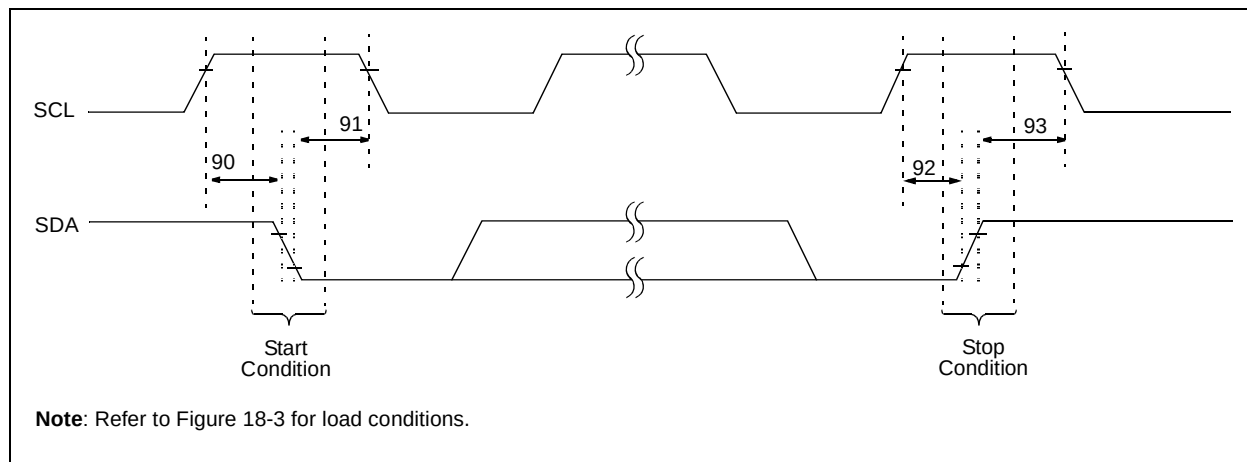
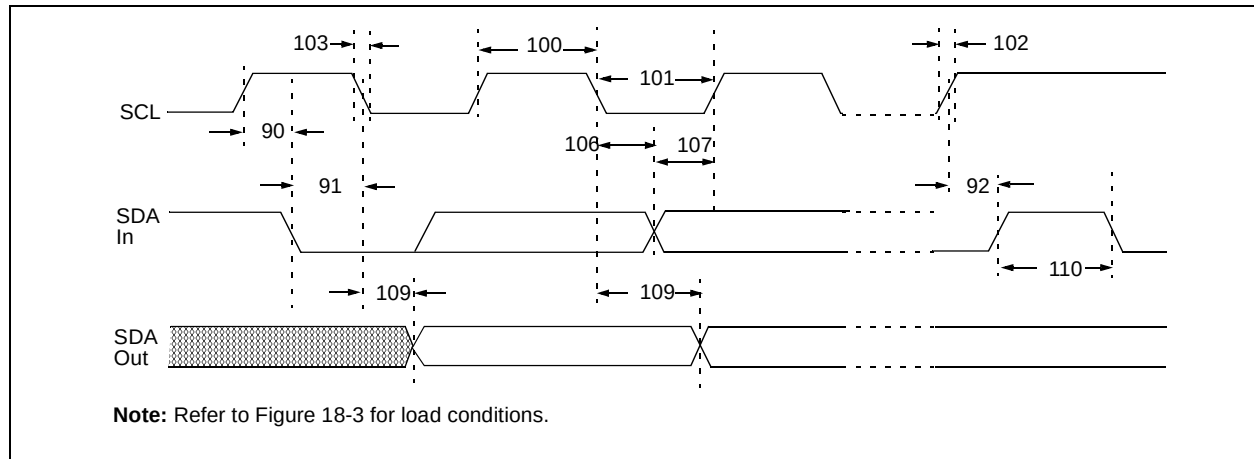


TABLE 18-9: I²C™ BUS START/STOP BITS REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
90*	TSU:STA	Start Condition Setup Time	100 kHz mode	4700	—	—	ns	Only relevant for Repeated Start condition
			400 kHz mode	600	—	—		
91*	THD:STA	Start Condition Hold Time	100 kHz mode	4000	—	—	ns	After this period, the first clock pulse is generated
			400 kHz mode	600	—	—		
92*	TSU:STO	Stop Condition Setup Time	100 kHz mode	4700	—	—	ns	
			400 kHz mode	600	—	—		
93	THD:STO	Stop Condition Hold Time	100 kHz mode	4000	—	—	ns	
			400 kHz mode	600	—	—		

* These parameters are characterized but not tested.

FIGURE 18-15: I²C™ BUS DATA TIMING



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TABLE 18-10: I²C™ BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
100*	T _{HIGH}	Clock High Time	100 kHz mode	4.0	—	μs
			400 kHz mode	0.6	—	μs
			SSP Module	1.5 T _{CY}	—	
101*	T _{LOW}	Clock Low Time	100 kHz mode	4.7	—	μs
			400 kHz mode	1.3	—	μs
			SSP Module	1.5 T _{CY}	—	
102*	T _R	SDA and SCL Rise Time	100 kHz mode	—	1000	ns
			400 kHz mode	20 + 0.1 C _B	300	ns C _B is specified to be from 10-400 pF
103*	T _F	SDA and SCL Fall Time	100 kHz mode	—	300	ns
			400 kHz mode	20 + 0.1 C _B	300	ns C _B is specified to be from 10-400 pF
90*	T _{SU:STA}	Start Condition Setup Time	100 kHz mode	4.7	—	μs
			400 kHz mode	0.6	—	μs Only relevant for Repeated Start condition
91*	T _{HD:STA}	Start Condition Hold Time	100 kHz mode	4.0	—	μs
			400 kHz mode	0.6	—	μs After this period, the first clock pulse is generated
106*	T _{HD:DAT}	Data Input Hold Time	100 kHz mode	0	—	ns
			400 kHz mode	0	0.9	μs
107*	T _{SU:DAT}	Data Input Setup Time	100 kHz mode	250	—	ns
			400 kHz mode	100	—	ns (Note 2)
92*	T _{SU:STO}	Stop Condition Setup Time	100 kHz mode	4.7	—	μs
			400 kHz mode	0.6	—	μs
109*	T _{AA}	Output Valid from Clock	100 kHz mode	—	3500	ns
			400 kHz mode	—	—	ns (Note 1)
110*	T _{BUF}	Bus Free Time	100 kHz mode	4.7	—	μs
			400 kHz mode	1.3	—	μs Time the bus must be free before a new transmission can start
	C _B	Bus Capacitive Loading	—	400	pF	

* These parameters are characterized but not tested.

- Note 1:** As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.
- 2:** A Fast mode (400 kHz) I²C™ bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement, T_{SU:DAT} ≥ 250 ns, must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line, T_R max. + T_{SU:DAT} = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.

FIGURE 18-16: AUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

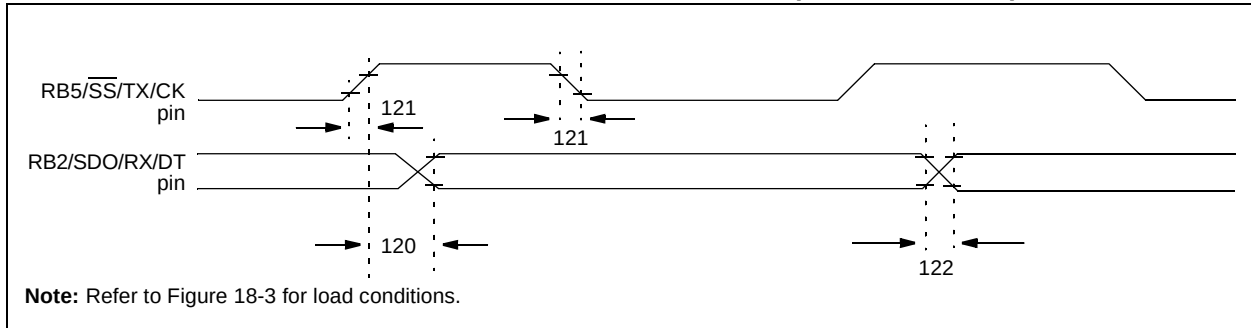


TABLE 18-11: AUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock High to Data Out Valid	—	—	80	ns	
					100	ns	
121	Tckrf	Clock Out Rise Time and Fall Time (Master mode)	—	—	45	ns	
					50	ns	
122	Tdtrf	Data Out Rise Time and Fall Time	—	—	45	ns	
					50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 18-17: AUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

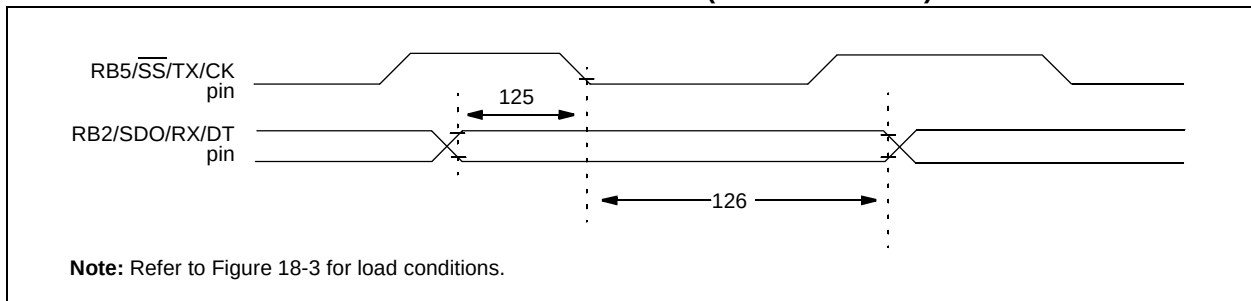


TABLE 18-12: AUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	SYNC RCV (MASTER & SLAVE) Data Setup before CK ↓ (DT setup time)	15	—	—	ns	
126	TckL2dtl	Data Hold after CK ↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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**TABLE 18-13: A/D CONVERTER CHARACTERISTICS: PIC16F87/88 (INDUSTRIAL, EXTENDED)
PIC16LF87/88 (INDUSTRIAL)**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10-bit	bit	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A03	EIL	Integral Linearity Error	—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A04	EDL	Differential Linearity Error	—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A06	EOFF	Offset Error	—	—	<±2	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A07	EGN	Gain Error	—	—	<±1	LSb	VREF = VDD = 5.12V, VSS ≤ VAIN ≤ VREF
A10	—	Monotonicity	—	guaranteed ⁽³⁾	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference Voltage (VREF+ – VREF-)	2.0	—	VDD + 0.3	V	
A21	VREF+	Reference Voltage High	AVDD – 2.5V		AVDD + 0.3V	V	
A22	VREF-	Reference Voltage Low	AVSS – 0.3V		VREF+ – 2.0V	V	
A25	VAIN	Analog Input Voltage	VSS – 0.3V	—	VREF + 0.3V	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	(Note 4)
A40	IAD	A/D Conversion Current (VDD)	PIC16F87/88	—	220	—	μA Average current consumption when A/D is on (Note 1)
			PIC16LF87/88	—	90	—	
A50	IREF	VREF Input Current (Note 2)	—	—	5	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN to charge CHOLD, see Section 12.1 “A/D Acquisition Requirements”. During A/D conversion cycle
			—	—	150	μA	

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** When A/D is off, it will not consume any current other than minor leakage current. The power-down current specification includes any such leakage from the A/D module.
- 2:** VREF current is from RA3 pin or VDD pin, whichever is selected as reference input.
- 3:** The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.
- 4:** Maximum allowed impedance for analog voltage source is 10 kΩ. This requires higher acquisition time.

FIGURE 18-18: A/D CONVERSION TIMING

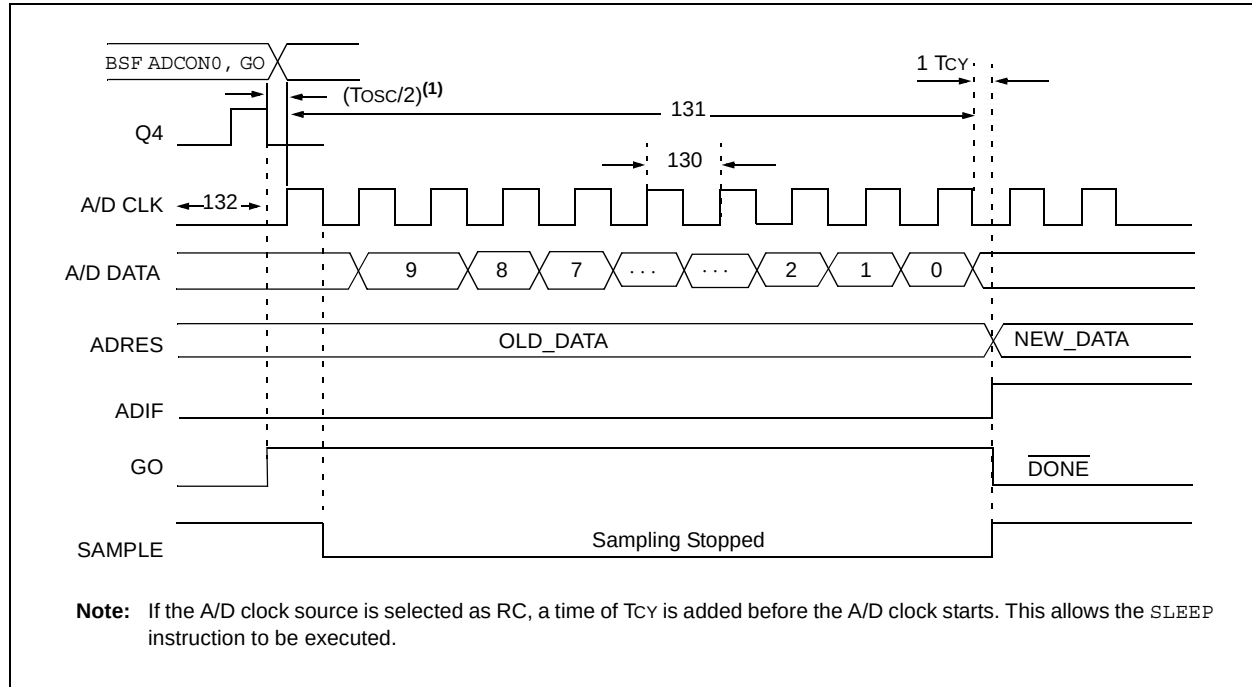


TABLE 18-14: A/D CONVERSION REQUIREMENTS

Param No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	PIC16F87/88	1.6	—	—	μs	TOSC based, VREF ≥ 3.0V
			PIC16LF87/88	3.0	—	—	μs	TOSC based, VREF ≥ 2.0V
			PIC16F87/88	2.0	4.0	6.0	μs	A/D RC mode
			PIC16LF87/88	3.0	6.0	9.0	μs	A/D RC mode
131	TCNV	Conversion Time (not including S/H time) (Note 1)			—	12	TAD	
132	TACQ	Acquisition Time		(Note 2)	40	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 LSb (i.e., 5.0 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
				10*	—	—	μs	
134	TGO	Q4 to A/D Clock Start		—	Tosc/2 §	—	—	If the A/D clock source is selected as RC, a time of Tcy is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

§ This specification ensured by design.

Note 1: ADRES registers may be read on the following T_{cy} cycle.

Note 2: See **Section 12.1 “A/D Acquisition Requirements”** for minimum conditions.

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NOTES:

19.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum” or “minimum” represents (mean + 3 σ) or (mean – 3 σ) respectively, where σ is a standard deviation, over the whole temperature range.

FIGURE 19-1: TYPICAL I_{DD} vs. F_{OSC} OVER V_{DD} (HS MODE)

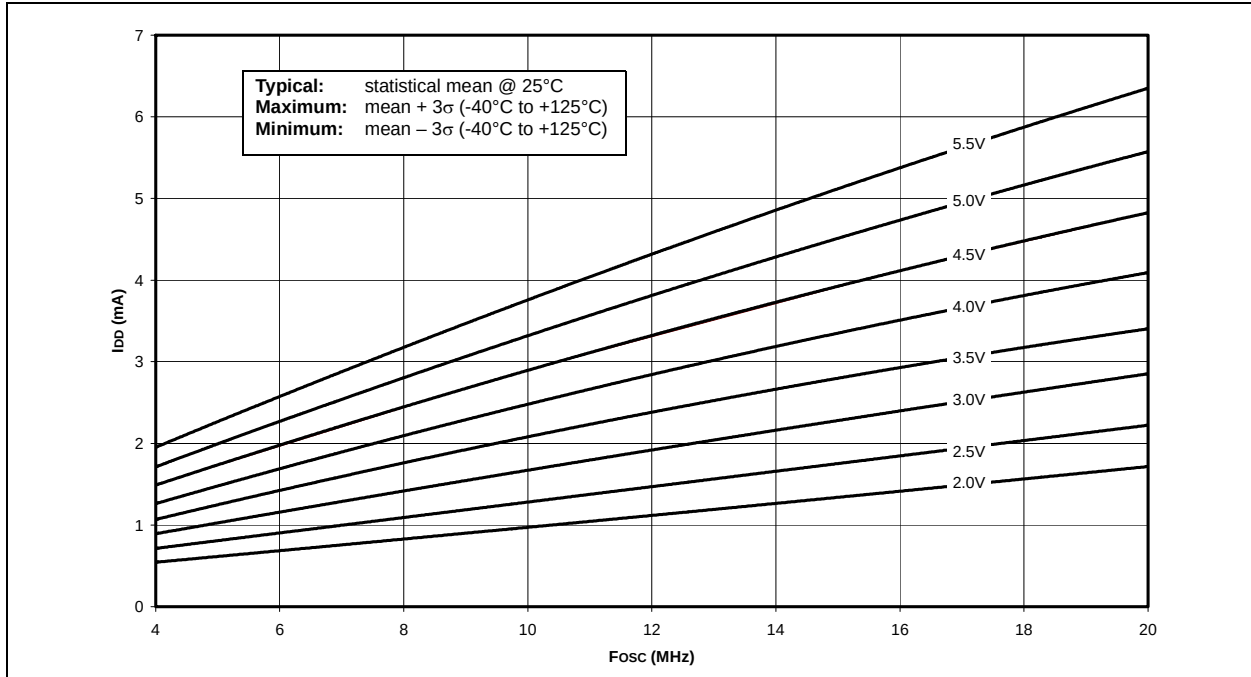
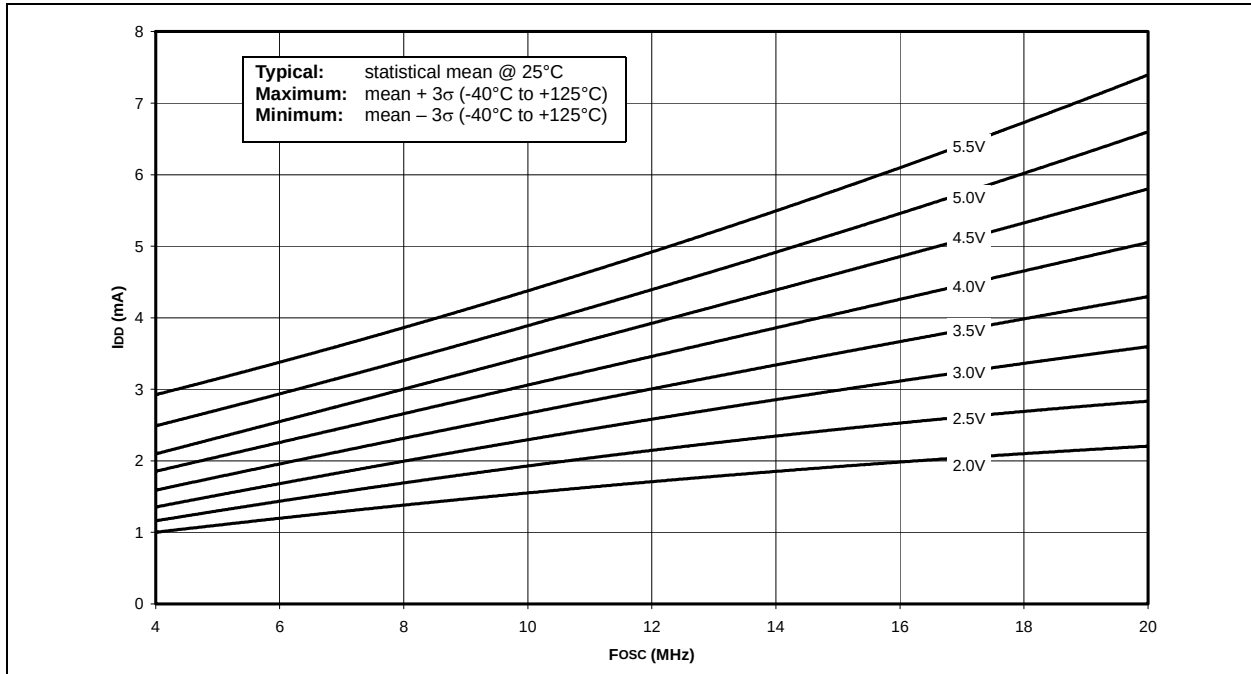


FIGURE 19-2: MAXIMUM I_{DD} vs. F_{OSC} OVER V_{DD} (HS MODE)



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FIGURE 19-3: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (XT MODE)

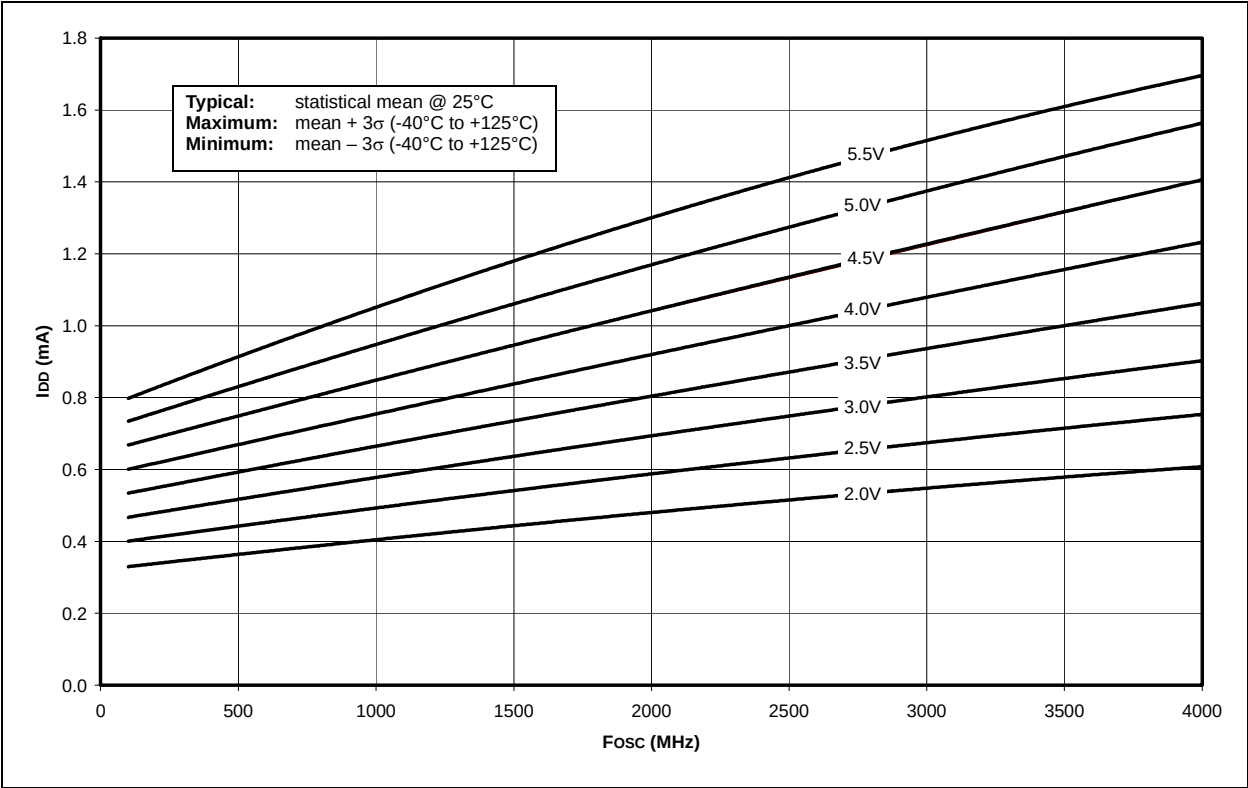


FIGURE 19-4: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (XT MODE)

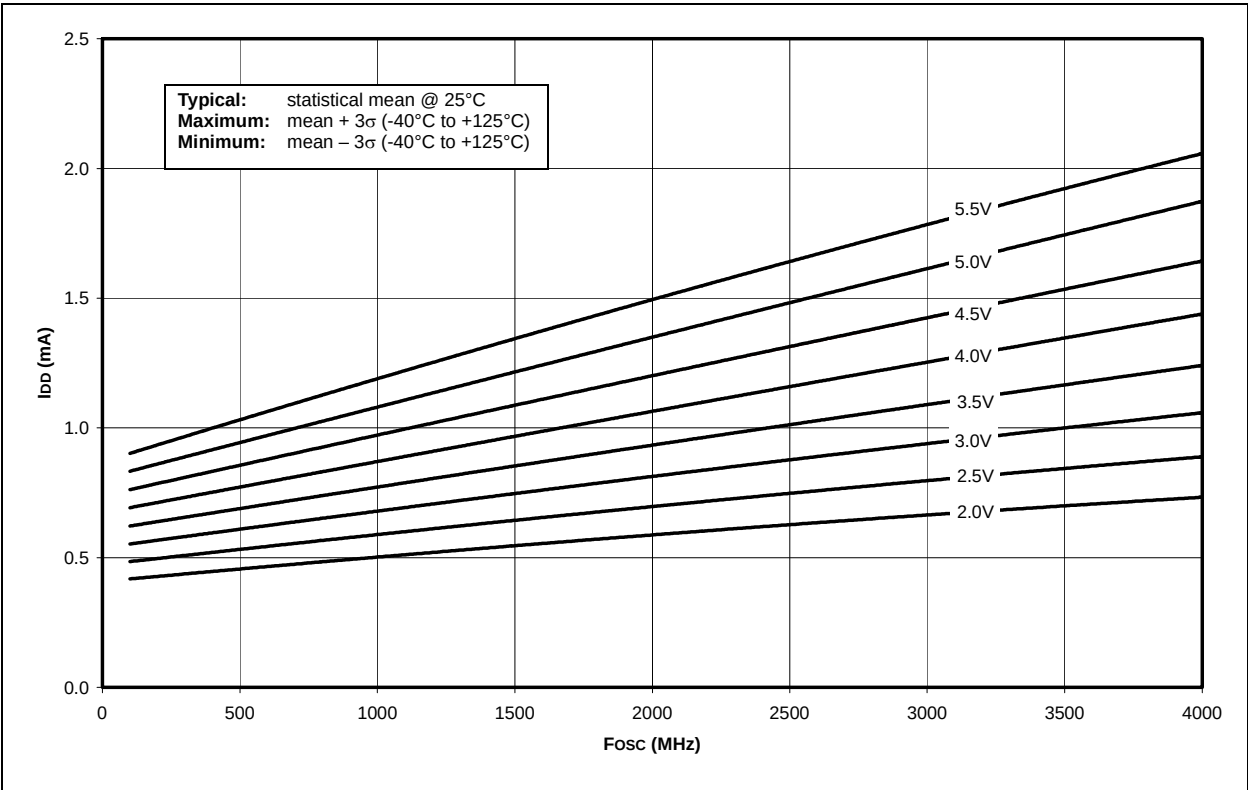


FIGURE 19-5: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (LP MODE)

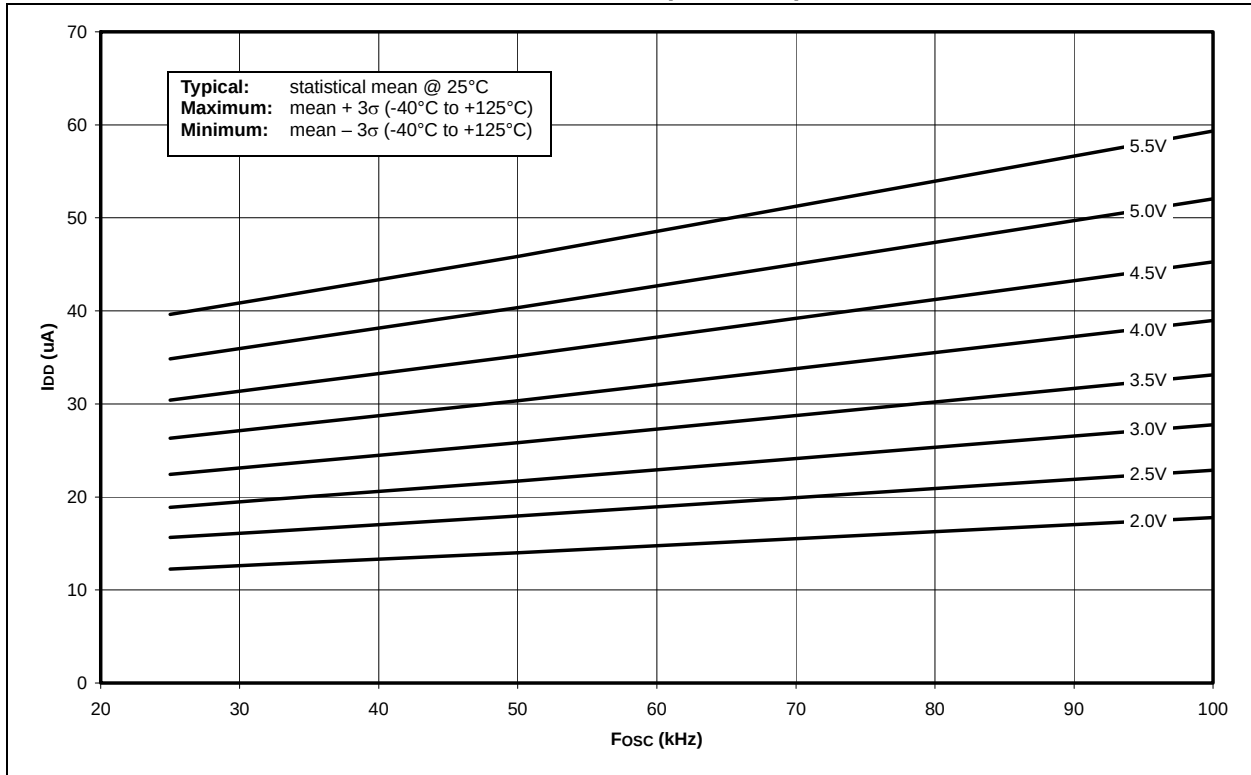
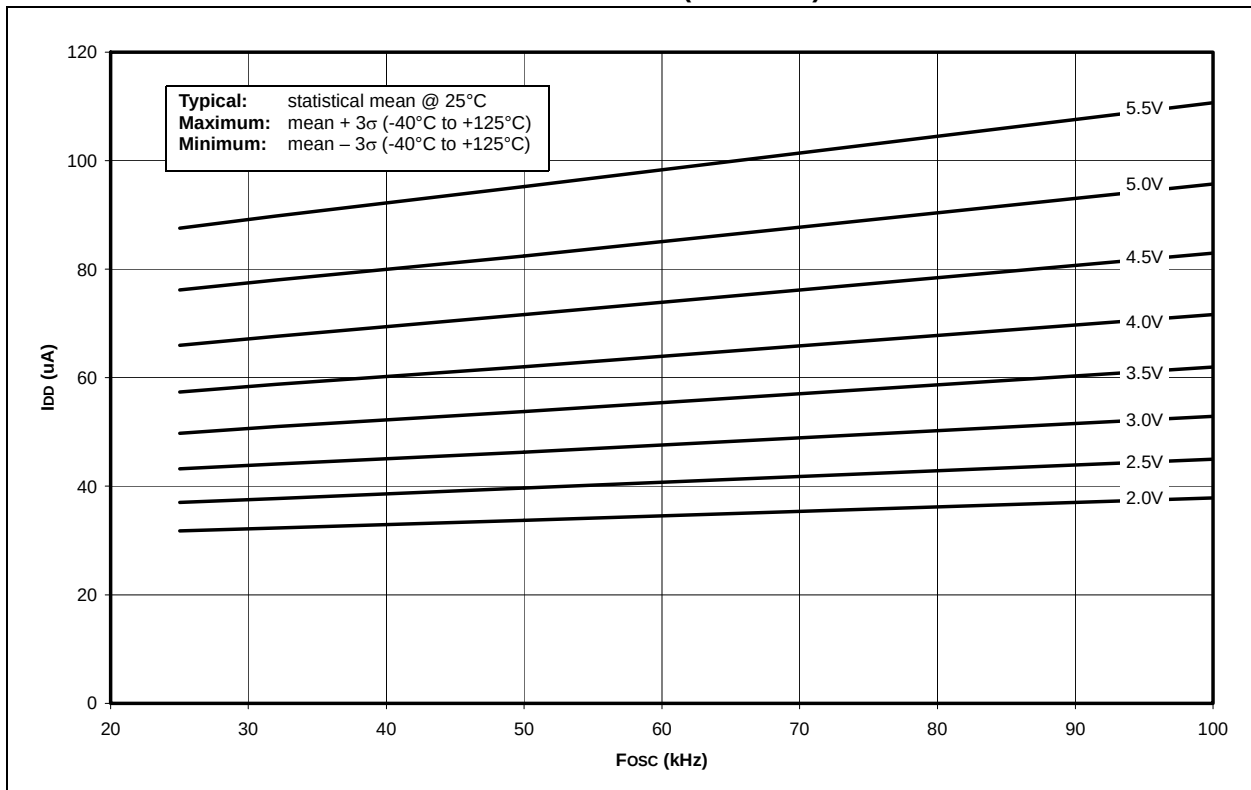


FIGURE 19-6: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (LP MODE)



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FIGURE 19-7: TYPICAL I_{DD} vs. V_{DD} , -40°C TO +125°C, 1 MHz TO 8 MHz (RC_RUN MODE, ALL PERIPHERALS DISABLED)

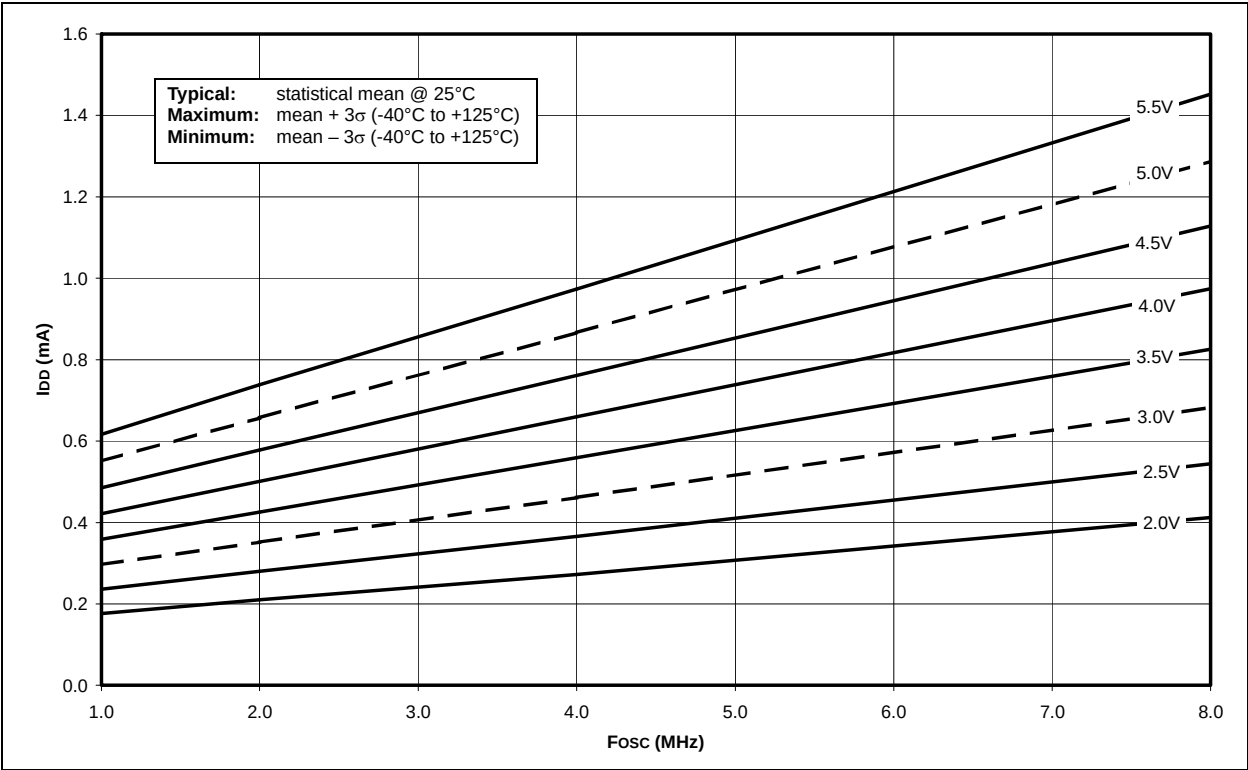


FIGURE 19-8: MAXIMUM I_{DD} vs. V_{DD} , -40°C TO +125°C, 1 MHz TO 8 MHz (RC_RUN MODE, ALL PERIPHERALS DISABLED)

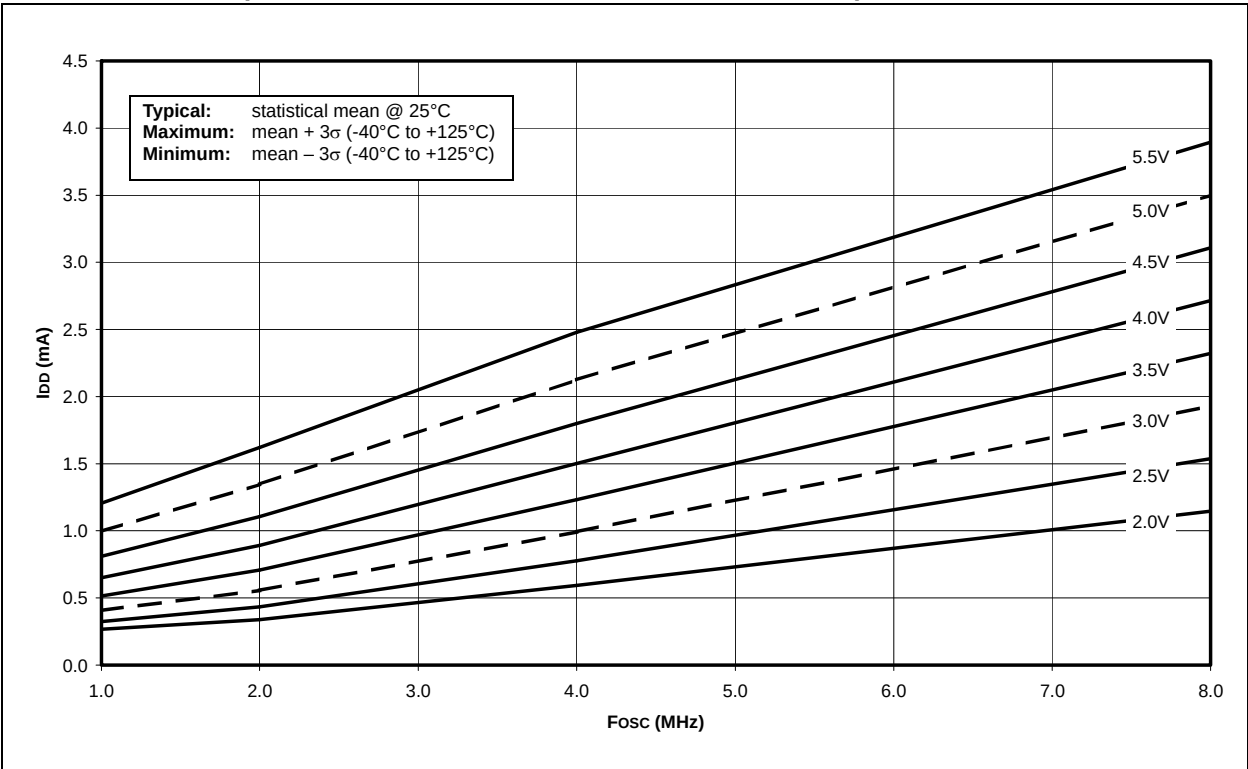


**FIGURE 19-9: I_{DD} vs. V_{DD} , SEC_RUN MODE, -10°C TO +125°C, 32.768 kHz
(XTAL 2 x 22 pF, ALL PERIPHERALS DISABLED)**

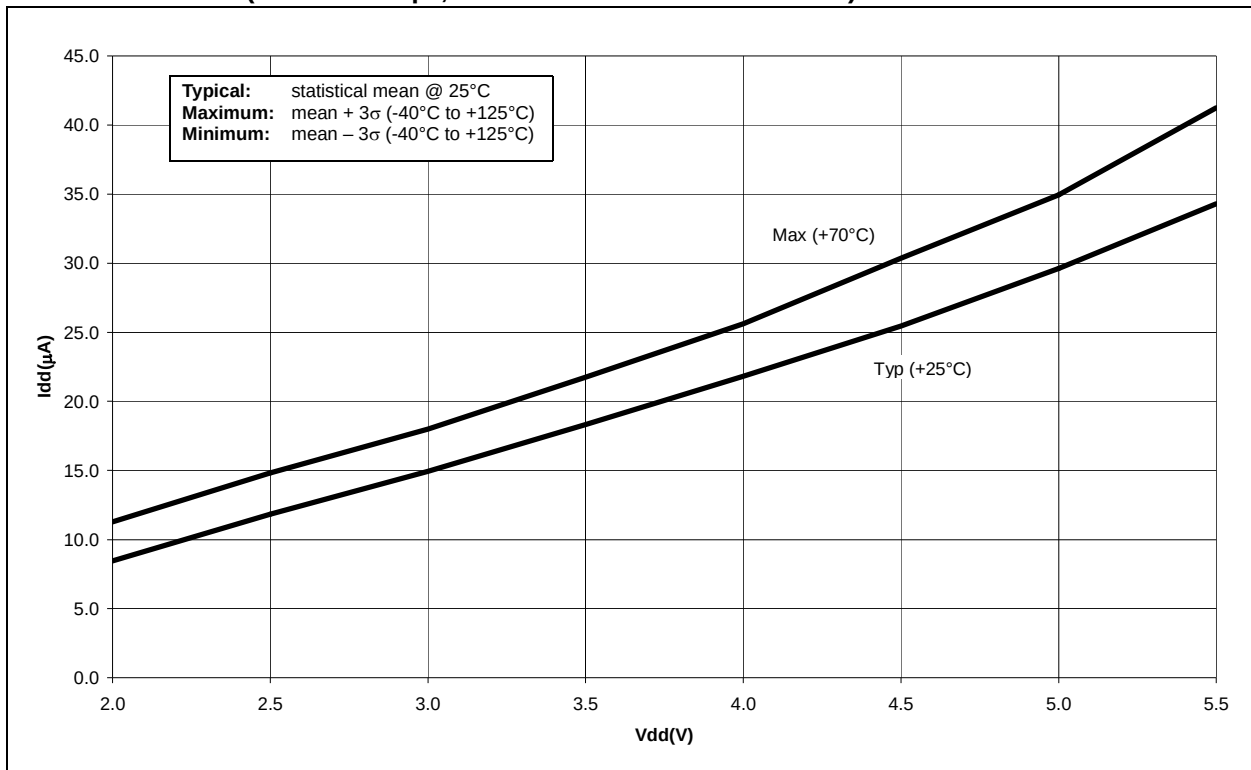
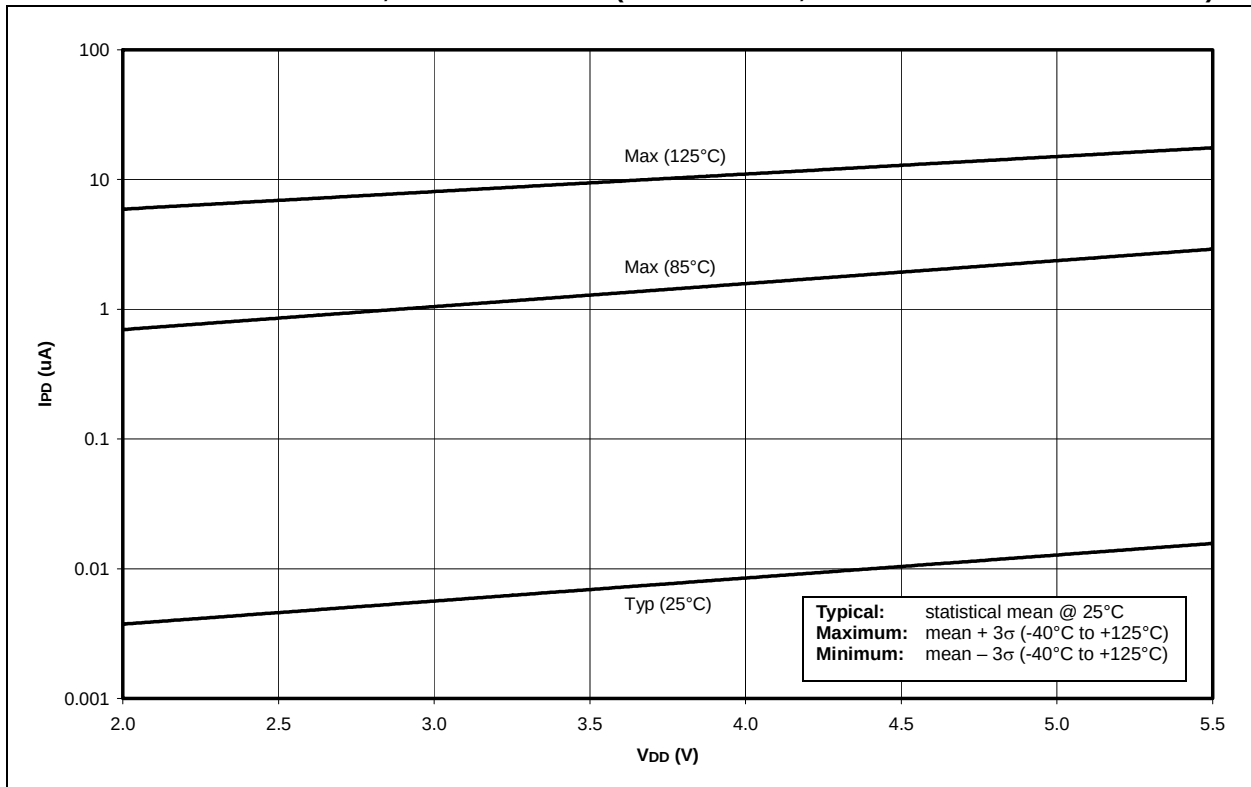


FIGURE 19-10: I_{PD} vs. V_{DD} , -40°C TO +125°C (SLEEP MODE, ALL PERIPHERALS DISABLED)



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FIGURE 19-11: AVERAGE F_{osc} vs. V_{DD} FOR VARIOUS VALUES OF R (RC MODE, $C = 20\text{ pF}$, $+25^\circ\text{C}$)

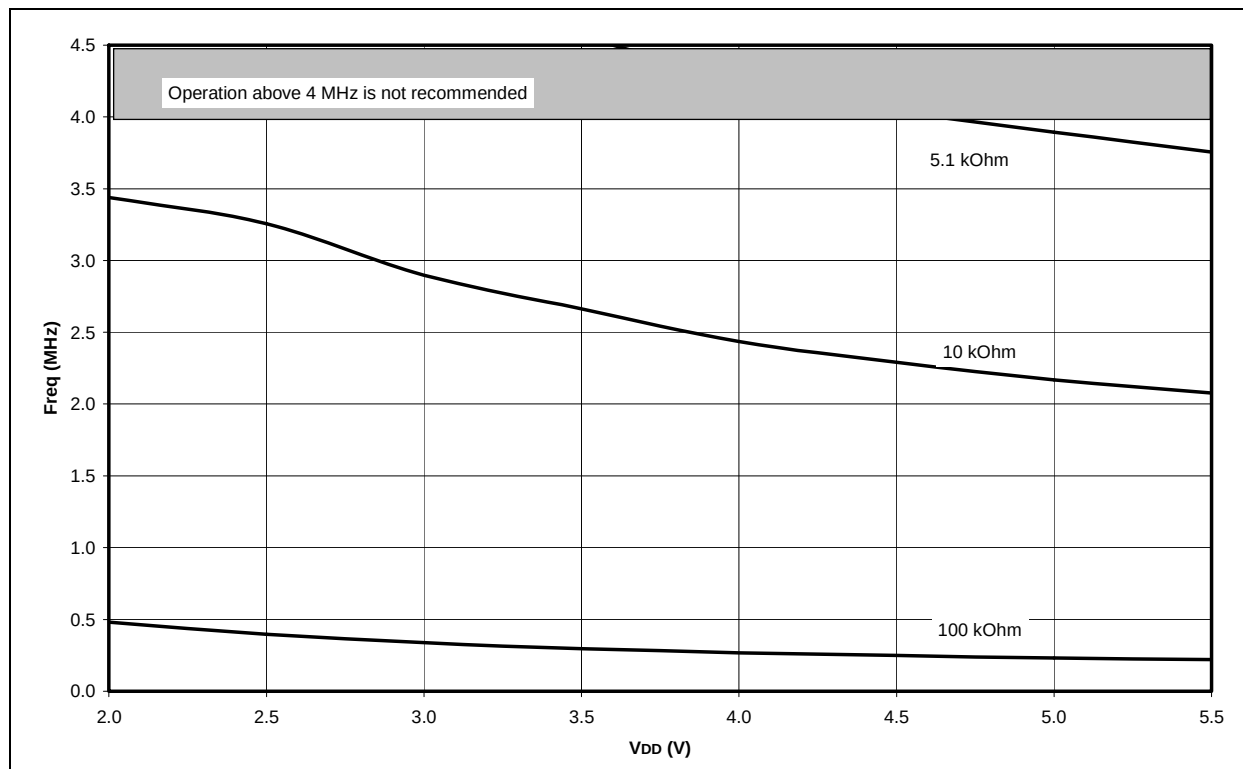


FIGURE 19-12: AVERAGE F_{osc} vs. V_{DD} FOR VARIOUS VALUES OF R (RC MODE, $C = 100\text{ pF}$, $+25^\circ\text{C}$)

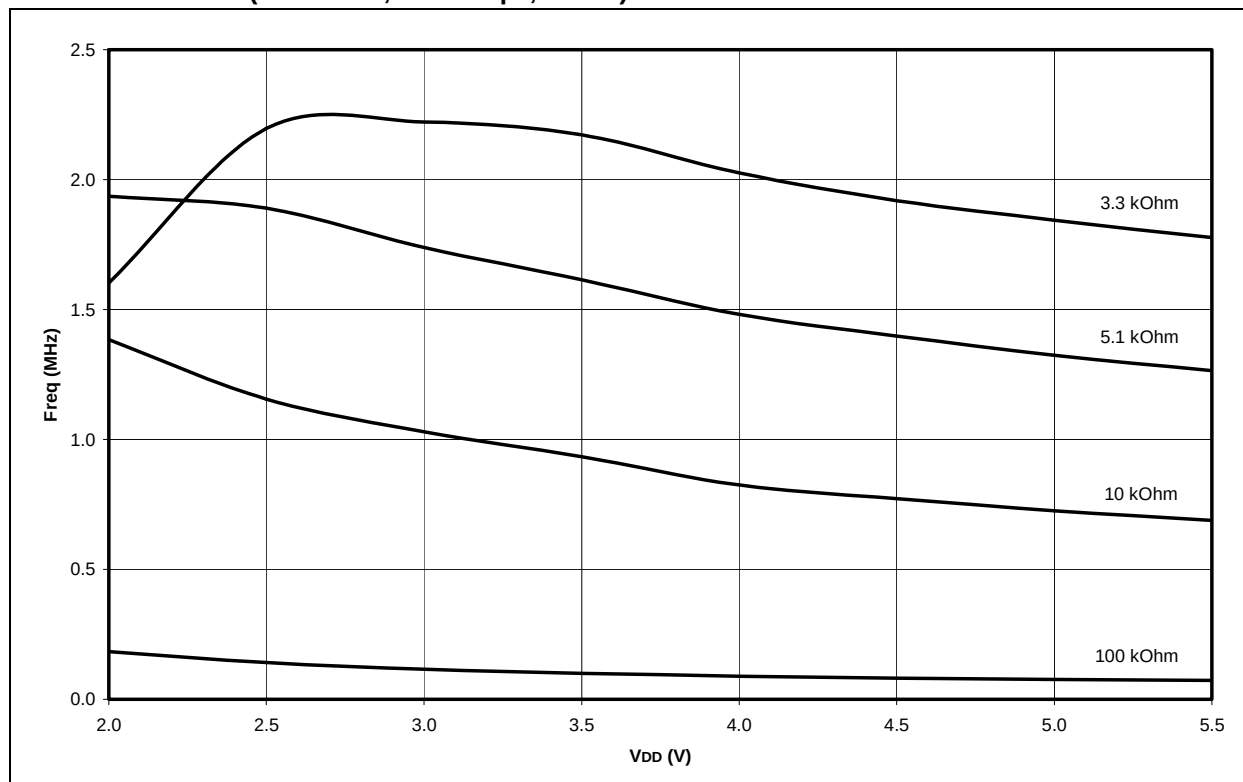


FIGURE 19-13: AVERAGE F_{osc} vs. V_{DD} FOR VARIOUS VALUES OF R
(RC MODE, C = 300 pF, +25°C)

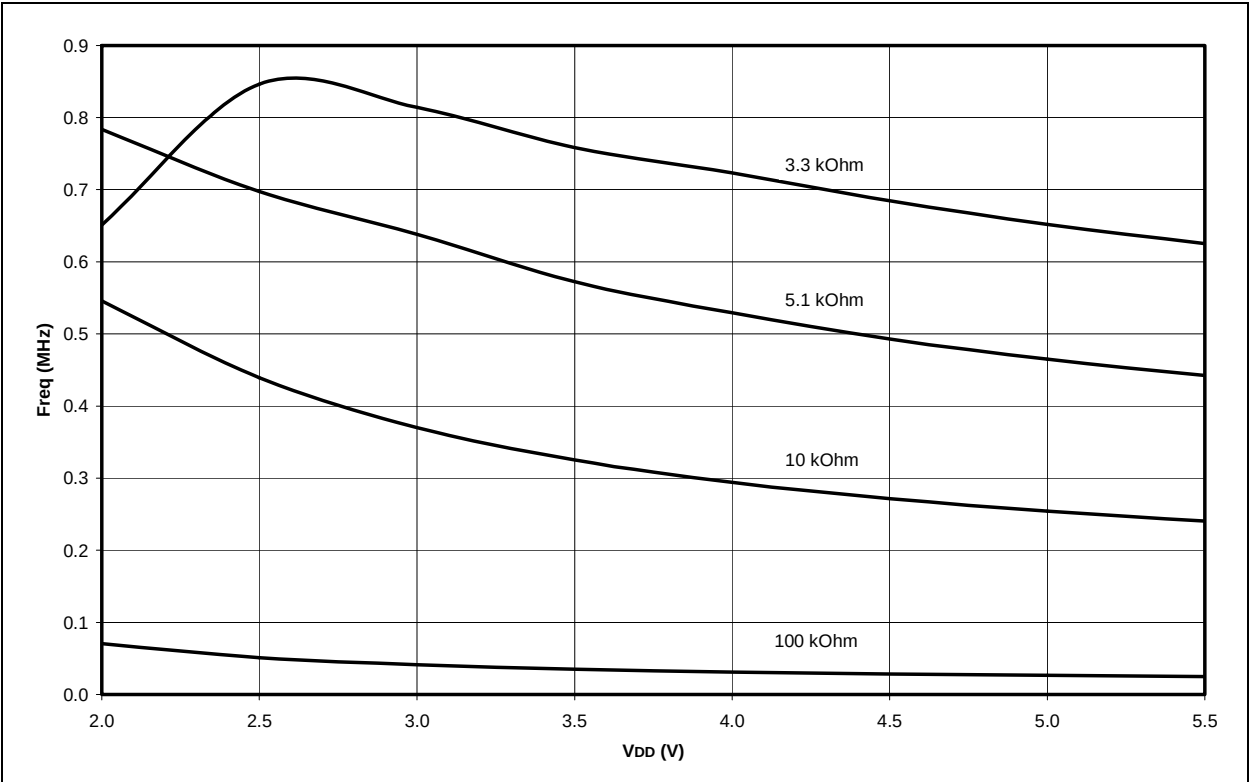
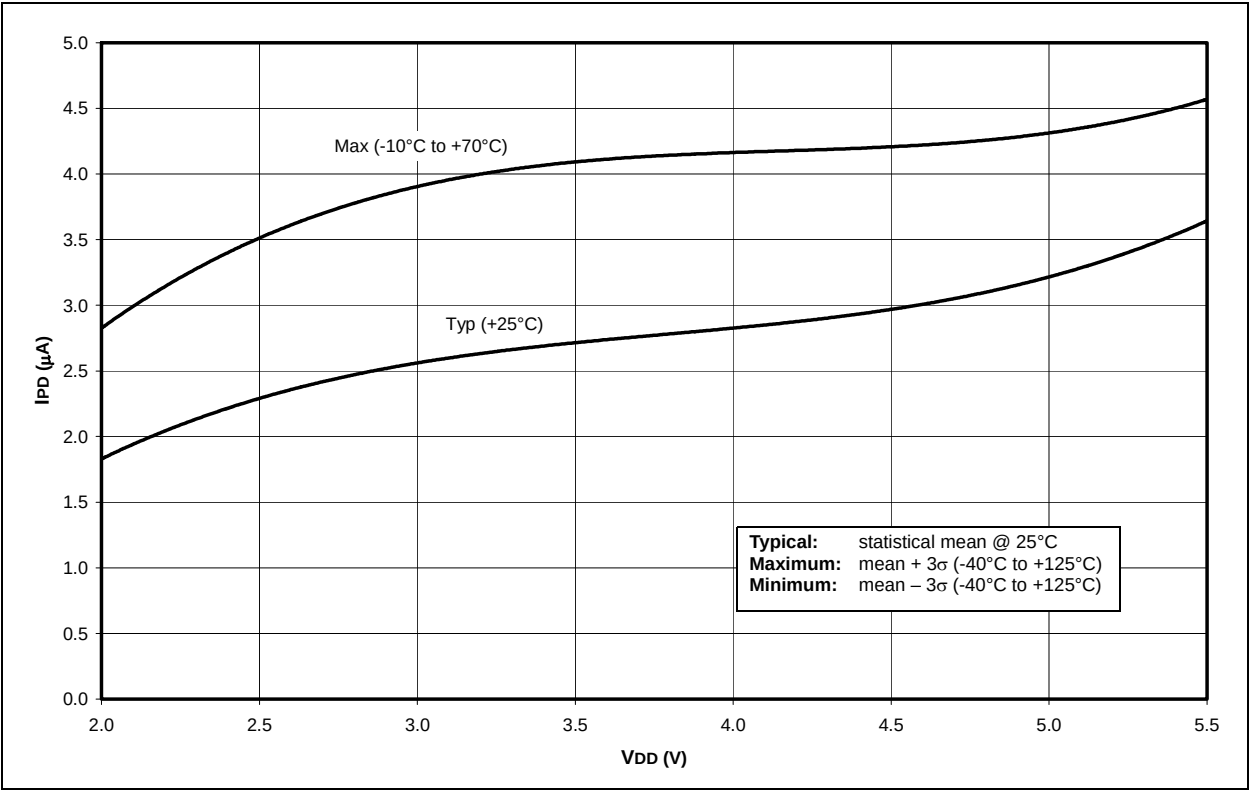


FIGURE 19-14: ΔI_{PD} TIMER1 OSCILLATOR, -10°C TO +70°C (SLEEP MODE, TMR1 COUNTER DISABLED)



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FIGURE 19-15: ΔI_{PD} WDT, -40°C TO +125°C (SLEEP MODE, ALL PERIPHERALS DISABLED)

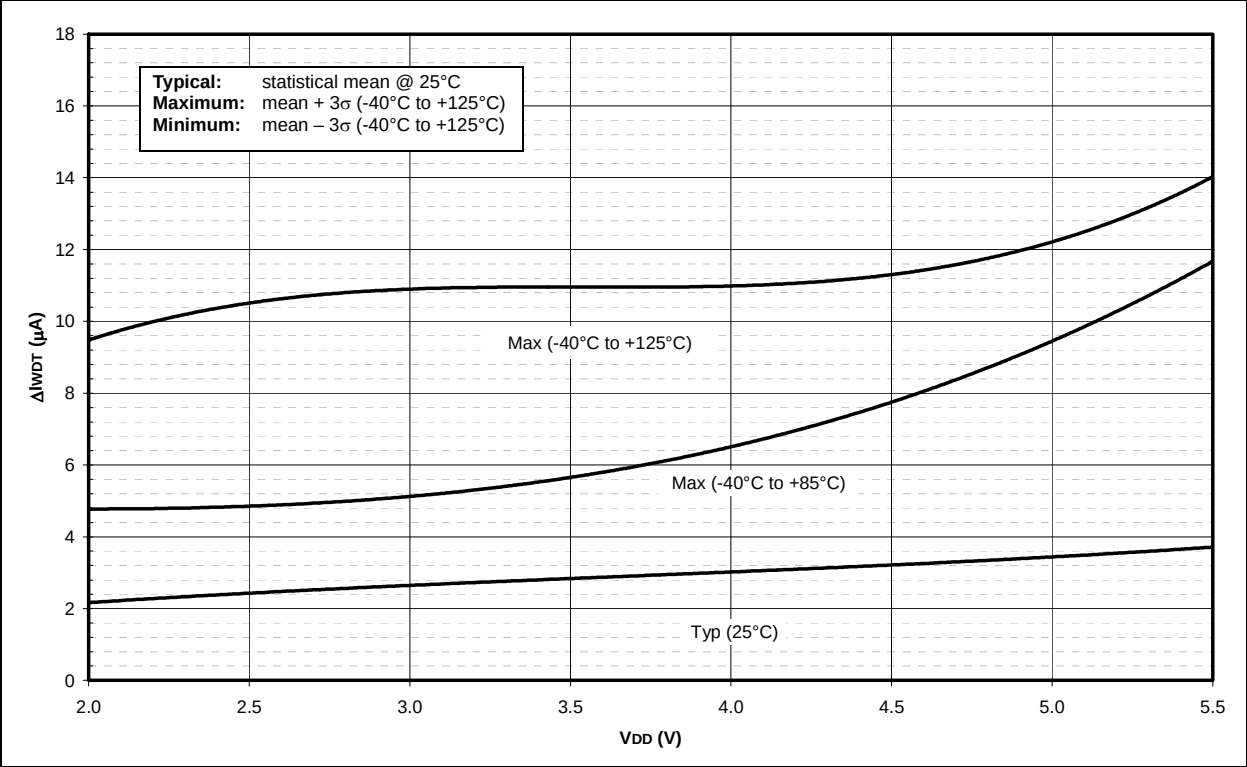


FIGURE 19-16: ΔI_{PD} BOR vs. V_{DD} , -40°C TO +125°C (SLEEP MODE, BOR ENABLED AT 2.00V-2.16V)

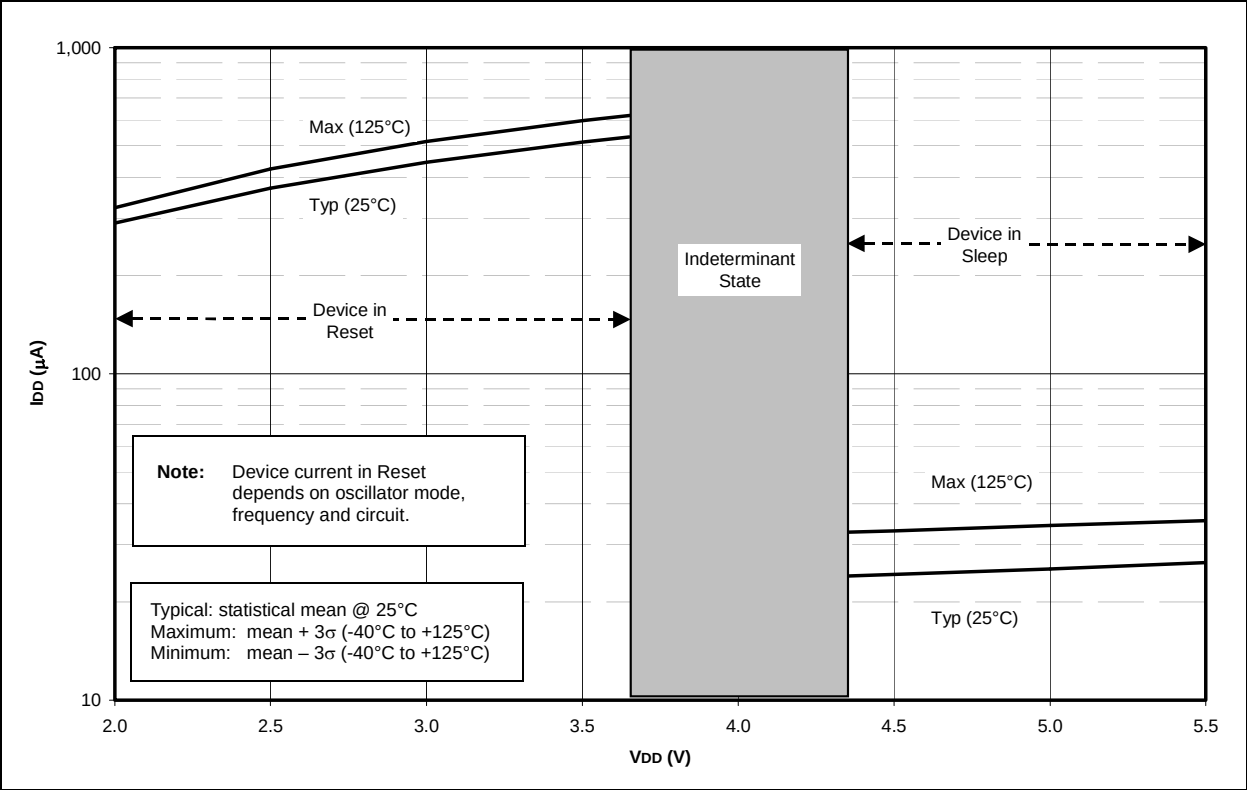


FIGURE 19-17: I_{PD} A/D, -40°C TO +125°C, SLEEP MODE, A/D ENABLED (NOT CONVERTING)

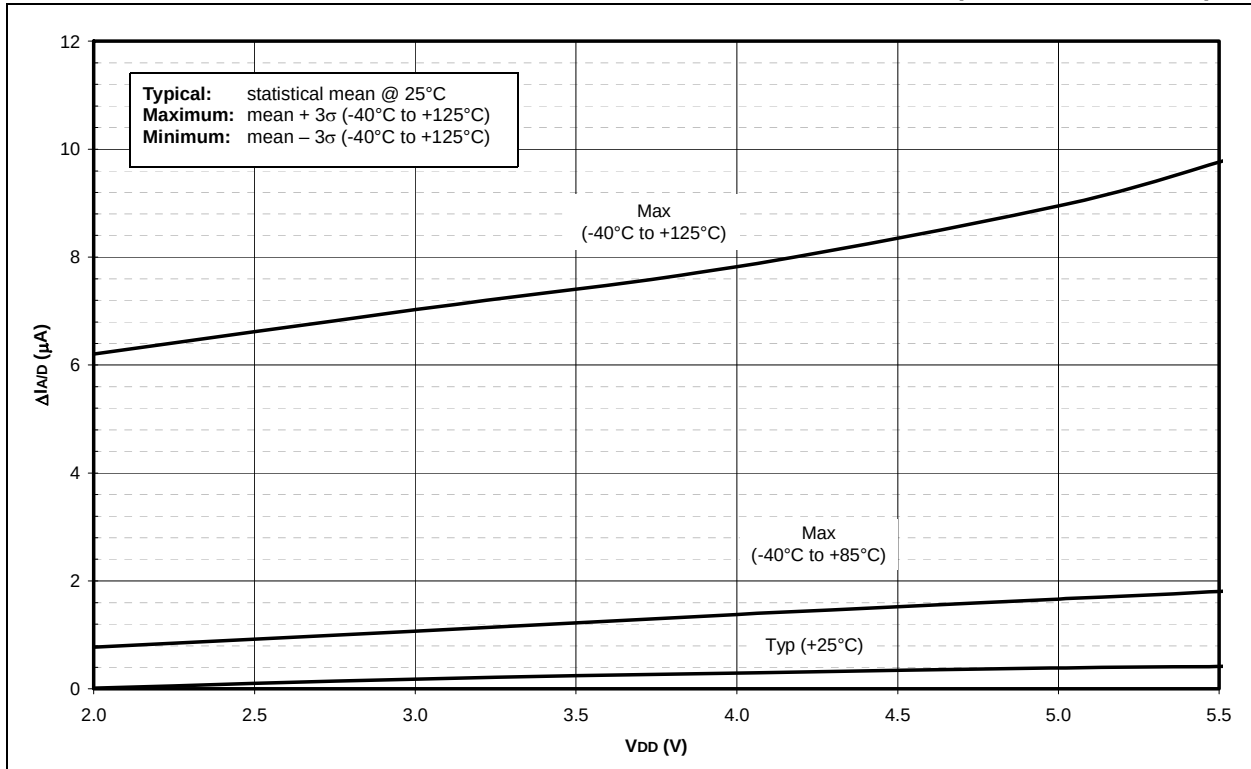
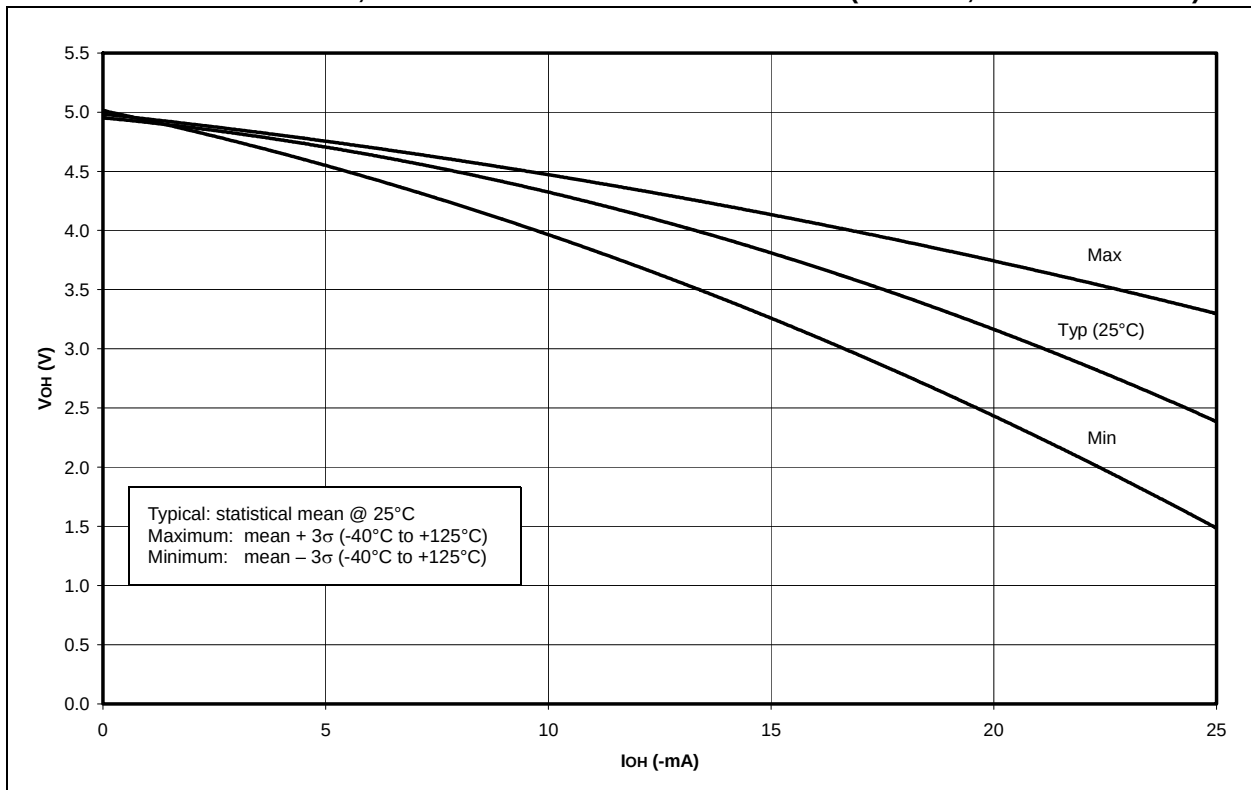


FIGURE 19-18: TYPICAL, MINIMUM AND MAXIMUM V_{OH} vs. I_{OH} ($V_{DD} = 5V$, -40°C TO +125°C)



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FIGURE 19-19: TYPICAL, MINIMUM AND MAXIMUM V_{OH} vs. I_{OH} ($V_{DD} = 3V$, $-40^{\circ}C$ TO $+125^{\circ}C$)

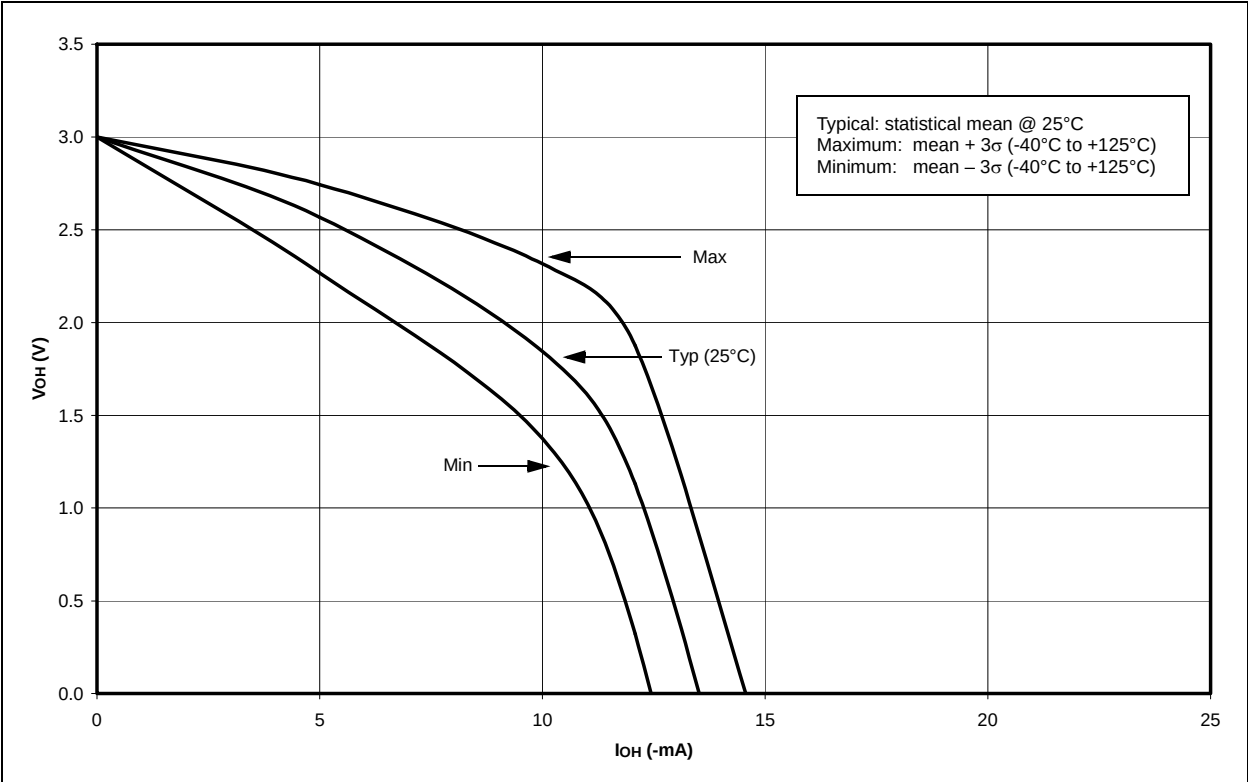


FIGURE 19-20: TYPICAL, MINIMUM AND MAXIMUM V_{OL} vs. I_{OL} ($V_{DD} = 5V$, $-40^{\circ}C$ TO $+125^{\circ}C$)

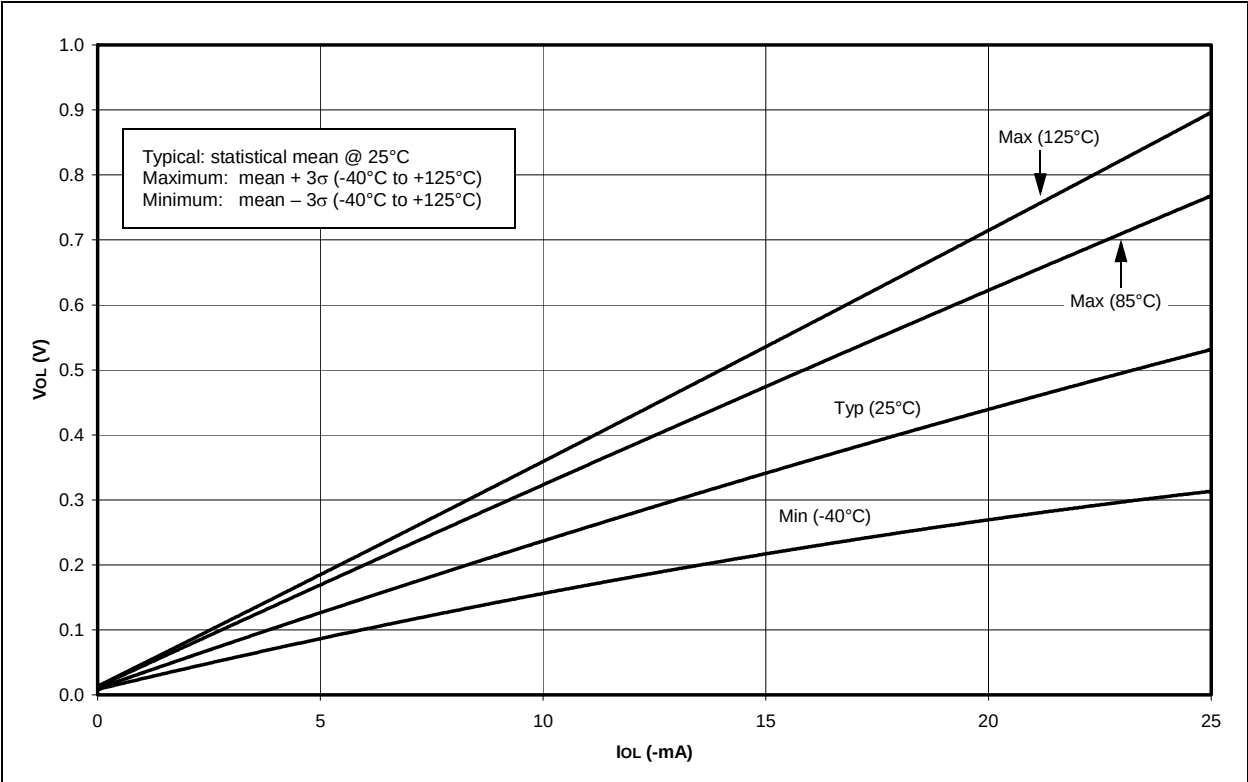


FIGURE 19-21: TYPICAL, MINIMUM AND MAXIMUM V_{OL} vs. I_{OL} ($V_{DD} = 3V$, $-40^{\circ}C$ TO $+125^{\circ}C$)

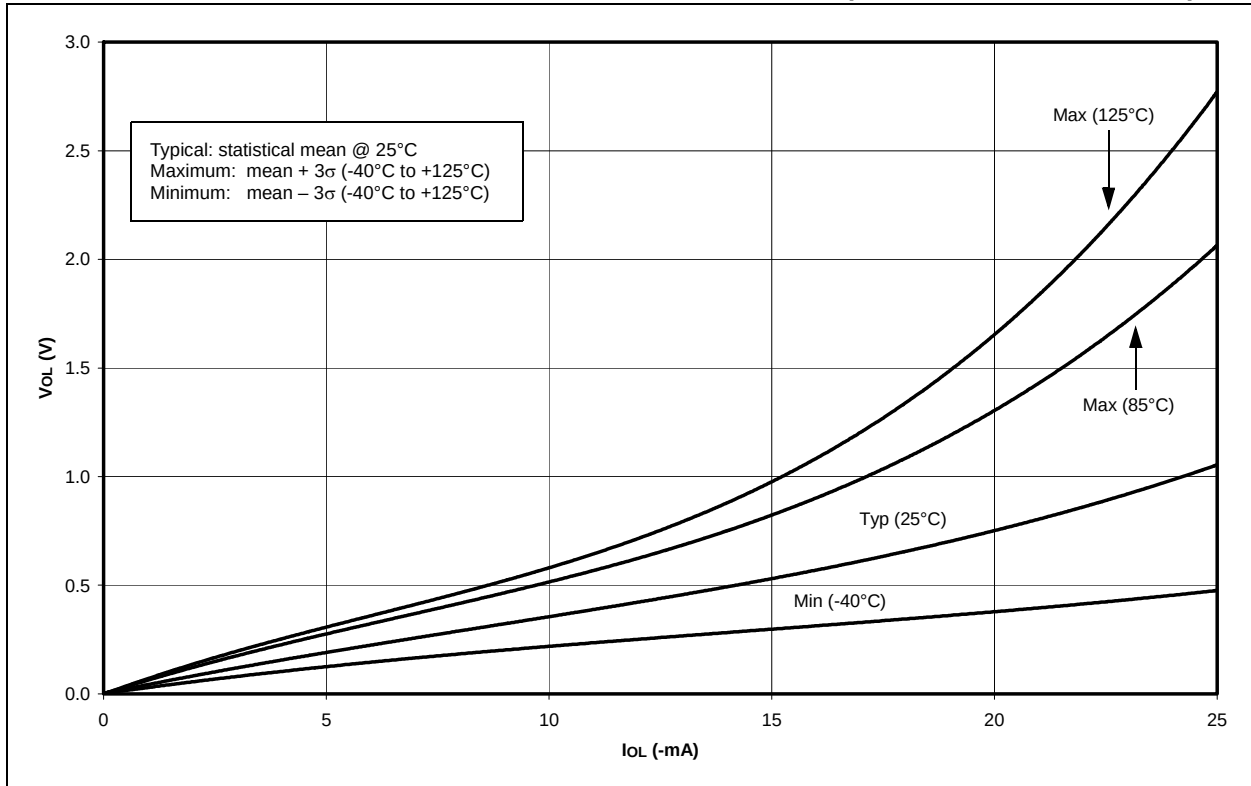
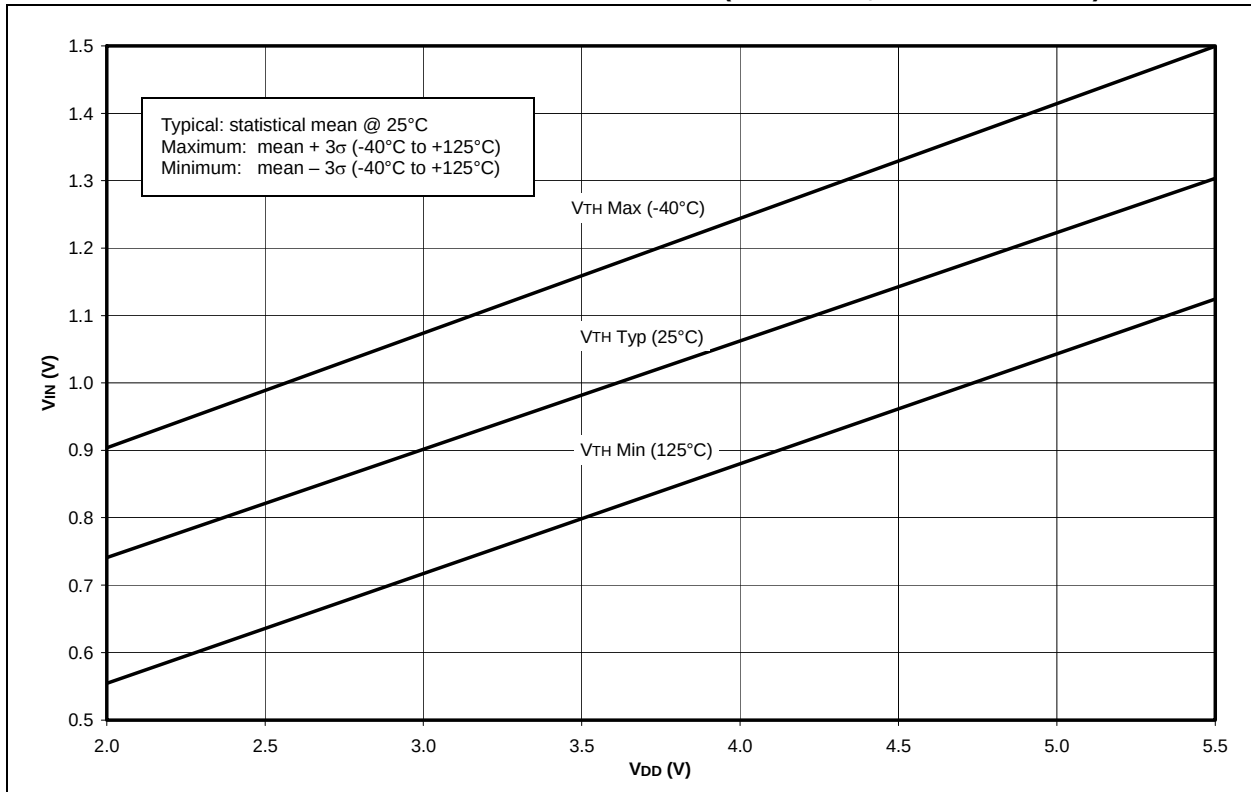


FIGURE 19-22: MINIMUM AND MAXIMUM V_{IN} vs. V_{DD} (TTL INPUT, $-40^{\circ}C$ TO $+125^{\circ}C$)



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FIGURE 19-23: MINIMUM AND MAXIMUM V_{IN} vs. V_{DD} (ST INPUT, -40°C TO $+125^{\circ}\text{C}$)

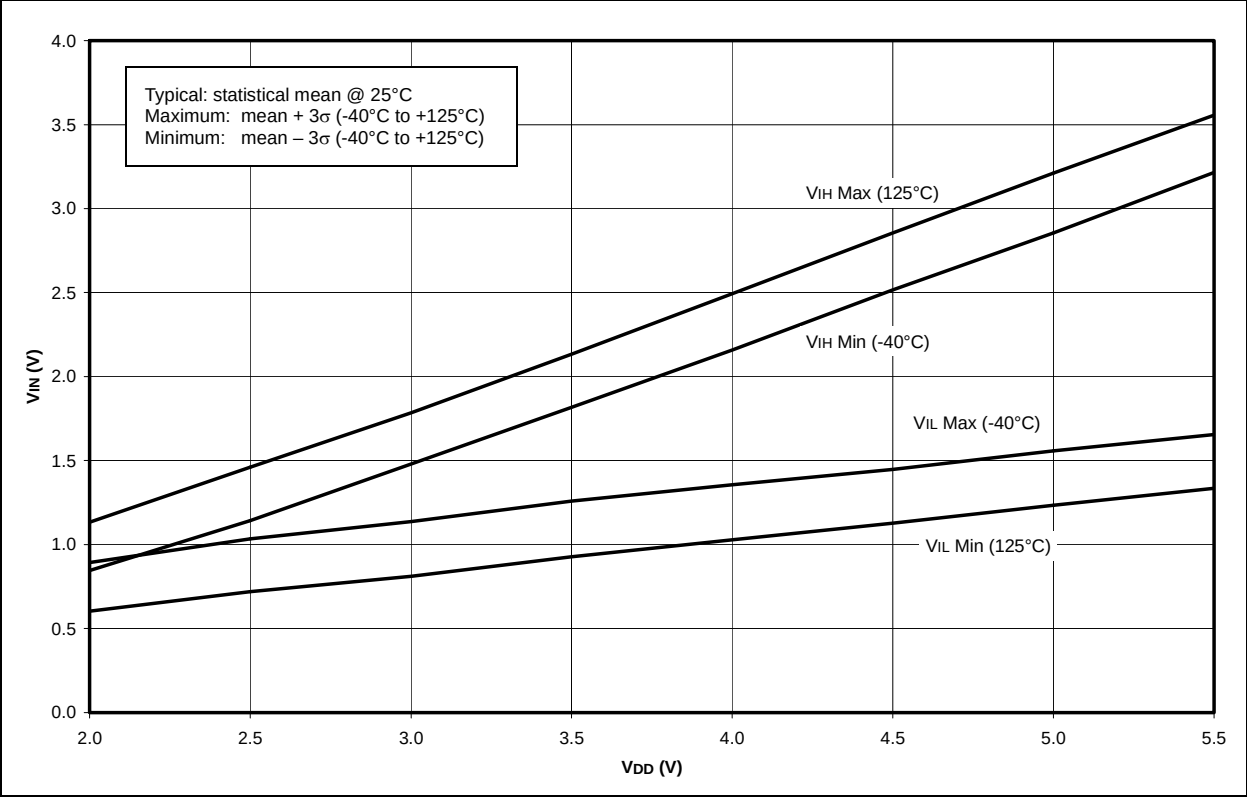


FIGURE 19-24: MINIMUM AND MAXIMUM V_{IN} vs. V_{DD} (I^2C^{TM} INPUT, -40°C TO $+125^{\circ}\text{C}$)

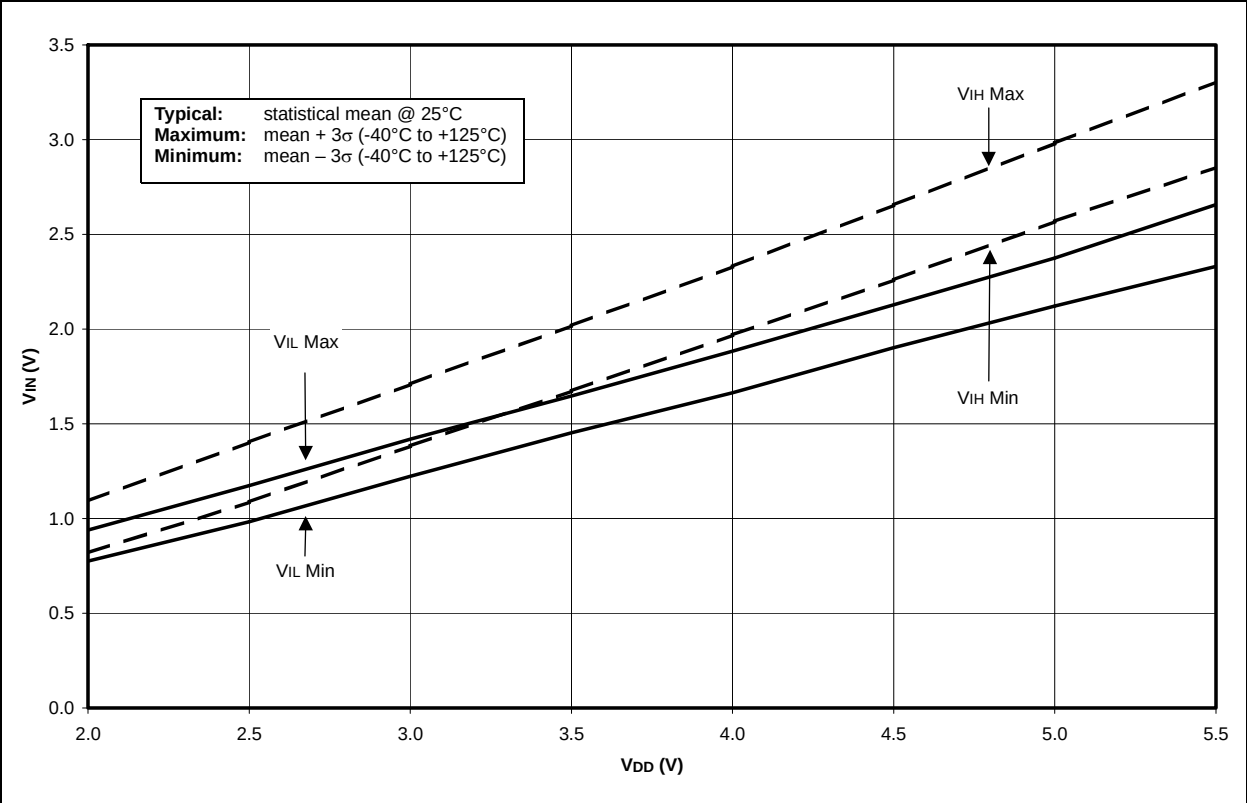


FIGURE 19-25: A/D NONLINEARITY vs. VREFH (VDD = VREFH, -40°C TO +125°C)

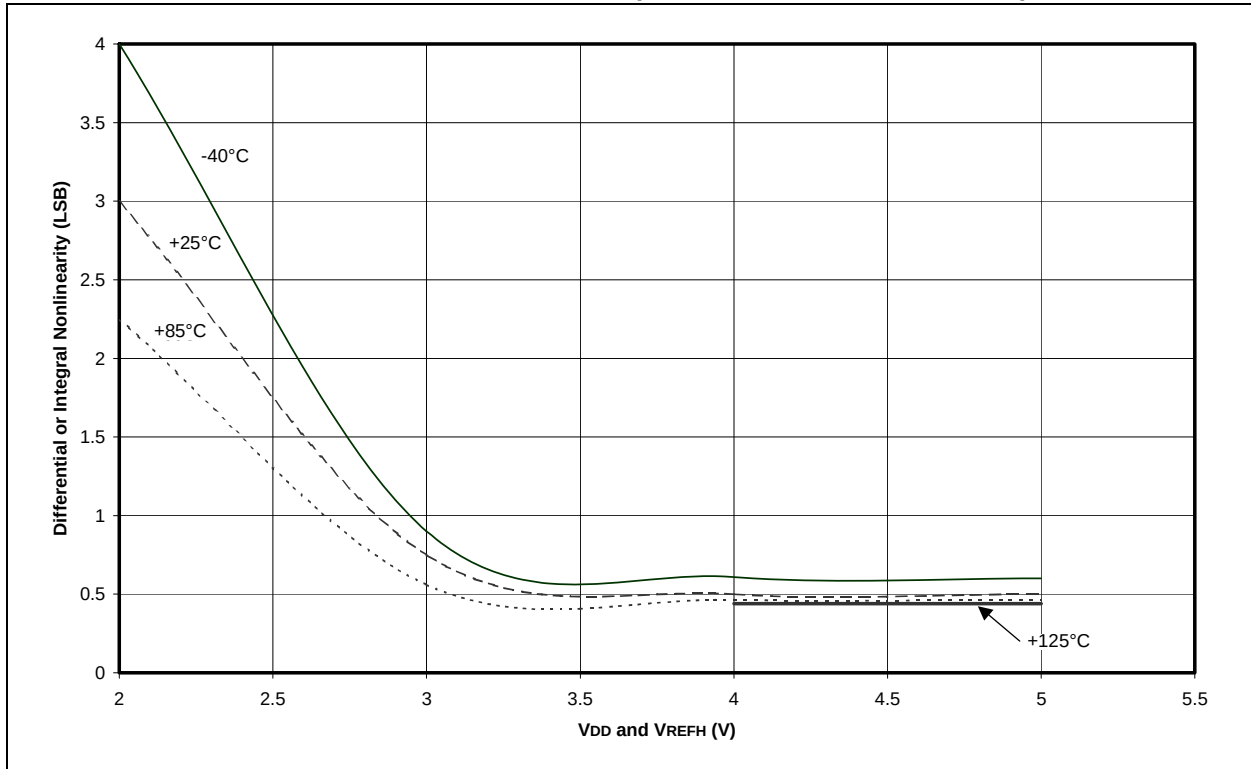
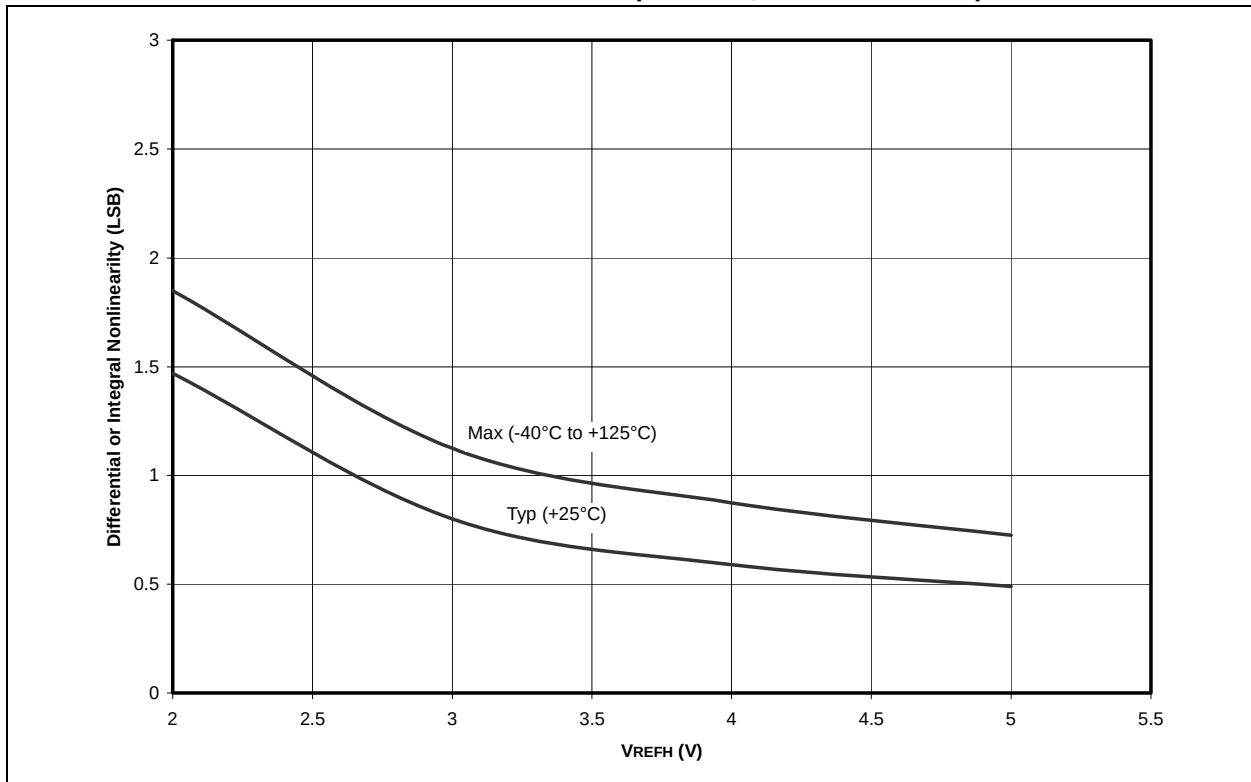


FIGURE 19-26: A/D NONLINEARITY vs. VREFH (VDD = 5V, -40°C TO +125°C)



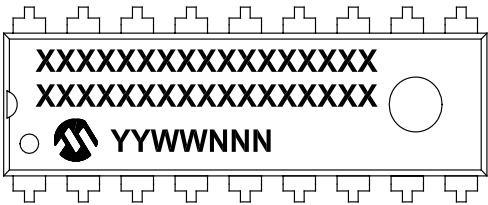
PIC16F87/88

NOTES:

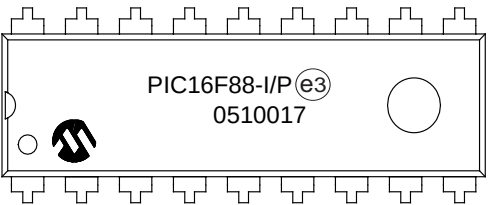
20.0 PACKAGING INFORMATION

20.1 Package Marking Information

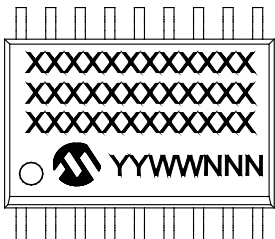
18-Lead PDIP (300 mil)



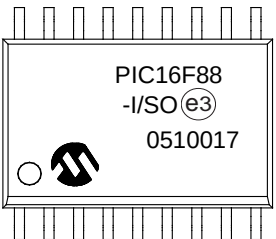
Example



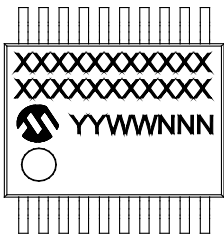
18-Lead SOIC (7.50 mm)



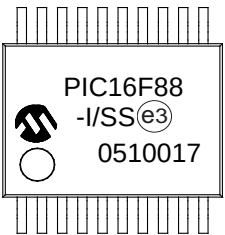
Example



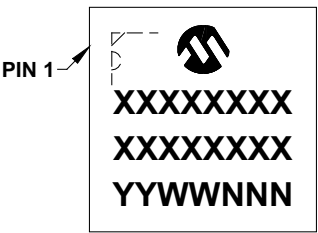
20-Lead SSOP (5.30 mm)



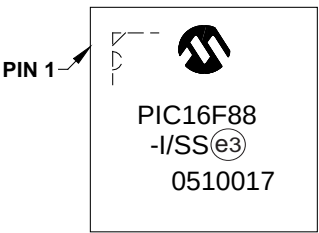
Example



28-Lead QFN (6x6 mm)



Example



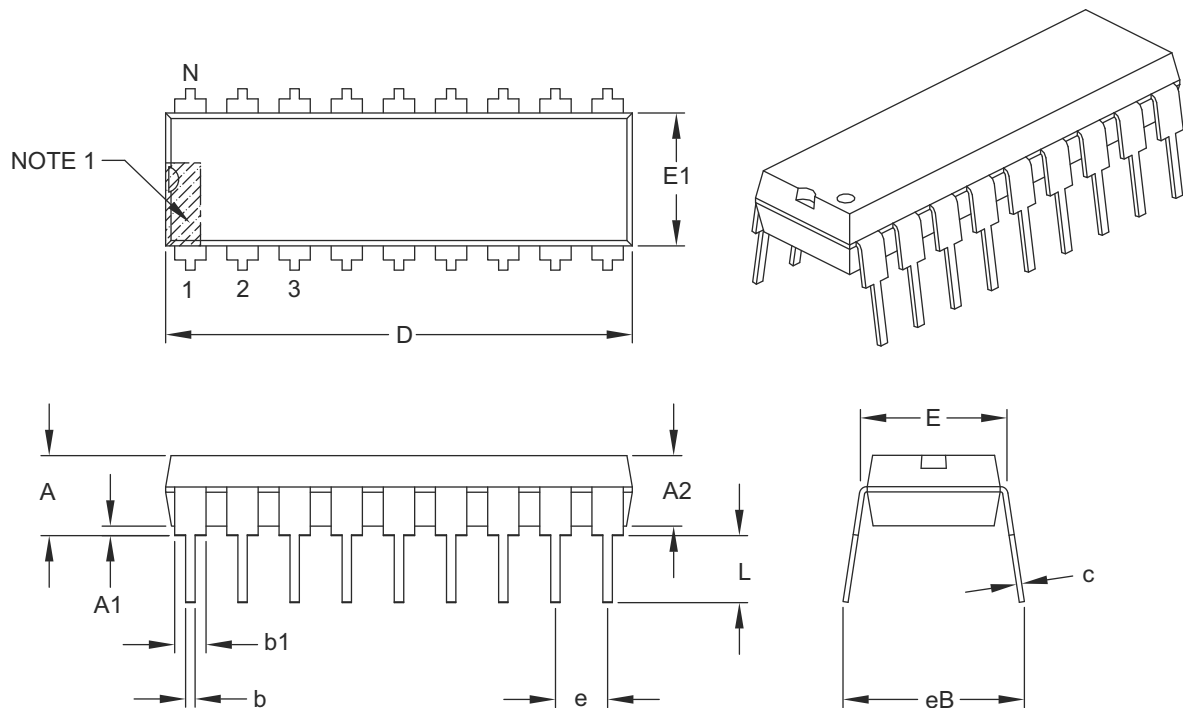
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	e3/	Week code (week of January 1 is week '01')
	NNNN	Alphanumeric traceability code
		Pb-free JEDEC designator for Matte Tin (Sn) e3
	*	This package is Pb-free. The Pb-free JEDEC designator () can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

PIC16F87/88

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



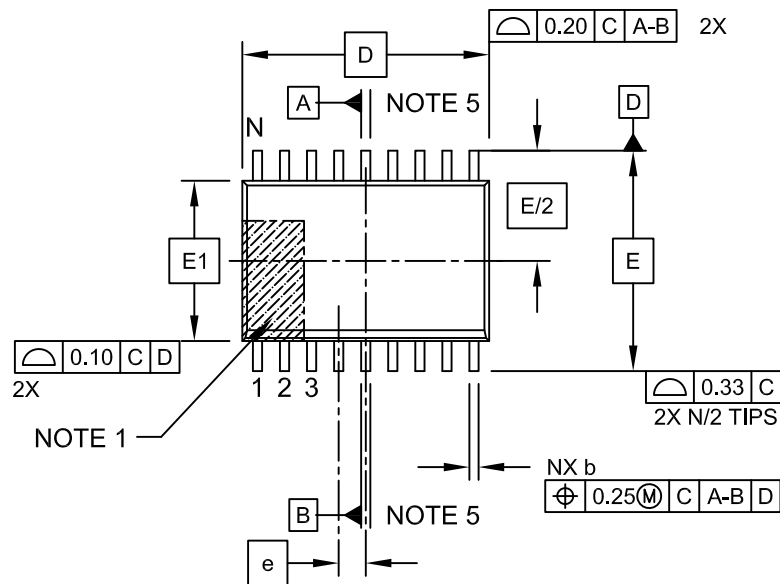
Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	18		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.880	.900	.920
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.014
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

- Notes:**
- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
 - 2. § Significant Characteristic.
 - 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
 - 4. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

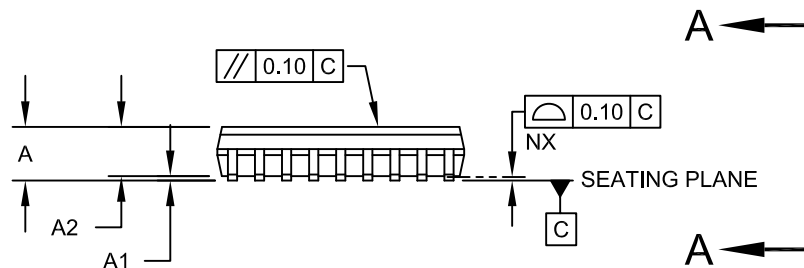
Microchip Technology Drawing C04-007B

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

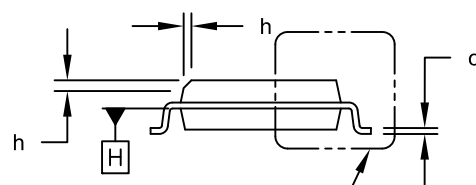
Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



TOP VIEW



SIDE VIEW

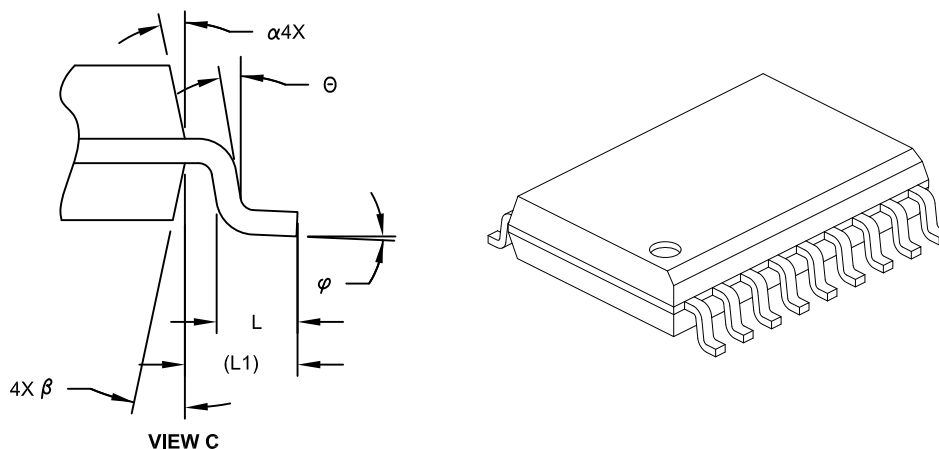


VIEW A-A

PIC16F87/88

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	18		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	2.65
Molded Package Thickness	A2	2.05	-	-
Standoff §	A1	0.10	-	0.30
Overall Width	E	10.30 BSC		
Molded Package Width	E1	7.50 BSC		
Overall Length	D	11.55 BSC		
Chamfer (Optional)	h	0.25	-	0.75
Foot Length	L	0.40	-	1.27
Footprint	L1	1.40 REF		
Lead Angle	θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.20	-	0.33
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

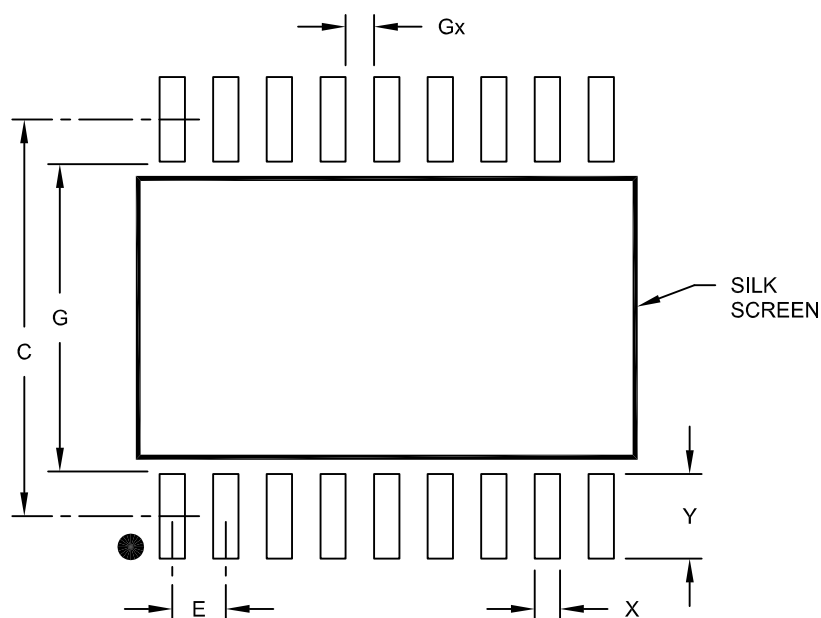
Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic
- Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
 - REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-051C Sheet 2 of 2

18-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		9.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

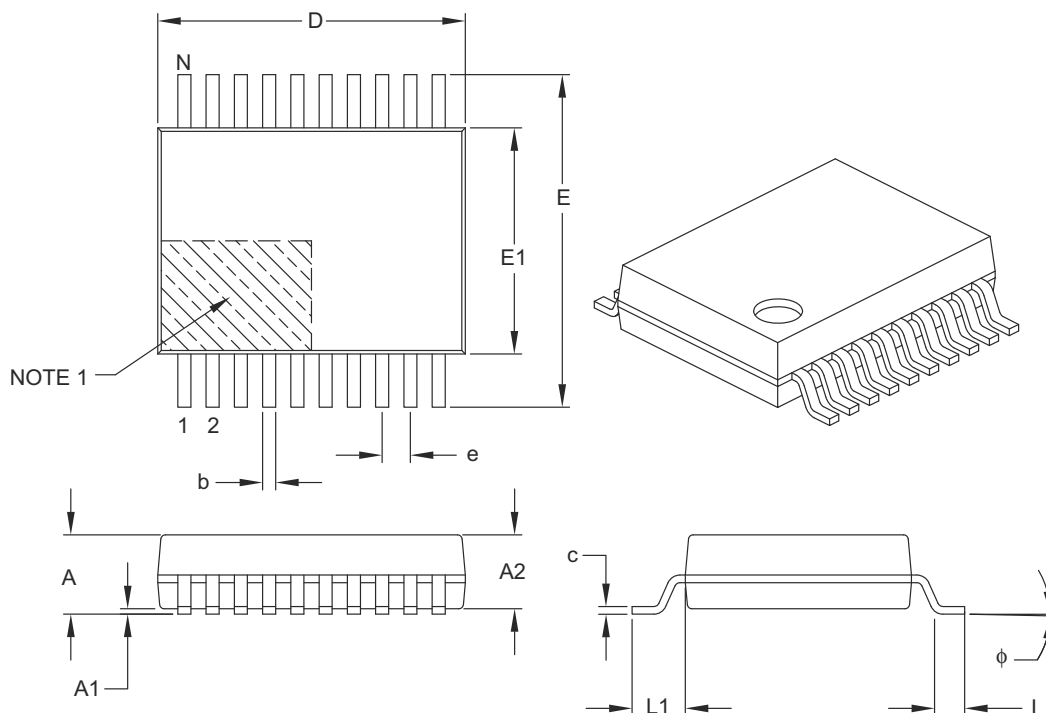
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2051A

PIC16F87/88

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	6.90	7.20	7.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

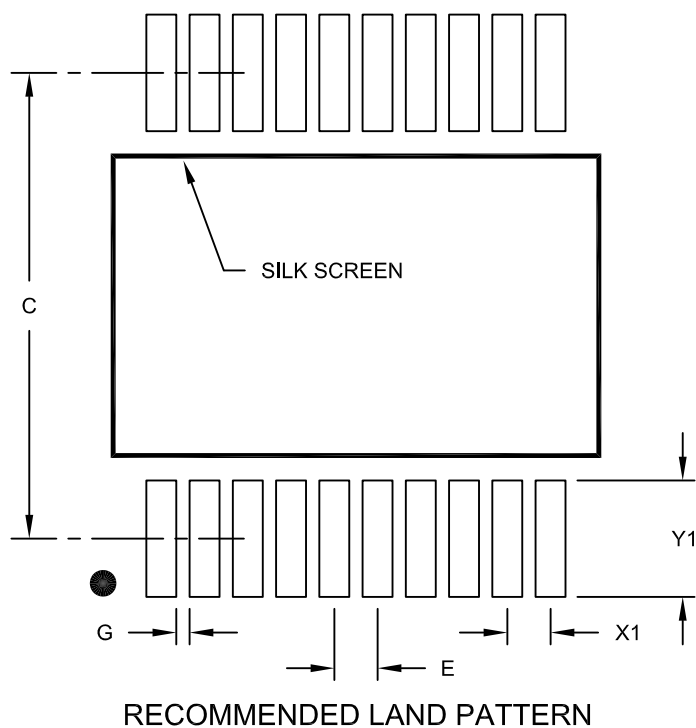
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

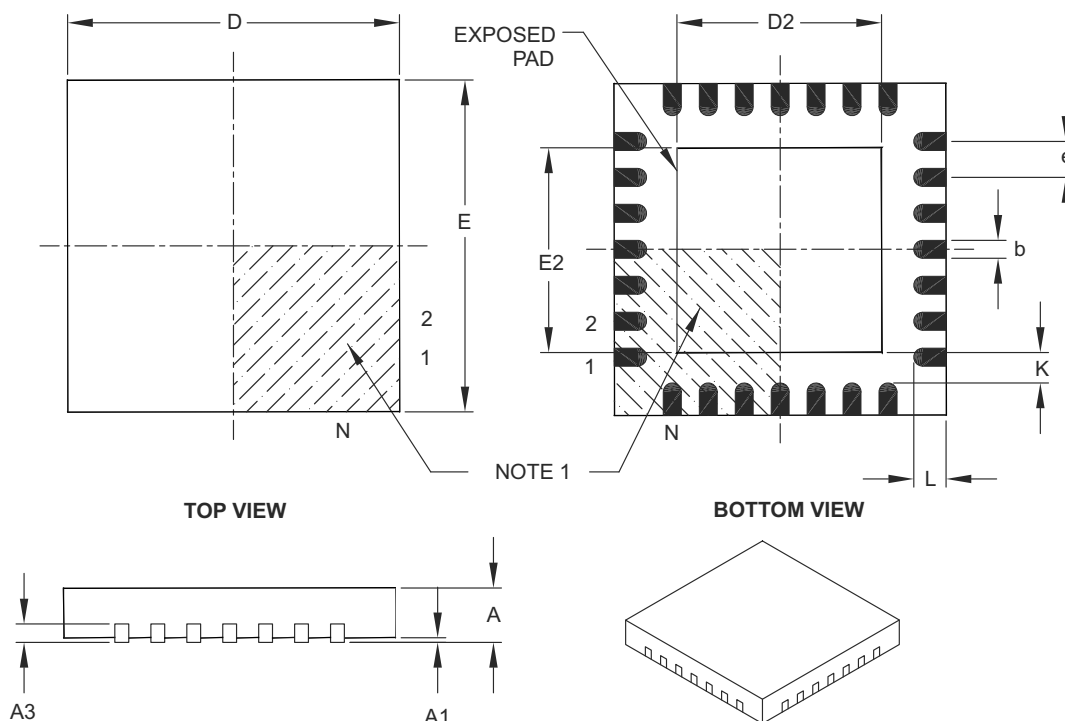
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

PIC16F87/88

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	6.00 BSC		
Exposed Pad Width	E2	3.65	3.70	4.20
Overall Length	D	6.00 BSC		
Exposed Pad Length	D2	3.65	3.70	4.20
Contact Width	b	0.23	0.30	0.35
Contact Length	L	0.50	0.55	0.70
Contact-to-Exposed Pad	K	0.20	—	—

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.

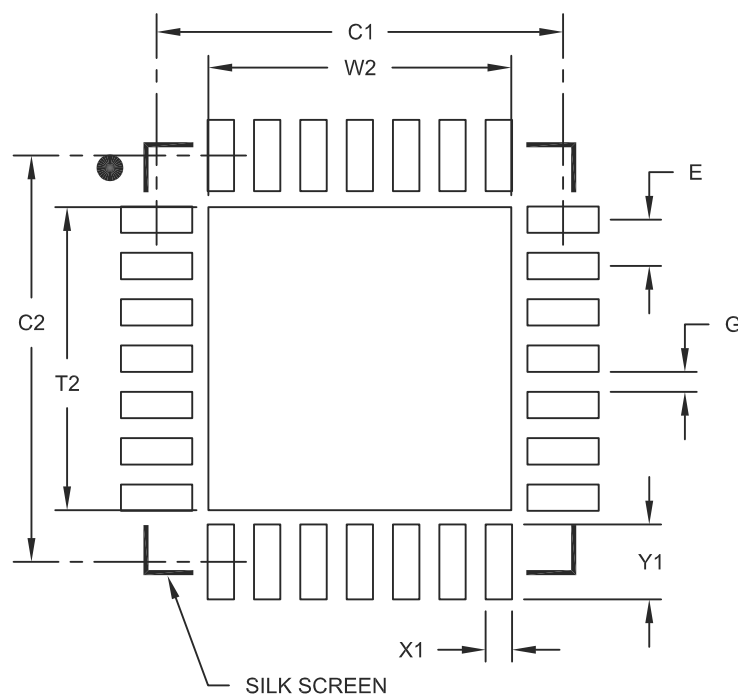
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

PIC16F87/88

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (November 2003)

Original data sheet for PIC16F87/88 devices.

Revision B (August 2003)

The specifications in **Section 18.0 “Electrical Characteristics”** have been updated to include the addition of maximum specifications to the DC Characteristics tables, text clarification has been made to **Section 4.6.2 “Clock Switching”** and there have been minor updates to the data sheet text.

Revision C (January 2005)

This revision includes the DC and AC Characteristics Graphs and Tables. The Electrical Specifications in **Section 18.0 “Electrical Characteristics”** have been updated and there have been minor corrections to the data sheet text.

Revision D (October 2011)

This revision updated the package marking and package outline drawings in **Section 20.0 “Packaging Information”**.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices in this data sheet are listed in Table B-1.

TABLE B-1: DIFFERENCES BETWEEN THE PIC16F87 AND PIC16F88

Features	PIC16F87	PIC16F88
Analog-to-Digital Converter	N/A	10-bit, 7-channel

PIC16F87/88

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