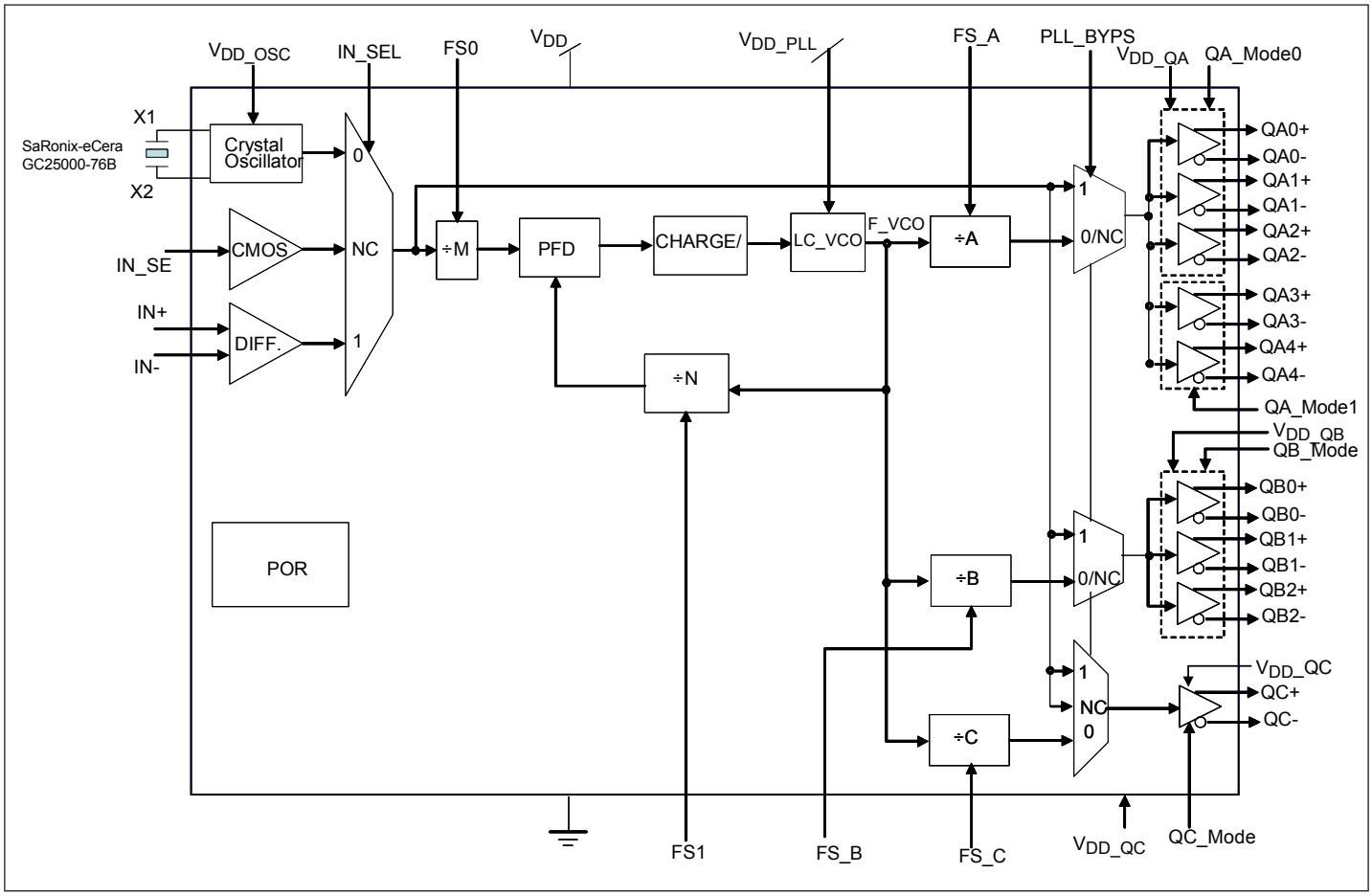
## Block Diagram



## Pin Description

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 1 | FS0 | Input (LVCMOS) | Frequency Select Pin. Use FS0=FS1=0 for all 25MHz input sources. Internal pull-down is 100K-Ohm |
| 2 | X1 | Input | Crystal input pin. No internal xtal load capacitance |
| 3 | X2 | Output | Crystal output pin. No internal xtal load capacitance |
| 4 | $V_{DD\_OSC}$ | Power | $V_{DD}$ for reference oscillator |
| 5 | IN_SEL | Input (LVCMOS) | Input mux selection pin |
| 6 | PLL_BYPS | Input (LVCMOS) | Optional mode to bypass PLL and have input reference source connect directly to outputs |
| 7 | GND | Power | Ground pin |
| 8 | FS1 | Input (LVCMOS) | Frequency Select Pin. Use FS0=FS1=0 for all 25MHz input sources. Internal pull-down is 100K-Ohm |
| 9 | QC_Mode | Input (LVCMOS) | Out mode control pin selects LVPECL or LVDS mode. If left floating, outputs are tri-stated |
| 10 | $V_{DDA}$ | Power | $V_{DD}$ for analog circuitry |
| 11 | GND | Power | Ground pin |
| 12 | $V_{DD\_PLL}$ | Power | $V_{DD}$ for PLL. |
| 13 | GND | Power | Ground pin |
| 14 | FS_B | Input (LVCMOS) | Frequency Select Pin for Bank B, Output Divider |
| 15 | GND | Power | Ground pin |
| 16 | FS_A | Input (LVCMOS) | Frequency Select Pin for Bank A, Output Divider |
| 17 | GND | Power | Ground pin |
| 18 | FS_C | Input (LVCMOS) | Frequency Select Pin for Bank C, Output Divider |
| 19 | QA_Mode1 | Input (LVCMOS) | Out mode control pin selects LVPECL or LVDS mode. If left floating, outputs are tri-stated |
| 20 | $V_{DD}$ | Power | $V_{DD}$ |
| 21 | GND | Power | Ground pin |
| 22, 23 | QC-, QC+ | Output (Differential) | Bank C LVDS/LVPECL selectable output. Controlled by QC_Mode pin |
| 24 | $V_{DD\_QC}$ | Power | $V_{DD}$ for bank C outputs |
| 25 | $V_{DD\_QA}$ | Power | $V_{DD}$ for bank A outputs |
| 26, 27 | QA4-, QA4+ | Output (Differential) | Bank A LVDS/LVPECL selectable output. Controlled by QA_Mode1 pin |
| 28, 29 | QA3-, QA3+ | Output (Differential) | Bank A LVDS/LVPECL selectable output. Controlled by QA_Mode1 pin |
| 30, 31 | QA2-, QA2+ | Output (Differential) | Bank A LVDS/LVPECL selectable output. Controlled by QA_Mode0 pin |

## Pin Description (Continued..)

| Pin Number | Pin Name | Type | Description |
|---|---|---|---|
| 32,<br>33 | QA1-,<br>QA1+ | Output (Differential) | Bank A LVDS/LVPECL selectable output. Controlled by QA_Mode0 pin |
| 34,<br>35 | QA0-,<br>QA0+ | Output (Differential) | Bank A LVDS/LVPECL selectable output. Controlled by QA_Mode0 pin |
| 36 | $V_{DD\_QA}$ | Power | $V_{DD}$ for bank A outputs |
| 37 | $V_{DD\_QB}$ | Power | $V_{DD}$ for bank B outputs |
| 38,<br>39 | QB0-,<br>QB0+ | Output (Differential) | Bank B LVDS/LVPECL selectable output. Controlled by QB_Mode pin |
| 40,<br>41 | QB1-,<br>QB1+ | Output (Differential) | Bank B LVDS/LVPECL selectable output. Controlled by QB_Mode pin |
| 42,<br>43 | QB2-,<br>QB2+ | Output (Differential) | Bank B LVDS/LVPECL selectable output. Controlled by QB_Mode pin |
| 44,<br>45 | QA_Mode0,<br>QB_Mode | Input (LVCMOS) | Out mode control pins select LVPECL, LVDS mode. If left floating, outputs are tri-stated |
| 46 | IN- | Input (Differential) | Frequency input pin, differential (accepts: LVDS, LVPECL, HCSL) |
| 47 | IN+ | Input (Differential) | Frequency input pin, differential (accepts: LVDS, LVPECL, HCSL) |
| 48 | IN_SE | Input | Frequency input pin, Single Ended |

## Input Mux Selection

| IN_SEL | Input |
|---|---|
| 0 | Select Crystal Input (Pins 2, 3) |
| 1 | Select IN+, IN- Differential Input (Pins 46, 47) |
| NC | Select IN_SE LVCMOS Input (pin 48) |

## PLL Bypass Control Function

| PLL_BYPS | PLL operation |
|---|---|
| 0 | PLL enabled |
| 1 | PLL bypassed |
| NC | PLL enabled for Banks A, B; Bank C is driven directly by the output of the input mux. |

## Input Divider Control Table

| FS0 | Divider Ratio |
|---|---|
| 0 | 1 |
| 1 | 5 |

## PLL Feedback Divider Control Table

| FS1 | Feedback Divider Ratio |
|---|---|
| 0 | 25 |
| 1 | 20 |

## Output Frequency Control Table

| FS_A | FS_B | FS_C | Output Frequency |
|---|---|---|---|
| 0 | 0 | 0 | 156.25 |
| 1 | 1 | 1 | 125 |
| NC | NC | NC | 312.5 |

## Bank A Output Control

| QA_Mode0 | QA[2:0] | QA_Mode1 | QA[4:3] |
|---|---|---|---|
| 0 | LVDS | 0 | LVDS |
| 1 | LVPECL | 1 | LVPECL |
| NC | Hi-Z | NC | Hi-Z |

## Bank B Output Control

| QB_Mode | QB[2:0] |
|---|---|
| 0 | LVDS |
| 1 | LVPECL |
| NC | Hi-Z |

## C-bank Output Interface Control Configuration

| QC_Mode | QC+/- |
|---|---|
| 0 | LVDS |
| 1 | LVPECL |
| NC | Hi-Z |

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature..... –65°C to +150°C
Supply Voltage to Ground Potential, $V_{DD}$ .....–0.5V to +4.6V
ESD Protection (HBM) ..... 2000 V

**Note: Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

## Operating Conditions

| Symbol | Parameters | Min. | Max. | Units |
|---|---|---|---|---|
| $V_{DD}$ | General Power Supply Voltage | 3.0 | 3.6 | V |
| $T_A$ | Ambient Temperature | –40 | 85 | °C |
| $I_{DD}$ | Power Supply Current | All outputs loaded | 425 | mA |
| $I_{DD\_A}$ | Power Supply Current for pin10 | | 13 | |
| $I_{DD\_PLL}$ | Power Supply Current for pin12 | | 30 | |
| $V_{DDA}$ | Analog Power Supply Voltage | 2.7 | 3.6 | V |
| $V_{DD\_PLL}$ | PLL Power Supply Voltage | 2.7 | 3.6 | |

## LVCMOS Input Electrical Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | FS0, FS1 | 2 | | | V |
| $V_{IL}$ | Input Low Voltage | | | | 0.8 | V |
| $V_{IH}$ | Input High Current | IN_SEL, PLL_BYPS, FS_A, FS_B, FS_C, QA_Mode, QB_Mode, QC_Mode | 2.6 | | | V |
| $V_{IL}$ | Input Low Current | | | | 0.8 | V |
| $I_{IH}$ | Input High Current | $V_{IN} = V_{DD}$ | | | 45 | µA |
| $I_{IL}$ | Input Low Current | $V_{IN} = 0V$ | -45 | | | µA |
| $R_{pu}$ | Internal pull up resistance | | | 100 | | KΩ |
| $R_{dn}$ | Internal pull down resistance | | | 100 | | KΩ |
| $T_{DC}$ | Input Duty Cycle | | 35 | | 65 | % |
| $C_{IN}$ | Input Capacitance[1] | | | 1.5 | | pF |
| $F_{IN}$ | Input Frequency | | 15 | | 160 | MHz |

**Note:**

1. There is no internal load capacitance built in to the X1 and X2 pins

## Differential Input Characteristics

| Symbol | Parameters | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | | $V_{DD}$ - 0.7 | V |
| $V_{IL}$ | Input Low Voltage | | $V_{DD}$ - 2.0 | | | V |
| $V_{CM}$ | Input Bias Voltage | | $V_{DD}$ - 1.8 | $V_{DD}$ / 2 | | V |
| $R_{IN}$ | Input Differential Impedence[2] | | 80 | 100 | 120 | Ω |
| $V_{IN-PP}$ | Input Differential Swing | | 0.3 | | 1.8 | $V_{PP}$ |
| $C_{IN}$ | Differential Input Capacitance | | | 1.5 | | pF |

**Note:**

1. 2. Differential input can be AC or DC coupled.

## LVPECL Output Characteristics (Over Operating Conditions. See Fig. 1 and 2 for load conditions.)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 25 | | 312.5 | MHz |
| $T_{rise}$ / $T_{fall}$ | Rise and Fall Time | 20% to 80%, single-ended | | | 400 | ps |
| $T_{DC}$ | Duty Cycle | Differential | 47 | | 53 | % |
| $J_{phase}$ | Integrated phase jitter | 12KHz-20MHz @ 156.25MHz, 25MHz Xtal input | | 0.54 | 1 | ps rms |
| $T_{DIS}$ | Output Disable Time | | | | 80 | ns |
| $T_{EN}$ | Output Enable Time | | | | 80 | ns |
| $T_{LOCK}$ | PLL Lock Time | | | | 2 | ms |
| $V_{PP}$ | Output peak-peak Voltage | Single-ended | 0.6 | | 1 | V |
| $V_{OH}$ | Output High Voltage | $V_{DD}$ = 3.3V | $V_{DD}$-1.4 | | $V_{DD}$-0.9 | V |
| $V_{OL}$ | Output Low Voltage | $V_{DD}$ = 3.3V | $V_{DD}$-2.0 | | $V_{DD}$-1.7 | V |

## LVDS Output Characteristics (Over Operating Conditions See Fig. 1 and 2 for load conditions.)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Output Frequency | | 25 | | 312.5 | MHz |
| $T_{rise}$ / $T_{fall}$ | Rise and Fall Time | 20% to 80%, single-ended | | | 270 | ps |
| $T_{DC}$ | Duty Cycle | Differential | 47 | | 53 | % |
| $J_{phase}$ | Integrated phase jitter | 12KHz-20MHz @ 156.25MHz, 25MHz Xtal input | | 0.54 | 1 | ps rms |

## LVDS Output Characteristics (Continued..)

| Symbol | Parameters | Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $T_{DIS}$ | Output Disable Time | | | | 80 | ns |
| $T_{EN}$ | Output Enable Time | | | | 80 | |
| $T_{LOCK}$ | PLL Lock Time | | | | 2 | ms |
| $\|V_{AMP}\|$[1] | Differential Output Voltage Amplitude | $\|V_{OH} - V_{OL}\|$ with 100Ω external termination | 250 | | 520 | mV |
| | | $\|V_{OH} - V_{OL}\|$ with 120Ω external termination | 250 | | 600 | |
| $V_{OH}$ | Output High Voltage | | | | 1.8 | V |
| $V_{OL}$ | Output Low Voltage | | 0.925 | | | |
| $V_{OS}$ | Output offset voltage | | 1.125 | | 1.375 | |
| $R_{OL}$ | Differential output impedance | | 85 | | 140 | Ω |

**Note:**

1. Valid for part numbers with date code after Y1338.

## Power Supply Noise Rejection Specification

| Parameter | Conditions | Min. | typ | Max. | Units |
|---|---|---|---|---|---|
| Supply Noise induced phase spur @ 156.25 NHz output (see note) | Fm = 100kHz to 400KHz | | -50 | | dBc |

**Note:**

1. Measured with 50mVp-p Sinusoidal Interference on the supply VDDQx, measured with the supply filter as shown in Figure 2.

## Crystal Characteristic (link to "http://www.pericom.com/saronix" for more detailed crystal specifications)

| Parameters | Description | Min | Typ | Max. | Units |
|---|---|---|---|---|---|
| OSCmode | Mode of Oscillation | Fundamental | | | |
| FREQ | Frequency | | 25 | | MHz |
| ESR(1) | Equivalent Series Resistance | | | 50 | Ohm |
| Cload | Load Capacitance | | 18 | | pF |
| Cshunt | Shunt Capacitance | | | 7 | pF |
| | Drive Level | | | 0.1 | mW |

**Note:**

1. ESR value is dependent upon frequency of oscillation

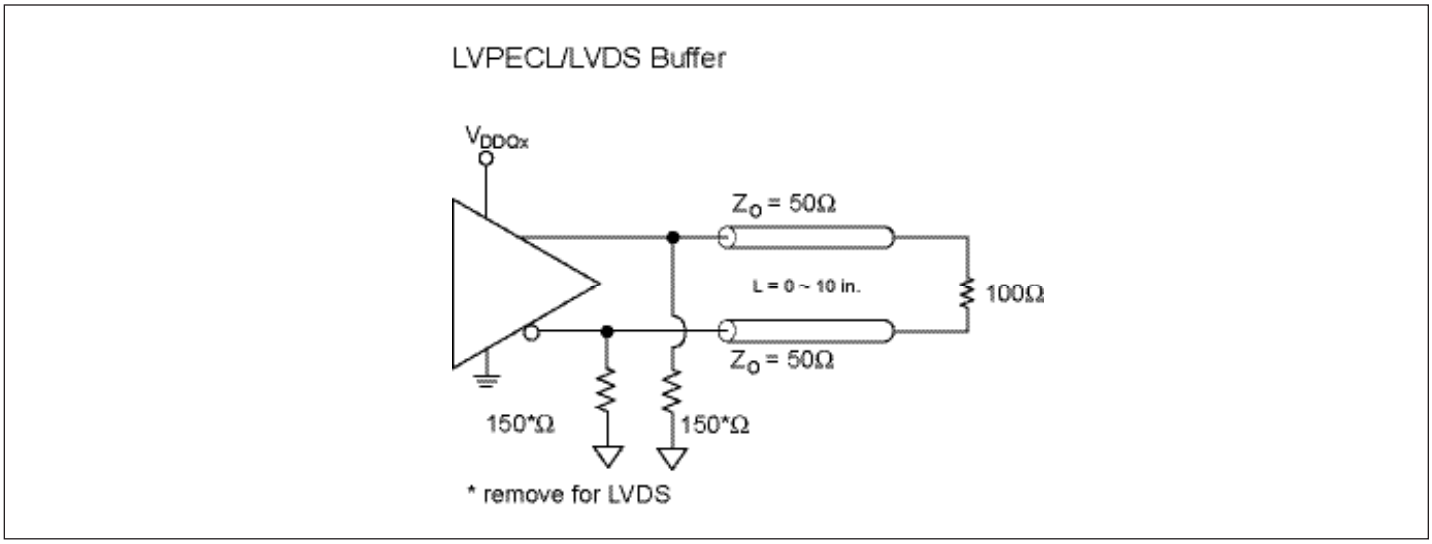



**Figure 1. Test Circuit**

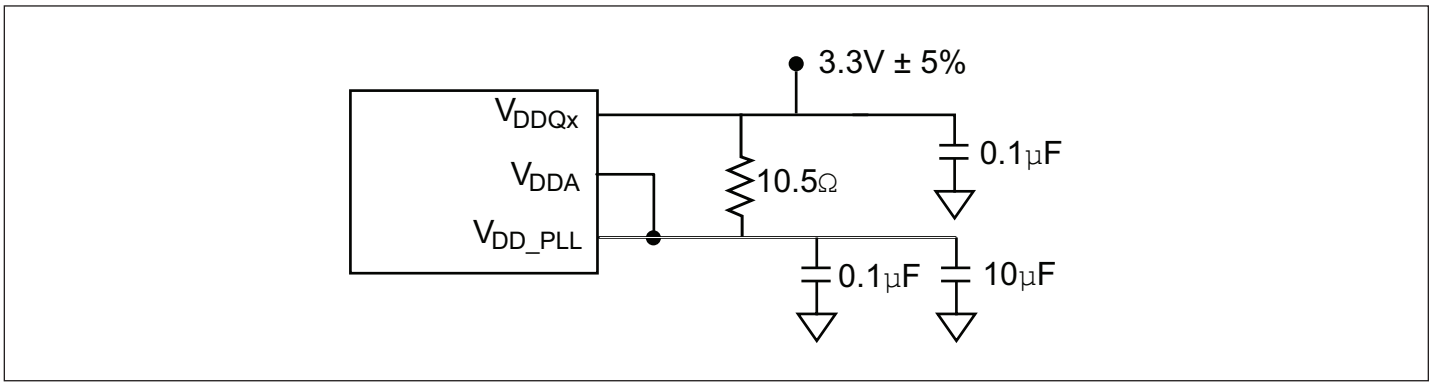
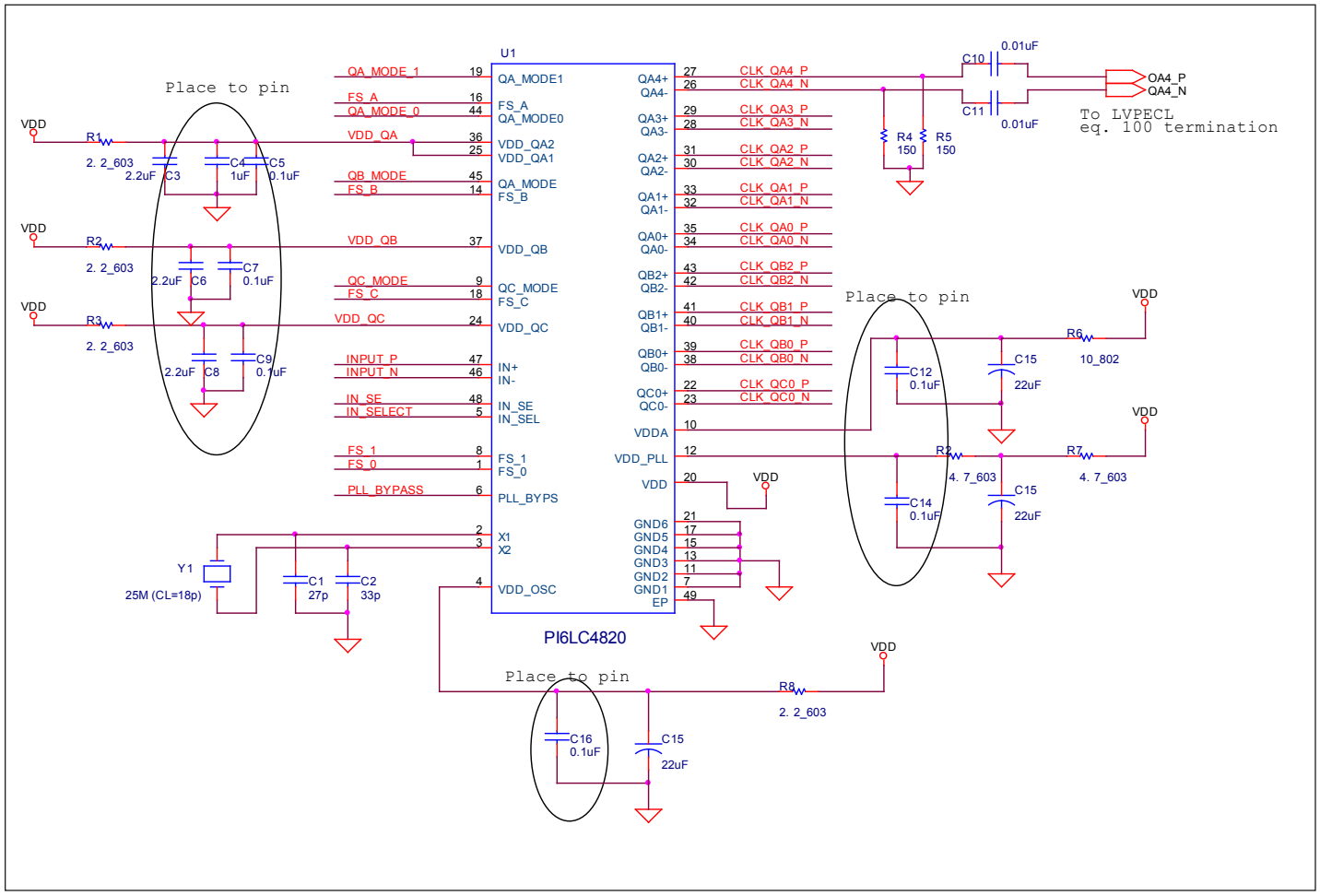



**Figure 2. Power Supply Filter**

## Application Notes

PI6LC4820 is a high performance and low jitter clock generator for advanced Gigabit Ethernet systems. It has three independent banks whose outputs can be set to LVPECL or LVDS and in 3 outputs frequencies : 125MHz, 156.25MHz, and 312.5MHz. It is critical to ensure the power supply is properly decoupled and the layout around the crystal is properly routed to achieve this low jitter performance. The following guide is highly recommended to be adopted into the system PCB designs.

## Power Decoupling Schematic




1) It is suggested to use the schematic's decoupling RC value to get best board noise filtering

2) Typical LVPECL is using 150Ω pull down in AC or DC coupling drive according to ASIC ref_clk I/O spec

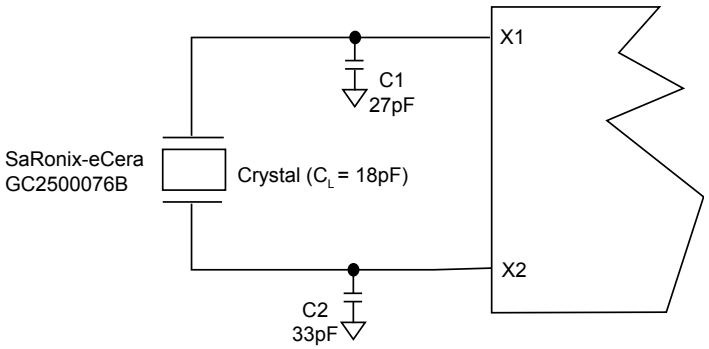
3) The crystal circuit C1/C2 load values are for CL=18pF crystal, they can be adjusted for other CL crystals

4) Please refer to the datasheet for other static I/O logic set for the request work modes and output frequencies

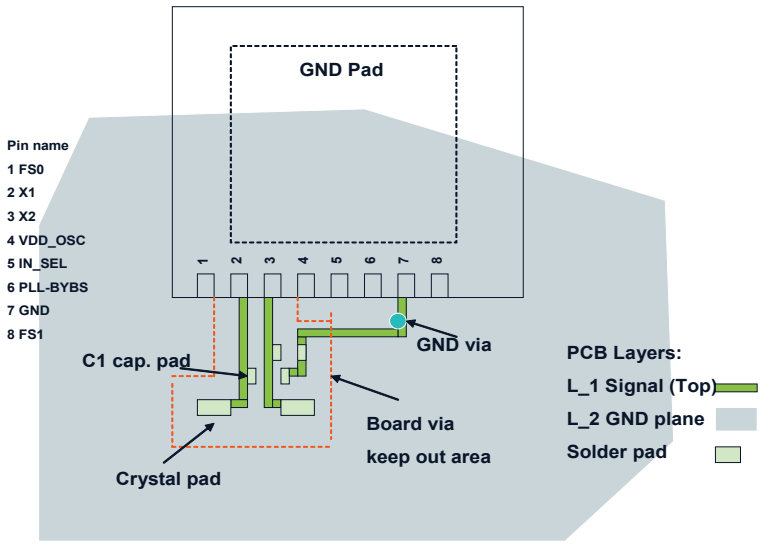
## Crystal circuit connection

The following diagram shows PI6LC4820 crystal circuit connection with a parallel crystal. For the CL=18pF crystal, it is suggested to use C1=27pF, C2=33pF. C1 and C2 can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts.

## Crystal Oscillator Circuit




## Crystal Circuit Oscillator




## Recommended Crystal Specification

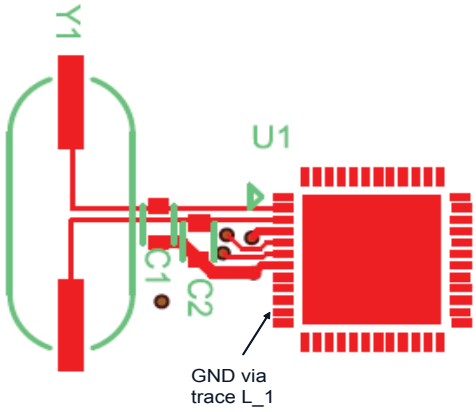
**Pericom recommends:**

a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf

b) FY2500081, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm, http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf

c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm, http://www.pericom.com/pdf/datasheets/se/FL.pdf

### Crystal Layout Example




1) X1 pin is the most sensitive as crystal amplifier input

2) X1 and X2 pins connected to crystal trace loop should be very narrow without any board via in the loop and keep the via out of the area

3) Place crystal as close to the IC as possible along with C1/C2 load caps. There should be no via at the top layer to the crystal

4) Keep crystal load cap. C1/C2 to GND sides as close as possible so that the minimum board noise could be coupled into the caps

## 4. VDD and GND Pins Layout

1) Small value decoupling caps. (0.1uF, 1uF, and 2.2uF) should be placed close to each VDD pin or via

2) Each GND pin should have its own via to the common GND plane

3) Thermal pad must be connected to the GND plane for better thermal distribution and signal conducting with reasonable via counts (>6)

## 5. LVPECL Differential Output Layout

1) 150Ω pull-down should be put close to clock output side with symmetrical position in one pair

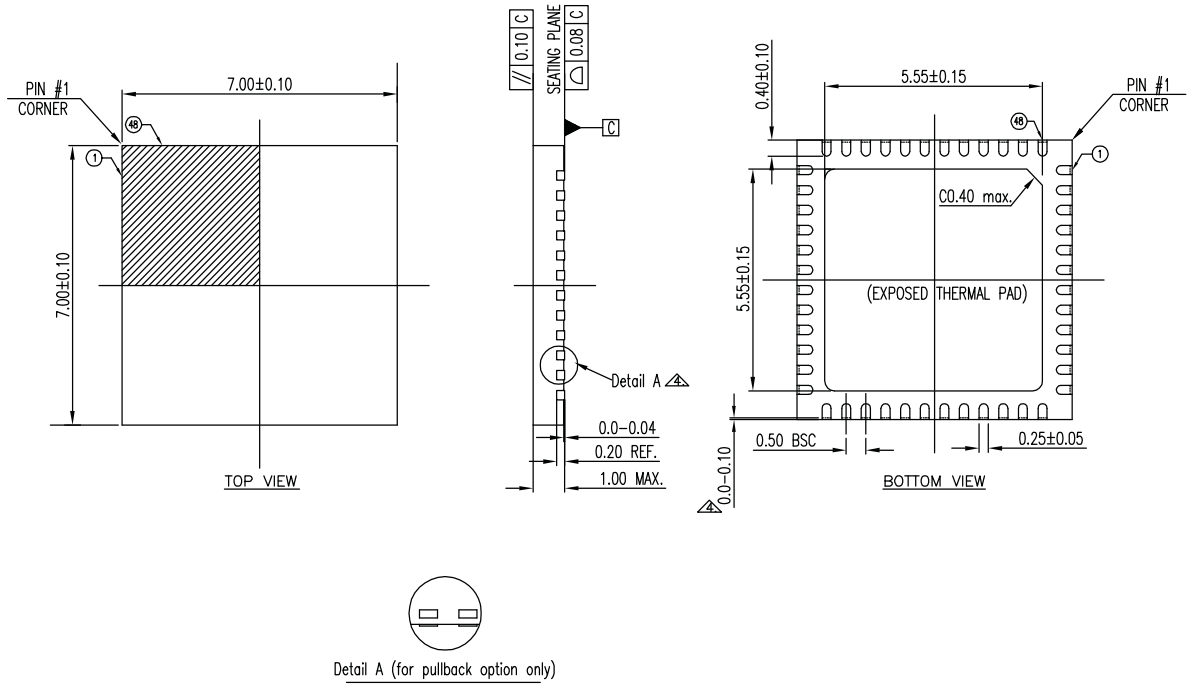
2) Do not share 150Ω pull-down GND via between each pairs

## 6. Differential Input

1) This device differential input (pin 47, 48) can accept 25MHz, 125MHz, and 156.25MHz frequencies in most common differential signals (LVPECL, LVDS, HCSL etc.) in either AC or DC coupling, with proper IN_SEL, FS0, and FS1 setting

2) The device differential input has equivalent 100Ω differential termination on chip, so PCB 100Ω external termination is normally not necessary.

## Packaging Mechanical: 48-Pin TQFN (ZD)




**Notes:**
1. All dimensions are in millimeters, angles are in degrees.
2. Refer JEDEC MO-220/VKKD
3. Thermal Pad Soldering Area
4. Depending on the method of lead termination at the edge of the package, pull back maybe present.

PERICOM Semiconductor Corporation — DATE: 08/09/12

DESCRIPTION: 48-Contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZD (ZD48)

DOCUMENT CONTROL #: PD-2045 — REVISION: E

12-0458

**Note:**

1. • For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

## Ordering Information(1-3)

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI6LC4820ZDE | ZD | 48-Pin, Pb-free & Green (TQFN) |

**Notes:**

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. 3. Adding an X suffix = Tape/Reel