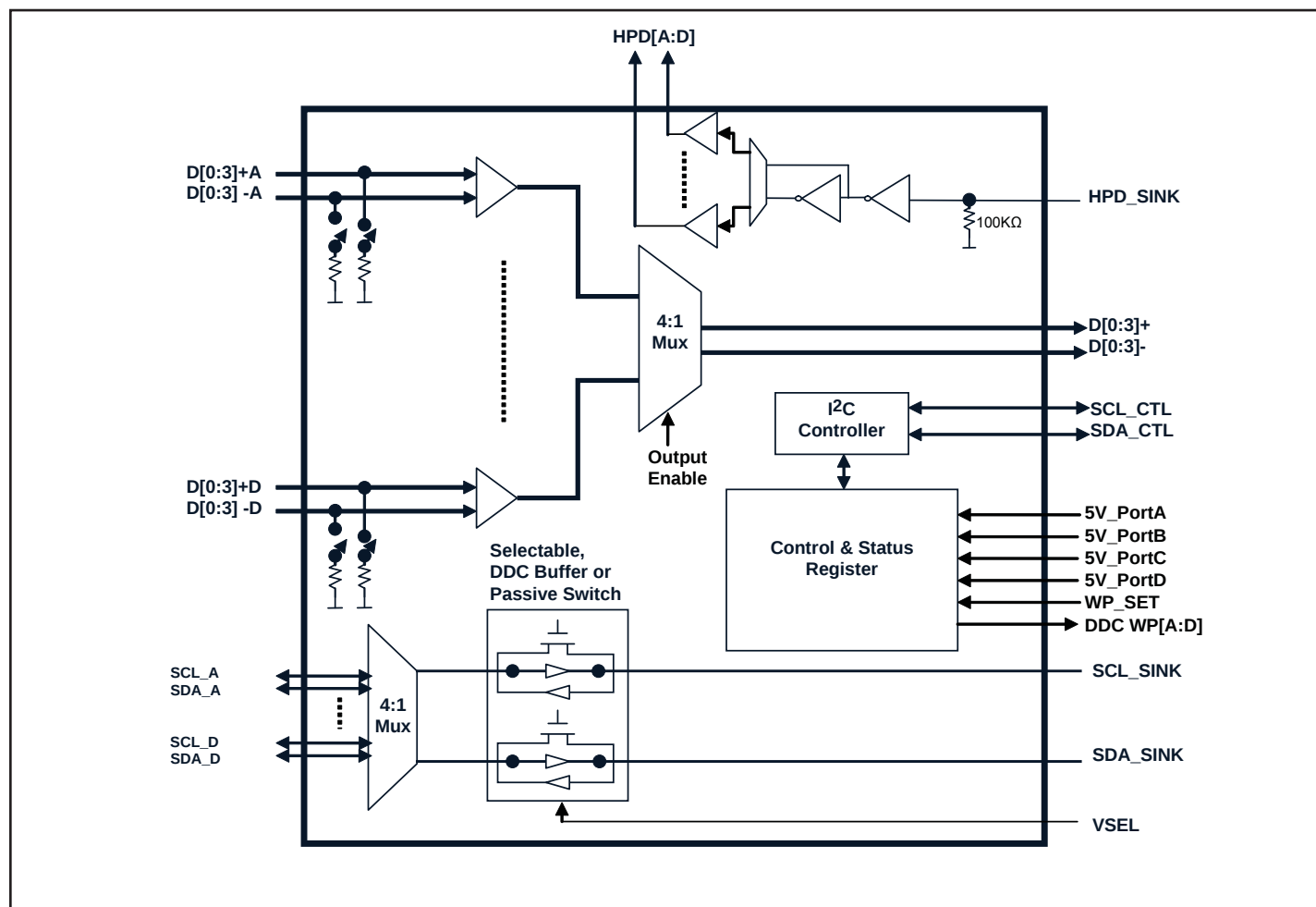
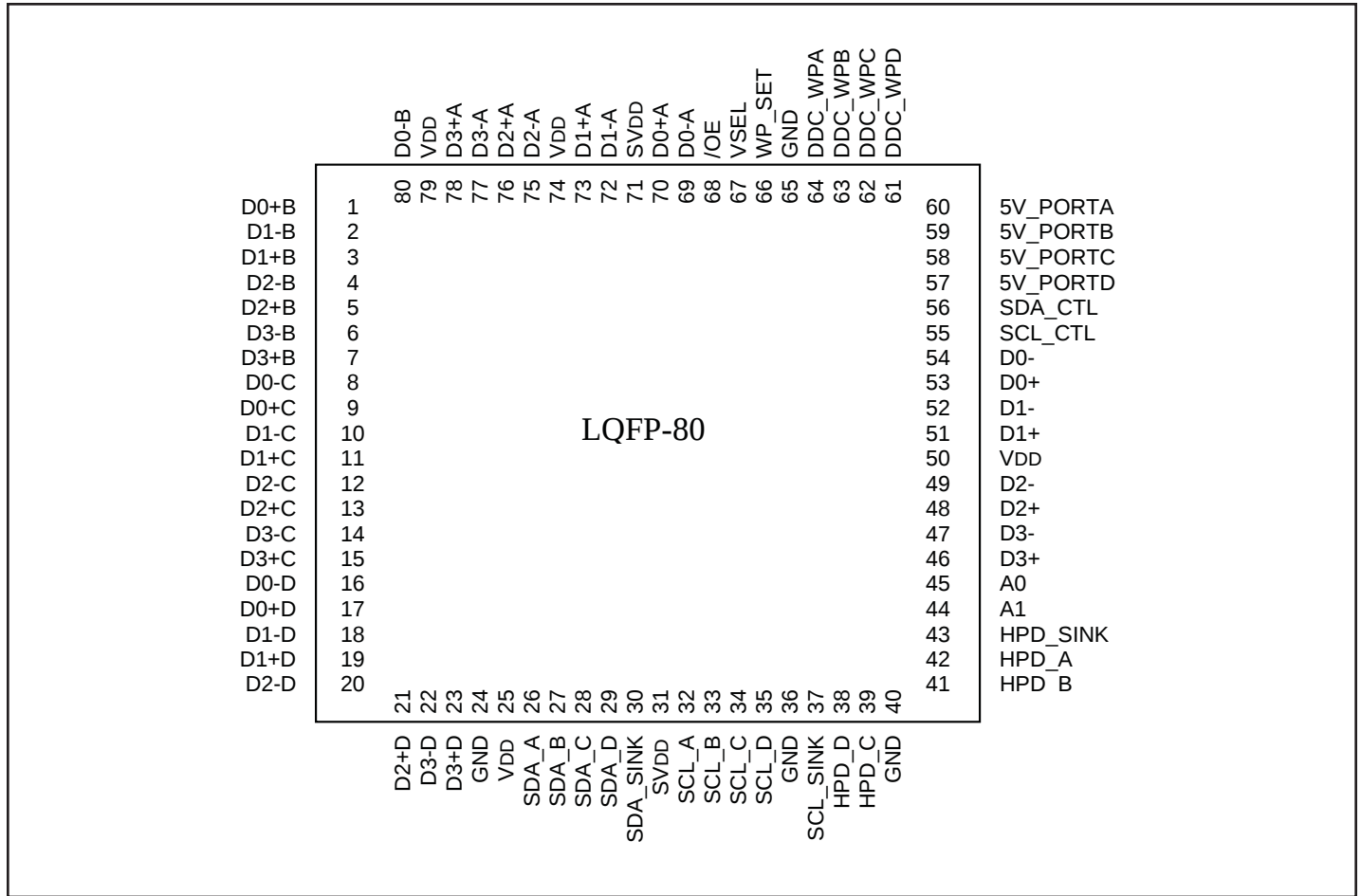


Block Diagram



Pin Assignment – 80-Contact LQFP



Pinout Table

Pin Name	I/O Type	Description
V _{DD}	I/O	3.3V power supply. When V _{DD} is off, the TMDS channels will be powered down.
SV _{DD}	I/O	3.3V standby power supply. SV _{DD} is for all side band signals, I ² C register and I ² C bus.
HPD_SINK	I	Sink side hot plug detector input. High: 5-V power signal asserted from source to sink and EDID is ready. Low: No 5-V power signal asserted from source to sink, or EDID is not ready.
HPD_A	O	Port A HPD output
HPD_B	O	Port B HPD output
HPD_C	O	Port C HPD output
HPD_D	O	Port D HPD output
D0+A D0-A D1+A D1-A D2+A D2-A D3+A D3-A	I	Port A TMDS inputs
D0+B D0-B D1+B D1-B D2+B D2-B D3+B D3-B	I	Port B TMDS inputs
D0+C D0-C D1+C D1-C D2+C D2-C D3+C D3-C	I	Port C TMDS inputs

Pin Name	I/O Type	Description
D0+D D0-D D1+D D1-D D2+D D2-D D3+D D3-D	I	Port D TMDS inputs
D0+ D0- D1+ D1- D2+ D2- D3+ D3-	O	TMDS outputs
SCL_A	I/O	Port A DDC Clock
SCL_B	I/O	Port B DDC Clock
SCL_C	I/O	Port C DDC Clock
SCL_D	I/O	Port D DDC Clock
SDA_A	I/O	Port A DDC Data
SDA_B	I/O	Port B DDC Data
SDA_C	I/O	Port C DDC Data
SDA_D	I/O	Port D DDC Data
SCL_SINK	I/O	Sink side DDC Clock
SDA_SINK	I/O	Sink side DDC Data
SCL_CTL	I/O	I²C Clock
SDA_CTL	I/O	I²C Data
WP_SET	I	WP_SET = 0 (Default), Set B1b[1] as INT Flag. WP_SET = 1, DDC_WP[A:D] is programmable by B1b[1].
DDC_WPA, DDC_WPB, DDC_WPC, DDC_WPD,	O	Open drain output. When WP_SET = 1, general purpose logic configured by B1b[1]
$\overline{\text{OE}}$	I	Output Enable control. Active low.
A1	I	I²C Address 1
A0	I	I²C Address 0

Pin Name	I/O Type	Description
5V_PortA, 5V_PortB, 5V_PortC, 5V_PortD	I	Connector 5V port.
VSEL	I	DDC buffer V _{IL} selection. VSEL = 0V, V _{IL} = 0.5V VSEL = 0.5 V _{DD} , V _{IL} =0.45V VSEL = V _{DD} , V _{IL} =0.6V

Truth Table

WP_SET	B1_b[1]	DDC_WP[A:D]
1	0	Hi_Z
1	1	0
0	X	Hi_Z

I²C Control Register

	b7	b6	b5	b4	b3	b2	b1	b0
Address Byte	1	0	1	0	1	A1 Hardware Selectable	A0 Hardware Selectable	0/1 *

* 0:Write; 1:Read

Data Byte 0: Control Register

Bit	Description	Type	Power Up Condition	Logic Settings
7	HDMI input port selection	R/W	0	00 = Port A 01 = Port B
6	HDMI input port selection	R/W	0	10 = Port C 11 = Port D
5	HPD Logic Selection	R/W	1	0 = Inverted 1 = Non Inverted
4	HPD Input Selection	R/W	0	0 = HPD_SINK 1 = I ² C Register Setting B0b[3:0]
3	HPD Port D Logic Setting	R/W	0	I. Byte0 b[4] = 1 HPD Port D Register setting II. Byte0 b[4] = 0 Test mode
2	HPD Port C Logic Setting	R/W	0	I. Byte0 b[4] = 1 HPD Port C Register setting II. Byte0 b[4] = 0 Test mode
1	HPD Port B Logic Setting	R/W	0	I. Byte0 b[4] = 1 HPD Port B Register setting II. Byte0 b[4] = 0 Test mode
0	HPD Port A Logic Setting	R/W	0	I. Byte0 b[4] = 1 HPD Port A Register setting II. Byte0 b[4] = 0 Test mode

Data Byte 1: Control Register

Bit	Description	Type	Power Up Condition	Logic Settings
7	HPD Output Stage selection	R/W	0	0 = Open Drain 1 = Output Buffer
6	Output Enable	R/W	1	0 = Output Disable (also drives switch into power down mode) 1 = Output Enable
5	5V_Port D connect	R	0	0 = Disconnected 1 = Connected; Set INT Flag
4	5V_Port C connect	R	0	0 = Disconnected 1 = Connected; Set INT Flag
3	5V_Port B connect	R	0	0 = Disconnected 1 = Connected; Set INT Flag
2	5V_Port A connect	R	0	0 = Disconnected 1 = Connected; Set INT Flag
1	INT Flag	R/W	0	When WP_SET = 0, B1b[1] is configured as INT flag. 0 = INT Flag Clear 1 = INT Flag Set When WP_SET = 1, B1b[1] is configured as DDC_WP input setting.
0	DDC channel selection	R/W	0	0 = Passive switch 1 = Active switch buffer

* External hardware control pin WP_SET will set B1b1 to be INT Flag or DDC_WP[0:3] input.

Bus transactions

Data transfers follow the format shown in Fig.1. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

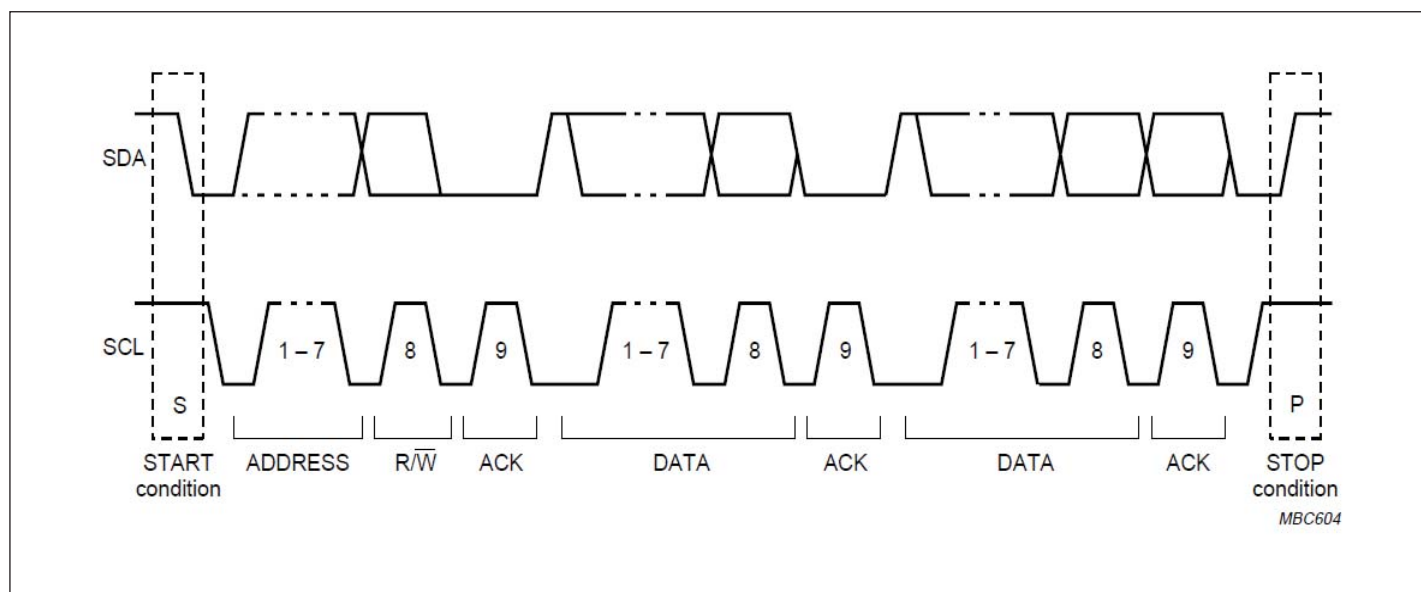


Figure 1: A Complete Data Transfer

Data is transmitted to the PI3HDMI2410 registers using the Write mode as shown in Figure 2. Data is read from the PI3HDMI2410 registers using the Read mode as shown in Figure 3.

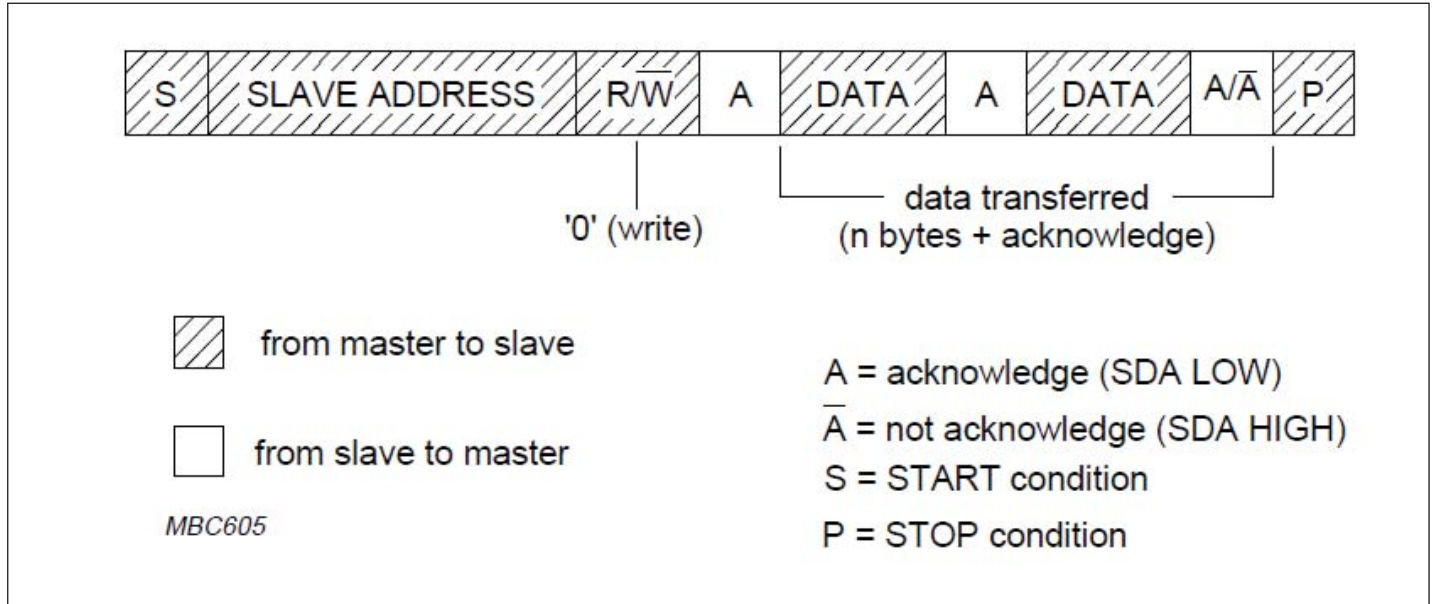


Figure 2 : Write to Control Register

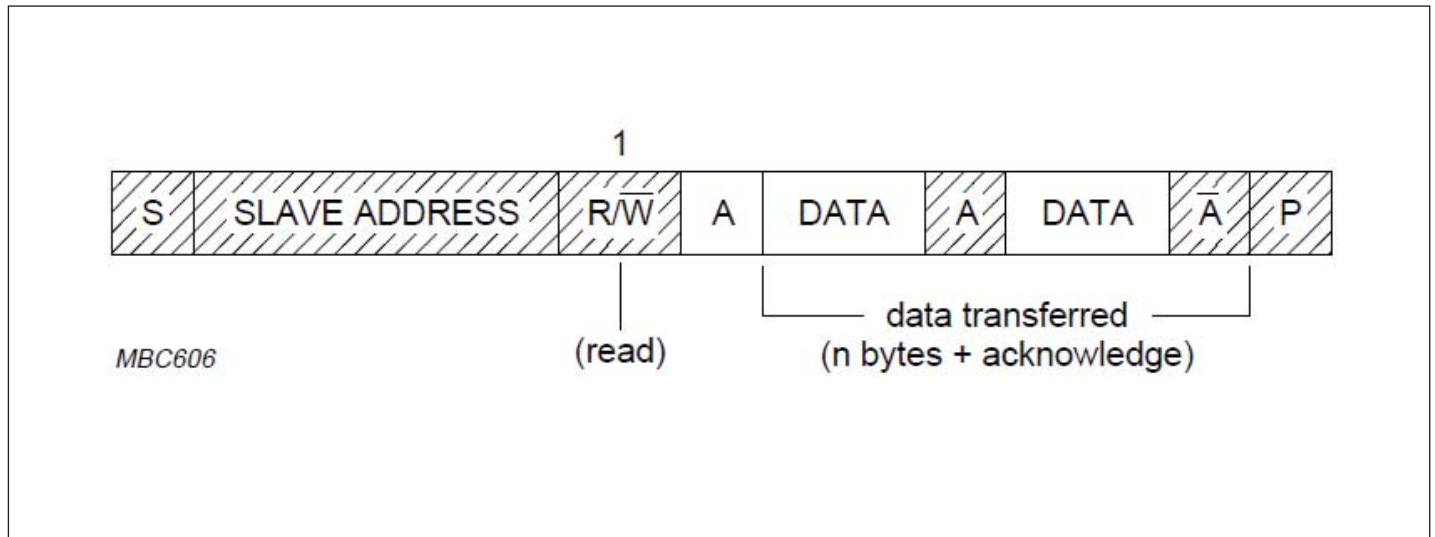
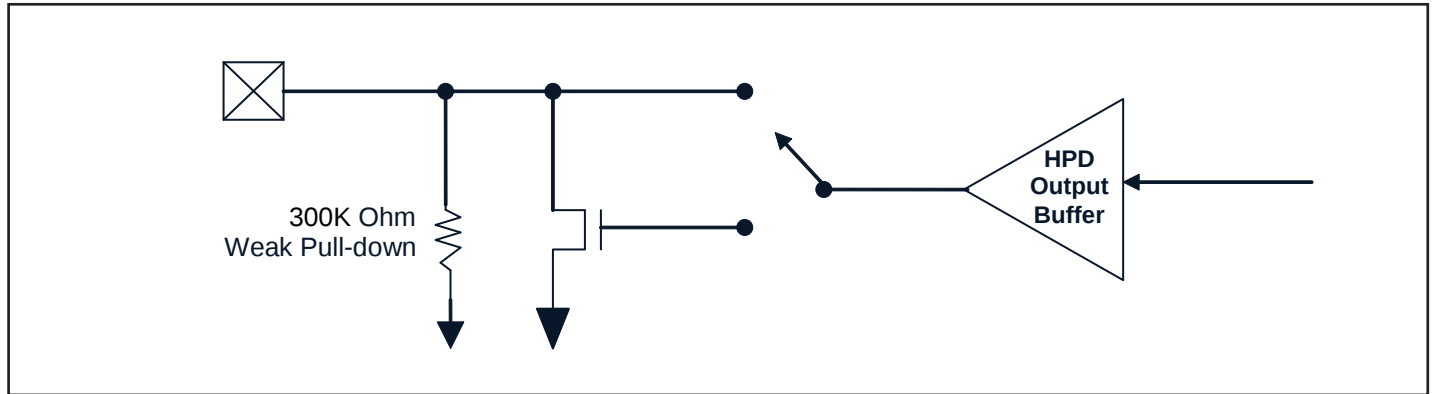


Figure 2 : Read to Control Register

HPD Output Buffer



Data Channel Pull-down Resistor Control

Pull-down resistor active conditions:

1. The Data Channel is unselected
2. Output enable control /OE is disable(/OE=High) or B1b[6]=Low, pull down on all channels
3. No normal operation voltage input (but standby voltage SVDD is still On), pull down on all channels

Output Enable control

Output Disable can be asserted through external $\overline{\text{OE}}$ pin or through I²C.

$\overline{\text{OE}}$	OE_I²C B1b[6]	Operation
Low	High	Enable
Low	Low	Disable
High	X	Disable

Default value: $\overline{\text{OE}}$ = Low ; Byte 1 b[6] = High

Absolute Maximum Ratings (Over operating free-air temperature range)

Item	Rating
Supply Voltage to Ground Potential	5.5V
All Inputs and Outputs	-0.5V to V _{DD} +0.5V
Ambient Operating Temperature	-40 to +85°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature	260°C

Stress beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+3.6	V

DC Specifications

V_{DD} = 3.3V ±10%, Ambient Temperature 0 to +70°C

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V _{DD}	Operating Voltage		3.0	3.3	3.6	V
I _{DD}	Supply Current	Output Enable		5.0	6	mA
I _{DDQ}	Quiescent Supply Current	Output Disable		1.7	2	
V _{OH_DDC}	DDC passive switch Output High Voltage	Test condition as I _O = 0 (open load), V _I = 5.5V	SV _{DD} -1.0			V
V _{OL_DDC}	DDC Buffer Output Low Voltage	Source side, I _{OL} = 3mA External pull-up to 3.3V from 1.5kΩ to 4.7kΩ			0.4	
		Sink side, I _{OL} = 3mA	0.65	0.75	0.95	

Symbol	Parameter	Conditions	Min	Nom	Max	Units
V_{IH_DDC}	DDC Buffer Input High Voltage	Source side (VSEL = 0)		1.7		V
		Sink side (VSEL = 0)		0.5		
V_{IL_DDC}	DDC Buffer Input Low Voltage	Source side			0.8	
		Sink side (VSEL = 0)	0.45	0.5	0.6	
$V_{IH_V5_A'}$ $V_{IH_V5_B'}$ $V_{IH_V5_C'}$ $V_{IH_V5_D'}$	Input High Voltage of 5V ports		2.4			
$V_{IL_V5_A'}$ $V_{IL_V5_B'}$ $V_{IL_V5_C'}$ $V_{IL_V5_D'}$	Input Low Voltage of 5V ports				0.8	
V_{OL_HPD}	Buffer Output Low Voltage	$I_{OL} = 4\text{ mA}$			0.4	
	Open Drain Output Low Voltage	$I_{OL} = 4\text{ mA}$	0		0.4	
V_{OH_HPD}	Buffer Output High Voltage	$I_{OH} = 3\text{ mA}$	2.4			
$I_{OFF\ (HPD)}$	Off Leakage Current	$V_{DD} = 0\text{V}, V_{IN} = 3.6\text{V}$		12	20	μA
		$V_{DD} = 0\text{V}, V_{IN} = 5.5\text{V}$		20	35	
I_{OZ_HPD}	Open Drain Output Leakage Current	$V_{DD} = 3.6\text{V}, V_{IN} = 3.6\text{V}$		12	15	
		$V_{DD} = 3.6\text{V}, V_{IN} = 5.5\text{V}$		21	38	
$V_{OL_DDC_WP}$	Open Drain Output Low Voltage	$I_{OL} = 4\text{ mA}$			0.4	V
C_{IO}^1	Input/output capacitance (Passive Switch)	$V_{DD} = 0\text{V or } 3.0\text{V}$, Frequency = 100kHz		6	9	pF

Note:

- Measured at $V_{bias} = 0\text{V or } 5\text{V}$, $V_{rms} = 0.2\text{V}$;
 $V_{bias} = 1.65\text{V}$, $V_{rms} = 0.9\text{V}$;
 $V_{bias} = 2.5\text{V}$, $V_{rms} = 1.2\text{V}$.

Dynamic Specifications

$V_{DD} = 3.3V \pm 10\%$, $T_A = -40$ to $+85^\circ C$, $GND = 0V$

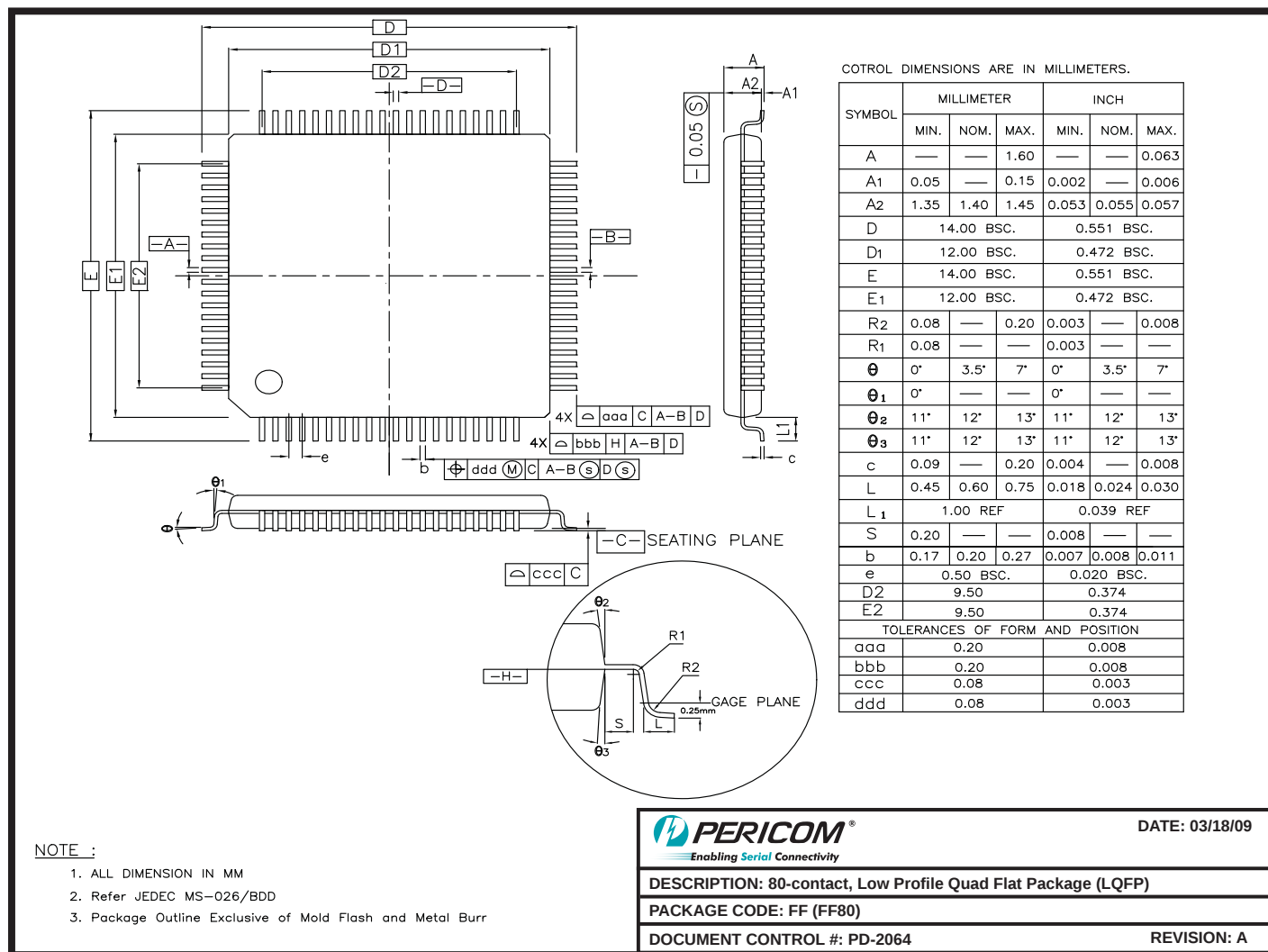
Parameter	Description	Conditions	Min	Typ	Max	Units
X_{TALK}	Crosstalk on High-speed Channels	$f = 1.13 \text{ GHz}$		-34		dB
		$f = 825 \text{ GHz}$		-36		
O_{IRR}	OFF Isolation on High-speed Channels	$f = 1.13 \text{ GHz}$		-28		
		$f = 825 \text{ GHz}$		-32		
I_{LOSS}	Defferential Insertion Loss on High-speed Channels	DR = 1.65Gbps		-1.5		dB
		DR = 2.0Gbps		-1.73		
		DR = 2.25Gbps		-1.82		
		DR = 3.0Gbps		-1.99		
		DR = 3.4Gbps		-2.08		
BW	-3dB BW for TMDS channels			2.5		GHz

Capacitance Measurement ($V_{DD} = 3.3V$, $T_A = 25^\circ C$)

Test Condition	Capacitance	Units
SDA_CTL	3.0	pF
SCL_CTL	2.3	
HPD_Sink	1.7	

$V_{bias} = 0.6V$

Packaging Mechanical: 80-Contact LQFP (FF)



07-0100

Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information

Ordering Code	Package Code	Package Type
PI3HDMI2410FFE	FF	Pb-free & Green, 80-Contact, LQFP

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel