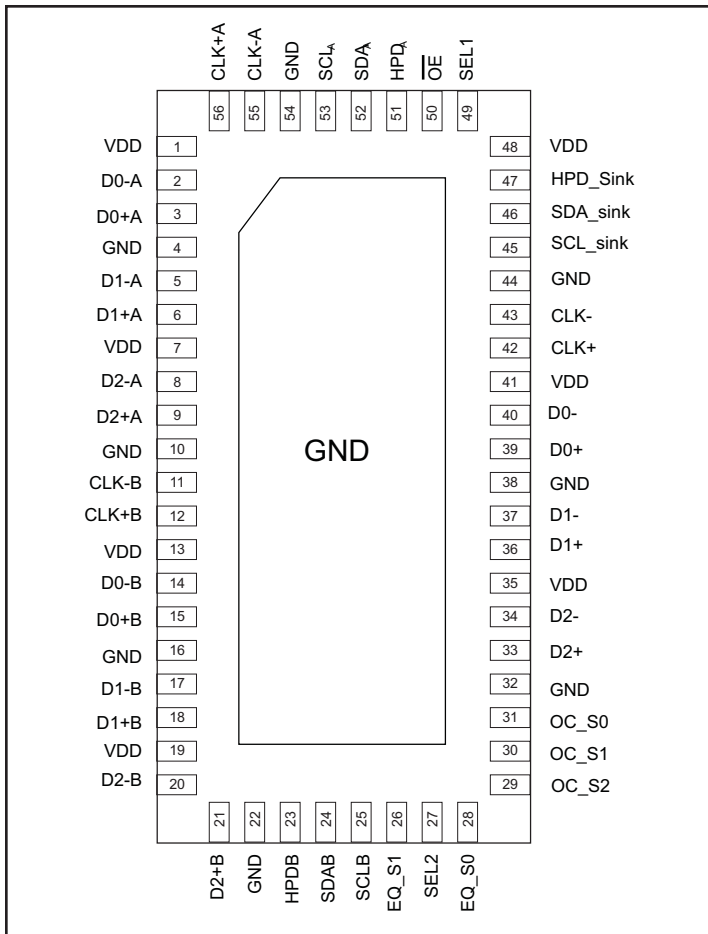
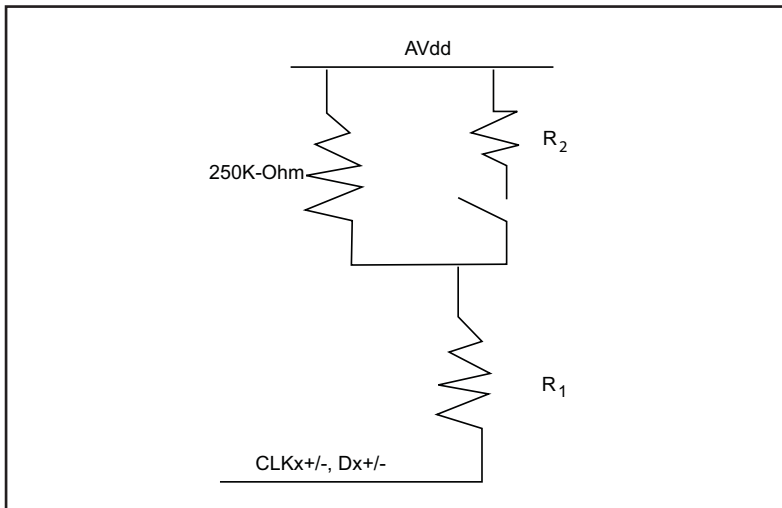


Pin Configuration (Top View)



Receiver Block

Each input has integrated equalization that can eliminate deterministic jitter caused by 25meter 24AWG cables. All activity can be configured using pin strapping. The Rx block is designed to receive all relevant signals directly from the HDMI™ connector without any additional circuitry, 3 High speed TMDS data, 1 pixel clock, 1 HPD signal, and DDC signals. TMDS channels have following termination scheme for Rx Sense support.

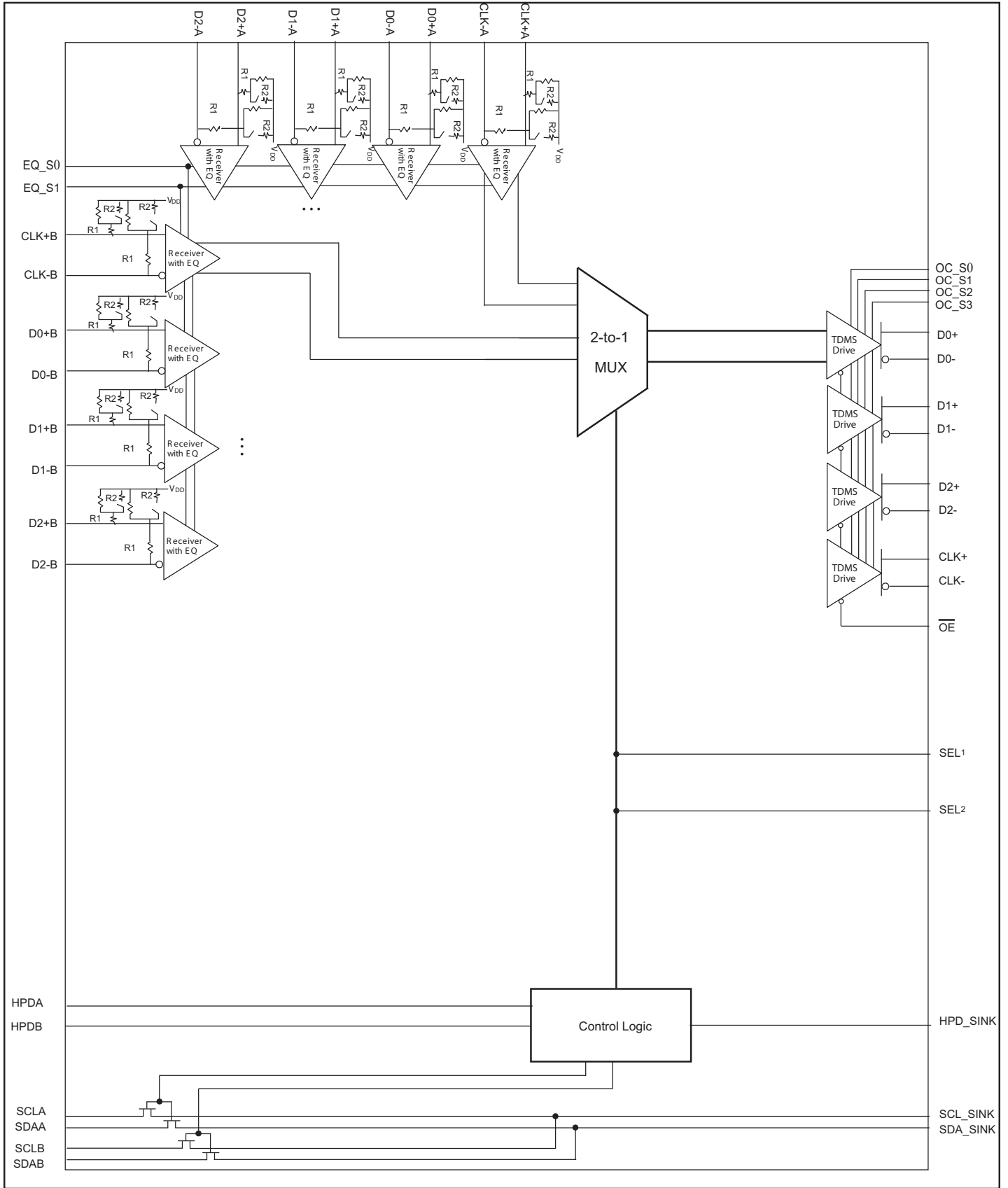


x = A or B

**Pin Description**

Pin #	Pin Name	I/O	Description
3 6 9 56	D <sub>0</sub> +A D <sub>1</sub> +A D <sub>2</sub> +A CLK+A	I	Port A TMDS Positive inputs
15 18 21 12	D <sub>0</sub> +B D <sub>1</sub> +B D <sub>2</sub> +B CLK+B	I	Port B TMDS Positive inputs
2 5 8 55	D <sub>0</sub> -A D <sub>1</sub> -A D <sub>2</sub> -A CLK-A	I	Port A TMDS Negative inputs
14 17 20 11	D <sub>0</sub> -B D <sub>1</sub> -B D <sub>2</sub> -B CLK-B	I	Port B TMDS Negative inputs
4, 10, 16, 22, 32, 38, 44, 54	GND		Ground
51	HPD <sub>A</sub>	O	Port A HPD output
23	HPD <sub>B</sub>	O	Port B HPD output
47	HPD_Sink	I	Sink side hot plug detector input.
50	$\overline{OE}$	I	Output Enable, Active LOW
53	SCL <sub>A</sub>	I/O	Port A DDC Clock
25	SCL <sub>B</sub>	I/O	Port B DDC Clock
45	SCL_Sink	I/O	Sink Side DDC Clock
52	SDA <sub>A</sub>	I/O	Port A DDC Data
24	SDA <sub>B</sub>	I/O	Port B DDC Data
46	SDA_Sink	I/O	Sink Side DDC Data
49	SEL1	I	Source Input Selector (See Truth Table)
1, 7, 13, 19, 35, 41, 48	V <sub>DD</sub>		3.3V Power Supply
39 36 33 42	D <sub>0</sub> + D <sub>1</sub> + D <sub>2</sub> + CLK+	O	TMDS positive outputs
40 37 34 43	D <sub>0</sub> - D <sub>1</sub> - D <sub>2</sub> - CLK-	O	TMDS negative outputs
28 26	EQ_S0 EQ_S1	I	Equalizer controls, Internal pull-ups are added to both.
31 30 29	OC_S0 OC_S1 OC_S2	I	Output buffer controls Note: all 3 pins have internal pull-ups
27	SEL2	I	Source Input Selector (See Truth Table)

Switch Block Diagram



### Truth Table

$\overline{OE}$	SEL1	SEL2	Function for TMDS output	HPD <sub>A</sub>	HPD <sub>B</sub>
0	1	X	Port A is active & TMDS Rx Termination on Port B goes to 250K-Ohm	HPD_sink	L
0	0	1	Port B is active, & TMDS Rx Termination on Port A goes to 250K-Ohm	L	HPD_sink
0	0	0	All TMDS outputs & TMDS inputs are Hi-Z, SCL/SDA (Port A & B) are off	L	L
1	X	X	All TMDS outputs are Hi-Z	Follow SEL1 and SEL2	Follow SEL1 and SEL2

### OC Setting Value Logic Table

Input Control Pins			Setting Value	
OC_S2 <sup>(1)</sup>	OC_S1 <sup>(1)</sup>	OC_S0 <sup>(1)</sup>	V <sub>swing</sub> (mV)	Pre-emphasis (dB)
1	1	1	500	0
1	1	0	750	0
1	0	1	1000	0
1	0	0	600	0
0	1	1	500	0
0	1	0	500	1.5
0	0	1	500	3.5
0	0	0	500	6

**Note:**

1. Integrated pull-ups

### EQ Setting Value Logic Table for high speed data bits (TMDS CLK input is left at 3dB default always)

EQ_S1 <sup>(1)</sup>	EQ_S0 <sup>(1)</sup>	Setting Value
0	0	15dB on all high speed data inputs
0	1	3dB on all high speed data inputs
1	0	8dB on all high speed data inputs
1	1	Optimized Equalization on all high speed data inputs (Default setting which can support all cable lengths from 1meter to 20meters)

**Notes:**

1) Integrated internal pull-ups

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage to Ground Potential.....	-0.5V to +4.0V
DC Input Voltage .....	-0.5V to $V_{DD}$
DC Output Current.....	120mA
Power Dissipation .....	1.0W

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
$V_{DD}$	Supply Voltage	3.135	3.3	3.465	V
$T_A$	Operating free-air temperature	0		70	°C
<b>TMDS Differential Pins (<math>D_{X\pm A}</math>, <math>D_{X\pm B}</math>, <math>CLK+A</math>, <math>CLK+B</math>)</b>					
$V_{ID}$	Receiver peak-to-peak differential input voltage	150		1560	mVp-p
$V_{IC}$	Input common mode voltage	2		$V_{DD} + 0.01$	V
$V_{DD}$	TMDS output termination voltage	3.135	3.3	3.465	V
$R_T$	Termination resistance	45	50	55	Ohm
	Signaling rate	0		2.5	Gbps
<b>Control Pins (<math>OC_{Sx}</math>, <math>EQ_{Sx}</math>, <math>SEL</math>, <math>\overline{OE}</math>)</b>					
$V_{IH}$	LVTTL High-level input voltage	2		$V_{DD}$	V
$V_{IL}$	LVTTL Low-level input voltage	GND		0.8	
<b>DDC Pins (<math>SCL</math>, <math>SCL\_SINK</math>, <math>SDA</math>, <math>SDA\_SINK</math>)</b>					
$V_{I(DDC)}$	Input voltage	GND		5.5	V
<b>Status Pins (<math>HPD\_SINK</math>)</b>					
$V_{IH}$	LVTTL High-level input voltage	2		5.3	V
$V_{IL}$	LVTTL Low-level input voltage	GND		0.8	

**TMDS Compliance Test Results**

Item	HDMI™ 1.3 Spec	Pericom Product Spec
<b>Operating Conditions</b>		
Termination Supply Voltage, $V_{DD}$	$3.3V \leq 5\%$	$3.30 \pm 5\%$
Terminal Resistance	50-Ohm $\pm 10\%$	45 to 55-Ohm
<b>Source DC Characteristics at TP1</b>		
Single-ended high level output voltage, $V_H$	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$
Single-ended low level output voltage, $V_L$	$(V_{DD} - 600mV) \leq V_L \leq (V_{DD} - 400mV)$	$(V_{DD} - 600mV) \leq V_L \leq (V_{DD} - 400mV)$
Single-ended output swing voltage, $V_{swing}$	$400mV \leq V_{swing} \leq 600mV$	$400mV \leq V_{swing} \leq 600mV$
Single-ended standby (off) output voltage, $V_{off}$	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$
<b>Transmitter AC Characteristics at TP1</b>		
Risetime/Falltime (20%-80%)	$75ps \leq \text{Risetime/Falltime} \leq 0.4 \text{ Tbit}$ ( $75ps \leq tr/tf \leq 242ps$ ) @ 1.65 Gbps	240ps
Intra-Pair Skew at Transmitter Connector, max	0.15 Tbit (90.9ps @ 1.65 Gbps)	60ps max
Inter-Pair Skew at Transmitter Connector, max	0.2 Tpixel (1.2ns @ 1.65 Gbps)	100ps max
Clock Jitter, max	0.25 Tbit (151.5ps @ 1.65 Gbps)	82ps max
<b>Sink Operating DC Characteristics at TP2</b>		
Input Differential Voltage Level, $V_{diff}$	$150 \leq V_{diff} \leq 1200mV$	$150mV \leq V_{DIFF} \leq 1200mV$
Input Common Mode Voltage Level, $V_{ICM}$	$(V_{DD} - 300mV) \leq V_{icm} \leq (V_{DD} - 37.5mV)$ Or $V_{DD} \pm 10\%$	$(V_{DD} - 300mV) \leq V_{icm} \leq (V_{DD} - 37.5mV)$ Or $V_{DD} \pm 10\%$
<b>Sink DC Characteristics When Source Disabled or Disconnected at TP2</b>		
Differential Voltage Level	$V_{DD} \pm 10mV$	$V_{DD} \pm 10mV$

**Electrical Characteristics** (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units	
I <sub>CC</sub>	Supply Current	V <sub>IH</sub> = V <sub>DD</sub> , V <sub>IL</sub> = V <sub>DD</sub> - 0.4V, R <sub>T</sub> = 50-Ohm, V <sub>DD</sub> = 3.3V, OC_SX = LOW, x = 0, 1, 2		120		mA	
P <sub>D</sub>	Power Dissipation			400		mW	
I <sub>CCQ</sub>	Standby Current	OE = HIGH, SEL1 = Low, SEL2 = Low, V <sub>DD</sub> = 3.3V		8		mA	
<b>TMDS Differential Pins (D<sub>x±A</sub>, D<sub>x±B</sub>, D<sub>x±</sub>, CLK±A, CLK±B, CLK±)</b>							
V <sub>OH</sub>	Single-ended high-level output voltage	V <sub>DD</sub> = 3.3V, R <sub>T</sub> = 50-Ohm Pre-emphasis/De-emphasis = 0dB	V <sub>DD</sub> - 10		V <sub>DD</sub> + 10	mV	
V <sub>OL</sub>	Single-ended low-level output voltage		V <sub>DD</sub> - 600		V <sub>DD</sub> - 400		
V <sub>swing</sub>	Single-ended output swing voltage		400		600		
V <sub>OD(O)</sub>	Overshoot of output differential voltage				6%	15%	2x V <sub>swing</sub>
V <sub>OD(U)</sub>	Undershoot of output differential voltage				12%	25%	
ΔV <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states				0.5	5	mV
I <sub>(OS)</sub>	Short circuit output current				12	mA	
V <sub>ODE(SS)</sub>	Steady state output differential voltage	OC_Sx = GND, D <sub>x±AB</sub> = 250 Mbps HDMI™ data pattern, X = 0, 1, 2 CLK±A, B = 25 MHz clock	560		840	mVp-p	
V <sub>ODE(PP)</sub>	Peak-to-peak output differential voltage		800		1200		
V <sub>I(open)</sub>	Single-ended input voltage under high impedance input or open input	I <sub>I</sub> = 10μA	V <sub>DD</sub> - 10		V <sub>DD</sub> + 10	mV	
R <sub>INT</sub>	Input termination resistance	V <sub>IN</sub> = 2.9V	45	50	55	Ohm	
<b>DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)</b>							
I <sub>lkg</sub>	Input leakage current	V <sub>I</sub> = 5.5V	-50		50	μA	
		V <sub>I</sub> = V <sub>DD</sub>	-20		20		
C <sub>IO</sub>	Input/output capacitance	V <sub>I</sub> = 0V		7.5		pF	
R <sub>ON</sub>	Switch resistance	I <sub>O</sub> = 3mA, V <sub>O</sub> = 0.4V		25	50	Ohm	
V <sub>PASS</sub>	Switch output voltage	V <sub>I</sub> = 3.3V, I <sub>I</sub> = 100μA	1.5 <sup>(2)</sup>	2.0	2.5 <sup>(3)</sup>	V	
<b>Status Pins (HPD)</b>							
V <sub>OH(TTL)</sub>	TTL High-level output voltage	I <sub>OH</sub> = -4mA	2.4			V	
V <sub>OL(TTL)</sub>	TTL Low-level output voltage	I <sub>OL</sub> = 4mA			0.4	V	

(Table Continued)

**Electrical Characteristics** (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
<b>Control Pins (SEL, <math>\overline{\text{OE}}</math>)</b>						
I <sub>IH</sub>	High-level digital input current	V <sub>IH</sub> = 2.0V or V <sub>DD</sub>	-10		10	μA
I <sub>IL</sub>	Low-level digital input current	V <sub>IL</sub> = GND or 0.8V	-10		10	
<b>Status Pins (HPD_SINK)</b>						
I <sub>IH</sub>	High-level digital input current	V <sub>IH</sub> = 5.3V	-50		50	μA
		V <sub>IH</sub> = 2.0V or V <sub>DD</sub>	-10		10	
I <sub>IL</sub>	Low-level digital input current	V <sub>IL</sub> = GND or 0.8V	-10		10	

**Notes:**

1. All typical values are at 25°C and with a 3.3V supply.
2. The value is tested in full temperature range at 3.0V.
3. The value is tested in full temperature range at 3.6V.



**Switching Characteristics** (over recommended operating conditions unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(1)</sup>	Max.	Units
<b>TMDS Differential Pins (Dx±, CLK±)</b>						
t <sub>pd</sub>	Propagation delay	V <sub>DD</sub> = 3.3V, R <sub>T</sub> = 50-Ohm, pre-emphasis/de-emphasis = 0dB			2000	ps
t <sub>r</sub>	Differential output signal rise time (20% - 80%)		75		240	
t <sub>f</sub>	Differential output signal fall time (20% - 80%)		75		240	
t <sub>sk(p)</sub>	Pulse skew			10	50	
t <sub>sk(D)</sub>	Intra-pair differential skew			23	50	
t <sub>sk(o)</sub>	Inter-pair differential skew <sup>(2)</sup>				100	
t <sub>jit(pp)</sub>	Peak-to-peak output jitter from CLK± residual jitter	pre-emphasis/de-emphasis = 0dB, Dx±A, B = 1.65 Gbps HDMI™ data pattern, x = 0, 1, 2 CLK±A, B = 165 MHz clock		15	30	ps
t <sub>jit(pp)</sub>	Peak-to-peak output jitter from Dx± residual jitter			18	50	
t <sub>DE</sub>	De-emphasis duration	de-emphasis = -3.5dB, Dx±A, B = 250 Mbps HDMI™ data pattern, x = 0, 1, 2 CLK±A, B = 25 MHz clock		240		
t <sub>sX</sub>	Select to switch output				10	ns
t <sub>en</sub>	Enable time				200	
t <sub>dis</sub>	Disable time				10	
<b>DDC I/O Pins (SCL, SCL_SINK, SDA, SDA_SINK)</b>						
t <sub>pd(DDC)</sub>	Propagation delay from SCLn to SCL_SINK or SDA <sub>n</sub> to SDA_SINK or SDA_SINK to SDA <sub>n</sub>	C <sub>L</sub> = 10pF		0.4	2.5	ns
<b>Control and Status Pins (SEL, HPD_SINK, HPD)</b>						
t <sub>pd(HPD)</sub>	Propagation delay (from HPD_SINK to the active port of HPD)	C <sub>L</sub> = 10pF		2	6.0	ns
t <sub>sx(HPD)</sub>	Switch time (from port select to the lat- est valid status of HPD)			3	6.5	

**Notes:**

- All typical values are at 25°C and with a 3.3V supply.
- t<sub>sk(o)</sub> is the magnitude of the difference in propagation delay times between any specified terminals of channel 2 to 4 of a device when inputs are tied together.

## Application Information

### Supply Voltage

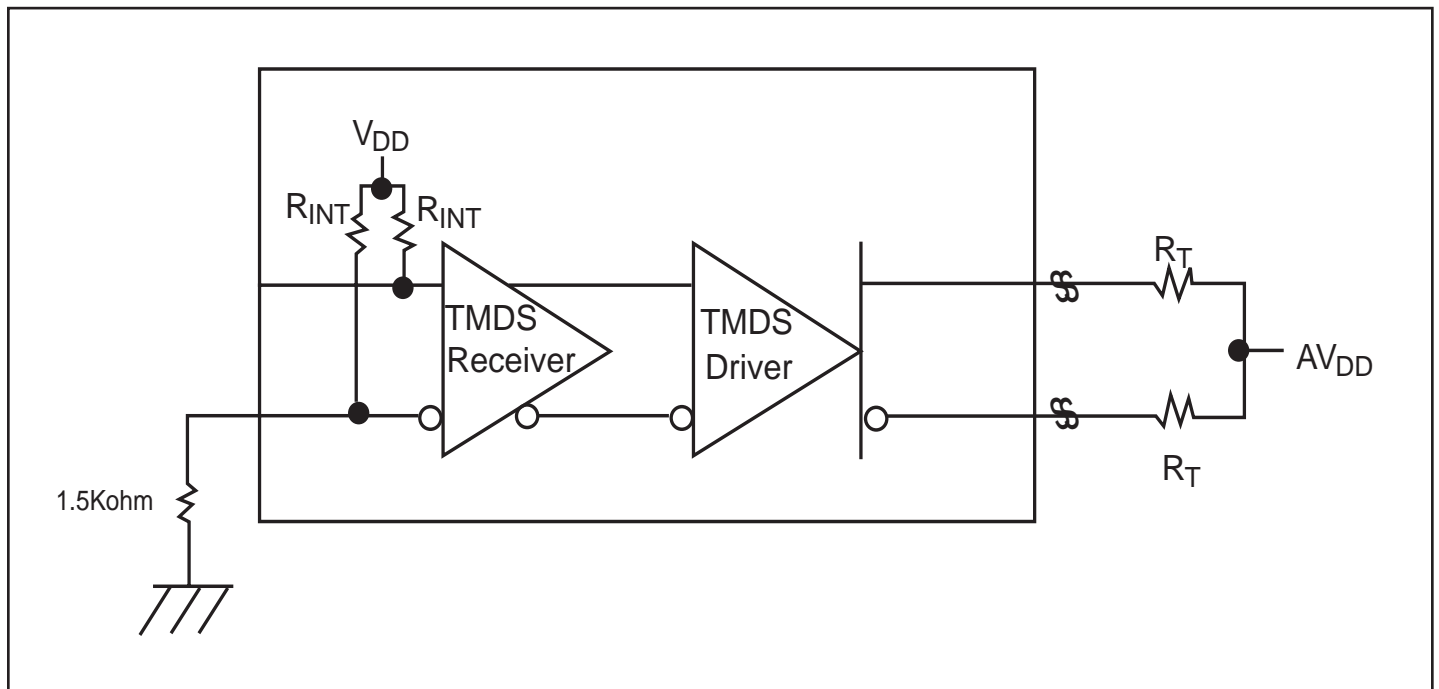
All V<sub>DD</sub> pins are recommended to have a 0.1μF capacitor tied from V<sub>DD</sub> to GND to filter supply noise

### TMDS inputs

Standard TMDS terminations have already been integrated into Pericom's PI3HDMI201 device. Therefore, external terminations are not required. Any unused port must be left floating and not tied to GND.

### TMDS output oscillation elimination

The TMDS inputs do not incorporate a squelch circuit. Therefore, we recommend the input to be externally biased to prevent output oscillation. One pin will be pulled high to  $V_{DD}$  with the other grounded through a 1.5Kohm resistor as shown.



TMDS Input Fail-Safe Recommendation

### Recommended Power Supply Decoupling Circuit

Figure 1 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1µF decoupling capacitors on each V<sub>DD</sub> pins of our part, there are four 0.1µF decoupling capacitors are put in Figure 1 with an assumption of only four V<sub>DD</sub> pins on our part, if there is more or less V<sub>DD</sub> pins on our Pericom parts, the number of 0.1µF decoupling capacitors should be adjusted according to the actual number of V<sub>DD</sub> pins. On top of 0.1µF decoupling capacitors on each V<sub>DD</sub> pins, it is recommended to put a 10µF decoupling capacitor near our part's V<sub>DD</sub>, it is for stabilizing the power supply for our part. Ferrite bead is also recommended for isolating the power supply for our part and other power supplies in other parts of the circuit. But, it is optional and depends on the power supply conditions of other circuits.

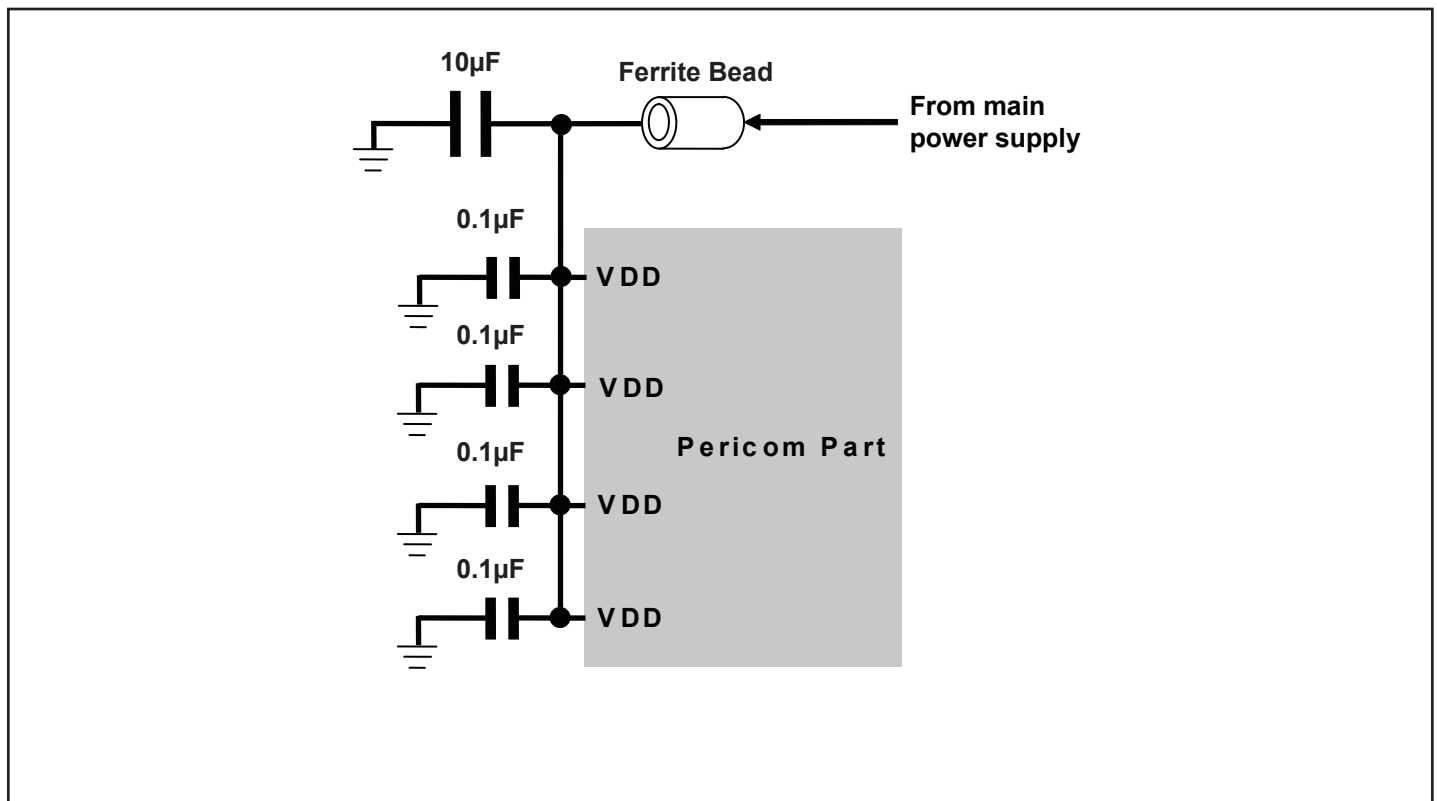


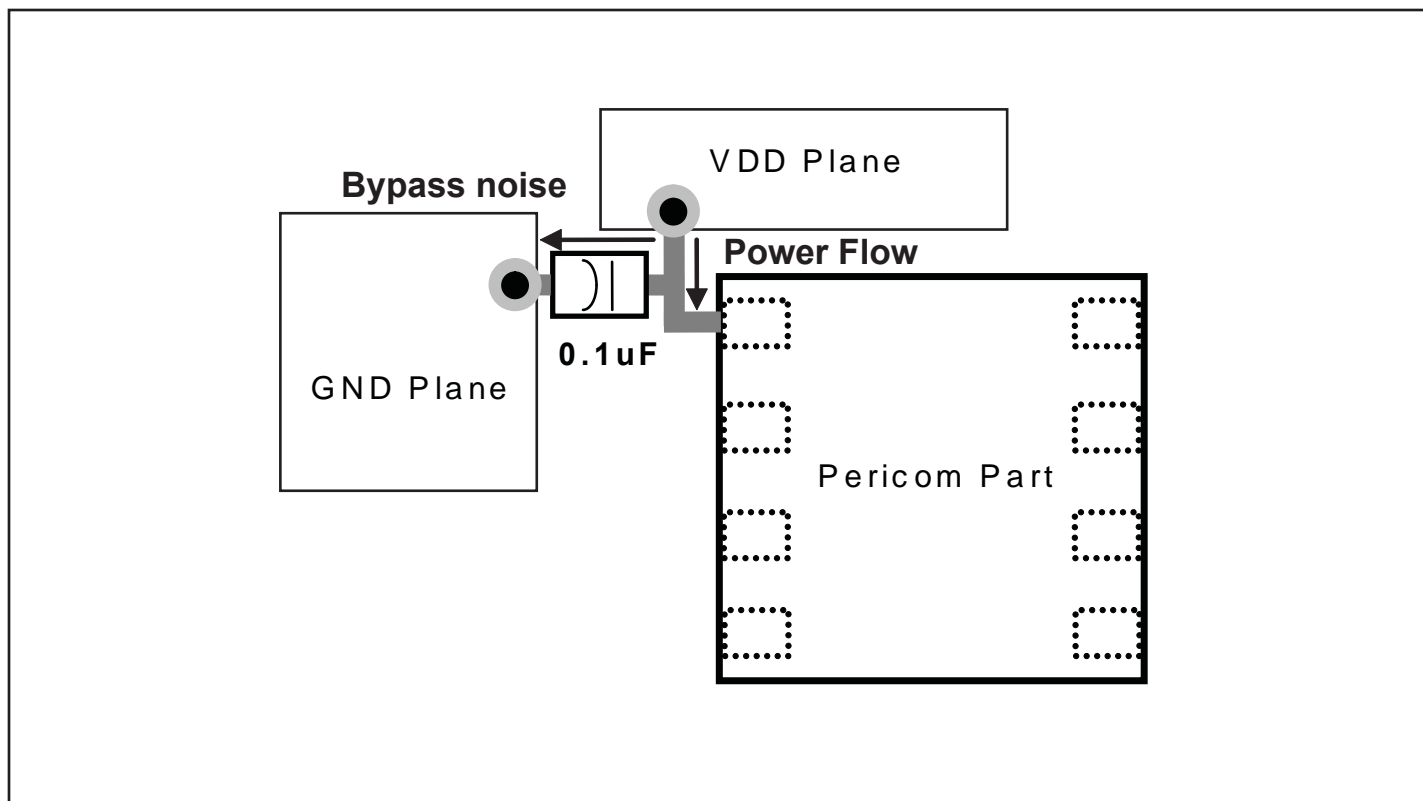
Figure 1 Recommended Power Supply Decoupling Circuit Diagram

### Requirements on the Decoupling Capacitors

There is no special requirement on the material of the capacitors. Ceramic capacitors are generally being used with typically materials of X5R or X7R.

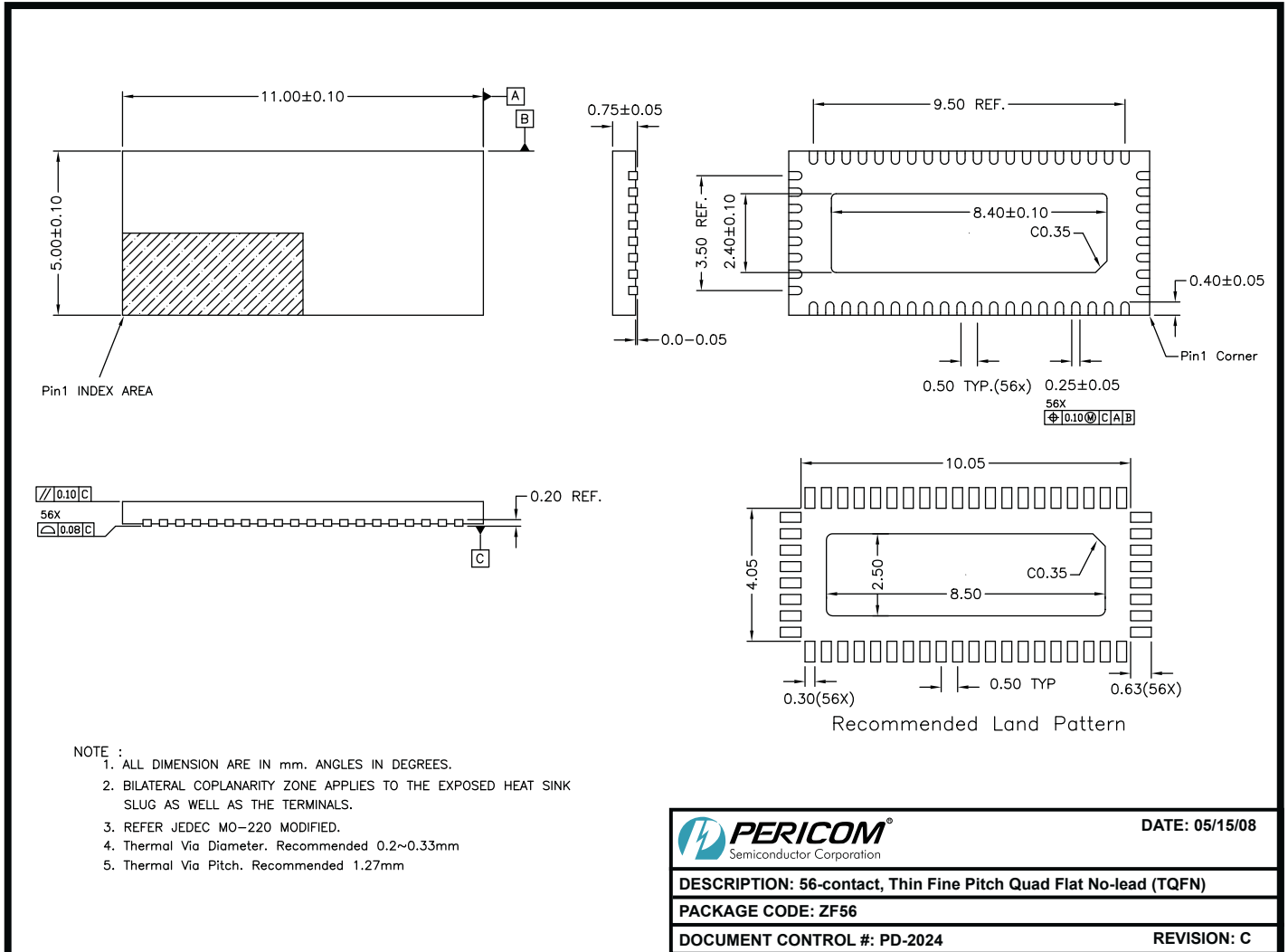
### Layout and Decoupling Capacitor Placement Consideration

- i. Each 0.1μF decoupling capacitor should be placed as close as possible to each V<sub>DD</sub> pin.
- ii. V<sub>DD</sub> and GND planes should be used to provide a low impedance path for power and ground.
- iii. Via holes should be placed to connect to V<sub>DD</sub> and GND planes directly.
- iv. Trace should be as wide as possible
- v. Trace should be as short as possible.
- vi. The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- vii. 10μF capacitor should also be placed closed to our part and should be placed in the middle location of 0.1μF capacitors.
- viii. Avoid the large current circuit placed close to our part; especially when it is shared the same V<sub>DD</sub> and GND planes. Since large current flowing on our V<sub>DD</sub> or GND planes will generate a potential variation on the V<sub>DD</sub> or GND of our part.



**Figure 2 Layout and Decoupling Capacitor Placement Diagram**

**Package Mechanical: 56-pin, Low Profile Quad Flat Package (ZF56)**



08-0208

**Ordering Information**

Ordering Code	Package Code	Package Description
PI3HDMI201ZFE	ZF	56-pin, Pb-free & Green TQFN

**Notes:**

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- Adding an X Suffix = Tape/Reel
- HDMI & DeepColor are trademarks of Silicon Image