

### 3. Applications

- Replacing mechanical switches
- Hermetically sealed keys on a keyboard
- Switches for medical applications
- Switches for use in explosive environments
- Audio control: on/off, channel, volume
- Sliders and wheel-switches
- Vandal proof switches
- Switches in or under the upholstery, leather, handles, mats, carpets, tiles and glass
- Switches for home automation
- Use of standard metal sanitary parts (for example a tap) as switch
- Portable communication and entertainment units
- White goods control panel

### 4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF8885T/1	SOIC28	plastic small outline package; 28 leads; body width 7.5 mm	PCF8885T
PCF8885TS/1	TSSOP28	plastic small outline package; 28 leads; body width 4.4 mm	PCF8885TS

### 5. Marking

Table 2. Marking codes

Type number	Marking code
PCF8885T/1	PCF8885T
PCF8885TS/1	PCF8885TS

6. Block diagram

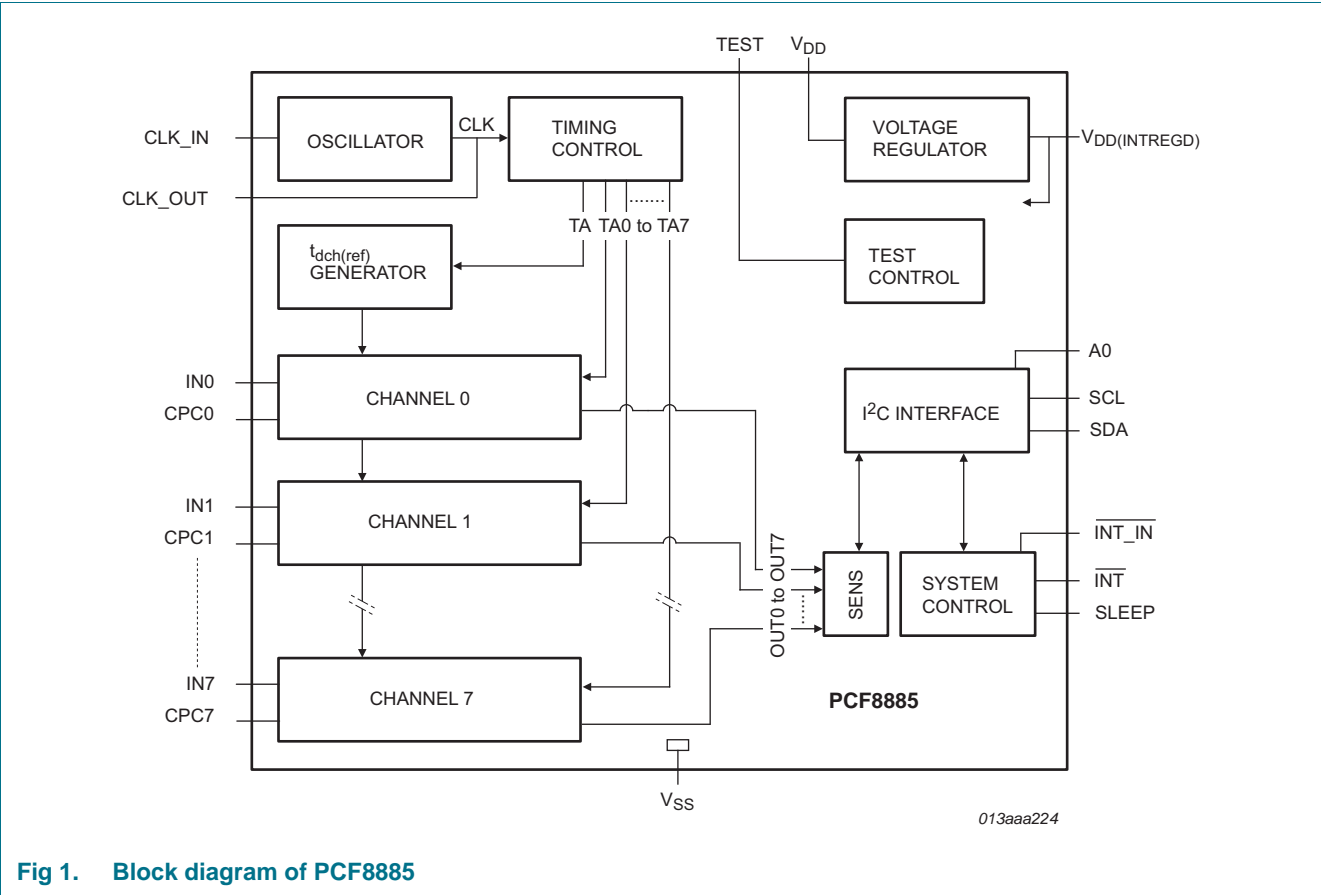
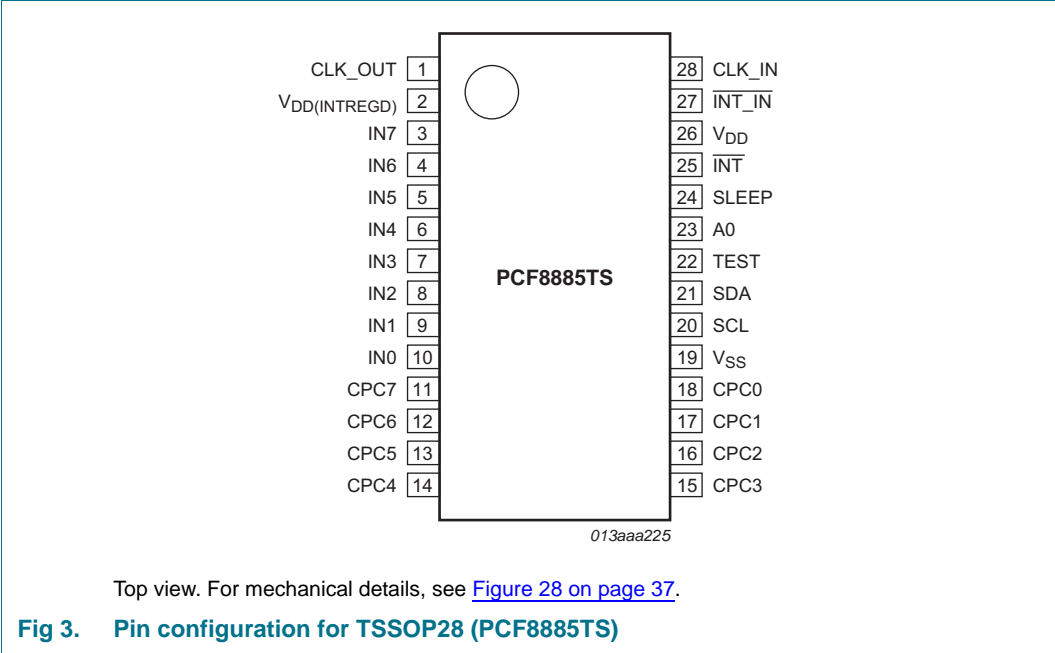
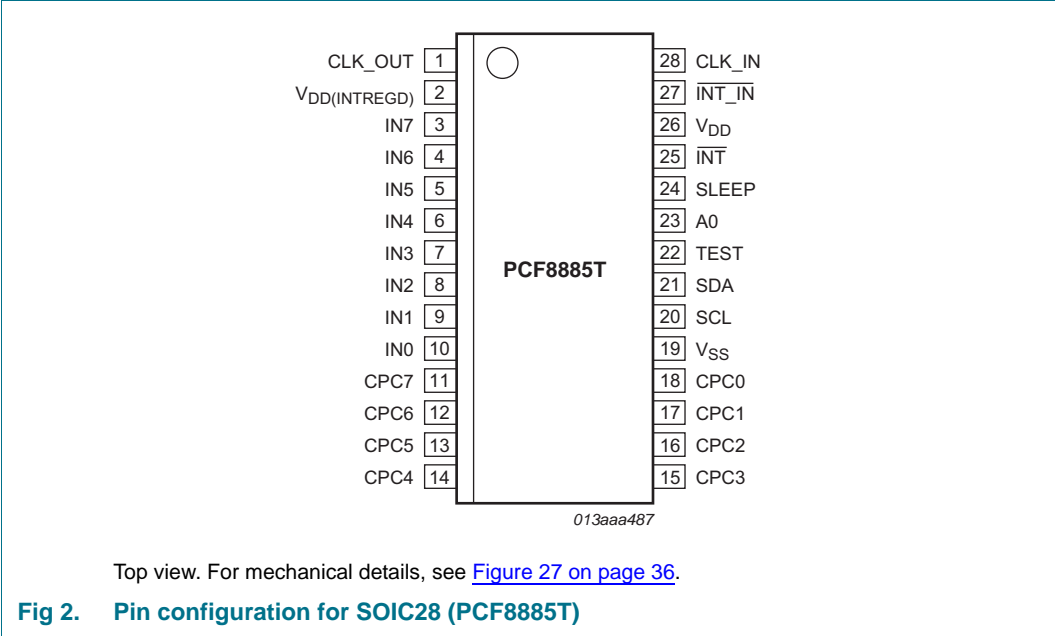


Fig 1. Block diagram of PCF8885

7. Pinning information

7.1 Pinning



## 7.2 Pin description

Table 3. Pin description

Symbol	Pin		Type	Description
	PCF8885T	PCF8885TS		
CLK_OUT	1	1	output	clock output for chip cascading and synchronization
V <sub>DD(INTREGD)</sub> <sup>[1]</sup>	2	2	supply	internal regulated supply reference voltage
IN7 to IN0	3 to 10	3 to 10	analog input/output	sensor input, channel 0 to 7 <sup>[2]</sup>
CPC7 to CPC0	11 to 18	11 to 18	analog input/output	reservoir capacitor, channel 0 to 7 <sup>[2]</sup>
V <sub>SS</sub>	19	19 <sup>[3]</sup>	supply	ground supply voltage
SCL	20	20	input	serial clock line
SDA	21	21	input/output	serial data line
TEST	22	22	input	test pin; must be connected to V <sub>SS</sub>
A0	23	23	input	I <sup>2</sup> C subaddress LSB <sup>[4]</sup>
SLEEP	24	24	input	sleep mode; connect to V <sub>DD</sub> to force the circuit into low-power sleep mode
$\overline{\text{INT}}$	25	25	output	interrupt output
V <sub>DD</sub>	26	26	supply	supply voltage
$\overline{\text{INT\_IN}}$	27	27	input	interrupt input for chip cascading; connect to V <sub>DD</sub> if not used
CLK_IN	28	28	input	clock input; for the secondary chip when the primary chip provides the clock signal

[1] The internal regulated supply voltage output must be decoupled with a decoupling capacitor to V<sub>SS</sub>.

[2] If a channel is not used, the appropriate sensor input line has to be left open, the corresponding CPCn has to be connected to V<sub>SS</sub> and the channel should be disabled in the MASK register (see [Table 10 on page 16](#)).

[3] The die paddle (exposed pad) is connected to V<sub>SS</sub> and should be electrically isolated.

[4] Used to address two devices, for example: low address 3Ah, high address 3Bh.

8. Functional description

The sensing plates have to be connected to the sensor input pins IN0 to IN7. The discharge times ( $t_{dch}$ ) on the sensor input pins, are compared to the discharge time ( $t_{dch(ref)}$ ) of an internal RC timing element. The comparison is done sequentially for each sensor input pin. The RC timing circuits are periodically charged from  $V_{DD(INTREGD)}$  and then discharged via a resistor to  $V_{SS}$ . The charge-discharge cycle for each channel is governed by the sampling rate ( $f_s$ ). The channels are sampled sequentially, while the reference element is activated at the sampling point of each channel (see timing diagram in [Figure 4](#)).

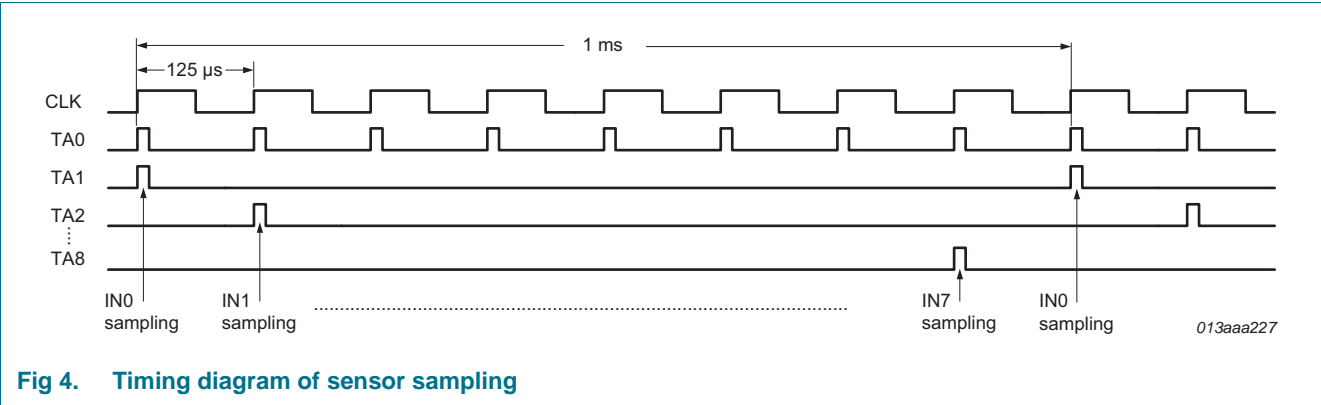


Fig 4. Timing diagram of sensor sampling

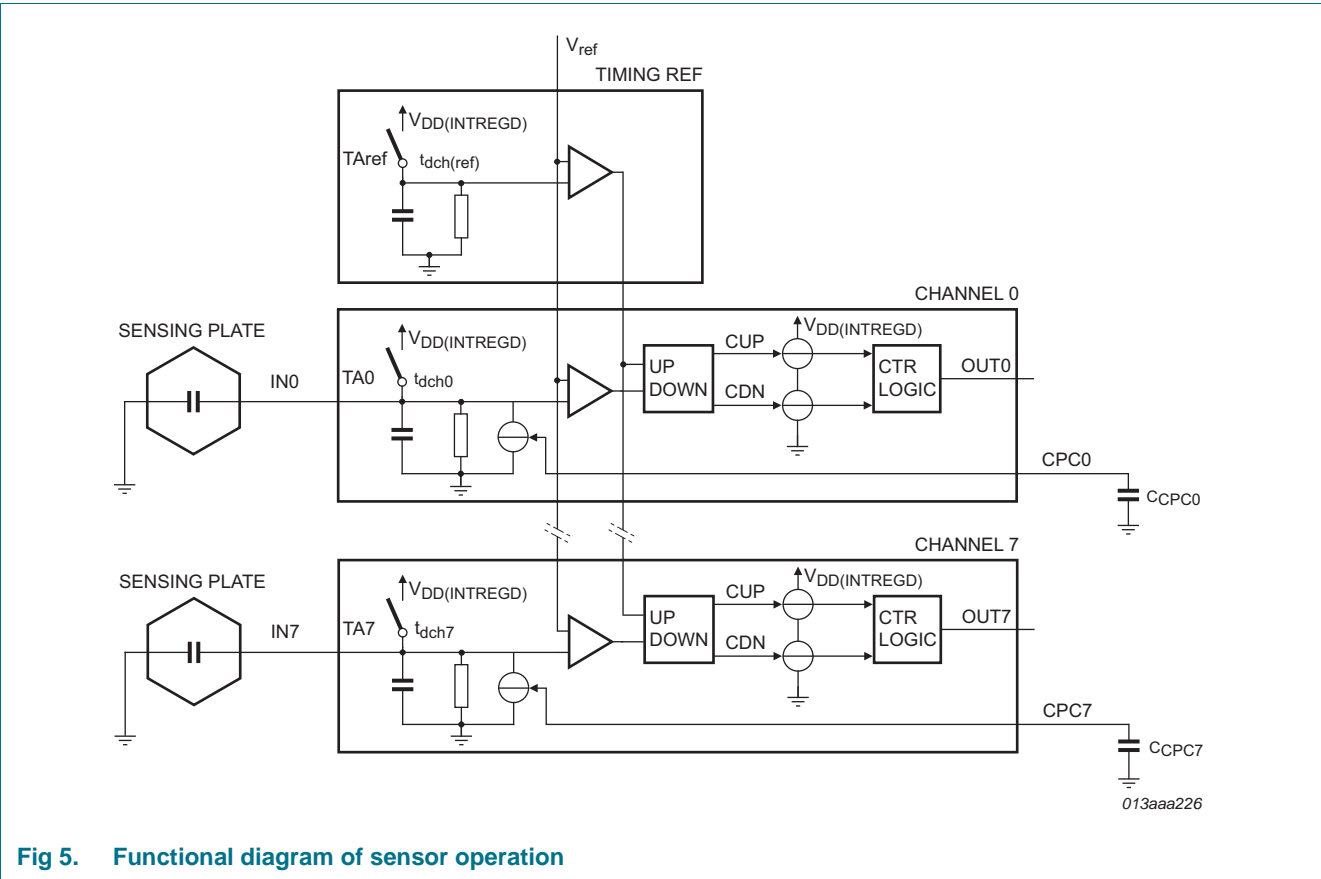


Fig 5. Functional diagram of sensor operation

When the voltage of an RC combination falls below the level  $V_{ref}$ , the appropriate comparator output changes. The logic following the comparators determines which comparator switched first. If the reference comparator switched first, then a pulse is given on CUP. If the sensor comparator switched first, then a pulse is given on CDN. [Figure 5](#) illustrates the functional principle of the PCF8885.

The pulses control the charge on the external capacitors  $C_{CPC}$  on pins CPC0 to CPC7. Every time a pulse is given on CUP, the capacitor  $C_{CPC}$  is charged through a current source ( $I_{source}$ ) from  $V_{DD(INTREGD)}$  for a fixed time causing the voltage on  $C_{CPC}$  to rise by a small increment. Likewise when a pulse occurs on CDN, capacitor  $C_{CPC}$  is discharged through a current sink ( $I_{sink}$ ) towards ground for a fixed time, causing the voltage on  $C_{CPC}$  to fall by a small decrement. The voltage on  $C_{CPC}$  controls an additional current sink ( $I_{CPC}$ ) that causes the capacitance attached to the input pins IN[0:7] to be discharged more quickly. This arrangement constitutes a closed loop control system, that constantly tries to equalize the discharge time ( $t_{dch}$ ) with the reference discharge time ( $t_{dch(ref)}$ ). In the equilibrium state, the discharge times are nearly equal and the pulses alternate between CUP and CDN.

The counter following this logic counts the pulses CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or the other way round. The outputs OUT0 to OUT7 are only activated when 64 consecutive pulses occurred on CUP. Low-level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

The sampling rate ( $f_s$ ) is derived from the internally generated oscillator frequency. The oscillator frequency can be adjusted within a specified range by programming the CLKREG register (see [Table 9 on page 14](#)).

The status of the output signals OUT0 to OUT7 is stored in the SENS register (see [Table 8 on page 14](#)). An interrupt is generated on changes of the sensor states.

## 9. Commands

The operation of the PCF8885 can be controlled by 12 commands and four configuration- and status-registers (see [Section 10 on page 10](#)). Several configuration settings can be programmed using single commands without associated data transfer. The configuration register can however also be written using the write-config command. The clock and mask registers can only be programmed using the write-clock and write-mask commands.

### 9.1 Command overview

**Table 4. Commands of PCF8885**

Command	Operation code	Description	Transfer type	Reference
soft-reset	00000000	brings chip to reset state	command	<a href="#">Section 9.2</a> , <a href="#">Section 10.2.2.2</a>
clear-INT	00000011	deactivates interrupt generation on pin INT	command	<a href="#">Section 10.2.2.1</a>
sleep	00000101	enter sleep mode	command	<a href="#">Section 9.3</a>
wake-up	00000110	enter active mode	command	
write-config	00110000	write configuration register	write 1 byte	<a href="#">Section 10.2</a>
read-config	00110011	read configuration register	read 1 byte	
write-clock	00110101	write clock setting register	write 1 byte	<a href="#">Section 10.4</a>
read-clock	00110110	read clock setting register	read 1 byte	
write-mask	00111001	write the mask register	write 1 byte	<a href="#">Section 10.5</a>
read-mask	00111010	read the mask register	read 1 byte	
int-over-I <sup>2</sup> C	00111100	put the device in int-over-I <sup>2</sup> C mode	command	<a href="#">Section 10.2.2.1</a>
read-sensor	-	read sensor state register and clears the INT line	direct read	<a href="#">Section 9.4</a> , <a href="#">Section 10.2.2.1</a>

### 9.2 Command: soft-reset

Reset takes place during power-on of the circuit. There is no external hardware reset input.

During operation, the device can be reset using the soft-reset command. The sensor channels and all registers are reset to the default values and the int-over-I<sup>2</sup>C mode is terminated. It does not affect the state of the analog section except for those functions that are controlled by configuration bits.

### 9.3 Commands: Sleep and wake-up

Sleep mode is implemented to save power during periods where no sensor activity is expected or supported.

In sleep mode, most of the circuit parts are put in power-down mode, in particular all analog blocks consuming static and dynamic power. This includes the oscillator, thus no internal activity remains. Also the voltage regulator is powered down, to reduce its standalone power consumption.

During sleep mode, the register configuration is maintained and the device remains responsive to I<sup>2</sup>C commands. The charges in the CPC capacitors however cannot be guaranteed, as there is no limitation on the duration of the sleep mode. Therefore the analog part has to perform a normal start-up phase, including the fast start procedure for the CPC capacitor charging.

Sleep mode is entered when the sleep command is received from the system controller or when the SLEEP pin is set to HIGH. Resume is done by the wake-up command, or by setting the SLEEP pin to LOW.

The hardware sleep mechanism using the SLEEP pin and the software sleep mechanism using the sleep or wake-up commands are independent of each other:

- If the device was put to sleep using the sleep command, a wake-up command resumes the operation. It cannot be resumed by activating the SLEEP pin.
- If the device was put to sleep by setting pin SLEEP to HIGH, then pin SLEEP must be set to LOW to resume operation. It cannot be resumed with the wake-up command.

## 9.4 Command: read-sensor

The read-sensor command is the main transaction to read the actual state information of the sensor state register SENS.

If the  $\overline{R/W}$  bit (LSB of the I<sup>2</sup>C slave address byte, see [Table 11 on page 21](#)) is set logic 1 the PCF8885 regards the transaction as the read-sensor command. The read-sensor command transaction supports a repeated reading of the SENS register (see [Section 10.3 on page 14](#)). When two circuits are used in a cascaded configuration, they alternately return their SENS register content in a single transaction

The protocols for the repeated read mode and the alternating read mode are described in [Section 13.7 on page 21](#).



## 10. Registers

The PCF8885 has four registers storing the configuration and the status information of the device.

### 10.1 Register overview

**Table 5. Register overview**

The bit position labeled as *x* is not relevant; if read, it can be either logic 0 or logic 1.

Register name	Bit								Default value
	7	6	5	4	3	2	1	0	
CONFIG	OPM[1:0]		SWM	KM[1:0]		VROF	INTM	MSKMODE	00000000
SENS	CH[7:0]								00000000
CLKREG	CLO	CLI	x	FRQC[1:0]		FRQF[2:0]			00x01100
MASK	MSK[7:0]								11111111

### 10.2 Register: CONFIG

**Table 6. CONFIG - configuration register bit description**

Bit	Symbol	Value	Description	Reference
7 to 6	OPM[1:0]		main operation mode	<a href="#">Section 10.2.1.1</a>
		00 <sup>[1]</sup>	stand-alone device	
		01	secondary-chip in a cascade	
		10	primary-chip in a cascade	
		11	unused	
5	SWM		switching mode	<a href="#">Section 10.2.1.2</a>
		0 <sup>[1]</sup>	direct switching mode: sensor release clears the corresponding bit in the SENS register	
		1	latching mode: reading SENS register clears bits in the SENS register	
4 to 3	KM[1:0]		key-press mode	<a href="#">Section 10.2.1.3</a>
		00 <sup>[1]</sup>	N-key mode: each sensor activity is reflected in the SENS register	
		01	2-key mode: only first two keys are visible in the SENS register	
		10	1-key mode: only first key-press is visible in the SENS register	
		11	unused	

Table 6. CONFIG - configuration register bit description ...continued

Bit	Symbol	Value	Description	Reference
2	VROF		voltage regulation	<a href="#">Section 11</a>
		0 <sup>[1]</sup>	voltage regulation on	
		1	voltage regulation off	
1	INTM		interrupt generation mode	<a href="#">Section 10.2.2</a>
		0 <sup>[1]</sup>	an interrupt is generated by each bit changed in the SENS register (press and release)	
		1	an interrupt is generated by each bit set in the SENS register (press only)	
0	MSKMODE		channel masking mode	<a href="#">Section 10.5.1</a>
		0 <sup>[1]</sup>	normal power: masked out channels remain operational	
		1	low power: masked out channels are powered down	

[1] Default value.

All bits in this register can be written and read with the write-config and read-config commands.

## 10.2.1 Operating modes

### 10.2.1.1 Main operating modes

The PCF8885 can operate in three operating modes: as a stand-alone device or in a cascade as a primary-chip or a secondary-chip (see [Table 7](#)).

Table 7. Main operating modes

Conditions of	Main operating modes		
	Stand-alone <sup>[1]</sup>	Primary-chip	Secondary-chip
clock source	internal oscillator	internal oscillator	clock input
oscillator	enabled	enabled	disabled
clock output pin CLK_OUT	disabled	enabled	disabled
clock input pin CLK_IN	disabled	disabled	enabled

[1] Default operating mode after power-on.

The operating modes are implemented to support the application of two PCF8885 in the system (see [Section 13.8 on page 22](#)).

### 10.2.1.2 Switching modes

There is a one to one relationship between the channels IN[0:7] and the bits in the SENS register. The indication of the switching status of each channel is controlled by the two switching modes supported:

**Direct mode** — In direct mode, the sensor state is directly reflected in the SENS register. When the sensor is activated, the corresponding bit in the SENS register is immediately set logic 1. When the sensor is released, the bit is cleared (set logic 0) again. The bits are even cleared if the SENS register has not yet been read by the system controller.

**Latching mode** — In latching mode, every activated sensor sets the corresponding bit in the SENS register logic 1. When the sensor is released, the SENS register is unaffected. Reading the SENS register clears (set logic 0) those bits, whose sensor is not activated anymore.

After reset, the PCF8885 is set to direct switching mode.

### 10.2.1.3 Key-press modes

There are three key-press modes implemented in the PCF8885: N-key, 1-key, and 2-key mode.

**N-key mode** — In N-key mode, each sensor activity is reflected in register SENS according to the configured switching mode. The N-key mode is the default key-press mode after reset.

**1-key mode** — In 1-key mode, only the first sensor activation sets the corresponding bit in register SENS. All further activations of the other sensors are suppressed at the SENS register boundary. In this way, sensors in a keypad are masked out, which are activated accidentally because they are arranged next to the activated sensor.

The 1-key mode supports sensor matrix arrangements with two PCF8885, where one chip is attached to the columns and one to the rows (primary-chip and secondary-chip). Sensor activation sets 1 bit for the column and 1 bit for the row in the SENS register of the appropriate chip. Each activation of a sensor raises an interrupt. The system controller must handle the situation where the  $\overline{\text{INT}}$  is raised before the second sensor in the matrix has been activated.

**2-key mode** — In 2-key mode, only the two first sensor activations set the corresponding bits in register SENS. All further activations of the other sensors are suppressed at the SENS register boundary. This mode supports in particular the matrix arrangement of sensors using only one PCF8885, as illustrated in [Figure 26 on page 34](#). In this way, sensors in a matrix are masked out, which are activated accidentally because they are arranged next to the intended sensors. This mode properly handles a delay in sensor activation due to unequal sensor capacitance or area (non-centric sensor touching, and so on) as long as the intended sensors react before sensors which are activated accidentally. In 2-key mode, the  $\overline{\text{INT}}$  output is only activated after 2 bits have been set in the SENS register.

## 10.2.2 Interrupt generation

The PCF8885 provides two mechanisms to inform the system controller that a sensor activity has been detected.

### 10.2.2.1 Interrupt output $\overline{\text{INT}}$

The PCF8885 has an interrupt output,  $\overline{\text{INT}}$ , to flag to the system controller that a capacitive event has been detected. The controller can then fetch the sensor state by reading the SENS register over the I<sup>2</sup>C-bus.

The interrupt generation is controlled by the INTM bit in the CONFIG register (see [Table 6 on page 10](#)).

- If INTM is logic 0 (default), then the change (set or clear) of each bit in register SENS activates the  $\overline{\text{INT}}$  output.
- If INTM is logic 1, then only sensor press events, resulting in bits being set logic 1 in the SENS register, activate the  $\overline{\text{INT}}$  output. Sensor release events, which cause the corresponding bit in SENS to be cleared (set logic 0), do not activate the  $\overline{\text{INT}}$  output.

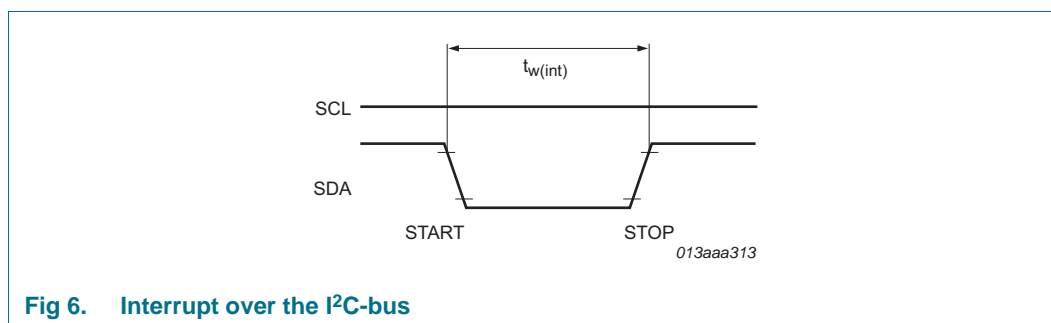
In 2-key mode, the  $\overline{\text{INT}}$  output is only activated after 2 bits have been set in the SENS register.

The interrupt is automatically cleared when the system controller reads the SENS register. Alternatively the  $\overline{\text{INT}}$  can be cleared by using the clear-INT command, without reading the actual sensor state.

#### 10.2.2.2 Interrupt over the I<sup>2</sup>C-bus

In applications where the sensing plates are remote from the microcontroller, the interrupt line can be saved by enabling the interrupt over I<sup>2</sup>C-bus.

The PCF8885 provides the feature of interrupt over the I<sup>2</sup>C-bus. The PCF8885 then behaves like an I<sup>2</sup>C master with restricted functionality. The interrupt is signaled by setting a START condition immediately followed by a STOP condition. It is illustrated in [Figure 6](#). No further I<sup>2</sup>C master capabilities are supported.



**Fig 6. Interrupt over the I<sup>2</sup>C-bus**

The system controller has to detect the START-STOP condition and react accordingly.

The interrupt over the I<sup>2</sup>C-bus can be enabled with the int-over-I<sup>2</sup>C command and disabled with the soft-reset command.

In interrupt over the I<sup>2</sup>C-bus mode, the functionality of the  $\overline{\text{INT}}$  output continues to work as described in [Section 10.2.2.1](#).

### 10.3 Register: SENS

Table 8. SENS - sensor state register bit description

Bit	Symbol	Value	Description
7 to 0	CH[7:0]	00000000 <sup>[1]</sup> to 11111111	sensor state of the respective channels IN7 to IN0

[1] Default value.

All bits in this register are read-only and can be read with the read-sensor command (see [Section 9.4](#)).

### 10.4 Register: CLKREG

Table 9. CLKREG - clock setting register bit description

Bit	Symbol	Value	Description
7	CLO		CLK_OUT switch
		0 <sup>[1]</sup>	CLK_OUT disabled (unless IC is in primary-chip mode)
		1	CLK_OUT enabled
6	CLI		CLK_IN switch
		0 <sup>[1]</sup>	CLK_IN disabled (unless IC is in secondary-chip mode)
		1	CLK_IN enabled, internal oscillator is powered down
5	-	- <sup>[2]</sup>	unused
4 to 3	FRQC[1:0]		clock frequency, coarse setting
		00	$f_{clk} = f_{osc}/64$
		01 <sup>[1]</sup>	$f_{clk} = f_{osc}/16$
		10	$f_{clk} = f_{osc}/4$
		11	$f_{clk} = f_{osc}$
2 to 0	FRQF[2:0]		oscillator tuning
		000	$f_{osc} = 0.5 \times f_{osc(nom)}$
		001	$f_{osc} = 0.625 \times f_{osc(nom)}$
		010	$f_{osc} = 0.75 \times f_{osc(nom)}$
		011	$f_{osc} = 0.875 \times f_{osc(nom)}$
		100 <sup>[1]</sup>	$f_{osc} = 1 \times f_{osc(nom)}$
		101	$f_{osc} = 1.25 \times f_{osc(nom)}$
		110	$f_{osc} = 1.5 \times f_{osc(nom)}$
		111	$f_{osc} = 1.75 \times f_{osc(nom)}$

[1] Default value.

[2] Should always be written with logic 0 and if read, it can be either logic 0 or logic 1.

All bits in this register can be written and read with the write-clock and read-clock commands.

#### 10.4.1 Clock generation and frequency adjustment

The PCF8885 contains an integrated oscillator as main clock source. With the values of FRQF[2:0], the oscillator frequency can be tuned (see [Equation 1](#)).

$$f_{osc} = m \times f_{osc(nom)} \quad (1)$$

The values of  $m$  can be varied in the range  $0.5 \leq m \leq 1.75$ , where  $m = 1.0$  corresponds to the default value of FRQF[2:0] = 100.

The internal clock frequency ( $f_{clk}$ ) is derived from the oscillator frequency with [Equation 2](#):

$$f_{clk} = f_{osc}/n \quad (2)$$

where the values for  $n$  are 1, 4, 16, or 64 and can be selected with FRQC[1:0]. The sensor sampling frequency ( $f_s$ ) is derived from the internal clock frequency with [Equation 3](#):

$$f_s = f_{clk}/8 \quad (3)$$

The eight sensors are sampled sequentially, which results in a default sensor sampling rate  $f_s$ .

In secondary-chip mode, the internal clock generator is stopped, and the circuit is clocked from the CLK\_IN input pin.

The tuning of the oscillator frequency and the programmable clock divider (see [Figure 7](#)) allows changing the sensor sampling rate, the adjustment of the reaction time and the power consumption of the PCF8885 over a wide range.

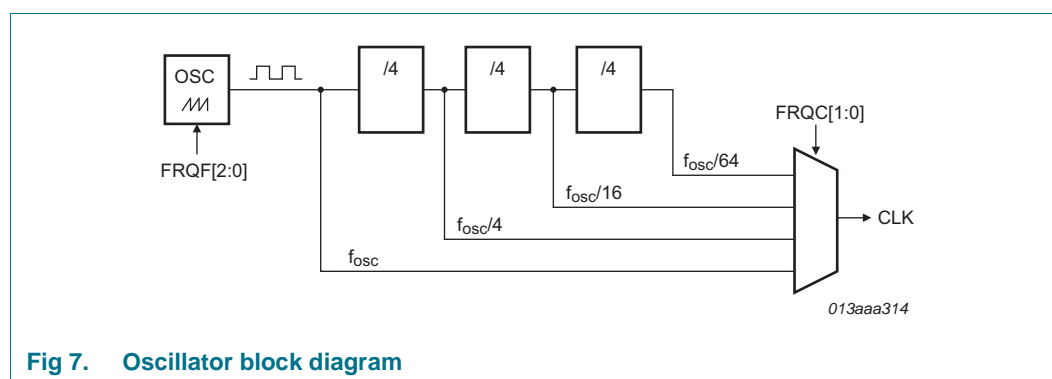


Fig 7. Oscillator block diagram

10.5 Register: MASK

Table 10. MASK - channel enable mask register bit description

Bit	Symbol	Value	Description
7 to 0	MSK[7:0]	00000000 to 11111111 <sup>[1]</sup>	enable or disable the respective sensor channels IN0 to IN7
		0	sensor channel is disabled
		1	sensor channel is enabled

[1] Default value.

All bits in this register can be written and read with the write-mask and read-mask commands.

10.5.1 Channel masking

The channel masking register MASK allows individual sensor channels to be enabled or disabled for particular applications or certain modes (for example only the on/off sensor should be active).

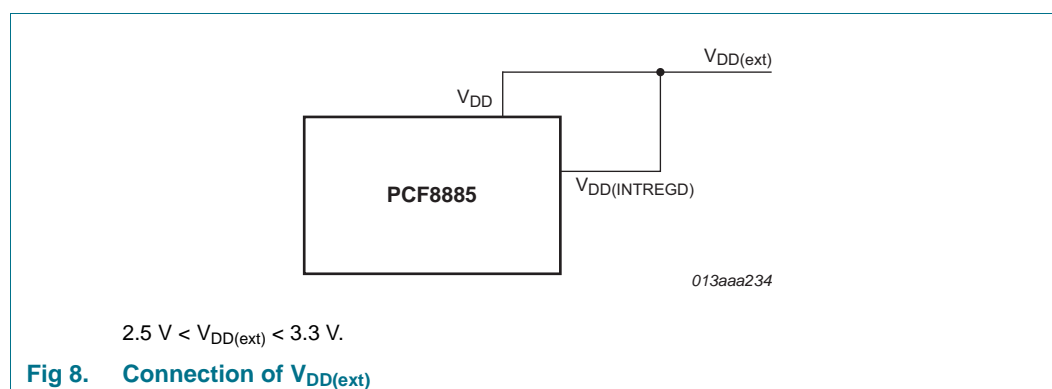
- When bit MSKMODE in register CONFIG (see [Table 6](#)) is set logic 0, then the disabled channels are continuously sampled, but switching events are not reflected in register SENS and do not cause interrupts.
- When bit MSKMODE in register CONFIG (see [Table 6](#)) is set logic 1, only channels which are enabled are sampled. Reducing the number of sampled channels also reduces the power consumption.

When a channel becomes newly enabled, the fast start-up method (see [Section 12](#)) is used to reach the functional state quickly.

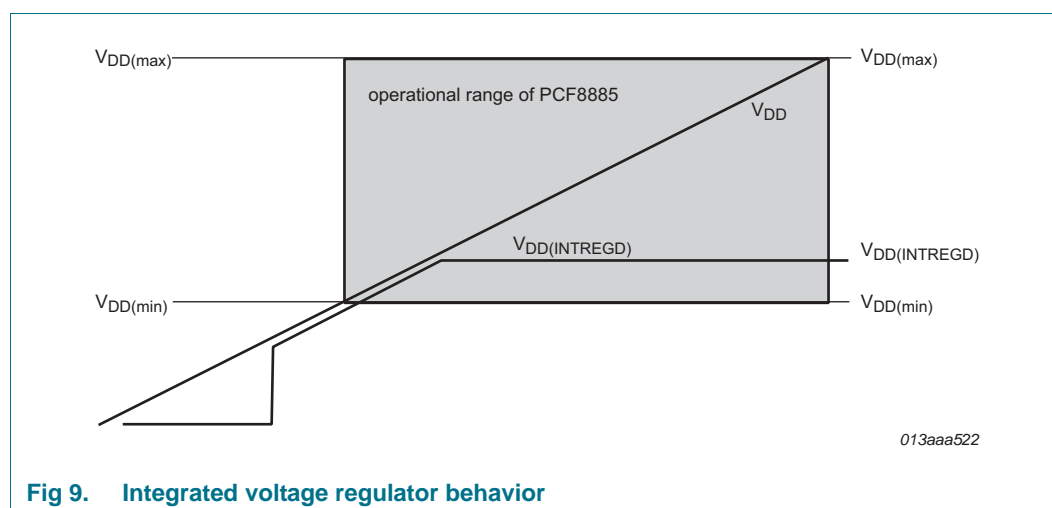
## 11. Power architecture

The circuit has an integrated voltage regulator, supplied by pin  $V_{DD}$ . The regulator provides an internal  $V_{DD(INTREGD)}$  supply of nominally 2.8 V.

If a stable and noise free external supply voltage with  $2.5\text{ V} < V_{DD(EXT)} < 3.3\text{ V}$  is available in the system,  $V_{DD(INTREGD)}$  can be provided from an external source (see [Figure 8](#)). In this case  $V_{DD}$  and  $V_{DD(INTREGD)}$  must both be connected to  $V_{DD(EXT)}$ . To reduce the current consumption, the internal voltage regulator should be shut down by setting bit VROF logic 1 (see [Table 6 on page 10](#)).



While the analog part of the circuit is powered from  $V_{DD(INTREGD)}$ , the I<sup>2</sup>C interface and the registers are powered from  $V_{DD}$ . Therefore the I<sup>2</sup>C interface remains accessible in sleep mode, and the register values are maintained when  $V_{DD(INTREGD)}$  is powered off.



[Figure 9](#) illustrates the behavior of the integrated voltage regulator. The gray area covers the operational range of the PCF8885. The analog part of the circuit and the switch logic is powered from  $V_{DD(INTREGD)}$ . The I<sup>2</sup>C interface and the registers are powered from  $V_{DD}$ . Therefore the I<sup>2</sup>C interface remains accessible in sleep mode, and the register values are maintained when  $V_{DD(INTREGD)}$  is powered off.



## 12. Start-up procedure

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After power-on the registers in the  $V_{DD}$  domain are reset, which includes the VROF bit controlling the voltage regulator. The regulator is therefore enabled, and the  $V_{DD(INTREGD)}$  domain is powered on. As soon as a sufficient  $V_{DD(INTREGD)}$  level is reached, the Power-On Reset (POR) is released.

After release of the POR in the  $V_{DD(INTREGD)}$  domain, the circuit starts with the sensor sampling in the fast start mode (increased charge-pump currents quickly charge the CPC capacitors close to their target value). As soon as the capacitor voltages are close to the target value, the fast start phase is terminated, and the capacitors are charged in fine steps to the final value. When this state is reached, the logic enables the up and down counters, and the sensors are operational.

This start-up mechanism is executed independently for each channel.

## 13. Characteristics of the I<sup>2</sup>C-bus

The PCF8885 has an I<sup>2</sup>C serial interface which operates as a slave receiver or transmitter. SDA and SCL are the data I/O and clock lines for the serial I<sup>2</sup>C Interface. SDA is used as an input or as an open-drain output. SDA is actively pulled LOW and is passively held HIGH by the external pull-up resistor on the I<sup>2</sup>C-bus.

In order to provide high link robustness, the I<sup>2</sup>C interface of the PCF8885 is Fast-mode compatible and provides a robust addressing and command scheme.

### 13.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see [Figure 10](#)).

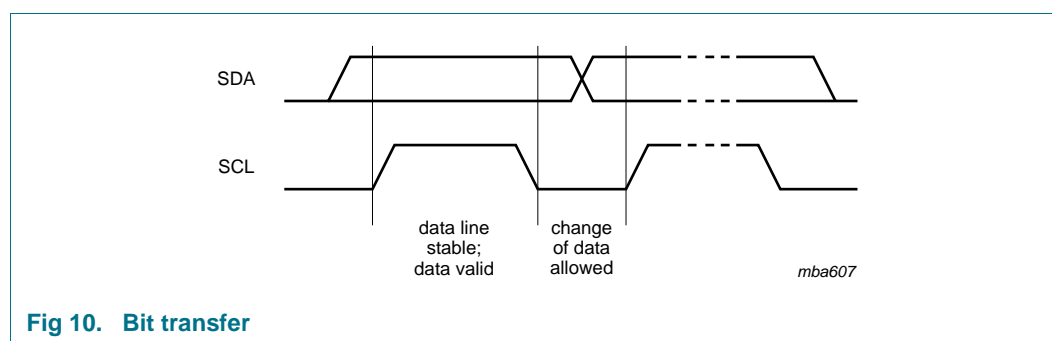


Fig 10. Bit transfer

#### 13.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are shown in [Figure 11](#).

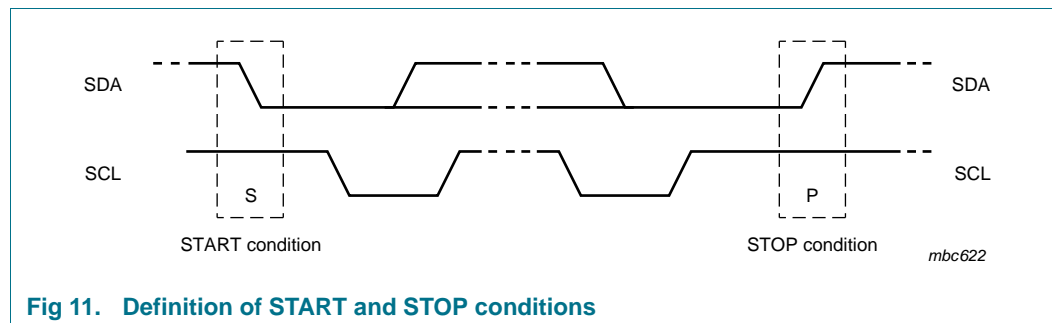


Fig 11. Definition of START and STOP conditions

### 13.2 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in [Figure 12](#).

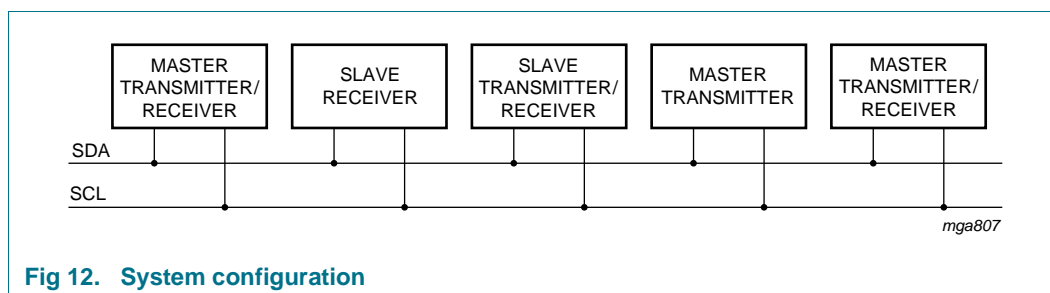


Fig 12. System configuration

### 13.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I<sup>2</sup>C-bus is shown in [Figure 13](#).

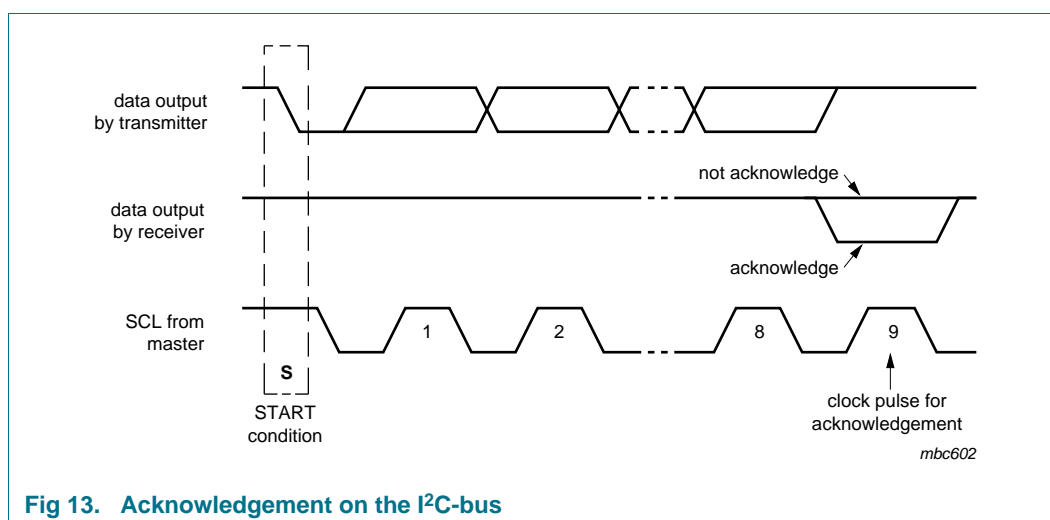


Fig 13. Acknowledgement on the I<sup>2</sup>C-bus

13.4 I<sup>2</sup>C-bus subaddress

Device selection depends on the I<sup>2</sup>C-bus slave address, on the transferred command data, and on the hardware subaddress.

Two I<sup>2</sup>C-bus slave addresses are used to address the PCF8885 (see [Table 11](#)).

Table 11. I<sup>2</sup>C slave address byte

Bit	Slave address							0
	7	6	5	4	3	2	1	
	MSB							LSB
Slave address	0	1	0	0	0	0	A0	R/W

The least significant bit of the slave address is bit  $R/\overline{W}$ . Bit 1 of the slave address is defined by connecting input A0 to either  $V_{SS}$  (logic 0) or  $V_{DD}$  (logic 1). Therefore, two instances of PCF8885 can be distinguished on the same I<sup>2</sup>C-bus.

13.5 I<sup>2</sup>C-bus protocol

The I<sup>2</sup>C-bus protocol is shown in [Figure 14](#). The sequence is initiated with a START condition (S) from the I<sup>2</sup>C-bus master which is followed by the slave address.

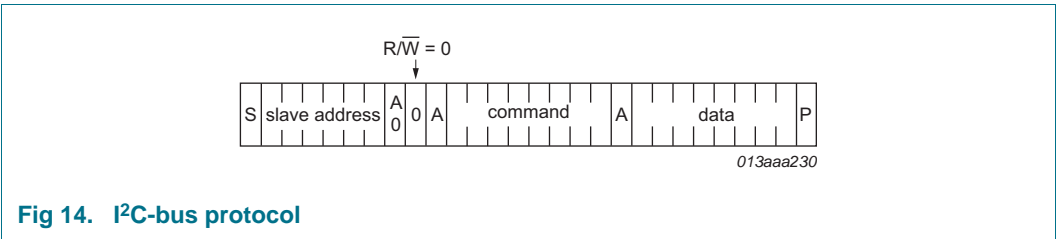


Fig 14. I<sup>2</sup>C-bus protocol

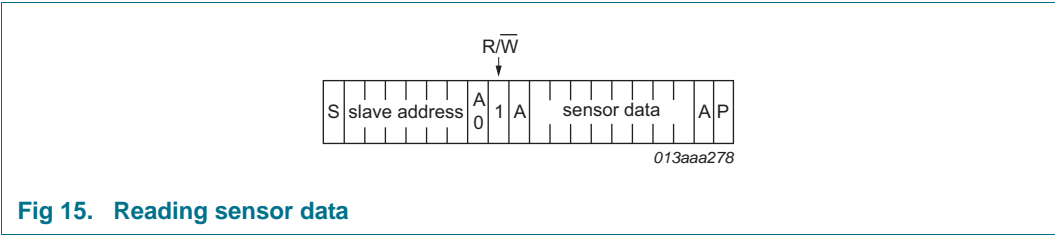
After acknowledgement, a command is sent, and after a further acknowledge a data byte is transmitted. After the last data byte, the I<sup>2</sup>C-bus master issues a STOP condition (P). Alternatively a START may be asserted to RESTART an I<sup>2</sup>C-bus access.

13.6 Fast-mode Plus (Fm+) support

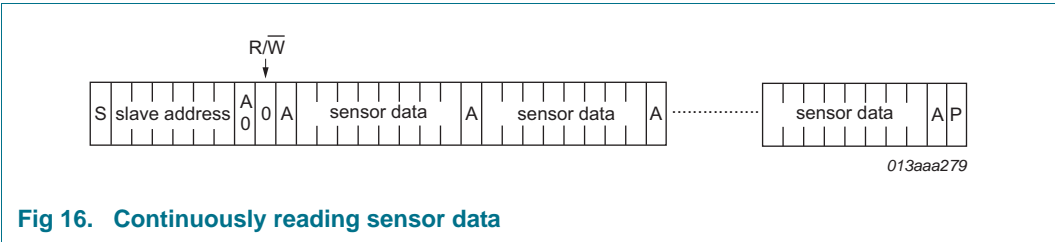
The Fast-mode Plus specification is supported. Besides providing a high transmission speed, the main characteristic of Fast-mode Plus is the increased drive strength, allowing lower impedance buses to be driven, and therefore less noise sensitive. Details on the Fast-mode Plus specification are given in [Ref. 15 “UM10204”](#).

13.7 Reading sensor data

The PCF8885 supports direct reading of the sensor state from the SENS register. If - after sending the address - the  $R/\overline{W}$  bit is immediately set to logic 1 without sending a command, the circuit recognizes that it must immediately return the content of the SENS register (see [Figure 15](#))

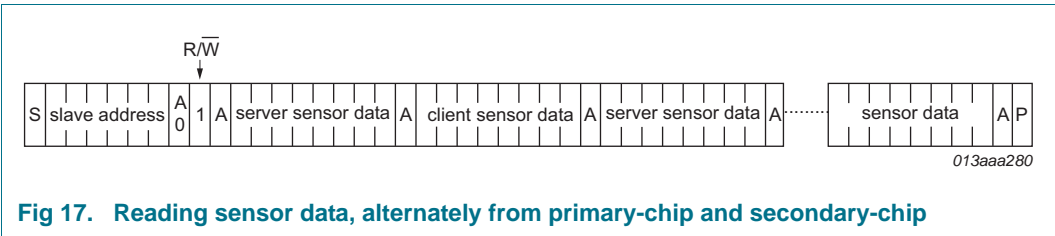


When the transaction, after reading the SENS register, is not terminated with a STOP bit, the PCF8885 repeatedly sends the content of SENS again. This provides a facility to observe the sensor activity continuously. This transaction is illustrated in [Figure 16](#).



Using two PCF8885 in a cascade (see [Section 13.8](#)), one has to be the primary-chip and the other the secondary-chip. When the direct read transaction is executed in a cascaded configuration, the primary-chip transmits its SENS content register immediately after the address byte, followed by the secondary-chip transmitting its SENS register content.

If the transaction - after reading the two SENS registers - is not terminated with a STOP bit, the primary-chip and the secondary-chip continue sending the content of the SENS registers alternately. Such a transaction is illustrated in [Figure 17](#).



It must be noted, that for this alternate data transfer only one PCF8885 has to be addressed. By definition the primary-chip must be addressed (A0 bit in the address set to logic 0). In this particular case, the secondary-chip reacts on the address of the primary-chip. For all other transactions targeting the secondary-chip, it must be properly addressed with A0 set to logic 1.

### 13.8 Device cascading

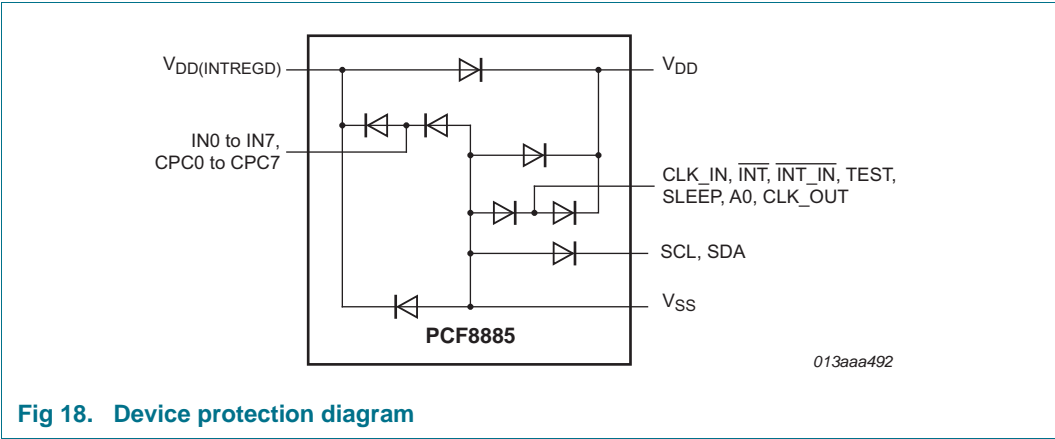
Two PCF8885 devices can be connected to the same I<sup>2</sup>C-bus, which facilitates up to 8 × 8 keypads.

The device provides the following features to guarantee robust operation and to simplify the system design using two devices:

- The 7-bit I<sup>2</sup>C address consists of 6 fixed bits and 1 selectable bit. The level externally applied to pin A0 (V<sub>DD</sub> or V<sub>SS</sub>) defines the LSB of the I<sup>2</sup>C slave address. In this way, two PCF8885 can be addressed on the same bus without the need for different hard coded I<sup>2</sup>C addresses.
- The sensor activity can be synchronized, so that interference between the sensors of the different chips is avoided. One chip is considered to be the primary-chip. It provides the sample clock on pin CLK\_OUT. The other chip is considered to be the secondary-chip. It uses the clock provided by the primary-chip instead of the internal clock. The primary-chip samples the sensors on the rising edge of the internal sample clock. The CLK\_IN signal is inverted to derive the sample clock in the secondary-chip. Therefore the secondary-chip samples its sensors on the negative edge of the sample clock of the primary-chip. In this way, no simultaneous sensor sampling occurs.  
Primary-chip or secondary-chip modes are enabled by programming the configuration register (see [Table 6 on page 10](#)).
- The interrupt signal can be cascaded. The  $\overline{\text{INT}}$  output of the primary-chip can be connected to the INT\_IN input of the secondary-chip. The  $\overline{\text{INT}}$  output of the secondary-chip is then an OR'ed combination of the two interrupts.
- If two devices are cascaded and the int-over-I<sup>2</sup>C mode is desired, then it is sufficient to put the secondary-chip in int-over-I<sup>2</sup>C mode. The primary-chip still signals an interrupt over the INT output to the INT\_IN input of the secondary-chip.

[Figure 26 on page 34](#) illustrates a typical example of an application using two PCF8885 circuits.

14. Internal circuitry



## 15. Limiting values

**Table 12. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD</sub>	supply voltage		−0.5	+8.0	V	
V <sub>DD(INTREGD)</sub>	internal regulated supply voltage		−0.5	+6.5	V	
V <sub>I</sub>	input voltage	on all input pins	−0.5	+6.5	V	
I <sub>SS</sub>	ground supply current		−50	+50	mA	
I <sub>SDA</sub>	current on pin SDA		−30	+30	mA	
I <sub>I/O(n)</sub>	input/output current on any other pin		−10	+10	mA	
P <sub>tot</sub>	total power dissipation		-	100	mW	
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		CDM	[2]			
		SOIC28 (PCF8885T/1)	-	±500	V	
		TSSOP28 (PCF8885TS/1)	-	±750	V	
I <sub>Iu</sub>	latch-up current		[3]	-	100	mA
T <sub>stg</sub>	storage temperature		[4]	−60	+125	°C
T <sub>amb</sub>	ambient temperature	operating device	−40	+85	°C	

[1] Pass level; Human Body Model (HBM) according to [Ref. 10 "JESD22-A114"](#).

[2] Pass level; Charged-Device Model (CDM), according to [Ref. 11 "JESD22-C101"](#).

[3] Pass level; latch-up testing, according to [Ref. 12 "JESD78"](#) at maximum ambient temperature (T<sub>amb(max)</sub>).

[4] According to the store and transport requirements (see [Ref. 17 "UM10569"](#)) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.



## 16. Static characteristics

**Table 13. Static characteristics**

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_{amb} = -40\text{ °C to }+85\text{ °C}$ ; unless otherwise specified; min and max values are not production tested, but verified on sampling basis.

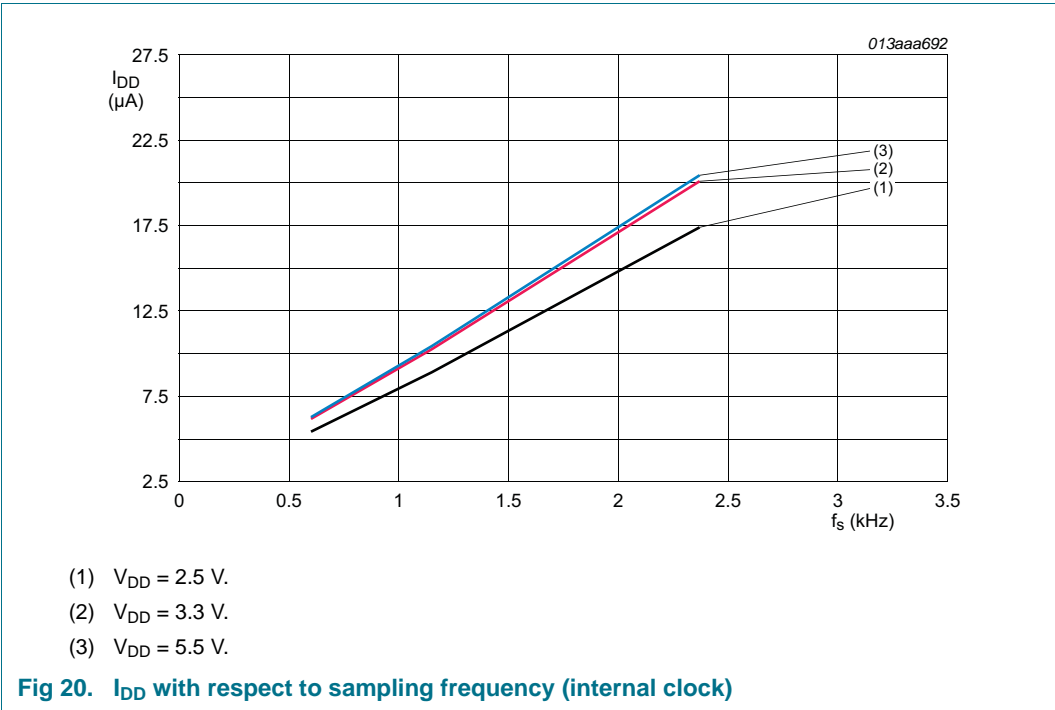
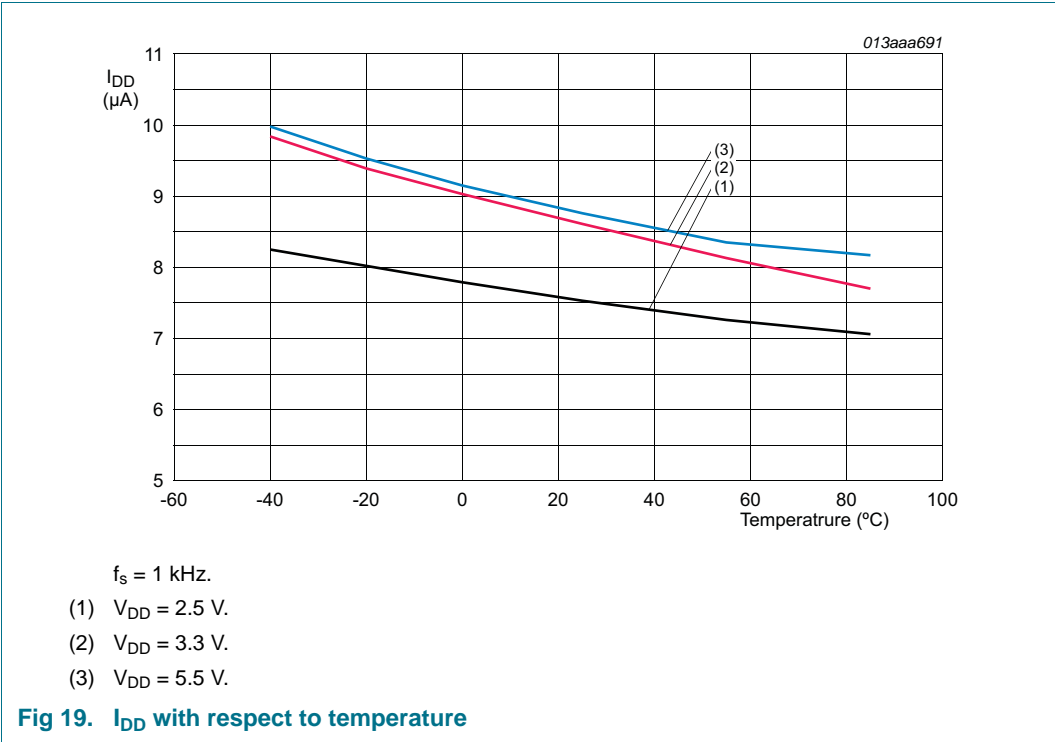
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>DD</sub>	supply voltage		2.5	-	5.5	V	
V <sub>DD(ext)</sub>	external supply voltage	V <sub>DD</sub> connected to V <sub>DD(INTREGD)</sub> ; internal regulator disabled	2.5	-	3.3	V	
V <sub>DD(INTREGD)</sub>	internal regulated supply voltage		[1]				
			2.5	2.9	3.3	V	
		external supplied	2.5	-	3.3	V	
I <sub>DD</sub>	supply current	idle state; f <sub>s</sub> = 1 kHz	[2]	-	10	20	μA
I <sub>DD(sleep)</sub>	sleep mode supply current		-	100	500	nA	
Digital inputs (CLK_IN, A0, INT_IN, TEST)							
V <sub>IL</sub>	LOW-level input voltage		V <sub>SS</sub>	-	0.3V <sub>DD</sub>	V	
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V	
Digital outputs (INT, CLK_OUT)							
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = 0.5 mA	V <sub>SS</sub>	-	0.2V <sub>DD</sub>	V	
V <sub>OH</sub>	HIGH-level output voltage	I <sub>O</sub> = 0.5 mA	0.8V <sub>DD</sub>	-	V <sub>DD</sub>	V	
Analog pins (IN0 to IN7 and CPC0 to CPC7)							
V <sub>CPC</sub>	voltage on pin CPC	usable control range	V <sub>SS</sub> + 0.5	-	V <sub>DD(INTREGD)</sub> – 0.5	V	
C <sub>in</sub>	input capacitance	sensing plate and parasitic	10	-	40	pF	
I <sup>2</sup> C interface pins (SDA, SCL)							
V <sub>IL</sub>	LOW-level input voltage		–0.5	-	0.3V <sub>DD</sub>	V	
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DD</sub>	-	5.5	V	
I <sub>OL</sub>	LOW-level output current	V <sub>DD</sub> = 5.0 V; V <sub>OL</sub> = 0.4 V	20	-	-	mA	
I <sub>L</sub>	leakage current		[3]	-	0	μA	
C <sub>i</sub>	capacitance for each I/O pin		-	-	10	pF	
External components							
C <sub>CPC</sub>	capacitance on pin CPC		[4]	22	100	470	nF
C <sub>dec</sub>	decoupling capacitance	on pins V <sub>DD(INTREGD)</sub> and V <sub>DD</sub> ; ceramic chip capacitor	-	100	-	nF	

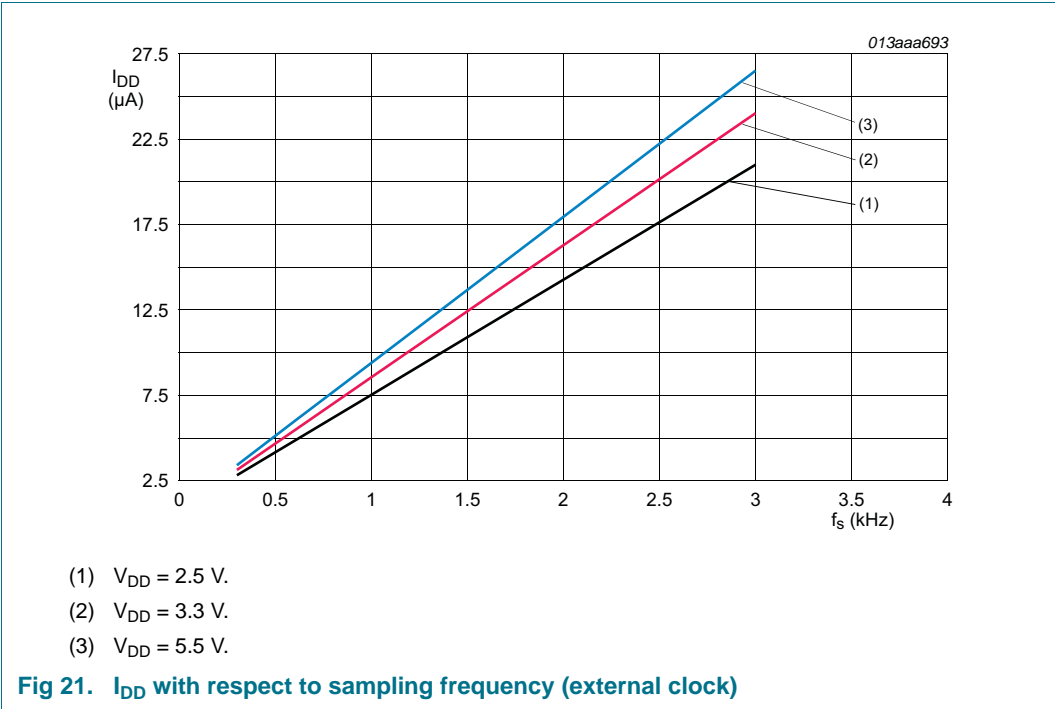
[1] See Figure 9 for an illustration of the voltage regulation behavior and the related parameters.

[2] Idle state is the steady state after completed power-on, without any mode change and without any activity on the sensor plates, and the voltages on the reservoir capacitors  $C_{CPC}$  are settled.

[3] In case of an ESD event, the value may increase slightly.

[4] The insulation resistance of the capacitor should be at least 5 G $\Omega$ .





## 17. Dynamic characteristics

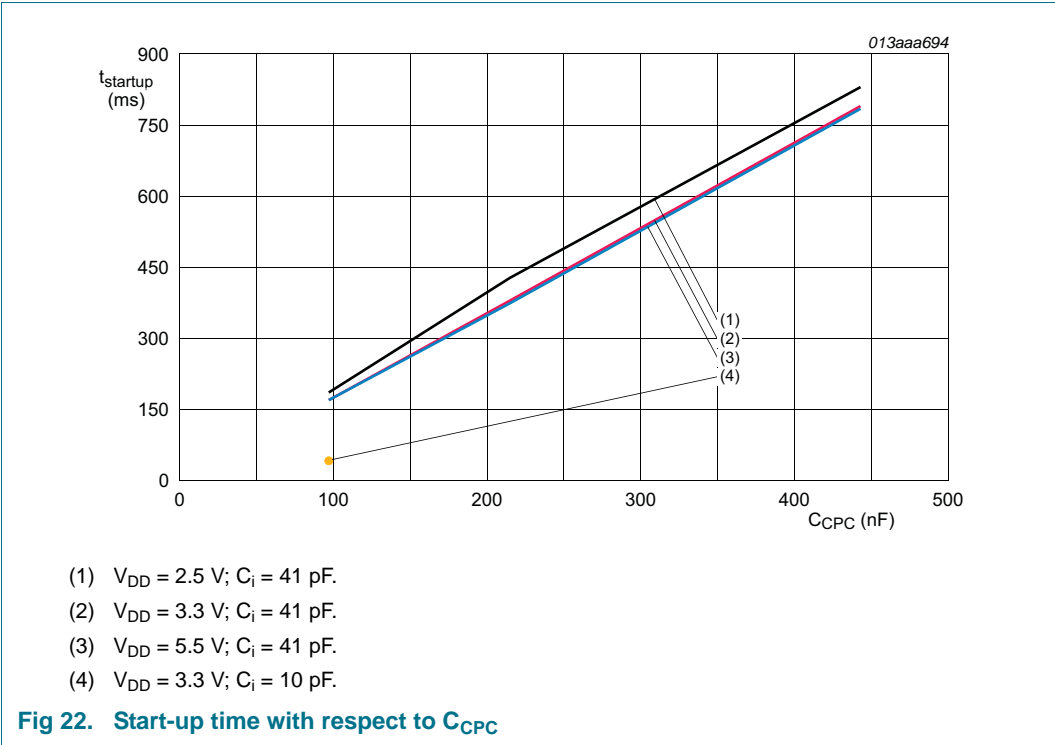
**Table 14. Dynamic characteristics**

$V_{DD} = 2.5\text{ V to }5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ ; unless otherwise specified; min and max values are not production tested, but verified on sampling basis.

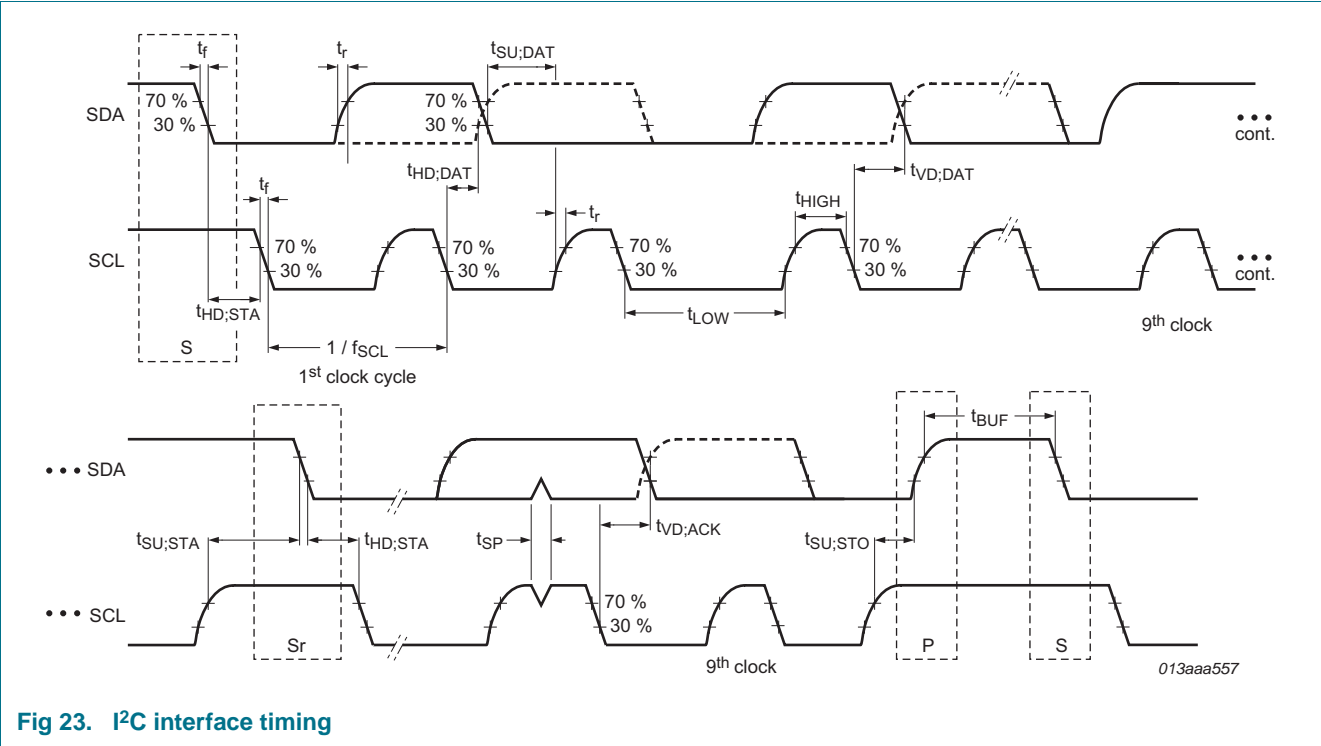
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>System timing</b>						
$t_{\text{startup}}$	start-up time	$C_{\text{CPC}} = 100\text{ nF}$ ; $f_s = 1\text{ kHz}$ ; $C_{\text{in}} = 40\text{ pF}$	-	200	-	ms
$f_{\text{osc}}$	oscillator frequency	internal RC oscillator; $\text{FRQF}[2:0] = 100$	[1] 58	80	112	kHz
$t_{\text{sw}}$	switching time	$f_s = 1\text{ kHz}$	[2] -	64	-	ms
<b>I<sup>2</sup>C interface characteristics (SDA, SCL)</b>						
$t_{\text{SP}}$	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns
$f_{\text{SCL}}$	SCL clock frequency		0	-	1000	kHz
$t_{\text{HD;STA}}$	hold time (repeated) START condition		0.26	-	-	$\mu\text{s}$
$t_{\text{SU;STA}}$	set-up time for a repeated START condition		0.26	-	-	$\mu\text{s}$
$t_{\text{LOW}}$	LOW period of the SCL clock		0.5	-	-	$\mu\text{s}$
$t_{\text{HIGH}}$	HIGH period of the SCL clock		0.26	-	-	$\mu\text{s}$
$t_{\text{HD;DAT}}$	data hold time		0	-	-	ns
$t_{\text{SU;DAT}}$	data set-up time		50	-	-	ns
$t_r$	rise time of both SDA and SCL signals		-	-	120	ns
$t_f$	fall time of both SDA and SCL signals		-	-	120	ns
$t_{\text{SU;STO}}$	set-up time for STOP condition		0.26	-	-	$\mu\text{s}$
$t_{\text{BUF}}$	bus free time between a STOP and START condition		0.5	-	-	$\mu\text{s}$
$C_b$	capacitive load for each bus line		-	-	550	pF
$t_{\text{VD;DAT}}$	data valid time		-	-	0.45	$\mu\text{s}$
$t_{\text{VD;ACK}}$	data valid acknowledge time		-	-	0.45	$\mu\text{s}$
$t_{\text{w(int)}}$	interrupt pulse width	interrupt over I <sup>2</sup> C	-	2	-	$\mu\text{s}$

[1] Default value.

[2] For switching, 64 consecutive CUP pulses are needed.

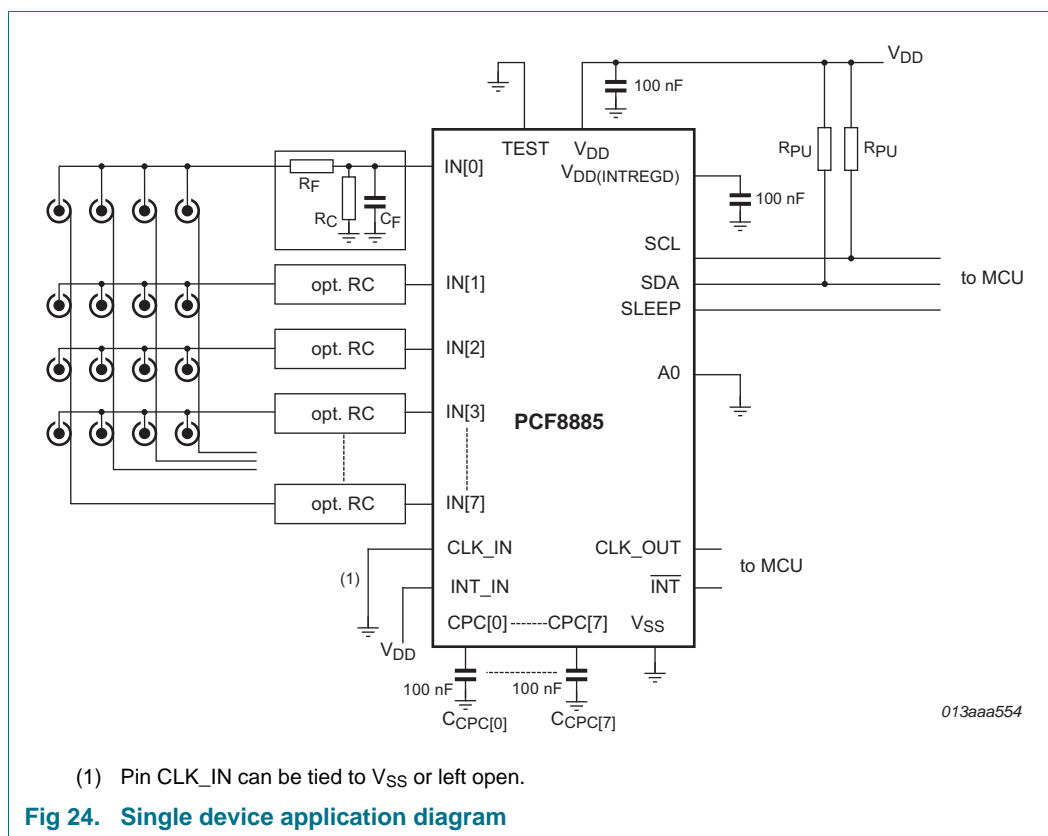


17.1 I²C interface timing



## 18. Application information

## 18.1 Single device application



18.2 28 sensor grid application in 2-key mode

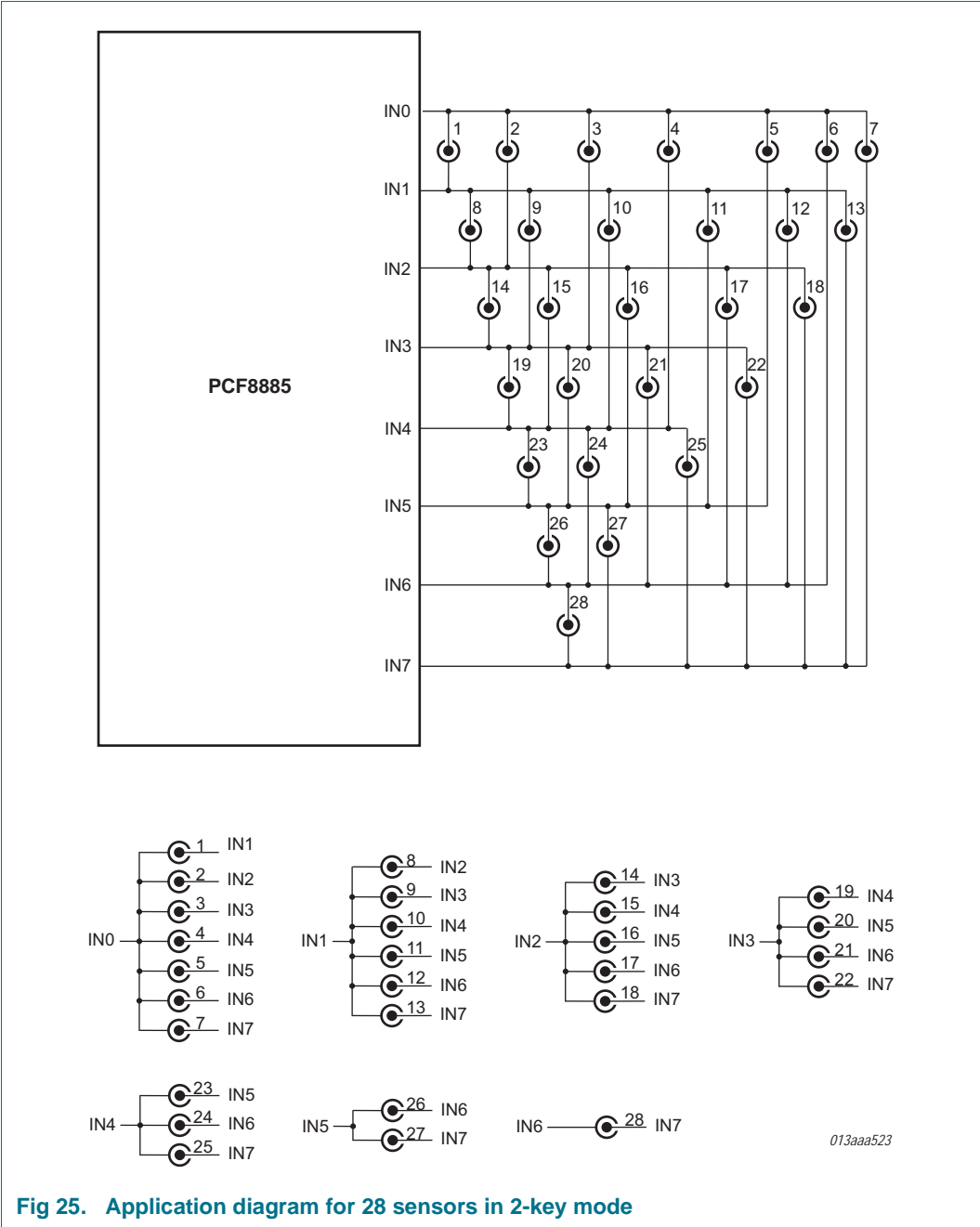
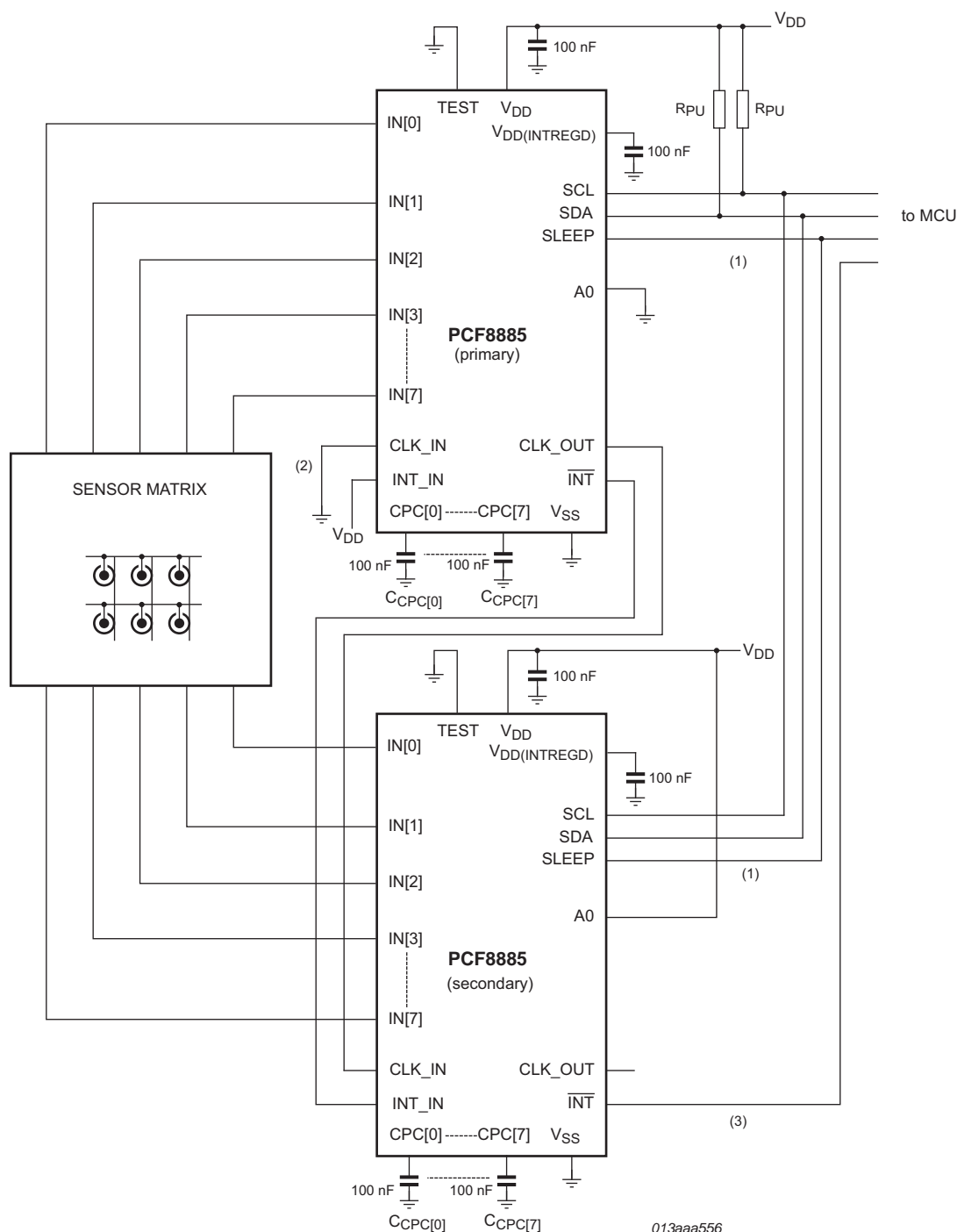


Fig 25. Application diagram for 28 sensors in 2-key mode

Table 15. Input combinations for a 28 sensor grid in 2-key mode

Sensor	Inputs							
	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
1	0	0	0	0	0	0	1	1
2	0	0	0	0	0	1	0	1
3	0	0	0	0	1	0	0	1
4	0	0	0	1	0	0	0	1
5	0	0	1	0	0	0	0	1
6	0	1	0	0	0	0	0	1
7	1	0	0	0	0	0	0	1
8	0	0	0	0	0	1	1	0
9	0	0	0	0	1	0	1	0
10	0	0	0	1	0	0	1	0
11	0	0	1	0	0	0	1	0
12	0	1	0	0	0	0	1	0
13	1	0	0	0	0	0	1	0
14	0	0	0	0	1	1	0	0
15	0	0	0	1	0	1	0	0
16	0	0	1	0	0	1	0	0
17	0	1	0	0	0	1	0	0
18	1	0	0	0	0	1	0	0
19	0	0	0	1	1	0	0	0
20	0	0	1	0	1	0	0	0
21	0	1	0	0	1	0	0	0
22	1	0	0	0	1	0	0	0
23	0	0	1	1	0	0	0	0
24	0	1	0	1	0	0	0	0
25	1	0	0	1	0	0	0	0
26	0	1	1	0	0	0	0	0
27	1	0	1	0	0	0	0	0
28	1	1	0	0	0	0	0	0





- (1) If the SLEEP pin is not used, it must be connected to V<sub>SS</sub>.
- (2) Pin CLK\_IN can be tied to V<sub>SS</sub> or left open.
- (3) Instead of the  $\overline{\text{INT}}$  pin, interrupt over I<sup>2</sup>C-bus can be used. If the  $\overline{\text{INT}}$  pin is not used, it must be left open.

**Fig 26. Cascaded application diagram**

[Figure 26](#) shows the typical connections for a general application using two chips. For simplicity, the sensors attached to the secondary-chip are not shown in this diagram. The sensors of the secondary-chip can be arranged independently of the sensors of the primary-chip or combined in a common larger matrix.

Both chips use different I<sup>2</sup>C addresses programmed by the voltage level applied to pin A0. The primary-chip has A0 connected to ground; the secondary-chip has A0 connected to V<sub>DD(ext)</sub>. In this way, each circuit is addressed individually.

In this case, the primary-chip is programmed to use the internal oscillator as clock reference. The primary-chip is also programmed to enable the clock output. The secondary-chip is programmed to use the clock output from the primary-chip as input clock. The internal oscillator of the secondary-chip is shut down to save power in this mode.

The interrupt output  $\overline{\text{INT}}$  of the primary-chip is routed to the  $\overline{\text{INT\_IN}}$  input of the secondary-chip, where it is OR'ed with the interrupt state of the secondary-chip.

The sensing plate capacitances may consist of a small metal area, for example behind an isolating layer. Illustrated in [Figure 26](#) is a 4 × 4 sensor arrangement. In this configuration, a sensor touch always excites two sensor plates at the same time.

The sensing plates are connected to a coaxial cable (for remote sensors) or a shielded connection, which in turn is connected to the input pin IN. The connection capacitance contributes to the input capacitance and must not be neglected. An internal low pass filter (not shown) is used to reduce RF interference. An additional low pass filter consisting of a resistor R<sub>F</sub> and capacitor C<sub>F</sub> can be added to the input to improve RF immunity further than required. For good performance, the total amount of capacitance on the input (C<sub>s</sub> + C<sub>CABLE</sub> + C<sub>F</sub>) should be in the proper range, the optimum point being around 30 pF. Even if the external filtering is not required, placing C<sub>F</sub> can help to bring the input capacitance to an optimal value. These conditions allow the control loop to adapt to the static capacitance on C<sub>S</sub> and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible, if an additional discharge resistor R<sub>C</sub> is used. Resistor R<sub>C</sub> simply reduces the discharge time such that the internal timing requirements can be fulfilled.

The sensitivity of the sensors can be influenced by the sensing plate area and capacitors C<sub>CPC</sub>. The sensitivity is reduced when C<sub>CPC</sub> is reduced. When maximum sensitivity is desired, C<sub>CPC</sub> can be increased, but it also increases sensitivity to interference. The CPC[0:7] pins have high impedance and are sensitive to leakage currents. Therefore C<sub>CPC</sub> should be a high-quality foil or ceramic capacitor, for example an X7R type.

For the choice of proper component values for a given application, the component specifications in [Section 16 on page 26](#) must be followed.

19. Package outline

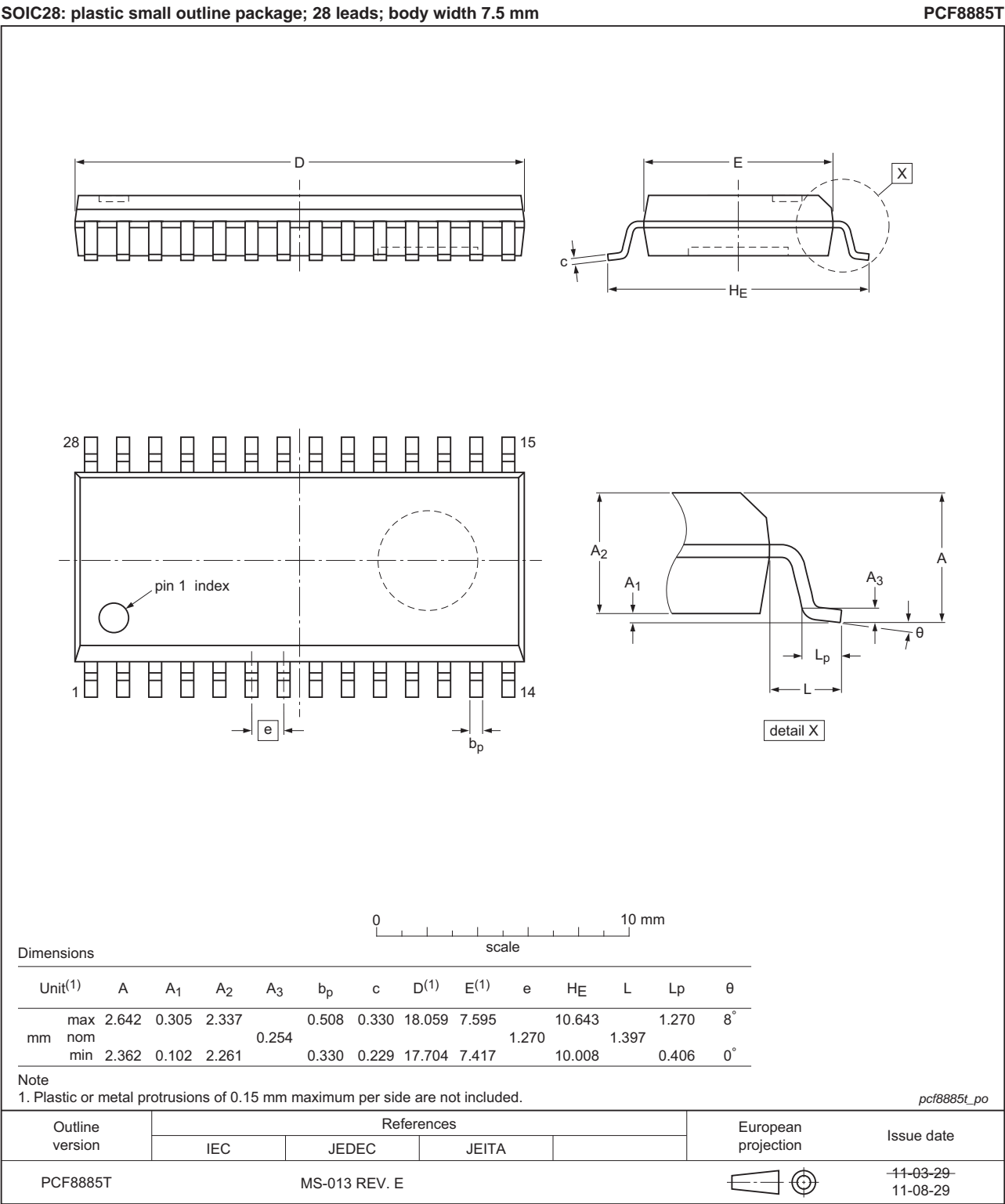


Fig 27. Package outline PCF8885T (SOIC28)

TSSOP28: plastic small outline package; 28 leads; body width 4.4 mm

PCF8885TS

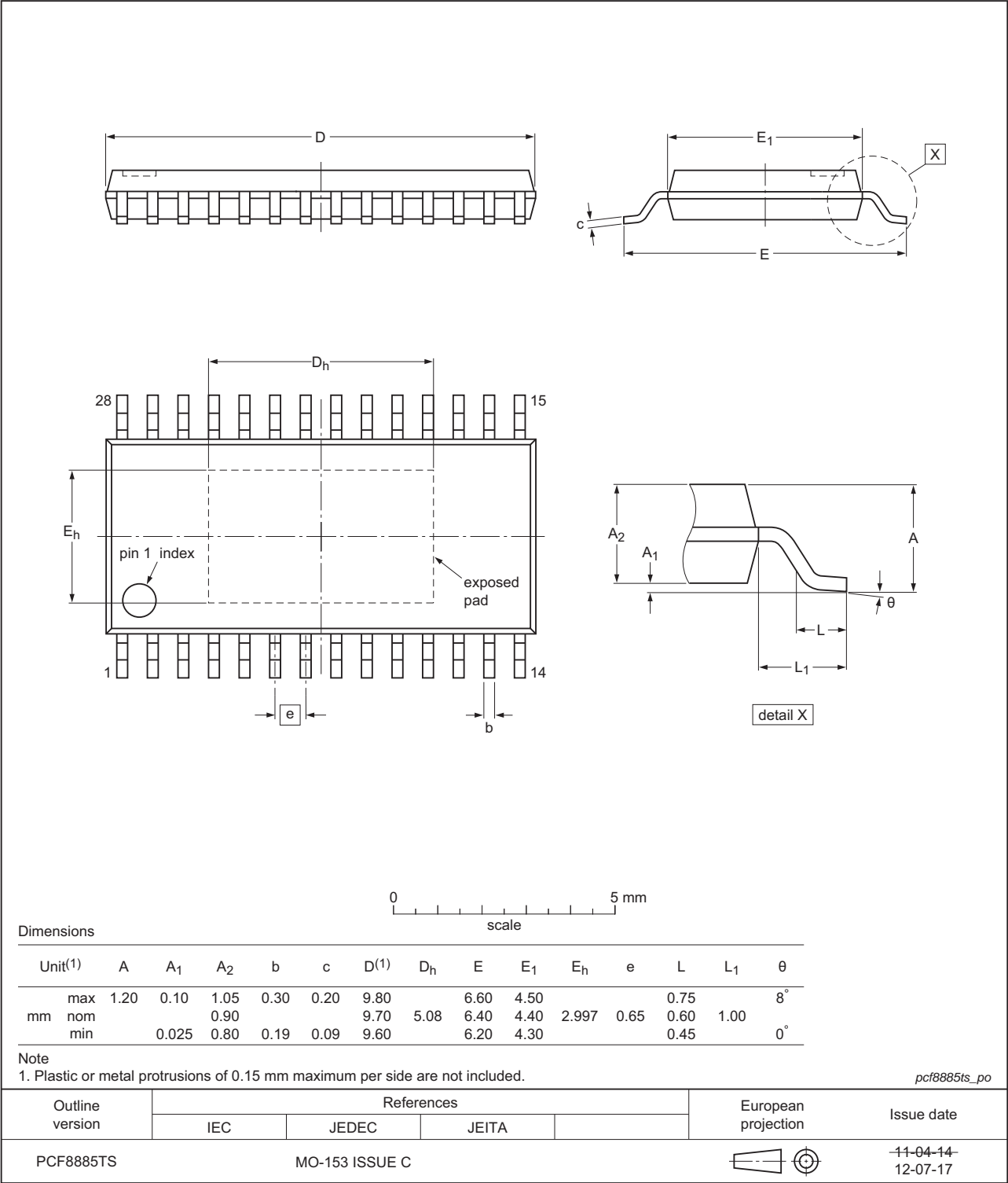


Fig 28. Package outline PCF8885TS (TSSOP28)

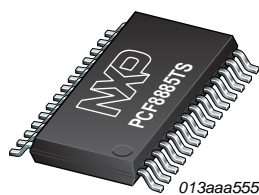


Fig 29. Three-dimensional package drawing of PCF8885

## 20. Packing information

### 20.1 Carrier tape information

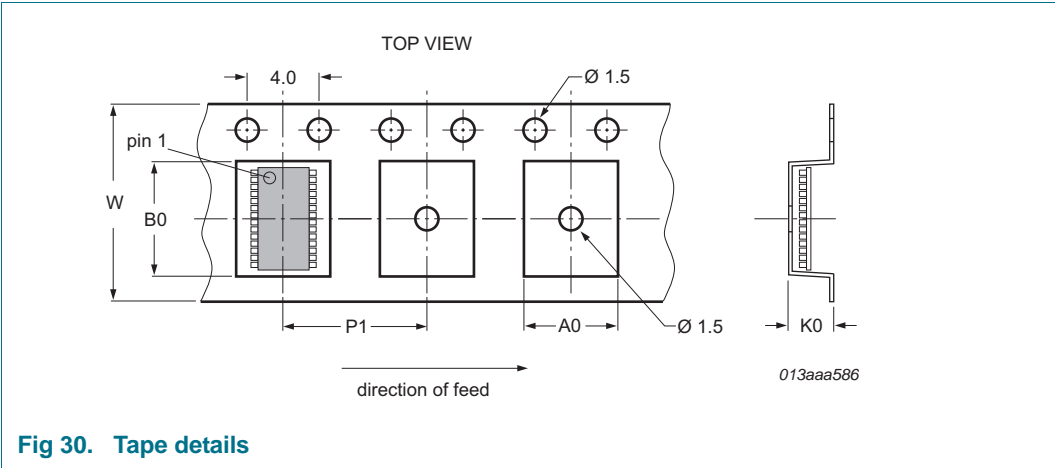


Table 16. Carrier tape dimensions

Symbol	Description	Value	Unit
A0	pocket width in x direction	6.8	mm
B0	pocket width in y direction	10.2	mm
K0	pocket height	1.6	mm
P1	sprocket hole pitch	8	mm
W	tape width in y direction	16	mm

## 21. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “Surface mount reflow soldering description”.

### 21.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 21.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components

- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 21.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 21.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 31](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 17](#) and [18](#)

Table 17. SnPb eutectic process (from J-STD-020C)

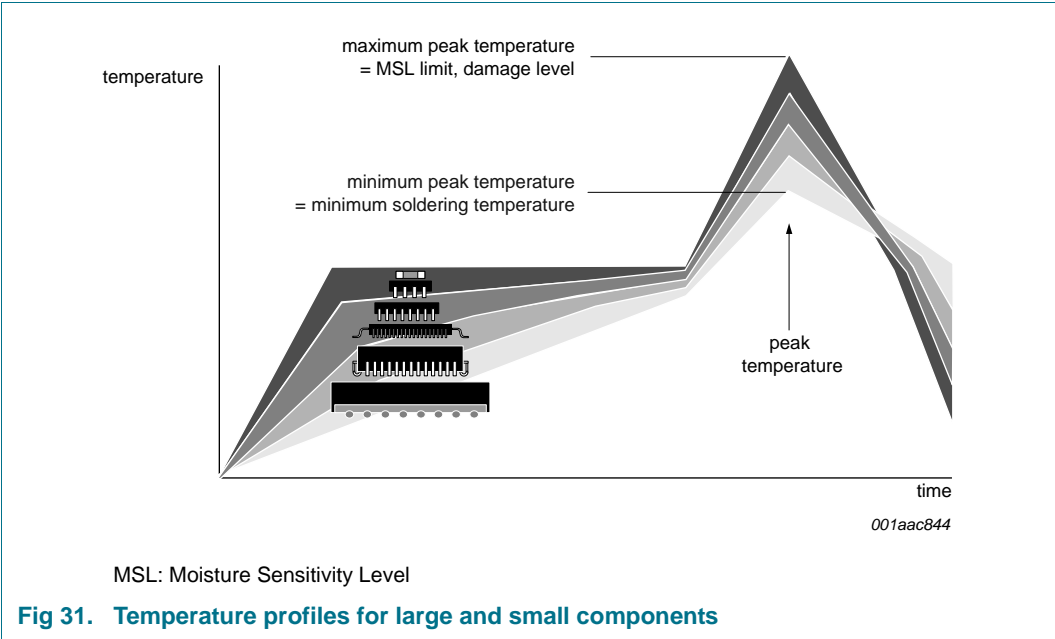
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 18. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 31](#).



For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.



## 22. Abbreviations

**Table 19. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
IC	Integrated Circuit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RF	Radio Frequency
SMD	Surface Mount Device

## 23. References

- [1] **AN10365** — Surface mount reflow soldering description
- [2] **AN10832** — PCF8883 - capacitive proximity switch with auto-calibration
- [3] **AN10853** — Handling precautions of ESD sensitive devices
- [4] **AN11122** — Water and condensation safe touch sensing with the NXP capacitive touch sensors
- [5] **AN11157** — Capacitive touch sensing with high EMC performance, Application Note
- [6] **AN11155** — General design guidelines for the NXP capacitive sensors
- [7] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
- [8] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
- [9] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
- [10] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
- [11] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
- [12] **JESD78** — IC Latch-Up Test
- [13] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- [14] **SNV-FA-01-02** — Marking Formats Integrated Circuits
- [15] **UM10204** — I<sup>2</sup>C-bus specification and user manual
- [16] **UM10505** — OM11057 quick start guide
- [17] **UM10569** — Store and transport requirements

## 24. Revision history

**Table 20. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8885 v.2	20121025	Product data sheet	-	PCF8885 v.1
Modifications:	<ul style="list-style-type: none"> <li>• Changed ESD values (<a href="#">Table 12</a>)</li> <li>• Changed oscillator frequency specification (<a href="#">Table 14</a>)</li> </ul>			
PCF8885 v.1	20120221	Product data sheet	-	-

## 25. Legal information

### 25.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## Capacitive 8-channel touch and proximity sensor with auto-calibration

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## 27. Contents

<b>1</b>	<b>General description</b> . . . . .	<b>1</b>	<b>17</b>	<b>Dynamic characteristics</b> . . . . .	<b>29</b>
<b>2</b>	<b>Features and benefits</b> . . . . .	<b>1</b>	17.1	I <sup>2</sup> C interface timing . . . . .	30
<b>3</b>	<b>Applications</b> . . . . .	<b>2</b>	<b>18</b>	<b>Application information</b> . . . . .	<b>31</b>
<b>4</b>	<b>Ordering information</b> . . . . .	<b>2</b>	18.1	Single device application . . . . .	31
<b>5</b>	<b>Marking</b> . . . . .	<b>2</b>	18.2	28 sensor grid application in 2-key mode . . .	32
<b>6</b>	<b>Block diagram</b> . . . . .	<b>3</b>	18.3	Cascaded application . . . . .	34
<b>7</b>	<b>Pinning information</b> . . . . .	<b>4</b>	<b>19</b>	<b>Package outline</b> . . . . .	<b>36</b>
7.1	Pinning . . . . .	4	<b>20</b>	<b>Packing information</b> . . . . .	<b>39</b>
7.2	Pin description . . . . .	5	20.1	Carrier tape information . . . . .	39
<b>8</b>	<b>Functional description</b> . . . . .	<b>6</b>	<b>21</b>	<b>Soldering of SMD packages</b> . . . . .	<b>39</b>
<b>9</b>	<b>Commands</b> . . . . .	<b>8</b>	21.1	Introduction to soldering . . . . .	39
9.1	Command overview . . . . .	8	21.2	Wave and reflow soldering . . . . .	39
9.2	Command: soft-reset . . . . .	8	21.3	Wave soldering . . . . .	40
9.3	Commands: Sleep and wake-up . . . . .	8	21.4	Reflow soldering . . . . .	40
9.4	Command: read-sensor . . . . .	9	<b>22</b>	<b>Abbreviations</b> . . . . .	<b>42</b>
<b>10</b>	<b>Registers</b> . . . . .	<b>10</b>	<b>23</b>	<b>References</b> . . . . .	<b>43</b>
10.1	Register overview . . . . .	10	<b>24</b>	<b>Revision history</b> . . . . .	<b>43</b>
10.2	Register: CONFIG . . . . .	10	<b>25</b>	<b>Legal information</b> . . . . .	<b>44</b>
10.2.1	Operating modes . . . . .	11	25.1	Data sheet status . . . . .	44
10.2.1.1	Main operating modes . . . . .	11	25.2	Definitions . . . . .	44
10.2.1.2	Switching modes . . . . .	11	25.3	Disclaimers . . . . .	44
10.2.1.3	Key-press modes . . . . .	12	25.4	Licenses . . . . .	45
10.2.2	Interrupt generation . . . . .	12	25.5	Trademarks . . . . .	45
10.2.2.1	Interrupt output INT . . . . .	12	<b>26</b>	<b>Contact information</b> . . . . .	<b>45</b>
10.2.2.2	Interrupt over the I <sup>2</sup> C-bus . . . . .	13	<b>27</b>	<b>Contents</b> . . . . .	<b>46</b>
10.3	Register: SENS . . . . .	14			
10.4	Register: CLKREG . . . . .	14			
10.4.1	Clock generation and frequency adjustment .	15			
10.5	Register: MASK . . . . .	16			
10.5.1	Channel masking . . . . .	16			
<b>11</b>	<b>Power architecture</b> . . . . .	<b>17</b>			
<b>12</b>	<b>Start-up procedure</b> . . . . .	<b>18</b>			
<b>13</b>	<b>Characteristics of the I<sup>2</sup>C-bus</b> . . . . .	<b>19</b>			
13.1	Bit transfer . . . . .	19			
13.1.1	START and STOP conditions . . . . .	19			
13.2	System configuration . . . . .	20			
13.3	Acknowledge . . . . .	20			
13.4	I <sup>2</sup> C-bus subaddress . . . . .	21			
13.5	I <sup>2</sup> C-bus protocol . . . . .	21			
13.6	Fast-mode Plus (Fm+) support . . . . .	21			
13.7	Reading sensor data . . . . .	21			
13.8	Device cascading . . . . .	22			
<b>14</b>	<b>Internal circuitry</b> . . . . .	<b>24</b>			
<b>15</b>	<b>Limiting values</b> . . . . .	<b>25</b>			
<b>16</b>	<b>Static characteristics</b> . . . . .	<b>26</b>			

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