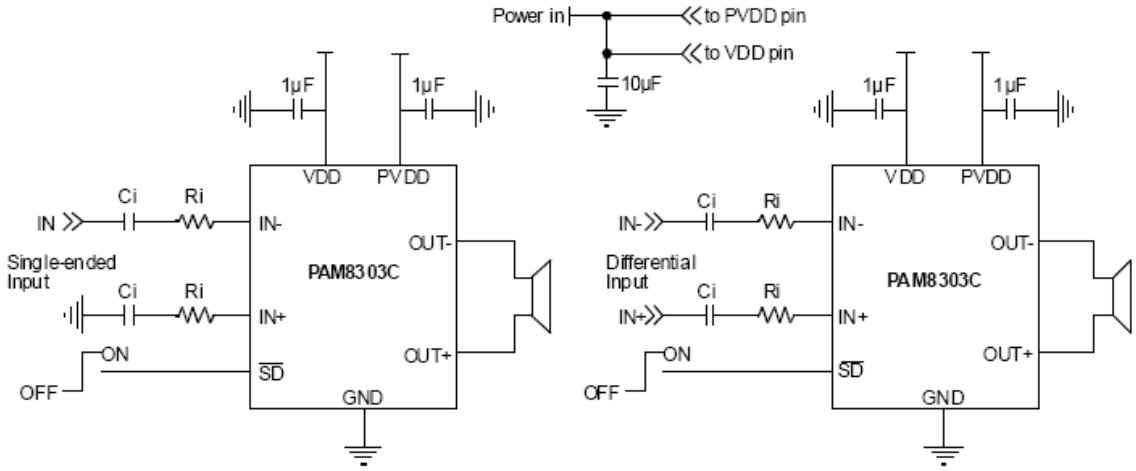
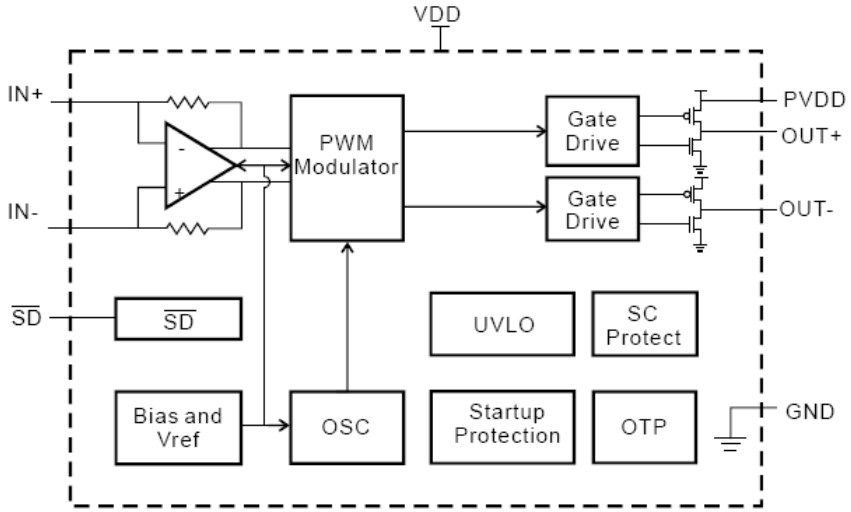
Typical Applications Circuit



Pin Descriptions

Pin Name	Pin Name				Function
	WCSP(A)(EOL)	U-DFN3030-8 (B)	U-DFN3030-8 (C)	MSOP-8 (B)	
OUT+	C3	1	5	1	Positive BTL Output
PVDD	B2	2	—	2	Power Supply
VDD	B1	3	6	3	Analog Power Supply
IN-	C1	4	4	4	Negative Differential Input
IN+	A1	5	3	5	Positive Differential Input
$\overline{SD}$	C2	6	1	6	Shutdown Terminal (Active Low)
GND	A2, B3	7	7	7	Ground
OUT-	A3	8	8	8	Negative BTL Output
NC	—	—	2	—	—

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

The following parameters are stress ratings only, and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods can affect device reliability. All voltages are with respect to ground.

Parameter	Rating	Unit
Supply Voltage	6.0	V
Input Voltage	-0.3 to V_{DD} +0.3	
Maximum Junction Temperature	150	°C
Storage Temperature	-65 to +150	
Soldering Temperature	+250, 10 sec	

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage Range	2.8 to 5.5	V
Ambient Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	°C

Thermal Information (Note 4)

Parameter	Package	Symbol	Max	Unit
Thermal Resistance (Junction to Ambient)	MSOP-8	θ_{JA}	180	°C/W
	U-DFN3030-8		47.9	
Thermal Resistance (Junction to Case)	MSOP-8	θ_{JC}	75	

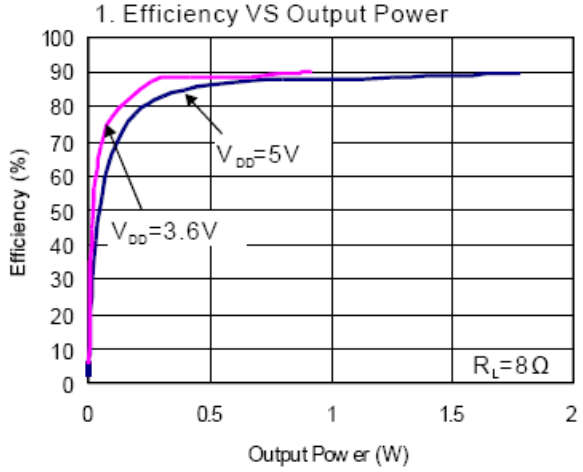
Note: 4. For the 9-pin CSP package, the thermal resistance is highly dependent on the PCB heat sink area. For example, the θ_{JA} can equal to 195°C/W with 50mm^2 total area or 135°C/W with 500mm^2 area. When using ground and power planes, the value is approximately 90°C/W.

Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = 2V/V, R_L = L(33µH) + R + L(33µH), unless otherwise specified.)

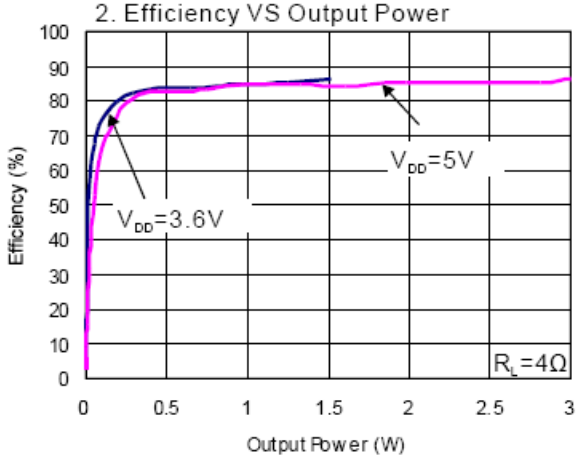
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage	—	—	2.8	—	5.5	V
P_O	Output Power	THD+N = 10%, f = 1kHz, R = 4Ω	V_{DD} = 5.0V	2.85	3.00	—	W
			V_{DD} = 3.6V	1.65	1.80	—	
			V_{DD} = 3.2V	1.20	1.35	—	
		THD+N = 1%, f = 1kHz, R = 4Ω	V_{DD} = 5.0V	2.50	2.66	—	W
			V_{DD} = 3.6V	1.15	1.30	—	
			V_{DD} = 3.2V	0.85	1.0	—	
		THD+N = 10%, f = 1kHz, R = 8Ω	V_{DD} = 5.0V	1.65	1.8	—	W
			V_{DD} = 3.6V	0.75	0.9	—	
			V_{DD} = 3.2V	0.55	0.7	—	
		THD+N = 1%, f = 1kHz, R = 8Ω	V_{DD} = 5.0V	1.3	1.5	—	W
			V_{DD} = 3.6V	0.55	0.72	—	
			V_{DD} = 3.2V	0.40	0.55	—	
THD+N	Total Harmonic Distortion Plus Noise	V_{DD} = 5.0V, P_O = 1W, R = 8Ω	f = 1kHz	—	0.28	0.35	%
		V_{DD} = 3.6V, P_O = 0.1W, R = 8Ω		—	0.40	0.45	
		V_{DD} = 3.2V, P_O = 0.1W, R = 8Ω		—	0.55	0.60	
		V_{DD} = 5.0V, P_O = 0.5W, R = 4Ω	f = 1kHz	—	0.20	0.25	%
		V_{DD} = 3.6V, P_O = 0.2W, R = 4Ω		—	0.35	0.40	
		V_{DD} = 3.2V, P_O = 0.1W, R = 4Ω		—	0.5	0.55	
PSRR	Power Supply Ripple Rejection	V_{DD} = 3.6V, Inputs AC-Grounded with C_{IN} = 1µF	f = 217Hz	—	-63	-55	dB
			f = 1kHz	—	-62	-55	
			f = 10kHz	—	-52	-40	
Dyn	Dynamic Range	V_{DD} = 5V, THD = 1%, R = 8Ω	f = 1kHz	85	95	—	
V_N	Output Noise	Inputs AC-Grounded	No A-Weighting	—	50	100	µV
			A-Weighting	—	30	60	
CMRR	Common-Mode Rejection Ratio	V_{IC} = 100m, V_{PP}, f =1kHz	—	40	63	—	dB
η	Peak Efficiency	R_L = 8Ω, THD = 10%	f = 1kHz	85	90	—	%
		R_L = 4Ω, THD = 10%		80	86	—	
I_Q	Quiescent Current	V_{DD} = 5.0V	R = 8Ω	—	7.5	12	mA
		V_{DD} = 3.6V		—	4.6	7	
		V_{DD} = 3.0V		—	3.6	5	
I_{SD}	Shutdown Current	V_{DD} = 3.0V to 5.0V	V_{SD} = 0.3V	—	0.5	2	µA
$R_{DS(ON)}$	Static Drain-to-Source On-State Resistor	CSP Package, High Side PMOS plus Low Side NMOS, I = 500mA	V_{DD} = 5.0V	—	280	350	—
			V_{DD} = 3.6V	—	300	375	—
			V_{DD} = 3.0V	—	325	400	—
		MSOP/DFN package, High-Side PMOS plus Low-Side NMOS, I = 500mA	V_{DD} = 5.0V	—	365	420	—
			V_{DD} = 3.6V	—	385	450	—
			V_{DD} = 3.0V	—	410	500	—
R_{IN}	Input Resistance	—		—	150	—	kΩ
f_{SW}	Switching Frequency	V_{DD} = 3V to 5V		—	370	—	kHz
G_V	Closed Loop Gain	V_{DD} = 3V to 5V		—	300	—	dB
V_{OS}	Output Offset Voltage	Input AC-Ground, V_{DD} = 5V		—	10	50	mV
V_{IH}	Enable Input High Voltage	V_{DD} = 5V		1.5	—	—	V
V_{IL}	Enable Input Low Voltage	V_{DD} = 5V		—	—	0.3	V

Typical Performance Characteristics (@T_A = +25°C, V_{DD} = 5V, f = 1kHz, Gain = 2V/V, unless otherwise specified.)

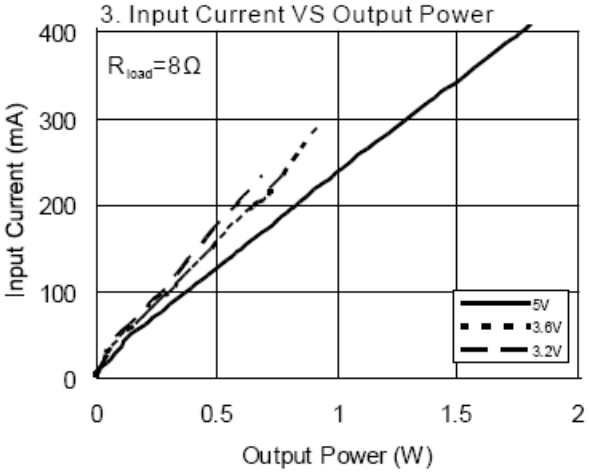
1. Efficiency VS Output Power



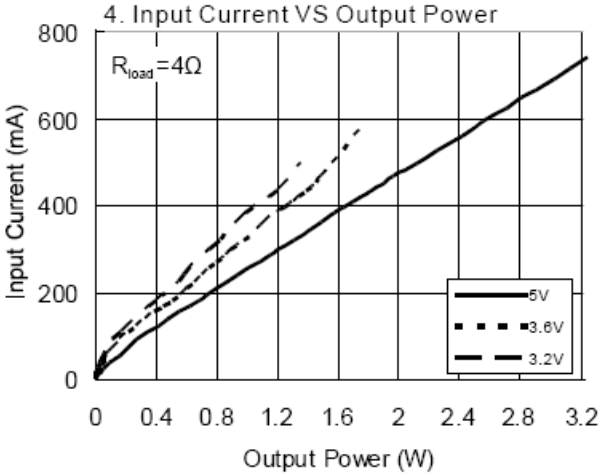
2. Efficiency VS Output Power



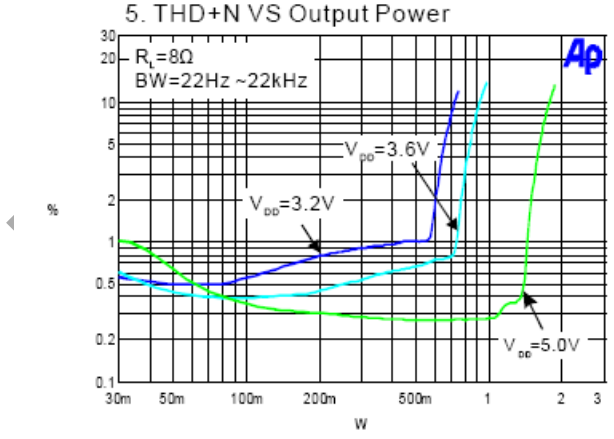
3. Input Current VS Output Power



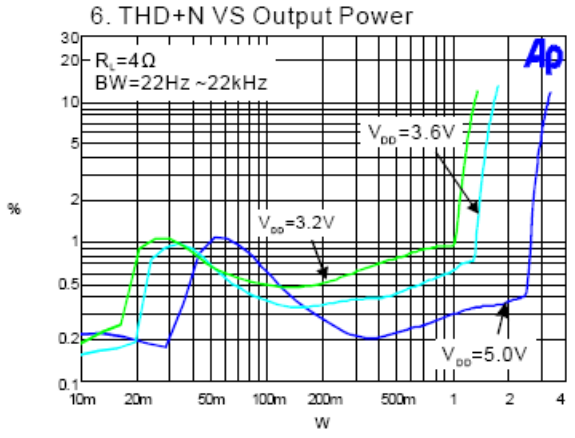
4. Input Current VS Output Power



5. THD+N VS Output Power

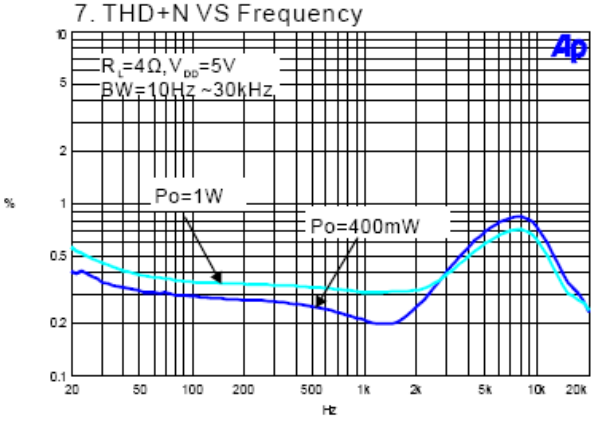


6. THD+N VS Output Power

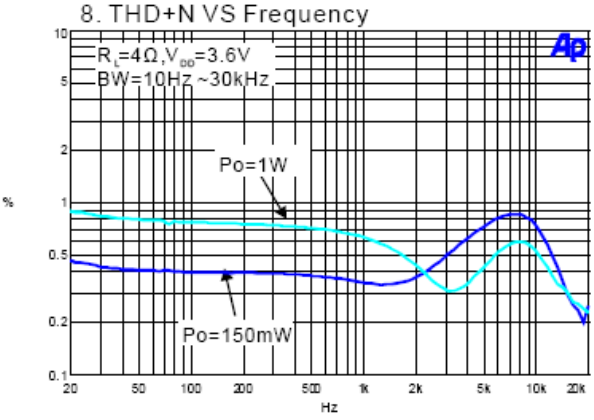


Typical Performance Characteristics (Cont.) (@T_A = +25°C, V_{DD} = 5V, f = 1kHz, Gain = 2V/V, unless otherwise specified.)

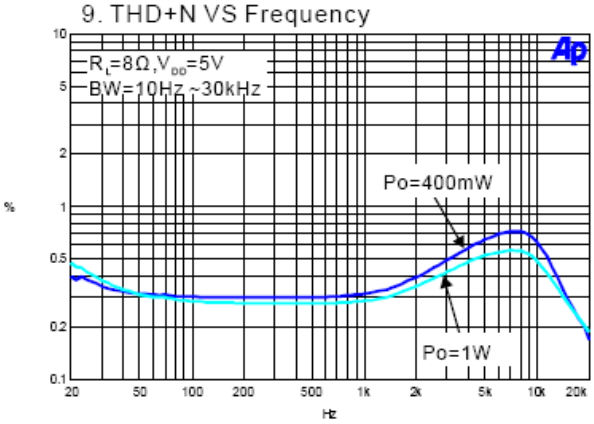
7. THD+N VS Frequency



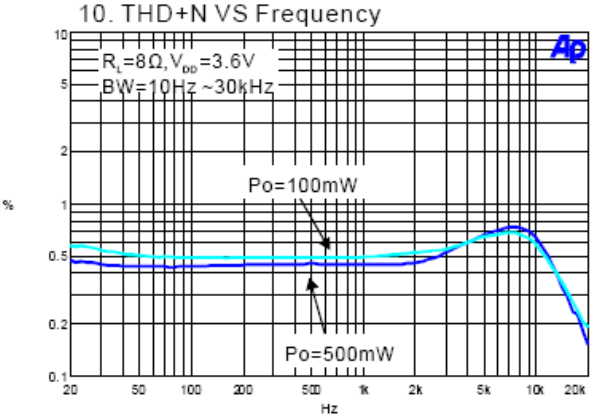
8. THD+N VS Frequency



9. THD+N VS Frequency

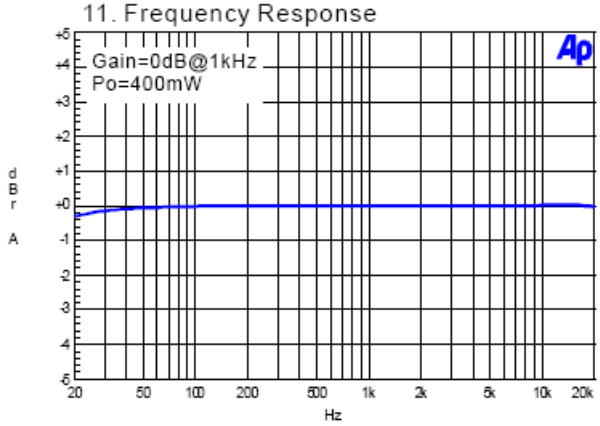


10. THD+N VS Frequency

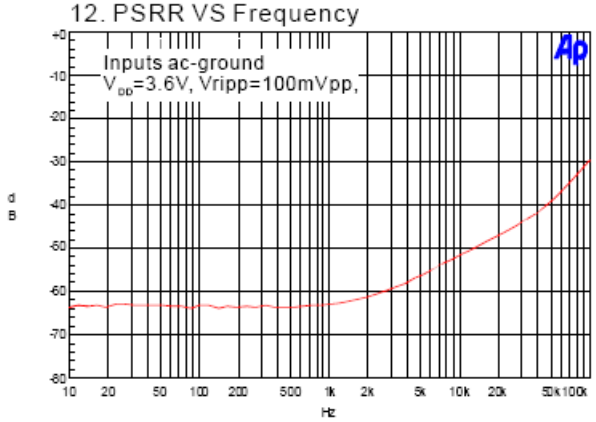


Typical Performance Characteristics (Cont.) (@T_A = +25°C, V_{DD} = 5V, f = 1kHz, Gain = 2V/V, unless otherwise specified.)

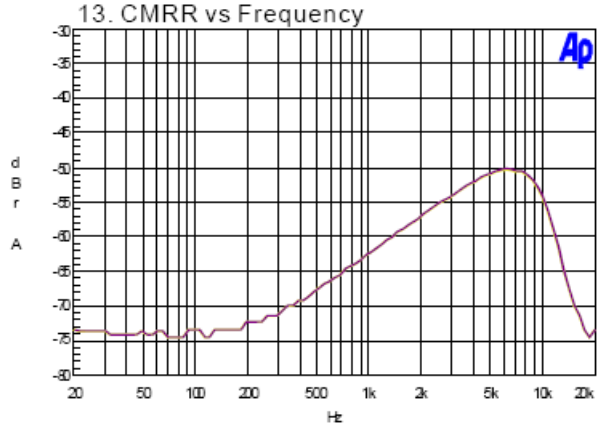
11. Frequency Response



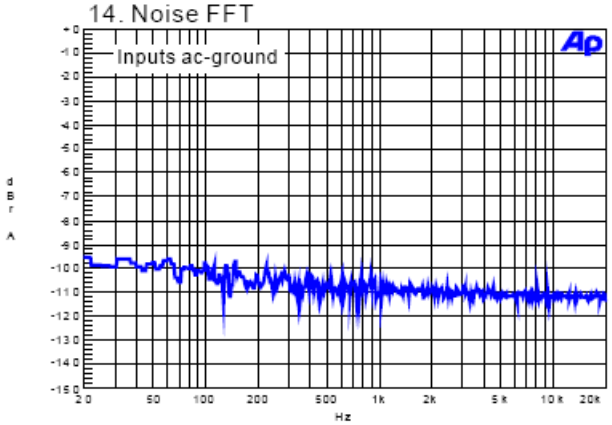
12. PSRR VS Frequency



13. CMRR vs Frequency

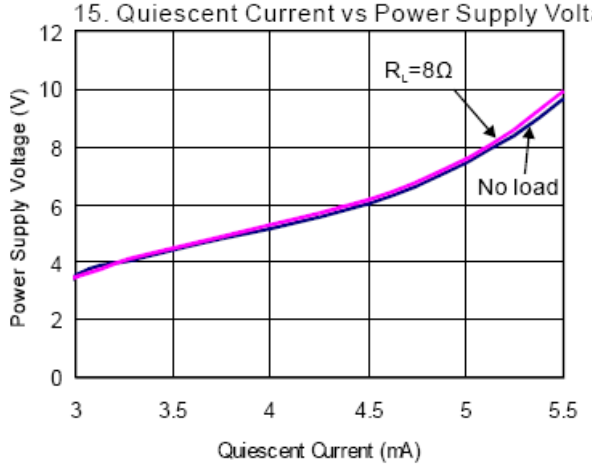


14. Noise FFT

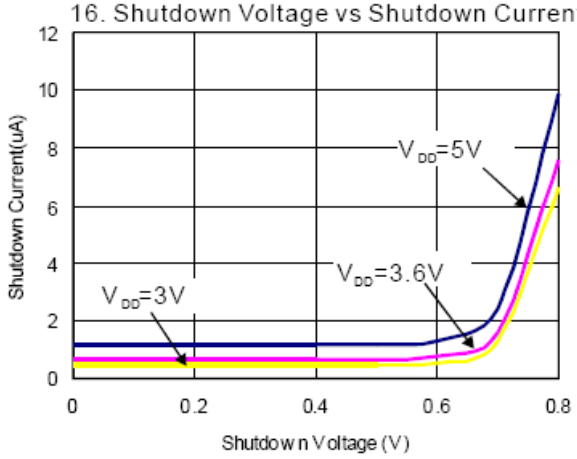


Typical Performance Characteristics (Cont.) (@T_A = +25°C, V_{DD} = 5V, f = 1kHz, Gain = 2V/V, unless otherwise specified.)

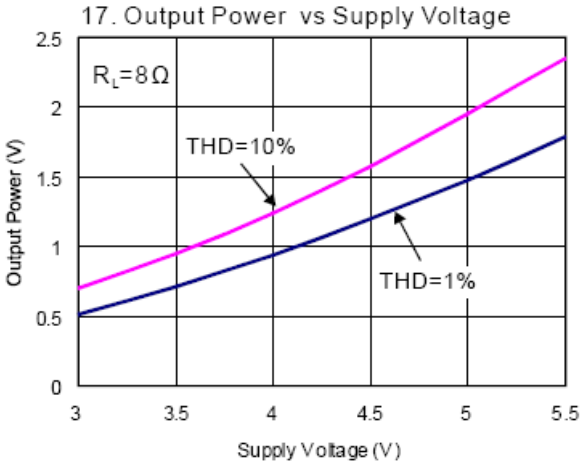
15. Quiescent Current vs Power Supply Voltage



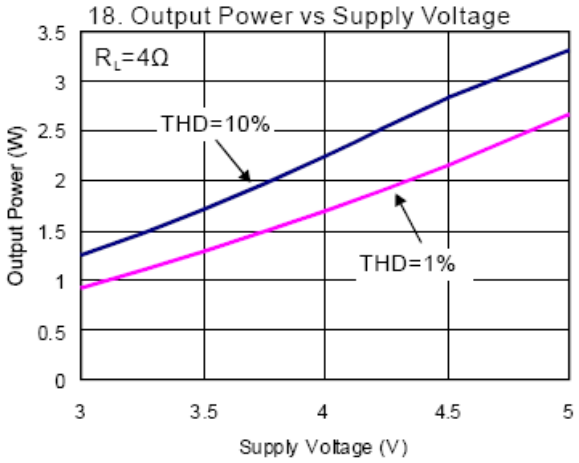
16. Shutdown Voltage vs Shutdown Current



17. Output Power vs Supply Voltage

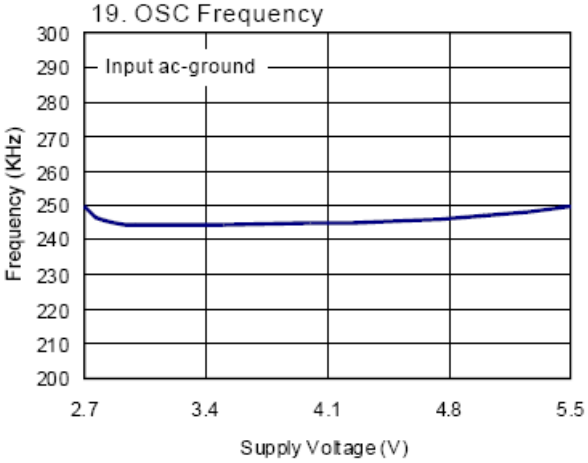


18. Output Power vs Supply Voltage

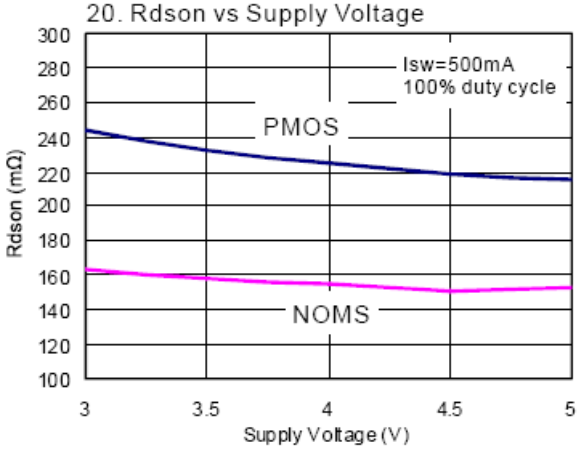


Typical Performance Characteristics (Cont.) (@T_A = +25°C, V_{DD} = 5V, f = 1kHz, Gain = 2V/V, unless otherwise specified.)

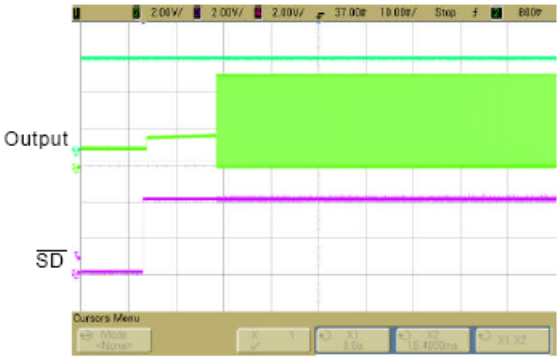
19. OSC Frequency



20. Rdson vs Supply Voltage

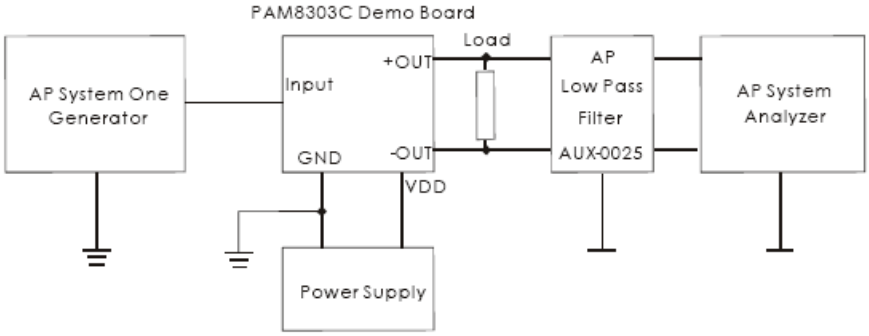


21. Start-up from Shutdown



Application Information

Test Setup for Performance Testing (Notes 5 & 6)



Notes: 5. The AP AUX-0025 low-pass filter is necessary for Class-D amplifier measurement with AP analyzer.
6. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Input Resistance (R_I)

The input resistors (R_I) set the gain of the amplifier according to the following equation.

$$\text{Gain} = \frac{2x150k\Omega}{R_I}\left(\frac{V}{V}\right)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the PAM8303C to limit noise injection on the high-impedance nodes.

For optimal performance the gain must be set to 2 × (R_I = 150k) or lower. Lower gain allows the PAM8303C to operate at its best and keeps a high voltage at the input, which makes the inputs less susceptible to noise. In addition to these features, higher value of R_I minimizes pop noise.

Input Capacitors (C_I)

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_I and the minimum input impedance, R_I, form is a high-pass filter with the corner frequency determined in the following equation.

$$f_C = \frac{1}{2\Pi R_I C_I}$$

It is important to consider how the value of C_I as the capacitor directly affects the low-frequency performance of the circuit. For example, when R_I is 150kΩ, and the specification calls for a flat bass, response is down to 150Hz. The equation is reconfigured as follows.

$$C_I = \frac{1}{2\Pi R_I F_{CI}}$$

When input-resistance variation is considered, the C_I is 7nF, so one would choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_I, R_I + R_F) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications.

For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at V_{DD}/2, which is likely higher than the source DC level. Note that it is important to confirm the capacitor polarity in the application.

Application Information (Cont.)

Decoupling Capacitor (C_S)

The PAM8303C is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power-supply decoupling also prevents the oscillations caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher-frequency transients, spikes, or digital hash on the line, a good low equivalent series resistance (ESR) ceramic capacitor, typically 1µF, is placed as close as possible to the device near each VDD and PVDD pin for the best operation. For filtering lower-frequency noise signals, a large ceramic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination as shown in Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies but with low impedance at low frequencies.

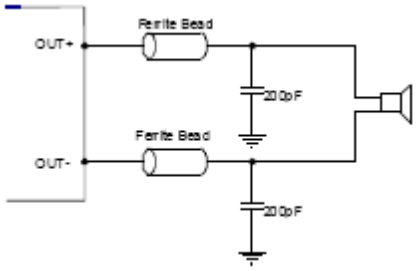


Figure 1. Ferrite Bead Filter to Reduce EMI

In order to reduce power consumption while not in use, the PAM8303C contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin. By switching the shutdown pin connected to GND, the PAM8303C supply current draw is minimized in idle mode.

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8303C contains shutdown circuitry that is used to turn off the amplifier's bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the pin. By switching the shutdown pin connected to GND, the PAM8303C supply-current draw will be minimized in idle mode.

Undervoltage Lockout (UVLO)

The PAM8303C incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.3V or below, the PAM8303C goes into a state of shutdown, and the device comes out of its shutdown state and restores to normal function only when reset the power supply or $\overline{SD}$ pin.

Thermal protection on the PAM8303C prevents the device from damage when the internal die temperature exceeds +135°C. There is a +15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device enters the shutdown state, and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreases by +30°C. This large hysteresis prevents motor-boating sound, and the device begins normal operation at this point with no external system interaction.

Pop and Click Circuitry

The PAM8303C contains circuitry to minimize turn-on and turn-off transients, or click and pops, where turn-on refers to either power supply turn on or device recovery from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device remains in mute mode until the reference voltage reaches half-supply voltage, 1/2 V_{DD}. As soon as the reference voltage is stable, the device begins full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power-supply voltage.

Application Information (Cont.)

PCB Layout Guidelines

Grounding

It is recommended to use plain grounding or separate grounds. Do not use one-line connecting-power GND and analog GND. Noise currents in the output power stage must be returned to output noise ground and nowhere else. When these currents circulate elsewhere, the currents can get into the power supply, the signal ground, and so on, or even worse, the currents can form a loop and radiate noise. Any of these instances results in degraded-amplifier performance. The output-noise ground that the logical returns for the output noise currents associated with Class-D switching must tie to system ground at the power exclusively. Signal currents for the inputs' reference must be returned to quiet ground. This ground only ties to the signal components and the GND pin. GND then ties to system ground.

Power Supply Line

Similar to the ground, V_{DD} and PV_{DD} must be separately connected to the system power supply. It is recommended that all of the trace be routed as short and thick as possible. For the power-line layout, a water stream, or any barricade, placed in the trace can result in the bad performance of the amplifier (as shown in Figure 2).

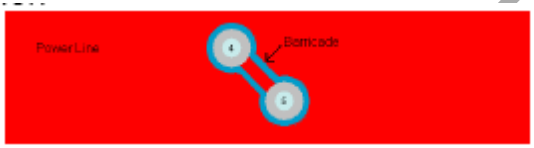


Figure 2. Power Line

Components Placement

Decoupling capacitors—as previously described, the high-frequency, 1µF decoupling capacitors should be placed as close to the power supply terminals (V_{DD} and PV_{DD}) as possible. Large bulk power supply decoupling capacitors (10µF or greater) must be placed near the PAM8303C on the PV_{DD} terminal.

Input resistors and capacitors must be placed very close to input pins.

Output filter—the ferrite EMI filter must be placed as close to the output terminals as possible for the best EMI performance, and the capacitors used in the filters must be grounded to system ground.

Ordering Information

PAM8303C X X X

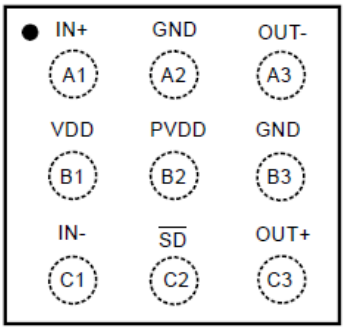
Pin Configuration	Package Type	Number of Pins
A	~~Z: WCSP~~	C: 8
B	Y: DFN3030-8	~~N: 9~~
C	S: MSOP-8	
(Refer to P2, 3 Pin Configuration		

Part Number	Package (Note 8)	Part Marking	Tape and Reel Quantity	Status (Note 7)
PAM8303CBYC	U-DFN3030-8	P8303C XXXYW	3000	In Production
PAM8303CBSC	MSOP-8	P8303C XXXYW	2500	In Production

Notes: 7. PAM8303CAZN (in package WCSP) is End of Life without any alternatives. PAM8303CCYC is End of Life, and the recommended alternative is PAM8303CBYC.
8. For packaging details, see https://www.diodes.com/design/support/packaging/diodes-packaging/diodes-package-outlines-and-pad-layouts/.

Marking Information

9 Ball WCSP (A) (EOL)
Top View

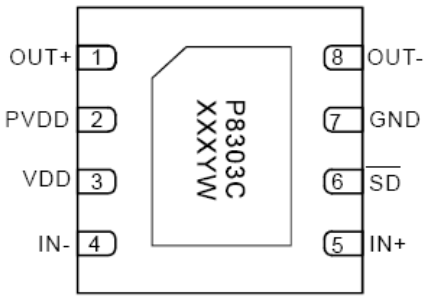


Marking

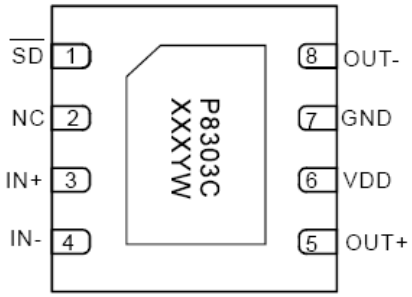
BH
YW

BH: Product Code of PAM8303C
Y: Year
W: Week

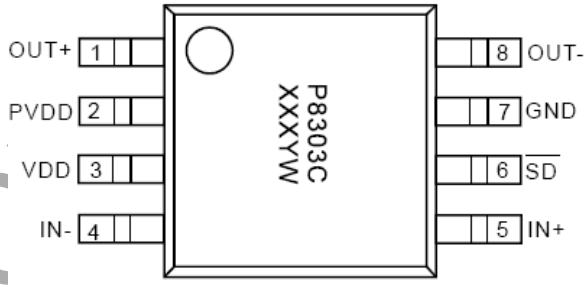
DFN3X3(B)
Top View



DFN3X3(C)
Top View



MSOP-8(B)
Top View

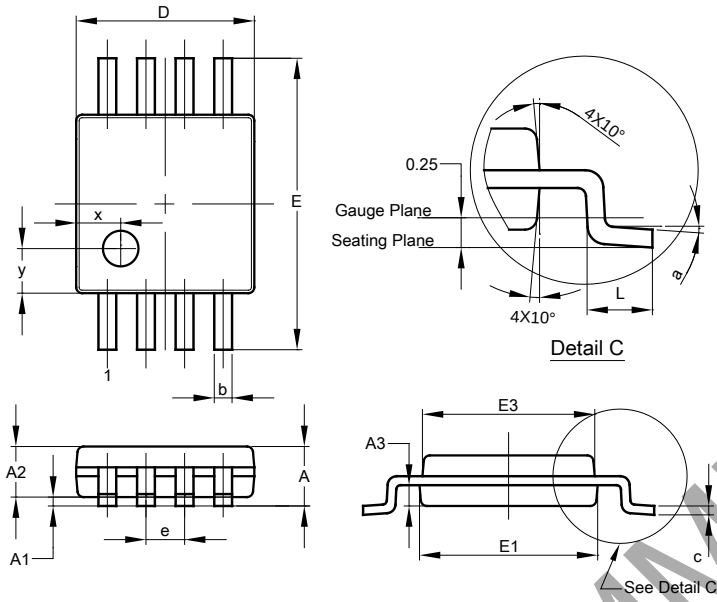


X: Internal Code
Y: Year
W: Week

Package Outline Dimensions (All dimensions in mm)

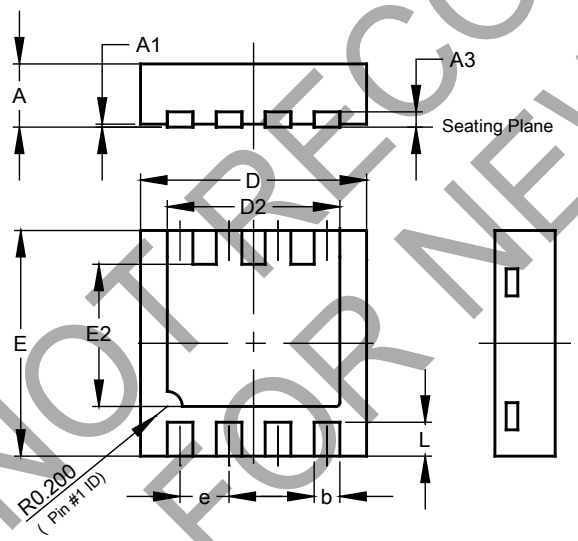
Please see http://www.diodes.com/package-outlines.html for the latest version.

MSOP-8



MSOP-8			
Dim	**Min**	**Max**	**Typ**
A	-	1.10	-
A1	0.05	0.15	0.10
A2	0.75	0.95	0.86
A3	0.29	0.49	0.39
b	0.22	0.38	0.30
c	0.08	0.23	0.15
D	2.90	3.10	3.00
E	4.70	5.10	4.90
E1	2.90	3.10	3.00
E3	2.85	3.05	2.95
e	-	-	0.65
L	0.40	0.80	0.60
a	0°	8°	4°
x	-	-	0.750
y	-	-	0.750
All Dimensions in mm			

U-DFN3030-8

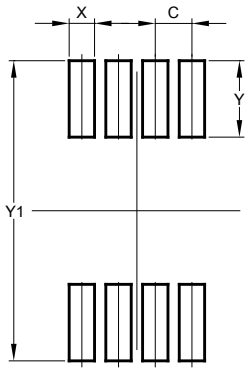


U-DFN3030-8			
Dim	**Min**	**Max**	**Typ**
A	0.57	0.63	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.29	0.39	0.34
D	2.90	3.10	3.00
D2	2.19	2.39	2.29
e	-	-	0.65
E	2.90	3.10	3.00
E2	1.64	1.84	1.74
L	0.30	0.60	0.45
All Dimensions in mm			

Suggested Pad Layout

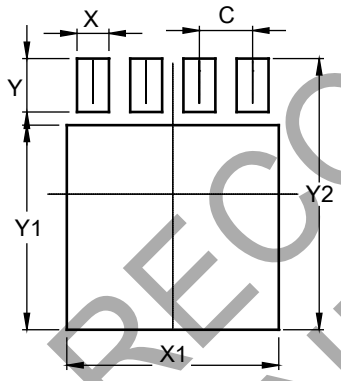
Please see http://www.diodes.com/package-outlines.html for the latest version.

MSOP-8



Dimensions	Value (in mm)
C	0.650
X	0.450
Y	1.350
Y1	5.300

U-DFN3030-8



Dimensions	Value (in mm)
C	0.650
X	0.390
X1	2.590
Y	0.650
Y1	2.490
Y2	3.300

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