OP777/OP727/OP747–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = 5.0 V, V_{CM} = 2.5 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage OP777	V_{OS}	+25°C < T_A < +85°C		20	100	µV
		–40°C < T_A < +85°C		50	200	µV
Offset Voltage OP727/OP747		+25°C < T_A < +85°C		30	160	µV
		–40°C < T_A < +85°C		60	300	µV
Input Bias Current	I_B	–40°C < T_A < +85°C		5.5	11	nA
Input Offset Current	I_{OS}	–40°C < T_A < +85°C		0.1	2	nA
Input Voltage Range			0		4	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 4 V	104	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 4.5 V	300	500		V/mV
Offset Voltage Drift OP777	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +85°C		0.3	1.3	µV/°C
Offset Voltage Drift OP727/OP747	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +85°C		0.4	1.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, –40 °C to +85 °C	4.88	4.91		V
Output Voltage Low	V_{OL}	I_L = 1 mA, –40 °C to +85 °C		126	140	mV
Output Circuit	I_{OUT}	$V_{DROPOUT}$ < 1 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 3 V to 30 V	120	130		dB
Supply Current/Amplifier OP777	I_{SY}	V_O = 0 V		220	270	µA
		–40°C < T_A < +85°C		270	320	µA
Supply Current/Amplifier OP727/OP747		V_O = 0 V		235	290	µA
		–40°C < T_A < +85°C		290	350	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.2		V/µs
Gain Bandwidth Product	GBP			0.7		MHz
NOISE PERFORMANCE						
Voltage Noise	e_np-p	0.1 Hz to 10 Hz		0.4		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.13		pA/√Hz

NOTES

Typical specifications: >50% of units perform equal to or better than the "typical" value.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ ±15 V, V_{CM} = 0 V, T_A = 25°C unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage OP777	V_{OS}	+25 °C < T_A < +85 °C		30	100	μV
		–40 °C < T_A < +85 °C		50	200	μV
Offset Voltage OP727/OP747	V_{OS}	+25 °C < T_A < +85 °C		30	160	μV
		–40 °C < T_A < +85 °C		50	300	μV
Input Bias Current	I_B	–40 °C < T_A < +85 °C		5	10	nA
Input Offset Current	I_{OS}	–40 °C < T_A < +85 °C		0.1	2	nA
Input Voltage Range			–15		+14	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –15 V to +14 V	110	120		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ, V_O = –14.5 V to +14.5 V	1,000	2,500		V/mV
Offset Voltage Drift OP777	$\Delta V_{OS}/\Delta T$	–40 °C < T_A < +85 °C		0.3	1.3	μV/°C
Offset Voltage Drift OP727/OP747	$\Delta V_{OS}/\Delta T$	–40 °C < T_A < +85 °C		0.4	1.5	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, –40 °C to +85 °C	+14.9	+14.94		V
Output Voltage Low	V_{OL}	I_L = 1 mA, –40 °C to +85 °C		–14.94	–14.9	V
Output Circuit	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.5 V to ±15 V	120	130		dB
Supply Current/Amplifier OP777	I_{SY}	V_O = 0 V		300	350	μA
		–40 °C < T_A < +85 °C		350	400	μA
Supply Current/Amplifier OP727/747		V_O = 0 V		320	375	μA
		–40 °C < T_A < +85 °C		375	450	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.2		V/μs
Gain Bandwidth Product	GBP			0.7		MHz
NOISE PERFORMANCE						
Voltage Noise	e_np-p	0.1 Hz to 10 Hz		0.4		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		15		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.13		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

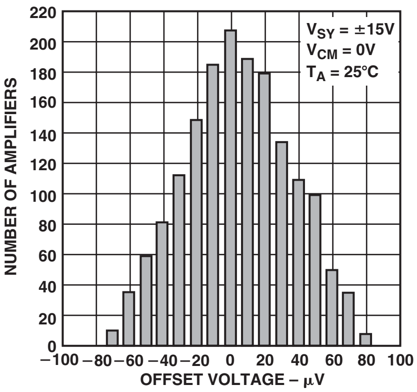
Supply Voltage . . . . 36 V
Input Voltage . . . . $–V_S – 5$ V to $+V_S + 5$ V
Differential Input Voltage . . . . ± Supply Voltage
Output Short-Circuit Duration to GND . . . . Indefinite
Storage Temperature Range
  RM, R, RU Packages . . . . –65°C to +150°C
Operating Temperature Range
  OP777/OP727/OP747 . . . . –40°C to +85°C
Junction Temperature Range
  RM, R, RU Packages . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . 300°C
Electrostatic Discharge (Human Body Model) . . . . 2000 V max

Package Type	θ_{JA}[3]	θ_{JC}	Unit
8-Lead MSOP (RM)	190	44	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

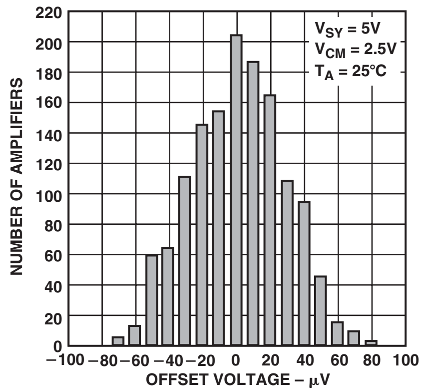
NOTES
[1]Absolute maximum ratings apply at 25°C, unless otherwise noted.
[2]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[3]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

CAUTION

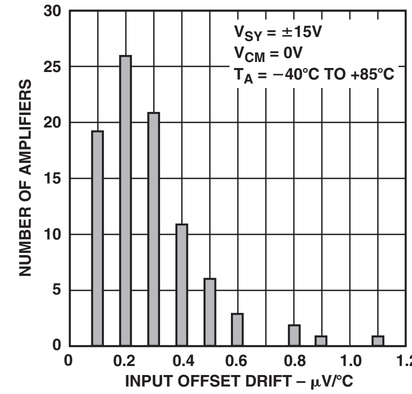
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP777/OP727/OP747 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



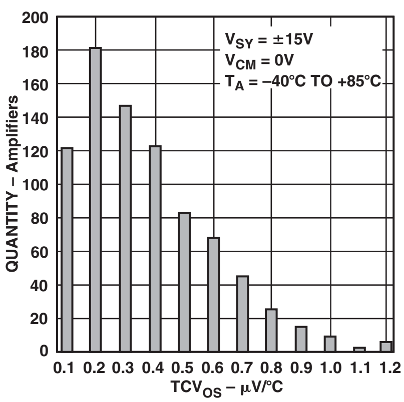
TPC 1. OP777 Input Offset Voltage Distribution



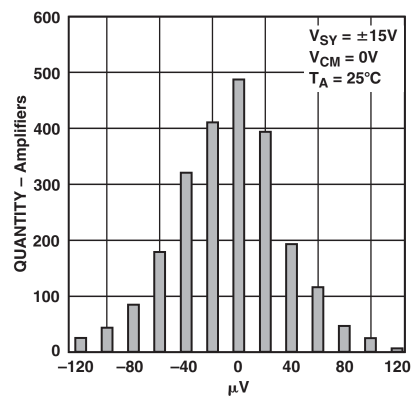
TPC 2. OP777 Input Offset Voltage Distribution



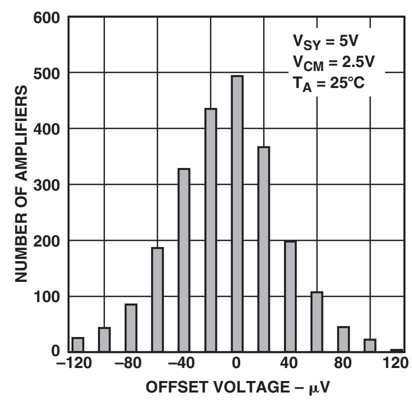
TPC 3. OP777 Input Offset Voltage Drift Distribution



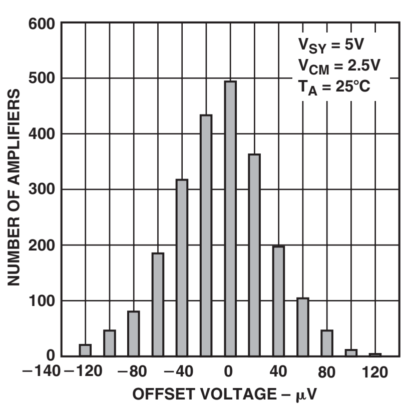
TPC 4. OP727/OP747 Input Offset Voltage Drift (TCV$_{OS}$ Distribution)



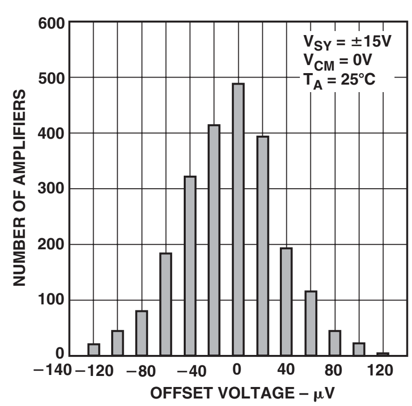
TPC 5. OP747 Input Offset Voltage Distribution



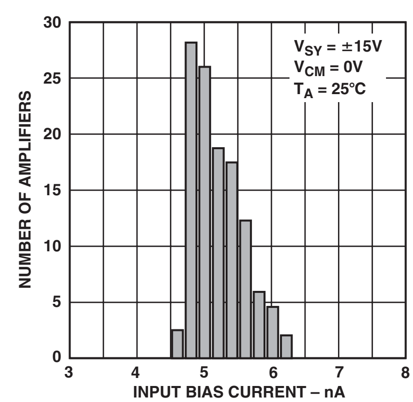
TPC 6. OP747 Input Offset Voltage Distribution



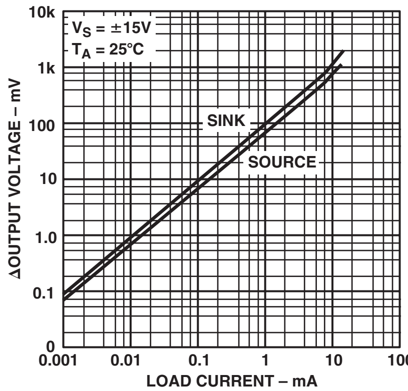
TPC 7. OP727 Input Offset Voltage Distribution



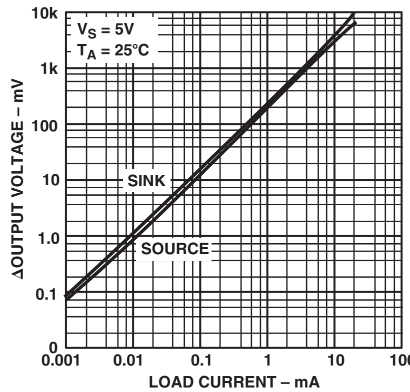
TPC 8. OP727 Input Offset Voltage Distribution



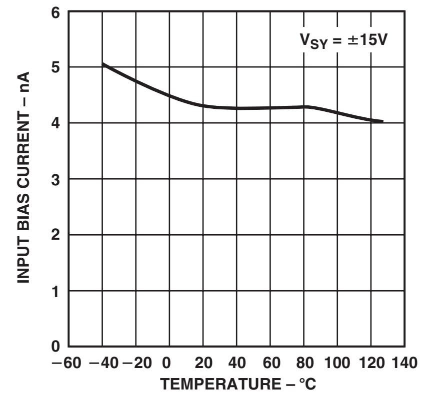
TPC 9. Input Bias Current Distribution



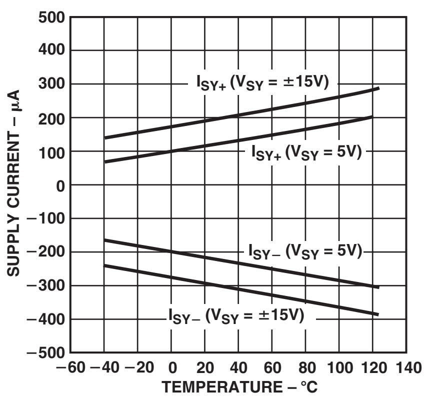
TPC 10. Output Voltage to Supply Rail vs. Load Current



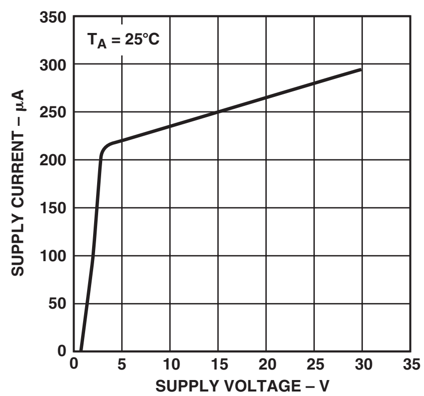
TPC 11. Output Voltage to Supply Rail vs. Load Current



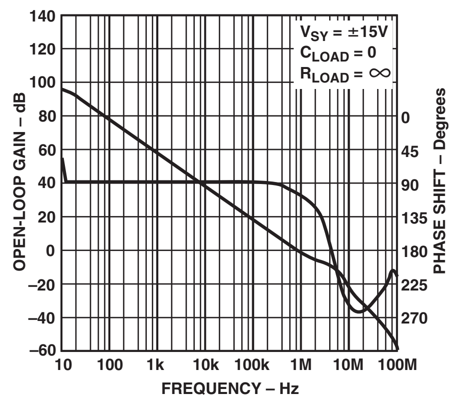
TPC 12. Input Bias Current vs. Temperature



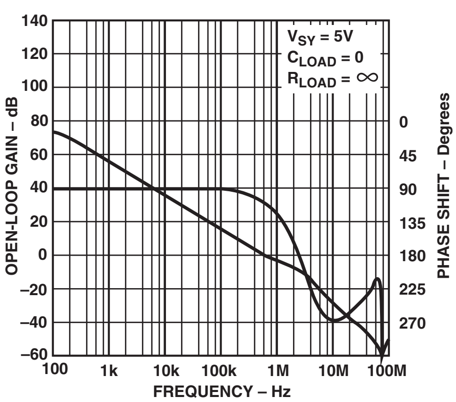
TPC 13. Supply Current vs. Temperature



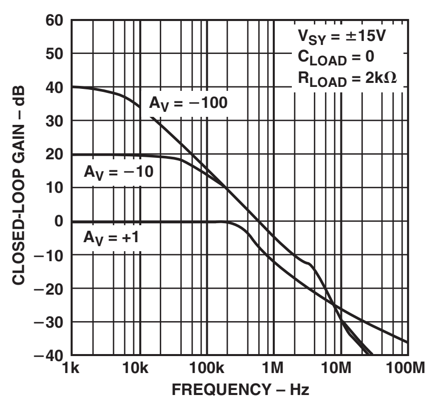
TPC 14. Supply Current vs. Supply Voltage



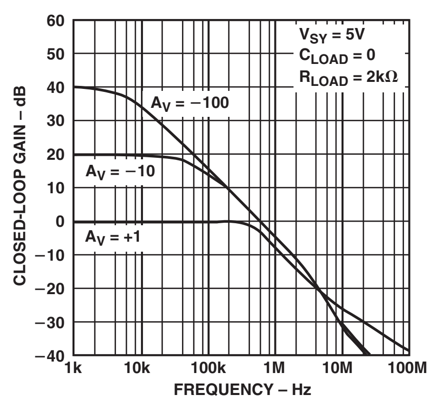
TPC 15. Open Loop Gain and Phase Shift vs. Frequency



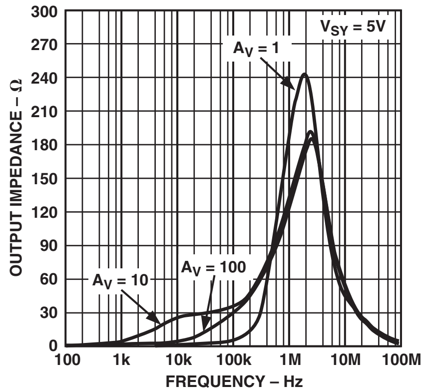
TPC 16. Open Loop Gain and Phase Shift vs. Frequency



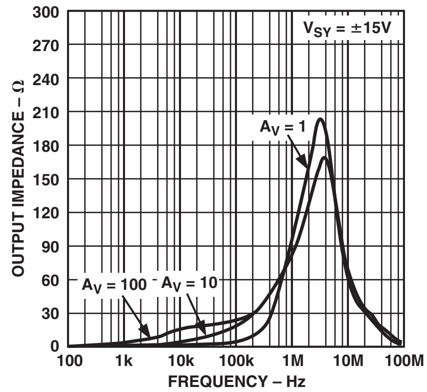
TPC 17. Closed Loop Gain vs. Frequency



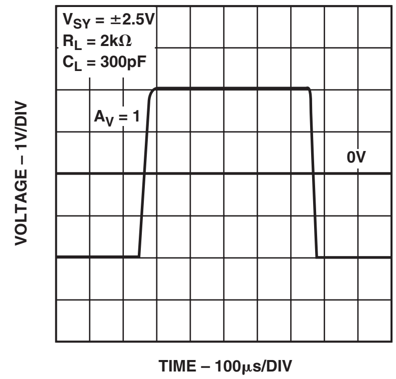
TPC 18. Closed Loop Gain vs. Frequency



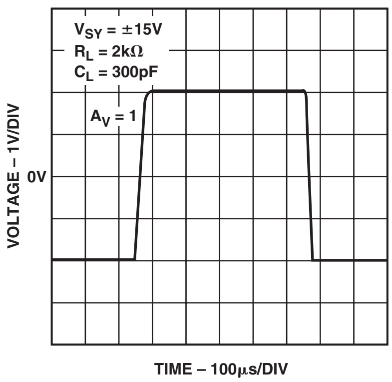
TPC 19. Output Impedance vs. Frequency



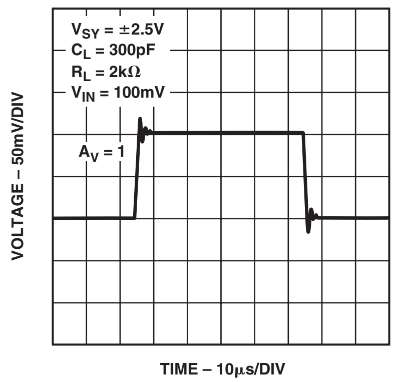
TPC 20. Output Impedance vs. Frequency



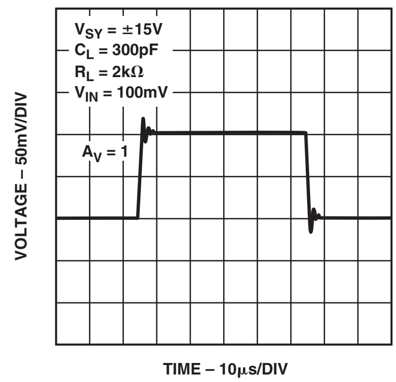
TPC 21. Large Signal Transient Response



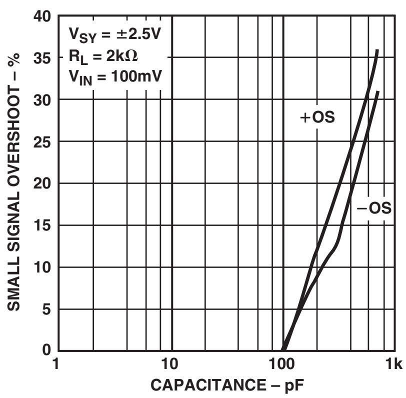
TPC 22. Large Signal Transient Response



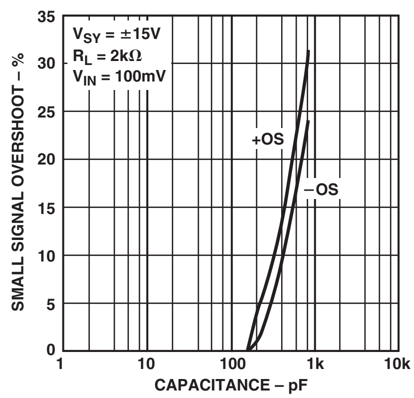
TPC 23. Small Signal Transient Response



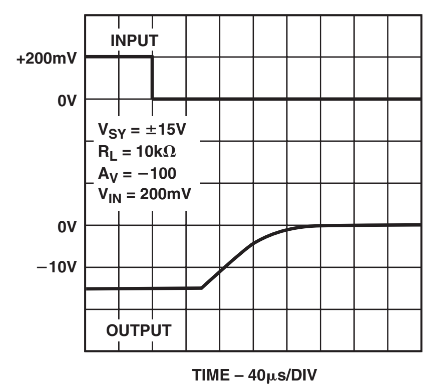
TPC 24. Small Signal Transient Response



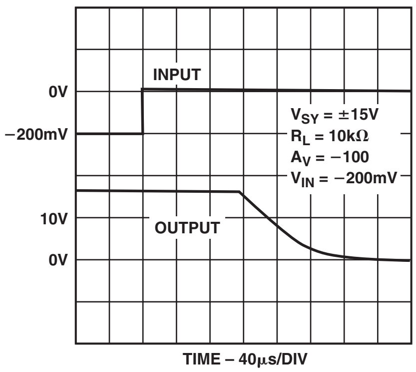
TPC 25. Small Signal Overshoot vs. Load Capacitance



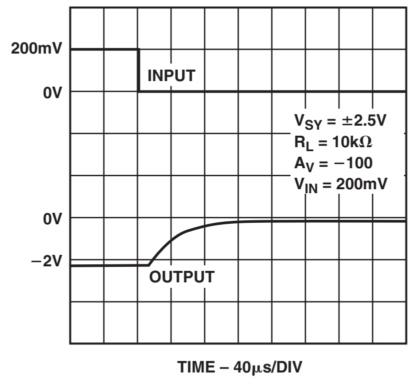
TPC 26. Small Signal Overshoot vs. Load Capacitance



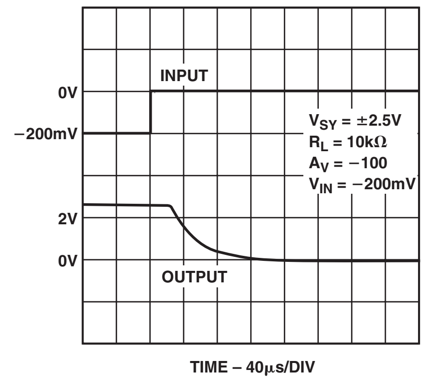
TPC 27. Negative Overvoltage Recovery



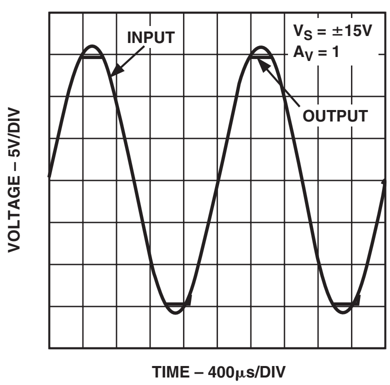
TPC 28. Positive Overvoltage Recovery



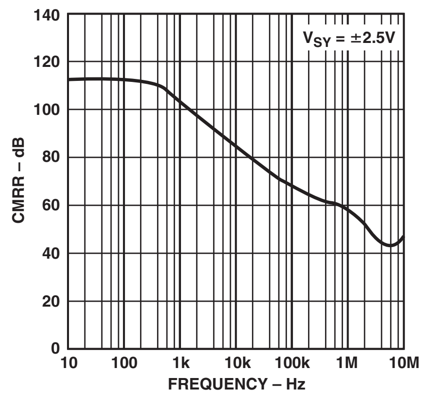
TPC 29. Negative Overvoltage Recovery



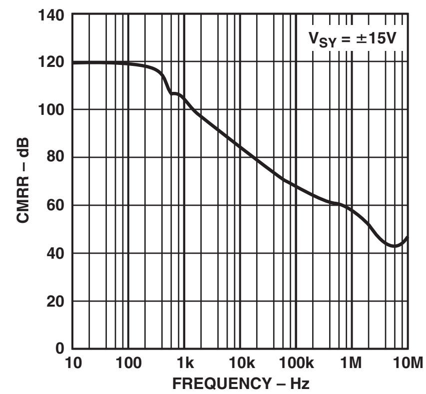
TPC 30. Positive Overvoltage Recovery



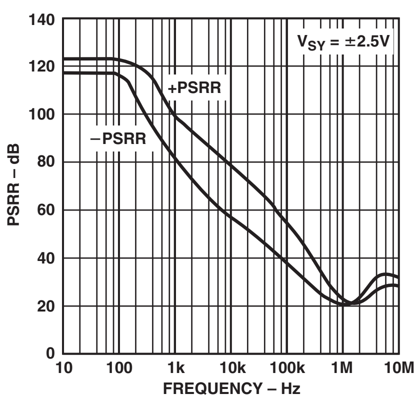
TPC 31. No Phase Reversal



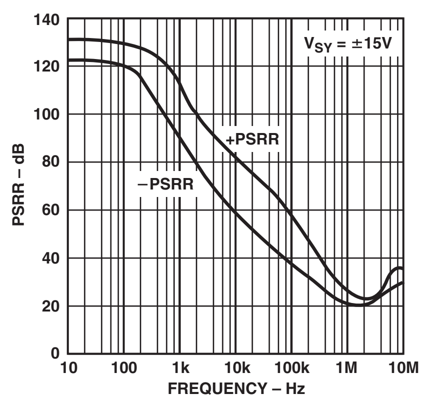
TPC 32. CMRR vs. Frequency



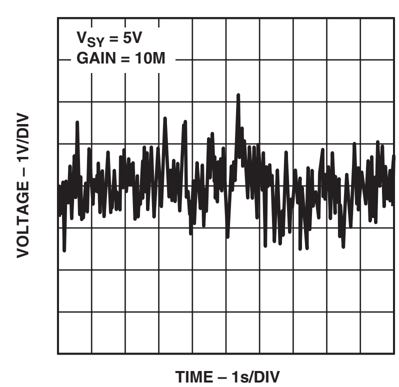
TPC 33. CMRR vs. Frequency



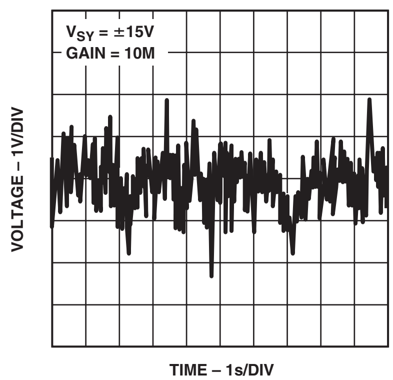
TPC 34. PSRR vs. Frequency



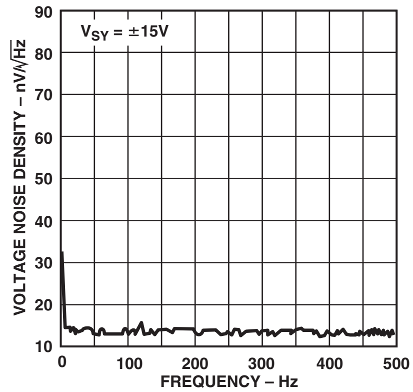
TPC 35. PSRR vs. Frequency



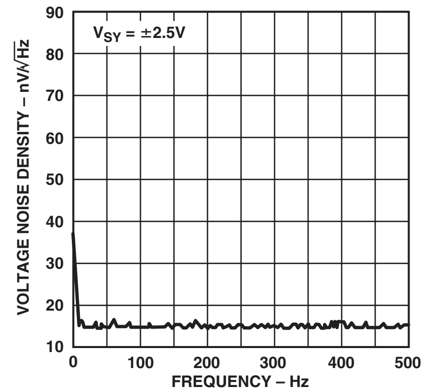
TPC 36. 0.1 Hz to 10 Hz Input Voltage Noise



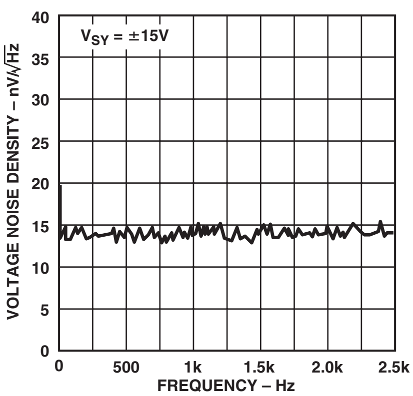
TPC 37. 0.1 Hz to 10 Hz Input Voltage Noise



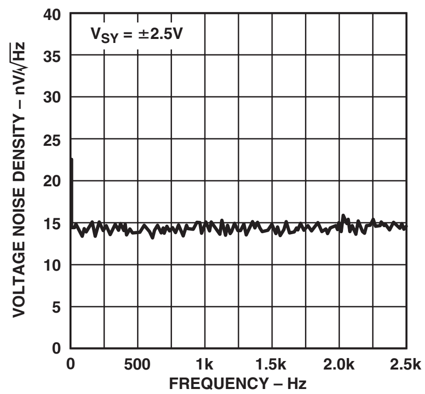
TPC 38. Voltage Noise Density



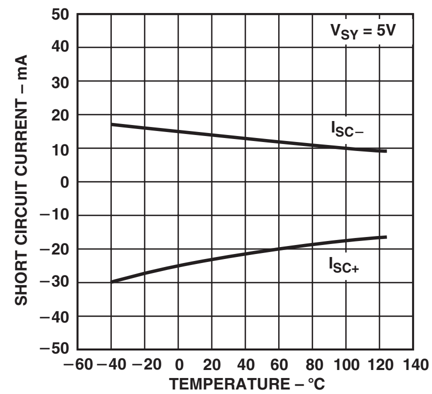
TPC 39. Voltage Noise Density



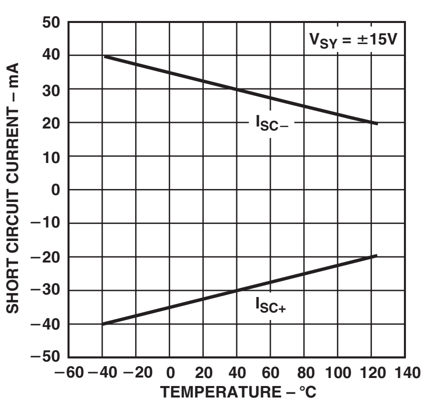
TPC 40. Voltage Noise Density



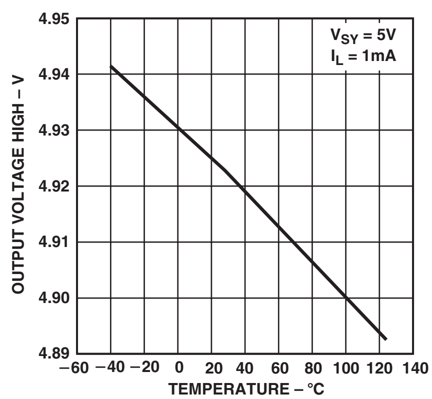
TPC 41. Voltage Noise Density



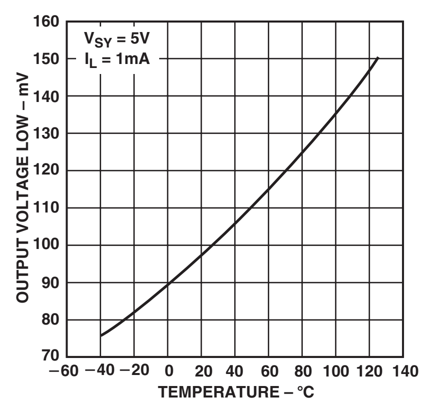
TPC 42. Short Circuit Current vs. Temperature



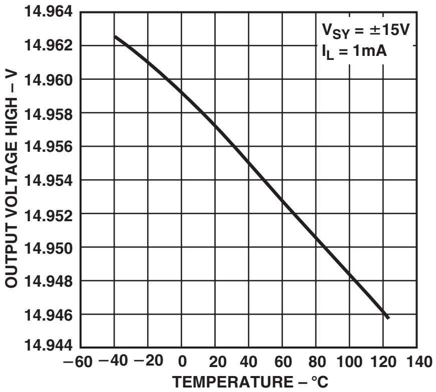
TPC 43. Short Circuit Current vs. Temperature



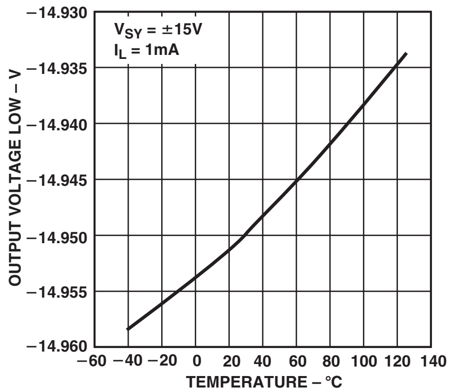
TPC 44. Output Voltage High vs. Temperature



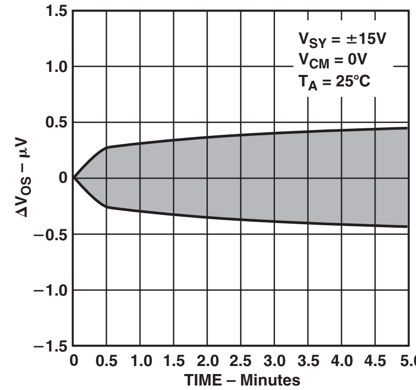
TPC 45. Output Voltage Low vs. Temperature



TPC 46. Output Voltage High vs. Temperature



TPC 47. Output Voltage Low vs. Temperature



TPC 48. Warm-Up Drift

BASIC OPERATION

The OP777/OP727/OP747 amplifier uses a precision Bipolar PNP input stage coupled with a high-voltage CMOS output stage. This enables this amplifier to feature an input voltage range which includes the negative supply voltage (often ground-in single-supply applications) and also swing to within 1 mV of the output rails. Additionally, the input voltage range extends to within 1 V of the positive supply rail. The epitaxial PNP input structure provides high breakdown voltage, high gain, and an input bias current figure comparable to that obtained with a "Darlington" input stage amplifier but without the drawbacks (i.e., severe penalties for input voltage range, offset, drift and noise). The PNP input structure also greatly lowers the noise and reduces the dc input error terms.

Supply Voltage

The amplifiers are fully specified with a single 5 V supply and, due to design and process innovations, can also operate with a supply voltage from 3.0 V up to 30 V. This allows operation from most split supplies used in current industry practice, with the advantage of substantially increased input and output voltage ranges over conventional split-supply amplifiers. The OP777/OP727/OP747 series is specified with (V_{SY} = 5 V, V– = 0 V and V_{CM} = 2.5 V which is most suitable for single-supply application. With PSRR of 130 dB (0.3 µV/V) and CMRR of 110 dB (3 µV/V) offset is minimally affected by power supply or common-mode voltages. Dual supply, ±15 V operation is also fully specified.

Input Common-Mode Voltage Range

The OP777/OP727/OP747 is rated with an input common-mode voltage which extends from the minus supply to within 1 V of the positive supply. However, the amplifier can still operate with input voltages slightly below V_{EE}. In Figure 2, OP777/OP727/OP747 is configured as a difference amplifier with a single supply of 3.0 V and negative dc common-mode voltages applied at the inputs terminals. A 400 mV p-p input is then applied to the noninverting input. It can be seen from the graph below that the output does not show any distortion. Micropower operation is maintained by using large input and feedback resistors.

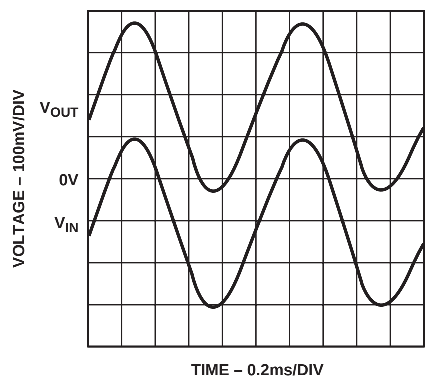


Figure 1. Input and Output Signals with V_{CM} < 0 V

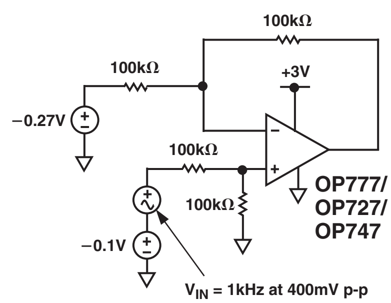


Figure 2. OP777/OP727/OP747 Configured as a Difference Amplifier Operating at V_{CM} < 0 V

Input Over Voltage Protection

When the input of an amplifier is more than a diode drop below V_{EE}, or above V_{CC}, large currents will flow from the substrate (V–) or the positive supply (V+), respectively, to the input pins which can destroy the device. In the case of OP777/OP727/OP747, differential voltages equal to the supply voltage will not cause any problem (see Figure 3). OP777/OP727/OP747 has built-in 500 Ω internal current limiting resistors, in series with the inputs, to minimize the chances of damage. It is a good practice to keep the current flowing into the inputs below 5 mA. In this context it should also be noted that the high breakdown of the input transistors removes the necessity for clamp diodes between the inputs of the amplifier, a feature that is mandatory on many precision op amps. Unfortunately, such clamp diodes greatly interfere with many application circuits such as precision rectifiers and comparators. The OP777/OP727/OP747 series is free from such limitations.

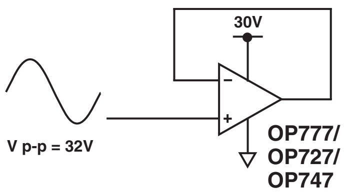


Figure 3a. Unity Gain Follower

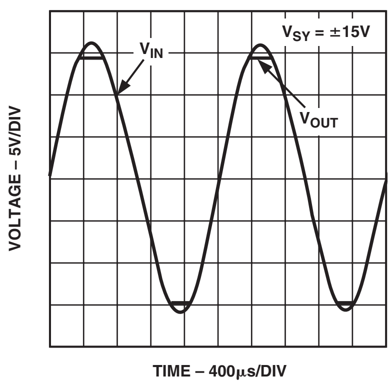


Figure 3b. Input Voltage Can Exceed the Supply Voltage Without Damage

Phase Reversal

Many amplifiers misbehave when one or both of the inputs are forced beyond the input common-mode voltage range. Phase reversal is typified by the transfer function of the amplifier effectively reversing its transfer polarity. In some cases this can cause lockup in servo systems and may cause permanent damage or nonrecoverable parameter shifts to the amplifier. Many amplifiers feature compensation circuitry to combat these effects, but some are only effective for the inverting input. Additionally, many of these schemes only work for a few hundred millivolts or so beyond the supply rails. OP777/OP727/OP747 has a protection circuit against phase reversal when one or both inputs are forced beyond their input common-mode voltage range. It is not recommended that the parts be continuously driven more than 3 V beyond the rails.

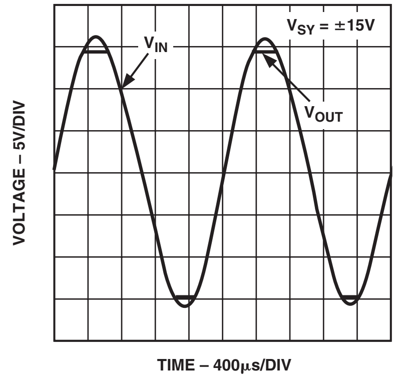


Figure 4. No Phase Reversal

Output Stage

The CMOS output stage has excellent (and fairly symmetric) output drive and with light loads can actually swing to within 1 mV of both supply rails. This is considerably better than similar amplifiers featuring (so-called) rail-to-rail bipolar output stages. OP777/OP727/OP747 is stable in the voltage follower configuration and responds to signals as low as 1 mV above ground in single supply operation.

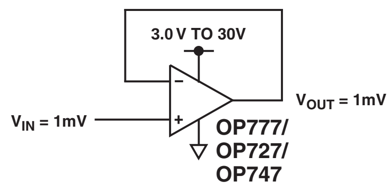


Figure 5. Follower Circuit

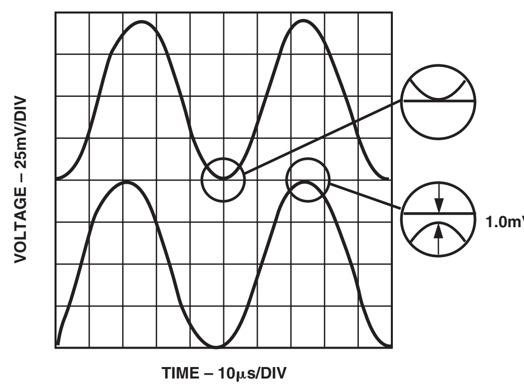


Figure 6. Rail-to-Rail Operation

Output Short Circuit

The output of the OP777/OP727/OP747 series amplifier is protected from damage against accidental shorts to either supply voltage, provided that the maximum die temperature is not exceeded on a long-term basis (see Absolute Maximum Rating section). Current of up to 30 mA does not cause any damage.

A Low-Side Current Monitor

In the design of power supply control circuits, a great deal of design effort is focused on ensuring a pass transistor's long-term reliability over a wide range of load current conditions. As a result, monitoring and limiting device power dissipation is of prime importance in these designs. Figure 7 shows an example of 5 V, single-supply current monitor that can be incorporated into the design of a voltage regulator with foldback current limiting or a high current power supply with crowbar protection. The design capitalizes on the OP777's common-mode range that extends to ground. Current is monitored in the power supply return where a 0.1 Ω shunt resistor, R_{SENSE}, creates a very small voltage drop. The voltage at the inverting terminal becomes equal to the voltage at the noninverting terminal through the feedback of Q1, which is a 2N2222 or equivalent NPN transistor. This makes the voltage drop across R1 equal to the voltage drop across R_{SENSE}. Therefore, the current through Q1 becomes directly proportional to the current through R_{SENSE}, and the output voltage is given by:

$$V_{OUT} = 5\,V - \left(\frac{R2}{R1} \times R_{SENSE} \times I_L\right)$$

The voltage drop across $R2$ increases with I_L increasing, so V_{OUT} decreases with higher supply current being sensed. For the element values shown, the V_{OUT} is 2.5 V for return current of 1 A.

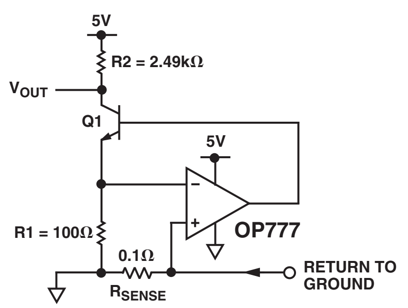


Figure 7. A Low-Side Load Current Monitor

The OP777/OP727/OP747 is very useful in many bridge applications. Figure 8 shows a single-supply bridge circuit in which its output is linearly proportional to the fractional deviation (δ) of the bridge. Note that δ = ΔR/R.

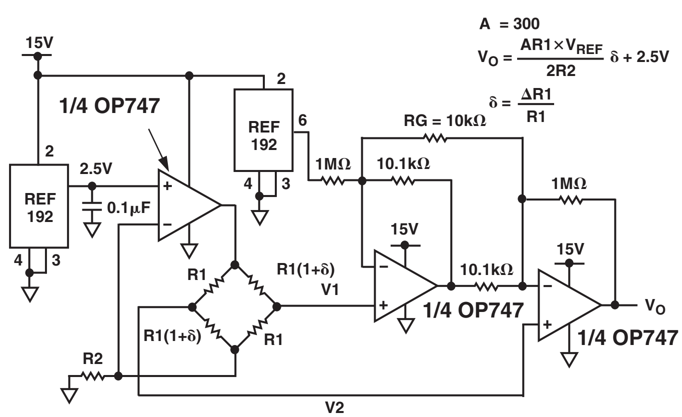


Figure 8. Linear Response Bridge, Single Supply

In systems where dual supplies are available, the circuit of Figure 9 could be used to detect bridge outputs that are linearly related to the fractional deviation of the bridge.

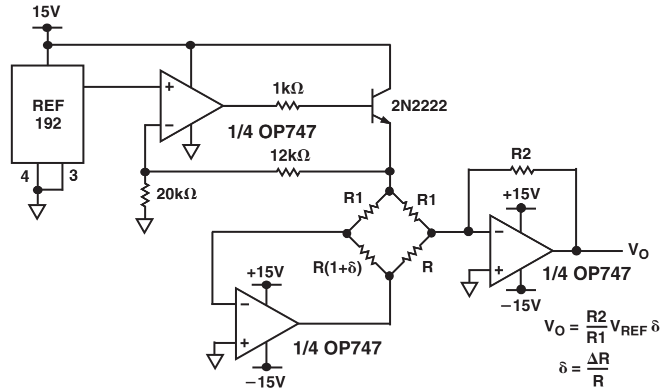


Figure 9. Linear Response Bridge

A single-supply current source is shown in Figure 10. Large resistors are used to maintain micropower operation. Output current can be adjusted by changing the R2B resistor. Compliance voltage is:

$$|V_L| \leq |V_{SAT}| - |V_S|$$

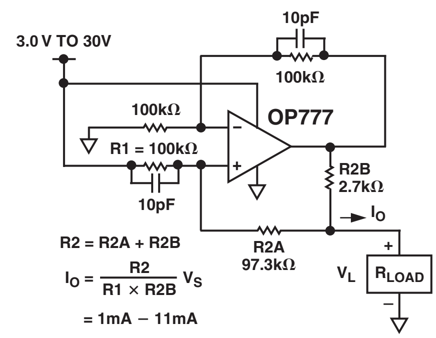


Figure 10. Single-Supply Current Source

A single-supply instrumentation amplifier using one OP727 amplifier is shown in Figure 11. For true difference R3/R4 = R1/R2. The formula for the CMRR of the circuit at dc is CMRR = 20 × log (100/(1–(R2 × R3)/(R1× R4)). It is common to specify the accuracy of the resistor network in terms of resistor-to-resistor percentage mismatch. We can rewrite the CMRR equation to reflect this CMRR = 20 × log (10000/% Mismatch). The key to high CMRR is a network of resistors that are well matched from the perspective of both resistive ratio and relative drift. It should be noted that the absolute value of the resistors and their absolute drift are of no consequence. Matching is the key. CMRR is 100 dB with 0.1% mismatched resistor network. To maximize CMRR, one of the resistors such as R4 should be trimmed. Tighter matching of two op amps in one package (OP727) offers a significant boost in performance over the triple op amp configuration.

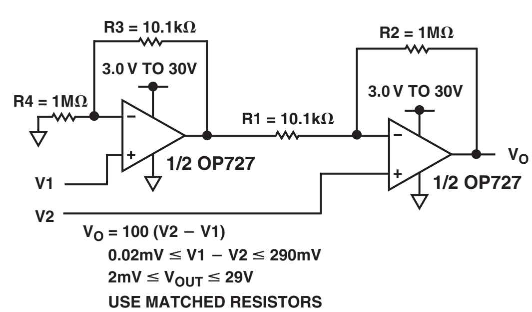


Figure 11. Single-Supply Micropower Instrumentation Amplifier

OUTLINE DIMENSIONS

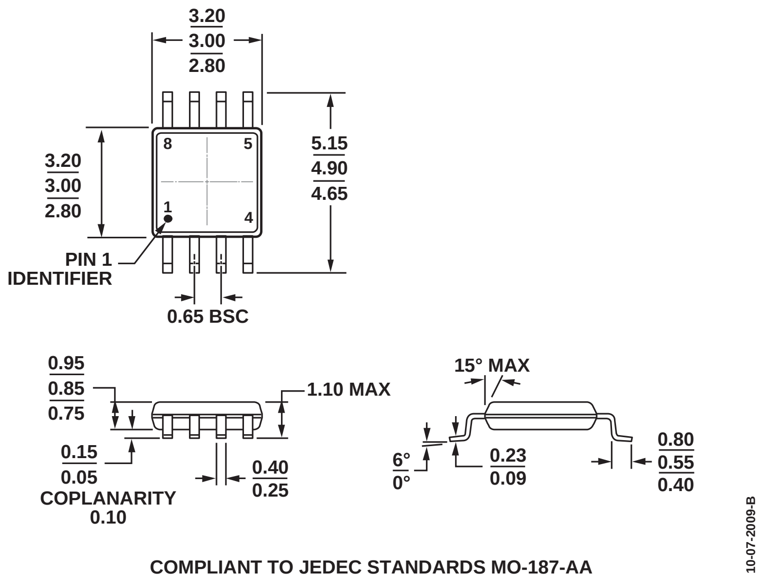


Figure 12. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

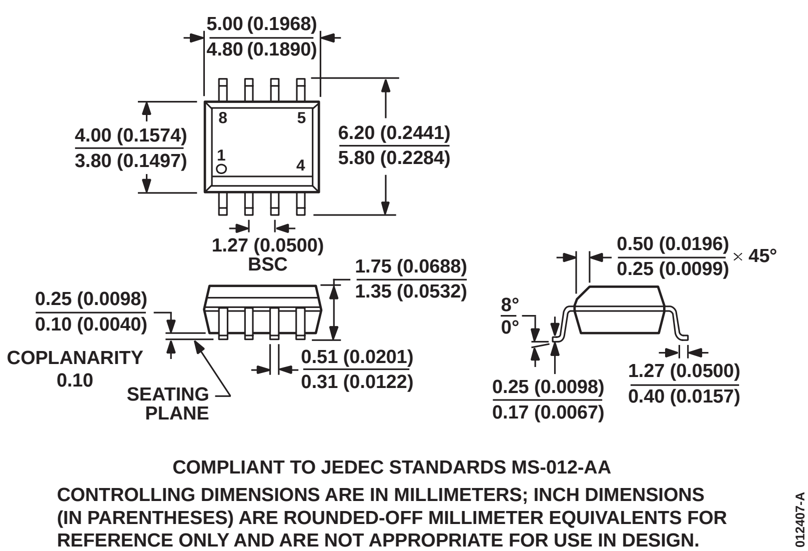


Figure 13. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

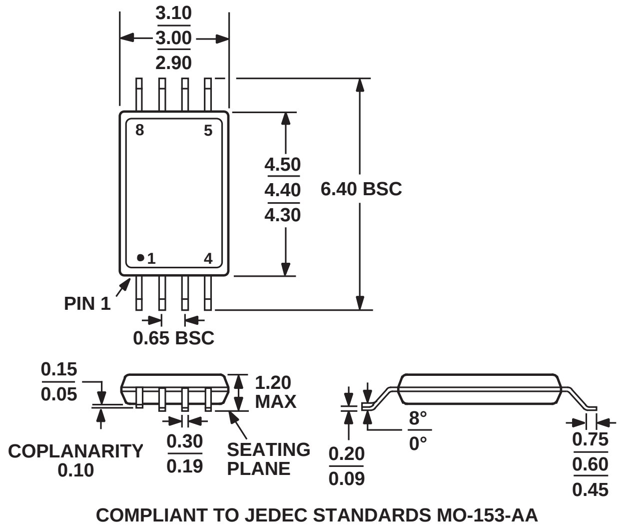


Figure 14. 8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)
Dimensions shown in millimeters

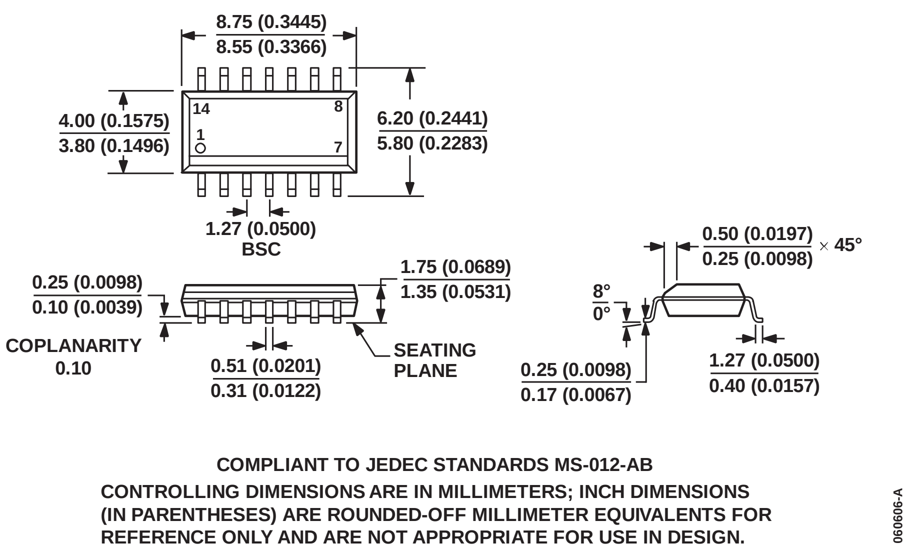


Figure 15. 14-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-14)
Dimensions shown in millimeters and (inches)

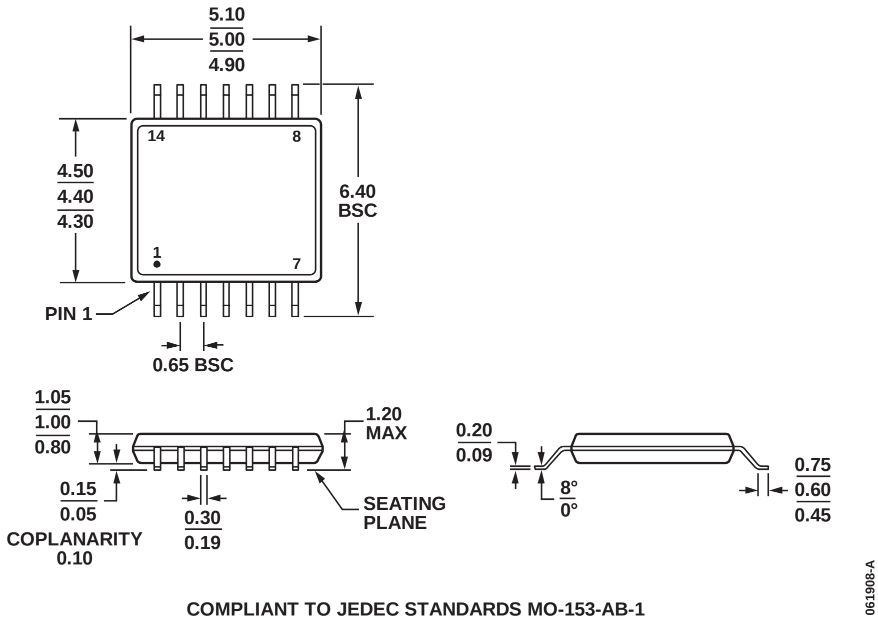


Figure 16. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
OP727AR	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP727AR-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP727AR-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP727ARUZ	–40°C to +85°C	8-Lead TSSOP	RU-8	
OP727ARUZ-REEL	–40°C to +85°C	8-Lead TSSOP	RU-8	
OP727ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP727ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP727ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP747ARU	–40°C to +85°C	14-Lead TSSOP	RU-14	
OP747ARU-REEL	–40°C to +85°C	14-Lead TSSOP	RU-14	
OP747ARUZ	–40°C to +85°C	14-Lead TSSOP	RU-14	
OP747ARUZ-REEL	–40°C to +85°C	14-Lead TSSOP	RU-14	
OP747ARZ	–40°C to +85°C	14-Lead SOIC	R-14	
OP747ARZ-REEL	–40°C to +85°C	14-Lead SOIC	R-14	
OP747ARZ-REEL7	–40°C to +85°C	14-Lead SOIC	R-14	
OP777ARMZ	–40°C to +85°C	8-Lead MSOP	RM-8	A1A
OP777ARMZ-REEL	–40°C to +85°C	8-Lead MSOP	RM-8	A1A
OP777ARZ	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP777ARZ-REEL	–40°C to +85°C	8-Lead SOIC_N	R-8	
OP777ARZ-REEL7	–40°C to +85°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

REVISION HISTORY

10/11—Rev. C to Rev. D

9/01—Rev. B to Rev. C

D02051-0-10/11(D)