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REVISION HISTORY

9/13—Rev. H to Rev. I

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Updated Outline Dimensions	14
Changes to Ordering Guide	16

9/10—Rev. G to Rev. H

Added WLCSP	Universal
Changes to Features Section.....	1
Changes to General Description Section	1
Added Figure 5; Renumbered Sequentially	1
Changes to Large-Signal Voltage Gain Parameter, Table 1	3
Changes to Table 2, Thermal Resistance Section, and Table 3 ...	4
Change to Figure 30	9
Added Figure 53.....	16
Changes to Ordering Guide	16

7/08—Rev. F to Rev. G

Changes to Phase Inversion Section	12
Deleted Figure 45.....	12
Added Figure 45 and Figure 46.....	12
Updated Outline Dimensions	14
Changes to Ordering Guide	16

10/04—Rev. E to Rev. F

Deleted 8-Lead PDIP	Universal
Added 8-Lead MSOP	Universal
Changes to Format and Layout.....	Universal
Changes to Features.....	1
Changes to Pin Configurations.....	1
Changes to General Description	1
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10/02—Rev. D to Rev. E

Edits to 8-Lead Epoxy DIP (P-Suffix) Pin.....	1
Edits to Ordering Guide	3
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9/02—Rev. C to Rev. D

Edits to 14-Lead SOIC (S-Suffix) Pin	1
Replaced 8-Lead SOIC (S-Suffix)	11

4/02—Rev. B to Rev. C

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Edits to Absolute Maximum Ratings	3
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20-Position Chip Carrier (RC Suffix) Deleted	11

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At $V_S = \pm 15.0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted; applies to both A and G grades.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP282 OP282 , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ OP482 OP482 , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.2	3	mV
					4.5	mV
				0.2	4	mV
					6	mV
Input Bias Current	I_B	$V_{CM} = 0\text{ V}$ $V_{CM} = 0\text{ V}^1$		3	100	pA
					500	pA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$ $V_{CM} = 0\text{ V}^1$		1	50	pA
					250	pA
Input Voltage Range			-11		+15	V
Common-Mode Rejection Ratio	CMRR	$-11\text{ V} \leq V_{CM} \leq +15\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	70	90		dB
Large-Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = \pm 13.5\text{ V}$ $R_L = 10\text{ k}\Omega$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	20			V/mV
			15			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			10		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$			8		$\text{pA}/^\circ\text{C}$
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 10\text{ k}\Omega$	13.5	13.9		V
Output Voltage Low	V_{OL}	$R_L = 10\text{ k}\Omega$		-13.9	-13.5	V
Short-Circuit Limit	I_{SC}	Source	3	10		mA
		Sink		-12	-8	mA
Open-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$		200		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 4.5\text{ V}$ to $\pm 18\text{ V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		25	316	$\mu\text{V}/\text{V}$
Supply Current/Amplifier	I_{SY}	$V_O = 0\text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		210	250	μA
Supply Voltage Range	V_S		± 4.5		± 18	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$	7	9		$\text{V}/\mu\text{s}$
Full-Power Bandwidth	BW_P	1% distortion		125		kHz
Settling Time	t_s	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			4		MHz
Phase Margin	ϕ_M			55		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		1.3		μV p-p
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		36		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n			0.01		$\text{pA}/\sqrt{\text{Hz}}$

¹ The input bias and offset currents are characterized at $T_A = T_J = 85^\circ\text{C}$. Bias and offset currents are guaranteed but not tested at -40°C .

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Input Voltage	$\pm 18\text{ V}$
Differential Input Voltage ¹	36 V
Output Short-Circuit Duration	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+85^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering 60 sec)	300°C

¹ For supply voltages less than $\pm 18\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device in socket for PDIP. θ_{JA} is specified for a device soldered in the circuit board for SOIC_N, MSOP, and WLCSP packages. This was measured using a standard 4-layer board.

Table 3.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP [RM]	142	45	$^{\circ}\text{C/W}$
8-Lead SOIC_N (S-Suffix) [R]	120	45	$^{\circ}\text{C/W}$
14-Lead PDIP (P-Suffix) [N]	83	39	$^{\circ}\text{C/W}$
14-Lead SOIC_N (S-Suffix) [R]	112	35	$^{\circ}\text{C/W}$
14-Ball WLCSP [CB] ^{1,2}	70	16	$^{\circ}\text{C/W}$

¹ Simulated thermal numbers per JESD51-9.

² Junction-to-board thermal resistance.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

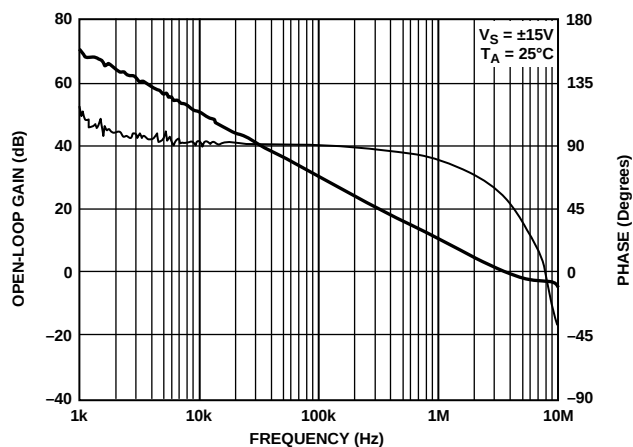


Figure 6. OP282 Open-Loop Gain and Phase vs. Frequency

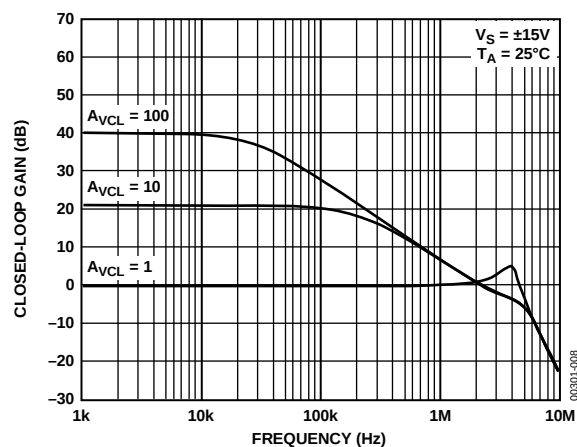


Figure 9. OP282 Closed-Loop Gain vs. Frequency

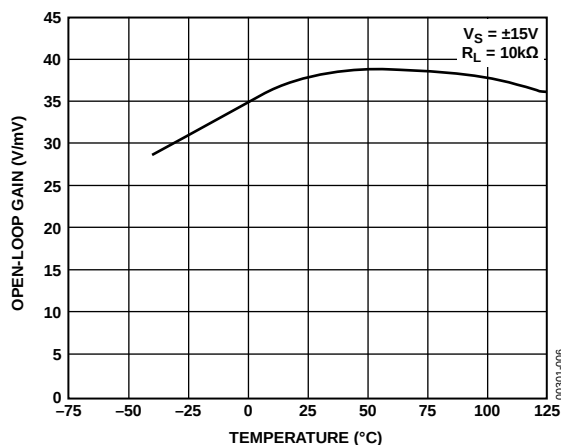


Figure 7. OP282 Open-Loop Gain vs. Temperature

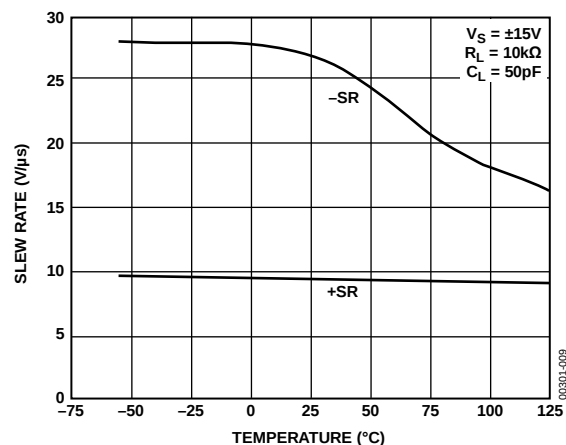


Figure 10. OP282 Slew Rate vs. Temperature

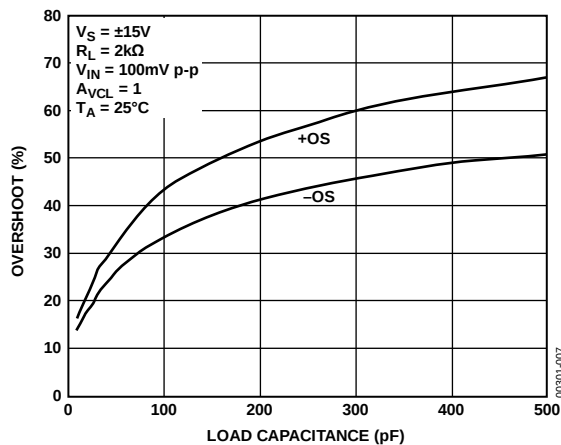


Figure 8. OP282 Small-Signal Overshoot vs. Load Capacitance

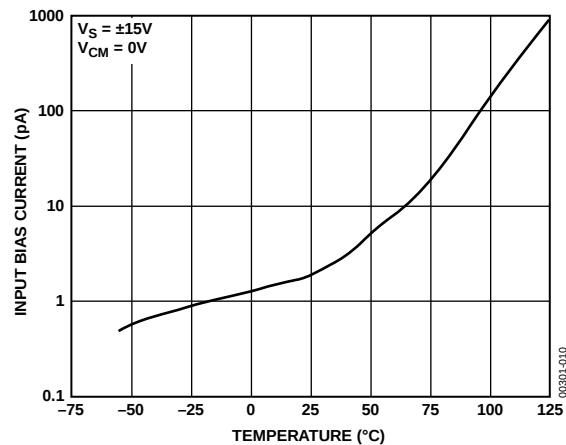


Figure 11. OP282 Input Bias Current vs. Temperature

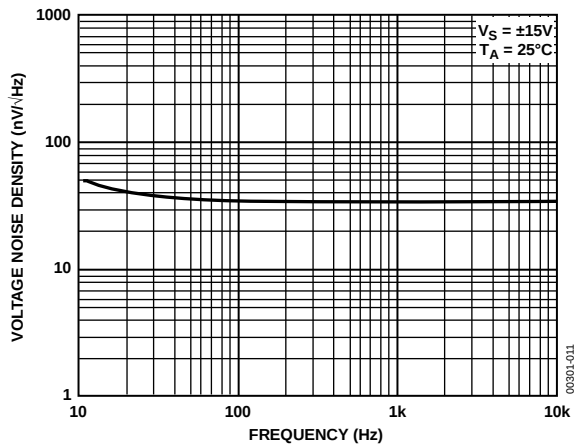


Figure 12. OP282 Voltage Noise Density vs. Frequency

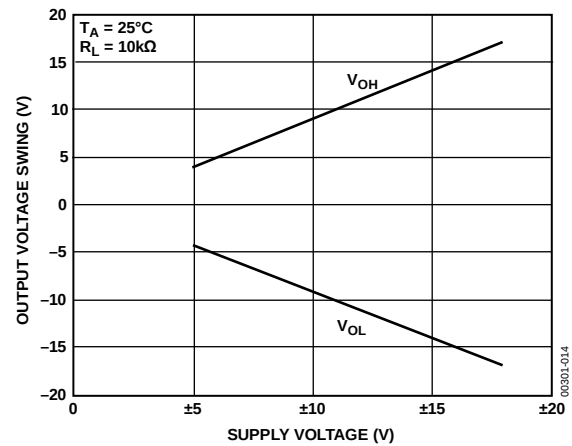


Figure 15. OP282 Output Voltage Swing vs. Supply Voltage

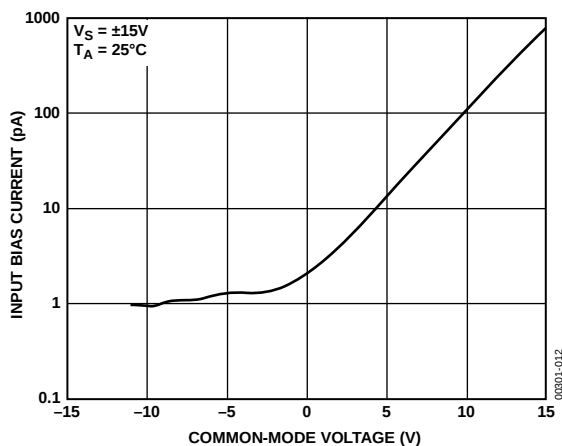


Figure 13. OP282 Input Bias Current vs. Common-Mode Voltage

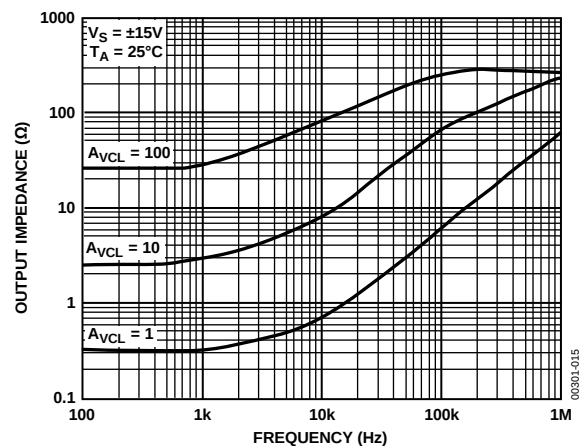


Figure 16. OP282 Closed-Loop Output Impedance vs. Frequency

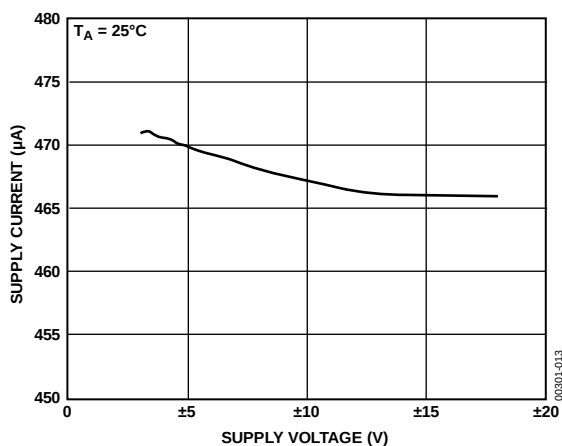


Figure 14. OP282 Supply Current vs. Supply Voltage

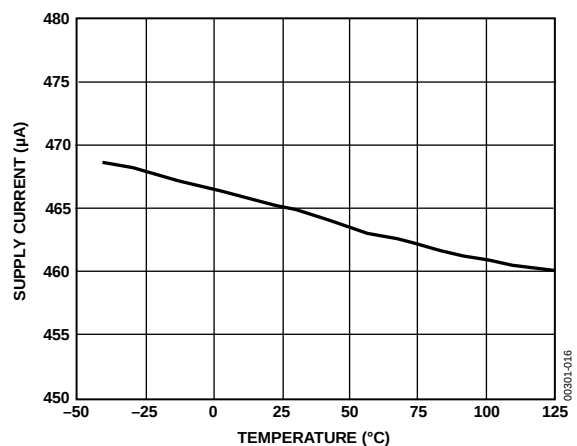


Figure 17. OP282 Supply Current vs. Temperature

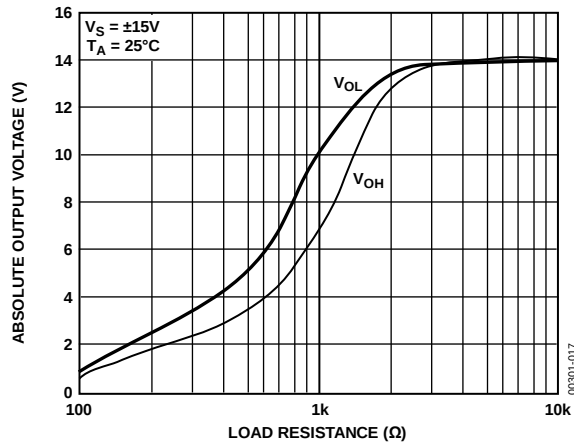


Figure 18. OP282 Absolute Output Voltage vs. Load Resistance

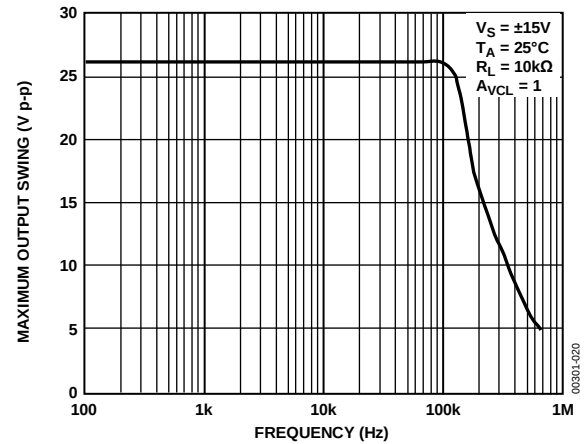


Figure 21. OP282 Maximum Output Swing vs. Frequency

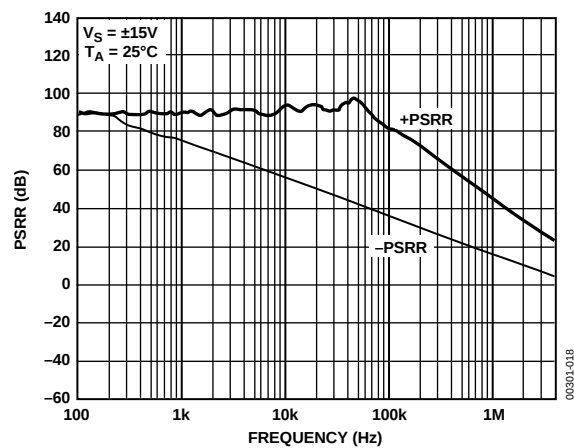


Figure 19. OP282 PSRR vs. Frequency

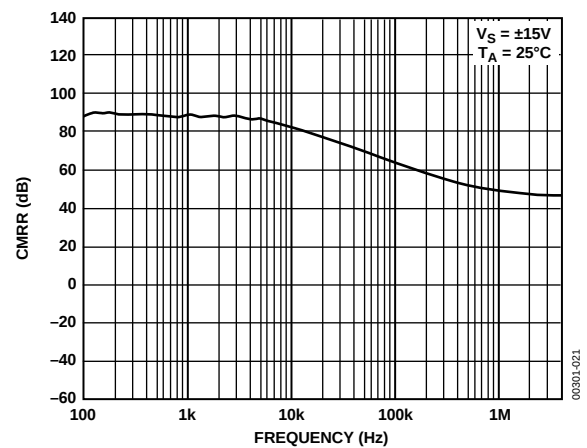


Figure 22. OP282 CMRR vs. Frequency

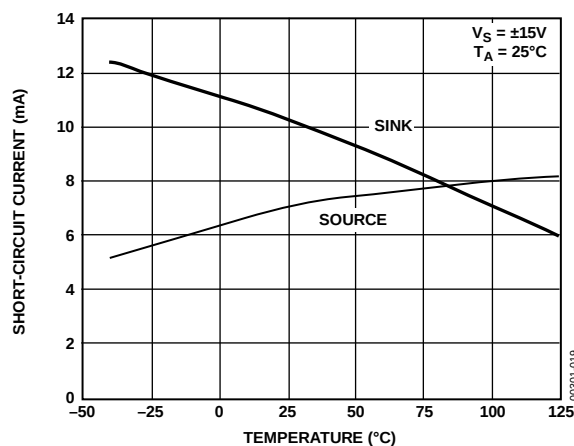


Figure 20. OP282 Short-Circuit Current vs. Temperature

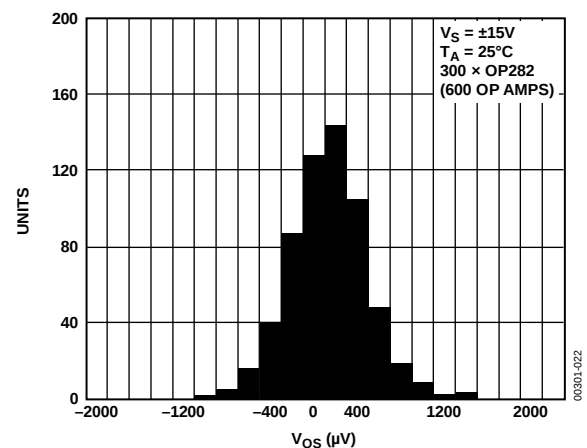


Figure 23. OP282 VOS Distribution, SOIC_N Package

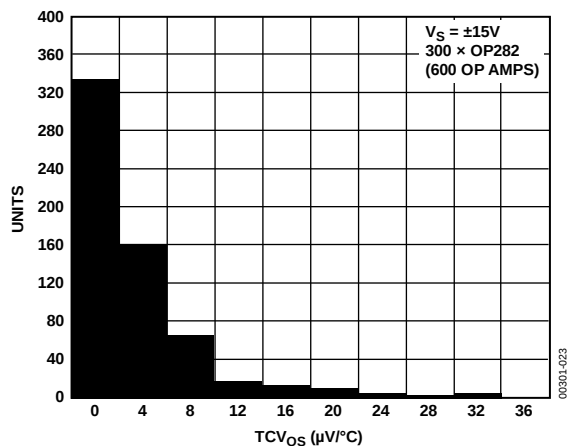


Figure 24. OP282 TCVOS Distribution, SOIC_N Package

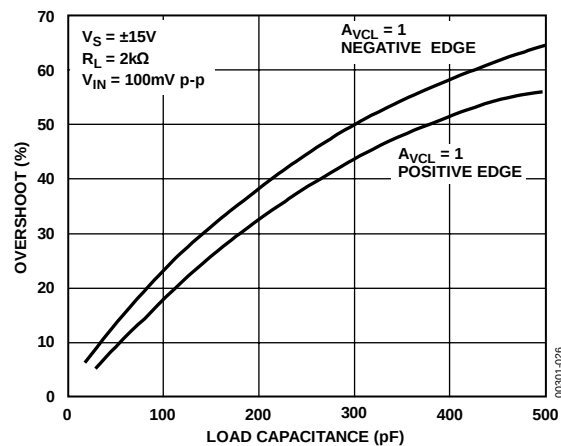


Figure 27. OP482 Small-Signal Overshoot vs. Load Capacitance

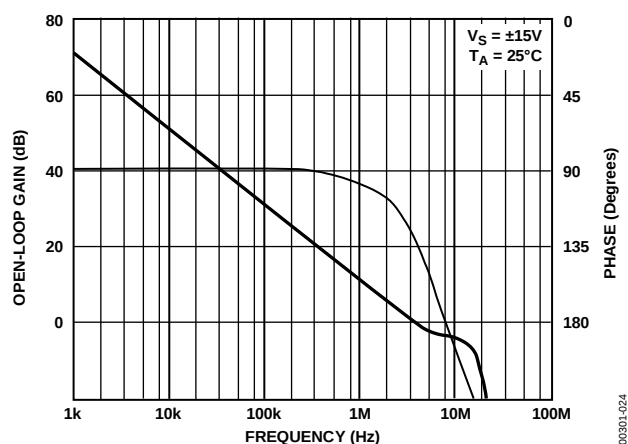


Figure 25. OP482 Open-Loop Gain and Phase vs. Frequency

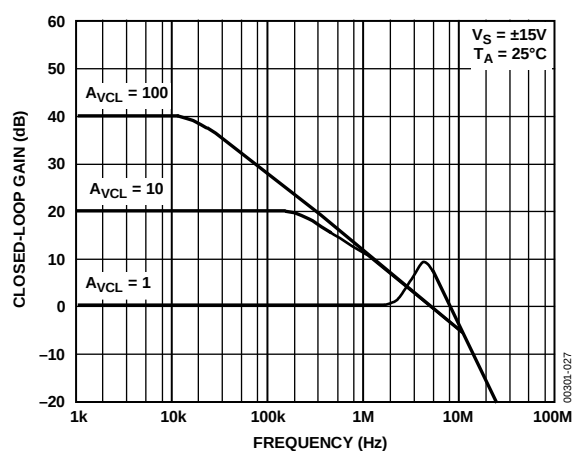


Figure 28. OP482 Closed-Loop Gain vs. Frequency

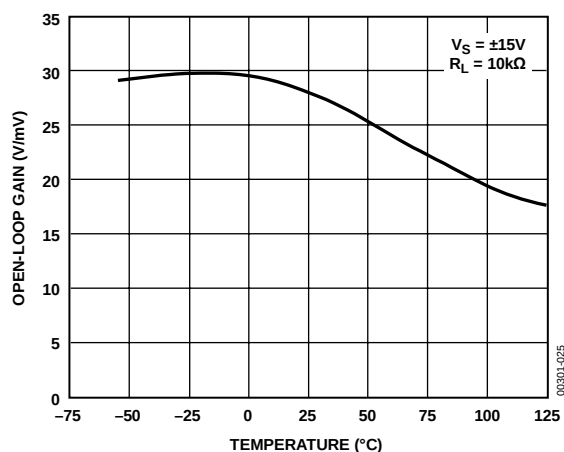


Figure 26. OP482 Open-Loop Gain vs. Temperature

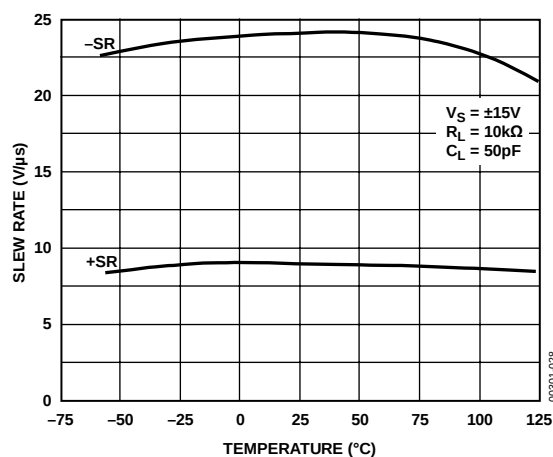


Figure 29. OP482 Slew Rate vs. Temperature

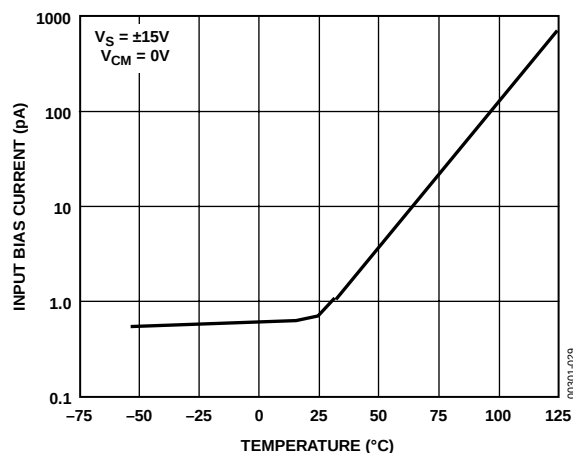


Figure 30. OP482 Input Bias Current vs. Temperature

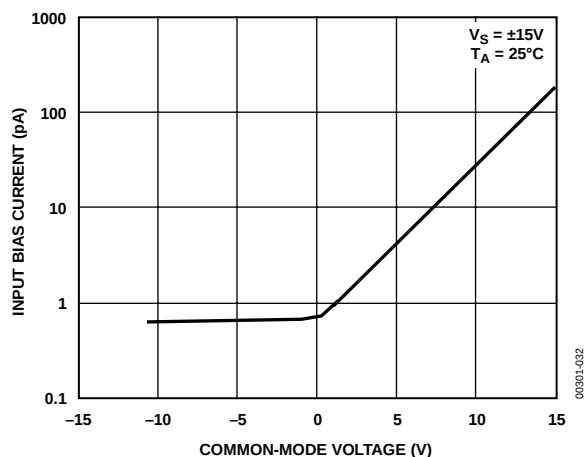


Figure 33. OP482 Input Bias Current vs. Common-Mode Voltage

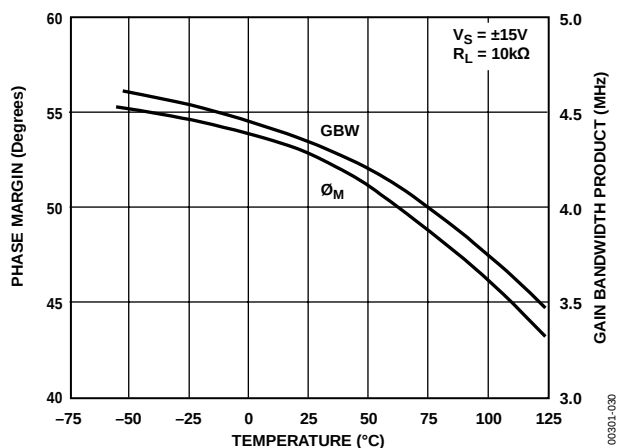


Figure 31. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature

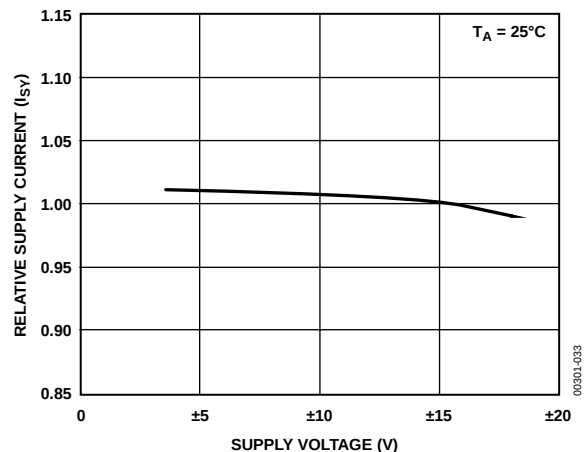


Figure 34. OP482 Relative Supply Current vs. Supply Voltage

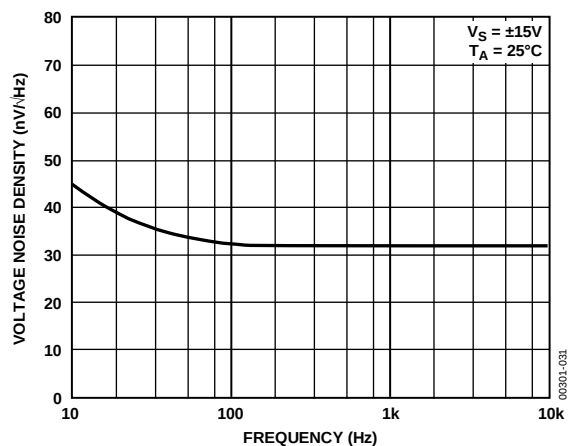


Figure 32. OP482 Voltage Noise Density vs. Frequency

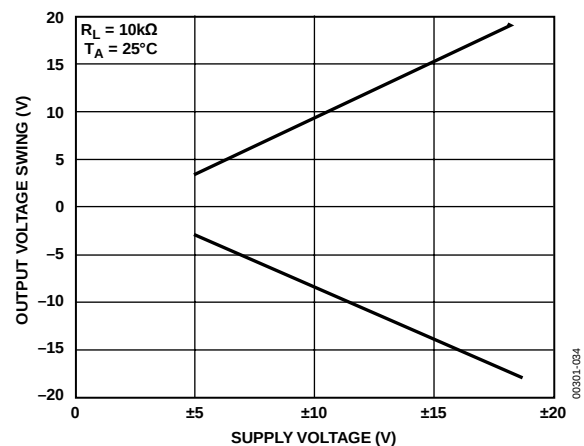


Figure 35. OP482 Output Voltage Swing vs. Supply Voltage

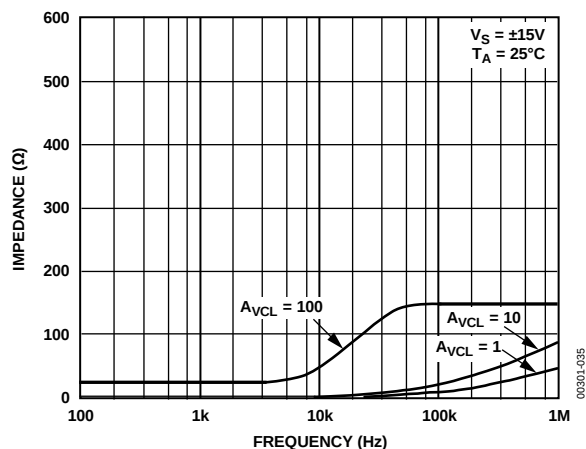


Figure 36. OP482 Closed-Loop Output Impedance vs. Frequency

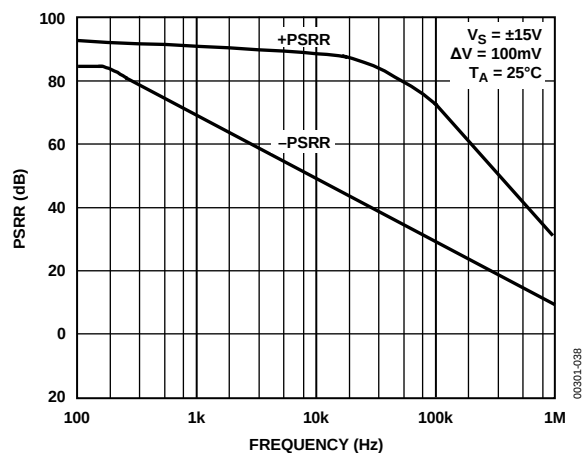


Figure 39. OP482 Power Supply Rejection Ratio (PSRR) vs. Frequency

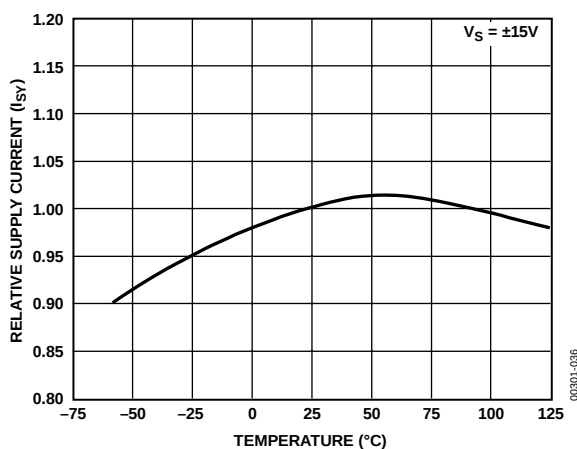


Figure 37. OP482 Relative Supply Current vs. Temperature

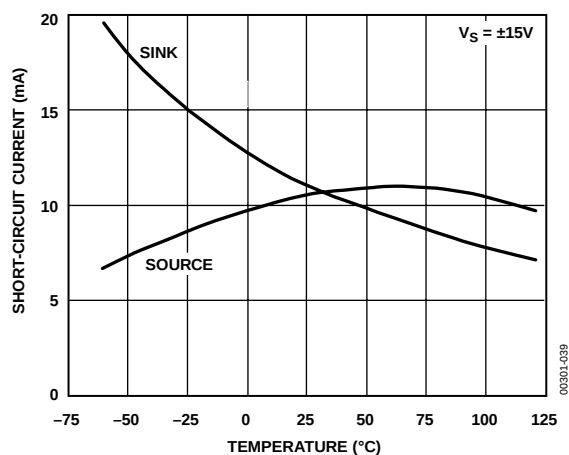


Figure 40. OP482 Short-Circuit Current vs. Temperature

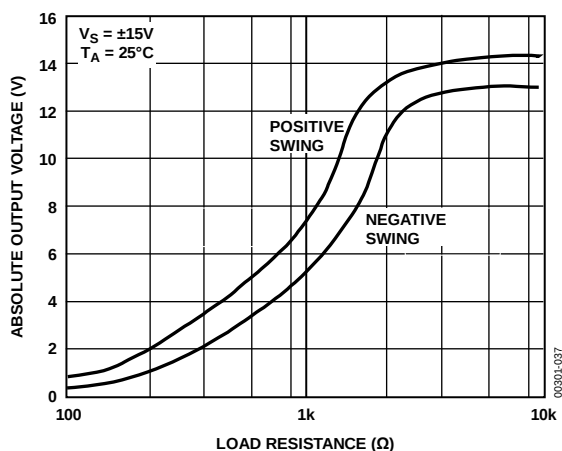


Figure 38. OP482 Maximum Output Voltage vs. Load Resistance

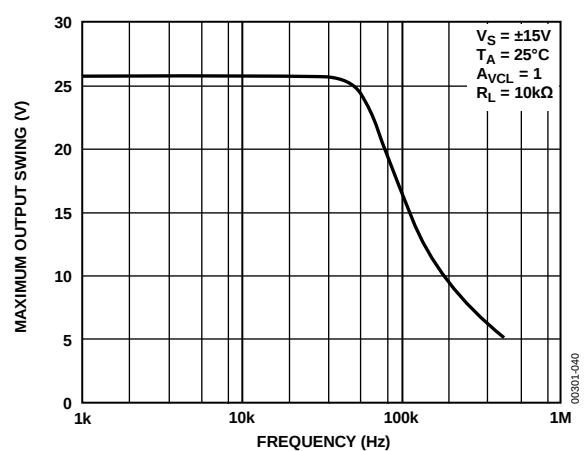


Figure 41. OP482 Maximum Output Swing vs. Frequency

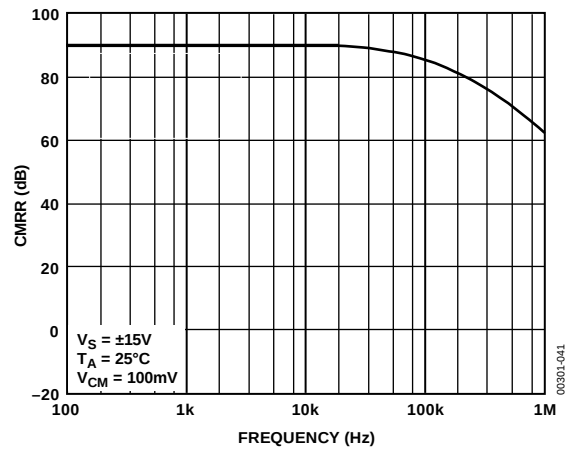
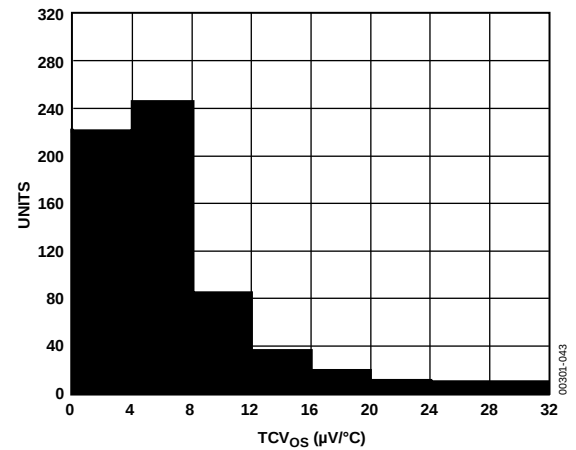
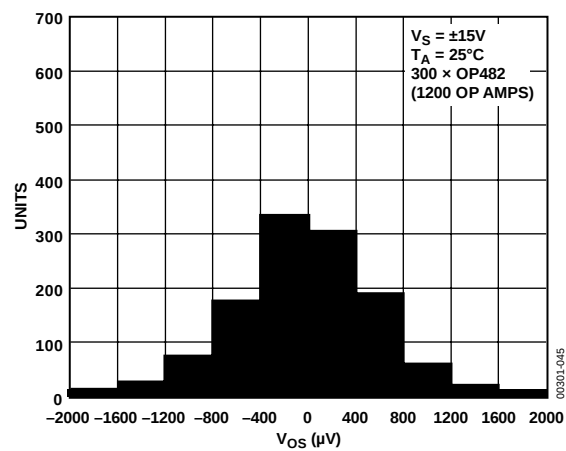


Figure 42. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

Figure 44. OP482 TCV_{OS} Distribution, PDIP PackageFigure 43. OP482 V_{OS} Distribution, PDIP Package

APPLICATIONS INFORMATION

The OP282 and OP482 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. OP282 and OP482 were tested and are guaranteed over a common-mode range ($-11\text{ V} \leq V_{CM} \leq +15\text{ V}$) that includes the positive supply.

One application where such sensing is commonly used is in the sensing of power supply currents. Therefore, the OP282/OP482 can be used in current sensing applications, such as the partial circuit shown in Figure 45. In this circuit, the voltage drop across a low value resistor, such as the $0.1\text{ }\Omega$ shown here, is amplified and compared to 7.5 V . The output can then be used for current limiting.

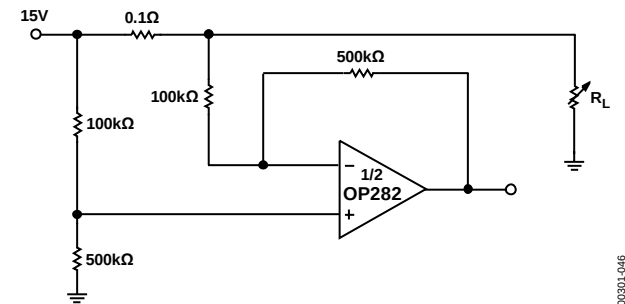


Figure 45. High-Side Signal Conditioning

PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282/OP482, a negative signal in excess of 11 V causes phase inversion. This is caused by saturation of the input stage, leading to the forward-biasing of a gate-drain diode. Phase reversal in the OP282/OP482 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit shown in Figure 46, D1 protects the op

amp against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

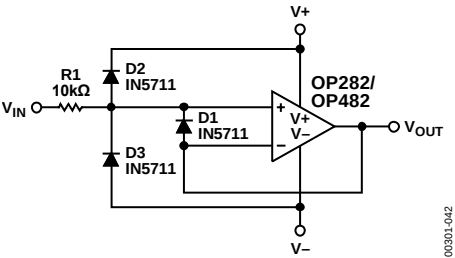


Figure 46. Phase Reversal Solution Circuit

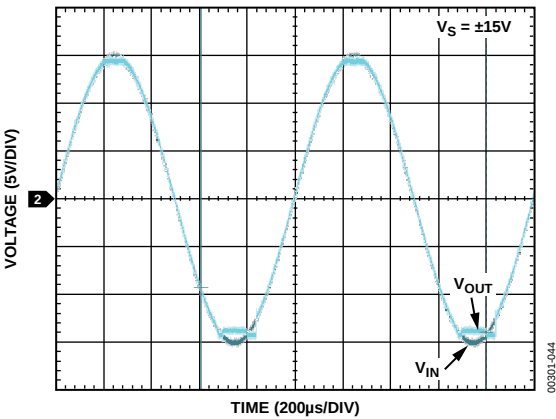


Figure 47. No Phase Reversal

ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282/OP482 make either one an excellent choice for many filter applications. There are many active filter configurations, but the four most popular configurations are Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

Table 4. Active Filter Configurations

Type	Selectivity	Overshoot	Phase	Amplitude (Pass Band)	Amplitude (Stop Band)
Butterworth	Moderate	Good	Nonlinear	Maximum flat	Equal ripple
Chebyshev	Good	Moderate		Equal ripple	
Elliptic	Best	Poor		Equal ripple	
Bessel (Thompson)	Poor	Best	Linear		

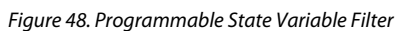
The circuit shown in Figure 48 can be used to accurately program the Q, the cutoff frequency (f_c), and the gain of a two-pole state variable filter. OP482 devices have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1.

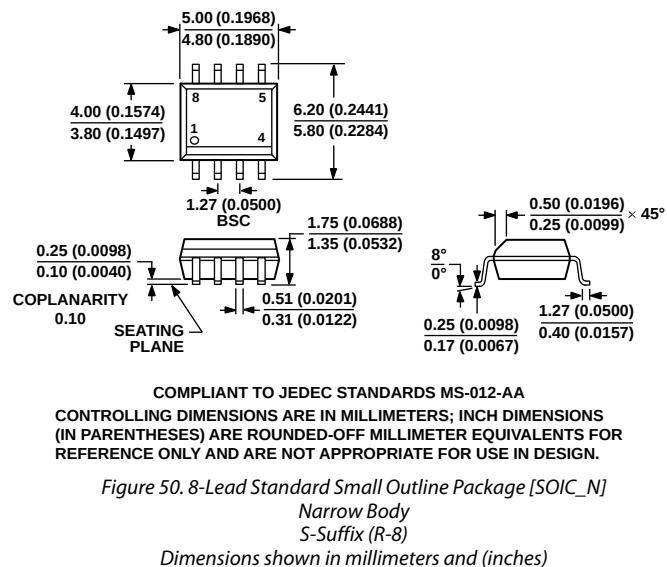
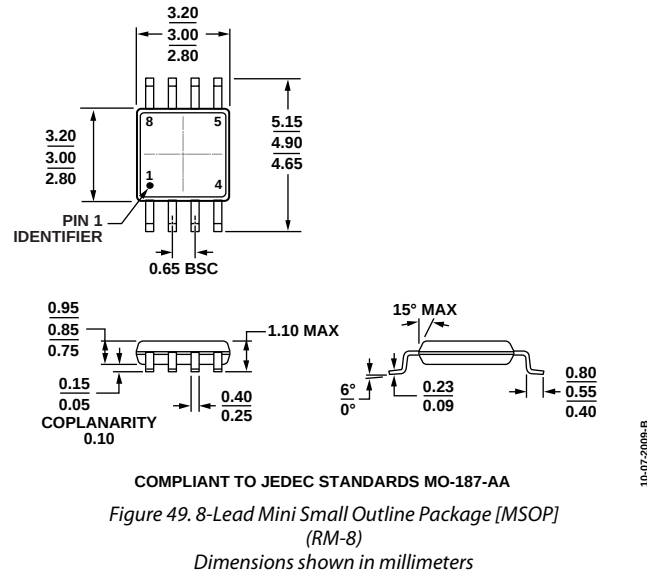
$$f_c = \frac{1}{2\pi R1C1} \left(\frac{D1}{256} \right)$$

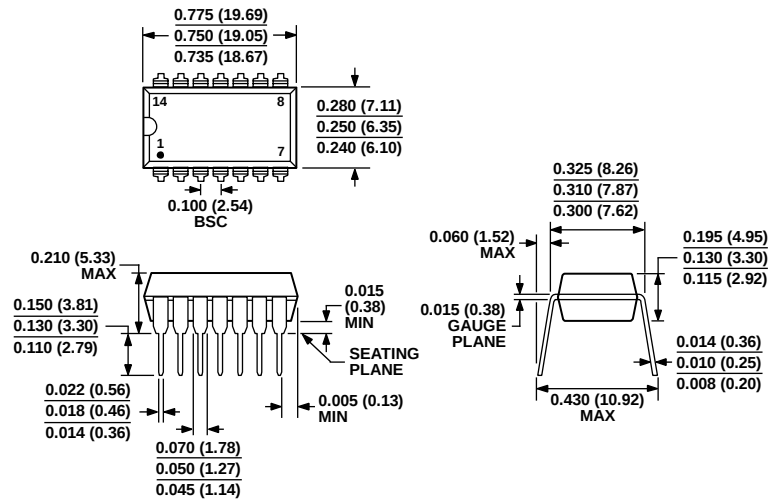
The gain of this circuit is set by adjusting D3. The gain equation is

$$Gain = \frac{R4}{R5} \left(\frac{D3}{256} \right)$$

$$Q = \frac{R2}{R3} \left(\frac{256}{D2} \right)$$


OUTLINE DIMENSIONS



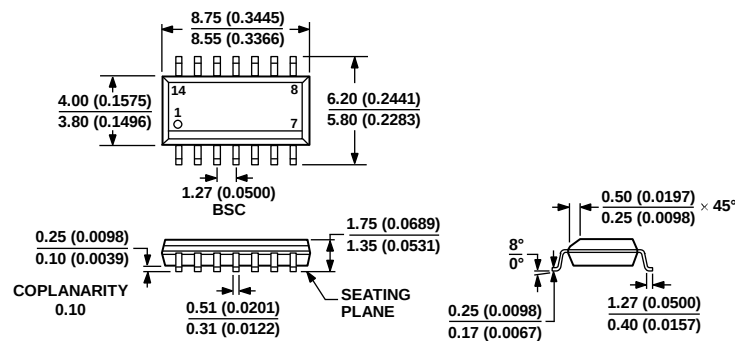


COMPLIANT TO JEDEC STANDARDS MS-001
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 51. 14-Lead Plastic Dual In-Line Package [PDIP]

P-Suffix (N-14)

Dimension shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-012-AB
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 52. 14-Lead Standard Small Outline Package [SOIC_N]

Narrow Body

S-Suffix (R-14)

Dimensions shown in millimeters and (inches)

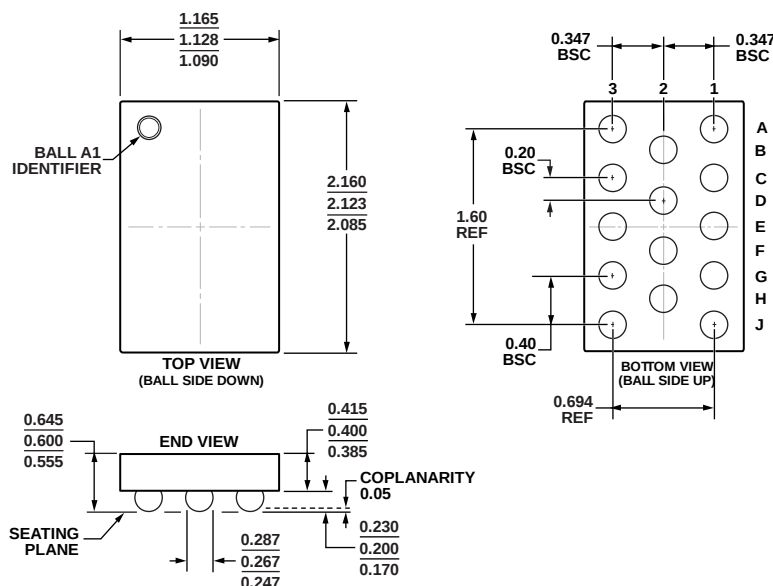


Figure 53. 14-Ball Wafer Level Chip Scale Package [WLCSP]
CB-14-2
Controlling dimensions are millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
OP282ARMZ	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282ARMZ-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	A0B
OP282GS	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GS-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP282GSZ-REEL7	−40°C to +85°C	8-Lead SOIC_N	S-Suffix (R-8)	
OP482ACBZ-RL	−40°C to +85°C	14-Ball WLCSP	CB-14-2	A2J
OP482ACBZ-R7	−40°C to +85°C	14-Ball WLCSP	CB-14-2	A2J
OP482GPZ	−40°C to +85°C	14-Lead PDIP	P-Suffix (N-14)	
OP482GS	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GS-REEL7	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	
OP482GSZ-REEL7	−40°C to +85°C	14-Lead SOIC_N	S-Suffix (R-14)	

¹ Z = RoHS Compliant Part.