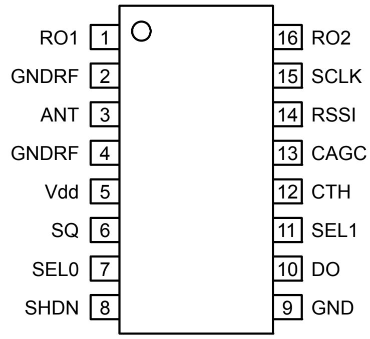
Pin Configuration



MICRF219AYQS

Pin Description

16-Pin QSOP	Pin Name	Pin Function
1	RO1	Reference Oscillator Input: Reference resonator input connection to pierce oscillator stage. May also be driven by external reference signal of 200mVp-p to 1.5V p-p amplitude maximum. Internal capacitance of 7pF to GND during normal operation.
2	GNDRF	Negative supply connection associated with ANT RF input.
3	ANT	Antenna Input: RF signal input from antenna. Internally AC coupled. It is recommended a matching network with an inductor-to-RF ground be used to improve ESD protection.
4	GNDRF	Ground connection for ANT RF input.
5	VDD	Positive supply connection for all chip functions. Bypass with 0.1µF capacitor located as close to the VDD pin as possible.
6	SQ	Squelch Control Logic-Level Input. An internal pull-up pulls the logic-input HIGH when the device is enabled. Bit D17 sets whether squelch is enabled or disabled when a logic-level signal is applied the SQ pin. See Squelch Enable Truth-Table on page
7	SEL0	Demodulator Filter Bandwidth Select Logic-Level Input. Internal pull-up (3uA typical) when not in shutdown or SLEEP mode. Used in conjunction with SEL1 to control D3 bandwidth LSB when serial interface contains default setting. It does not need to be defined in SLEEP mode.
8	SHDN	Shutdown control Logic-Level Input. A logic-level LOW enables the device. A logic-level HIGH places the device in low-power shutdown mode. An internal pull-up pulls the logic input HIGH.
9	GND	Negative supply connection for all chip functions except for RF input.
10	DO	Data Input and Output. Demodulated data output. May be blanked until bit checking test is acceptable. A current limited CMOS output during normal operation this pin is also used as a CMOS Schmitt input for serial interface data. A 25kΩ pull-down is present when device is in shutdown and sleep modes.
11	SEL1	Demodulator Filter Bandwidth Select Logic-Level Input: Internal (3uA typical) pull-up when not in shutdown or SLEEP mode. Used in conjunction with SEL0, to control D4 bandwidth MSB, when serial interface contains default setting. It does not need to be defined in SLEEP mode.
12	CTH	Demodulation threshold voltage integration capacitor. Capacitor-to-GND sets the settling time for the demodulation data slicing level. Values above 1nF are recommended and should be optimized for data rate and data profile.
13	CAGC	AGC filter capacitor. A capacitor, normally greater than 0.47µF, is connected from this pin-to-GND
14	RSSI	Received signal strength indication (output): Output is from a switched capacitor integrating op amp with 220Ω typical output impedance.
15	SCLK	Serial interface input clock. CMOS Schmitt input. A 25kΩ pull-down is present when device is in shutdown mode.
16	RO2	Reference resonator connection. Internal capacitance of 7pF to GND during normal operation.

Absolute Maximum Ratings[1]

Supply Voltage (VDD) .... +5V
Input Voltage. .... +5V
Junction Temperature .... +150ºC
Lead Temperature (soldering, 10sec.) .... 300°C
Storage Temperature (Ts) .... -65ºC to +150°C
Maximum Receiver Input Power .... +10dBm
EDS Rating[3] .... 2KV HBM

Operating Ratings[2]

Supply voltage (VDD) .... +3.0V to +3.6V
Ambient Temperature (T_A) .... –40°C to +105°C
Input Voltage (Vin) 3.6V
Maximum Input RF Power .... –20dBm
Receive Modulation Duty Cycle[6] .... 20~80%
Frequency Range .... 300MHz to 450MHz

Electrical Characteristics

Specifications apply for V_{DD} = 3.3V, GND = 0V, C_{AGC} = 4.7µF, C_{TH} = 0.1µF, f_{RX} = 433.92 MHz unless otherwise noted. **Bold** values indicate –40°C – T_A – 105°C. 1kbps data rate (Manchester encoded), reference oscillator frequency = 13.52127MHz.

Parameter	Condition	Min.	Typ.	Max.	Units
Operating Supply Current	Continuous Operation, f_{RX} = 315MHz		4.0		mA
	Continuous Operation, f_{RX} = 433.92MHz		6.0		
Shutdown Current			0.15		µA
Receiver					
Image Rejection			25		dB
1st IF Center Frequency	f_{RX} = 315MHz		0.86		MHz
	f_{RX} = 433.92MHz		1.2		
Receiver Sensitivity @ 1kbps (Note 4)	f_{RX} = 315 MHz, 50Ω BER=10^{-2}		–110		dBm
	f_{RX} = 433.92MHz, 50Ω BER=10^{-2}		–110		
IF Bandwidth	f_{RX} = 315MHz		235		kHz
	f_{RX} = 433.92MHz		330		
Antenna Input Impedance	f_{RX} = 315MHz		32 – j235		Ω
	f_{RX} = 433.92MHz		19 – j174		
Receive Modulation Duty Cycle	Note 5	20		80	%
AGC Attack / Decay Ratio	t_{ATTACK} / t_{DECAY}		0.1		
AGC Pin Leakage Current	T_A = 25ºC		±30		nA
	T_A = +105ºC		±800		nA
AGC Dynamic Range	RF_{IN} @ –40dBm		1.15		V
	RF_{IN} @ –100dBm		1.70		V
Reference Oscillator					
Reference Oscillator Frequency	f_{RX} = 315 MHz, Crystal Load Cap = 10pF		9.81563		MHz
	f_{RX} = 433.92 MHz, Crystal Load Cap = 10pF		13.52127		
Reference Oscillator Input Impedance	RO1		1.6		kΩ
Reference Oscillator Bias Voltage	RO2		1.15		V

Electrical Characteristics (Continued)

Specifications apply for V_{DD} = 3.3V, GND = 0V, C_{AGC} = 4.7µF, C_{TH} = 0.1µF, f_{RX} = 433.92 MHz unless otherwise noted. Bold values indicate –40°C – T_A – 105°C. 1kbps data rate (Manchester encoded), reference oscillator frequency = 13.52127MHz.

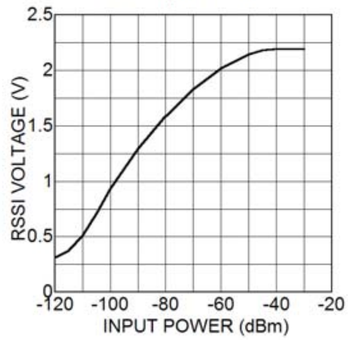
Parameter	Condition	Min.	Typ.	Max.	Units
Reference Oscillator Input Range		0.2		1.5	V_{P-P}
Reference Oscillator Source Current	V(REFOSC) = 0V		300		µA
Demodulator					
CTH Source Impedance	F_{REFOSC} = 9.81563 MHz		165		kΩ
	F_{REFOSC} = 13.52127MHz		120		
CTH Leakage Current	T_A = 25ºC T_A = +105ºC		±2 ±800		nA
Demodulator Filter Bandwidth @ 315MHz	Programmable, see application section	1170		9400	Hz
Demodulator Filter Bandwidth @ 434MHz	Programmable, see application section	1625		13000	Hz
Digital / Control Functions					
DO Pin Output Current	As output source @ 0.8 V_{DD} sink @ 0.2 V_{DD}		260 600		µA
Output Rise And Fall Times	Cl = 15pF, pin DO, 10-90%		2		µsec
Input High Voltage	Pins SCLK, DO (As input), SHDN,SEL0, SEL1,SQ	0.8V_{DD}			V
Input Low Voltage	Pins SCLK, DO (As input), SHDN, SEL0, SEL1,SQ			0.2V_{DD}	V
Output Voltage High	DO	0.8V_{DD}			V
Output Voltage Low	DO			0.2V_{DD}	V
RSSI					
RSSI DC Output Voltage Range	–100dBm		0.4		V
	–40dBm		2.0		
RSSI Response Slope	–110dBm to -40dBm		25		mV/dB
RSSI Output Current			400		µA
RSSI Output Impedance			250		Ω
RSSI Response Time	50% data duty cycle, input power to Antenna = -20dBm		0.3		sec

Notes:

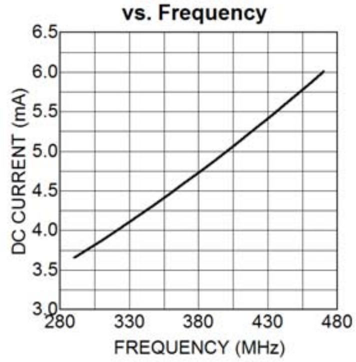
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside of its operating rating.
3. Device is ESD sensitive. Use appropriate ESD precautions. Exceeding the absolute maximum rating may damage the device.
4. Sensitivity is defined as the average signal level measured at the input necessary to achieve 10^{-2} BER (bit error rate). The input signal is defined as a return-to-zero (RZ) waveform with 50% average duty cycle (Manchester encoded) at a data rate of 1kbps.
5. When data burst does not contain preamble, duty cycle is defined as total duty cycle, including any "quiet" time between data bursts. When data bursts contain preamble sufficient to charge the slice level on capacitor C_{TH}, then duty cycle is the effective duty cycle of the burst alone. [For example, 100msec burst with 50% duty cycle, and 100msec "quiet" time between bursts. If burst includes preamble, duty cycle is $T_{ON}/(T_{ON}+t_{OFF})$= 50%; without preamble, duty cycle is $T_{ON}/(T_{ON}+ T_{OFF} + T_{QUIET})$ = 50msec/(200msec)=25%. T_{ON} is the (Average number of 1's/burst) × bit time, and T_{OFF} = ($T_{BURST} – T_{ON}$.)

Typical Characteristics

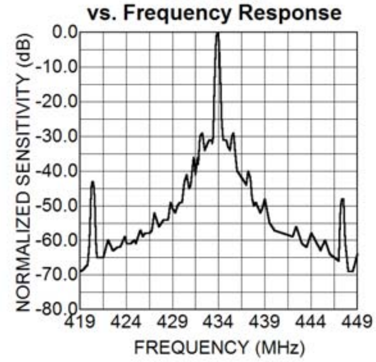
RSSI Voltage vs. Input Power



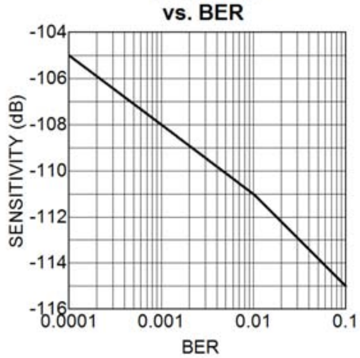
DC Current vs. Frequency



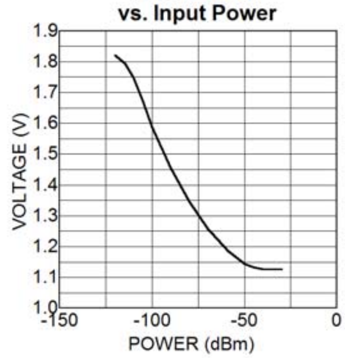
Selectivity vs. Frequency Response



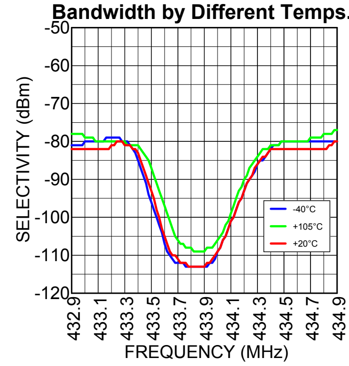
Sensitivity vs. BER



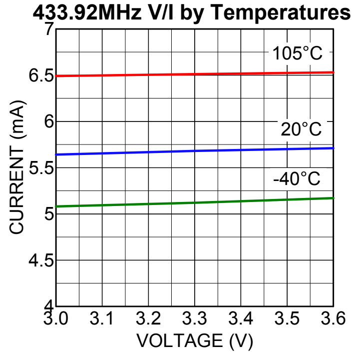
AGC Voltage vs. Input Power



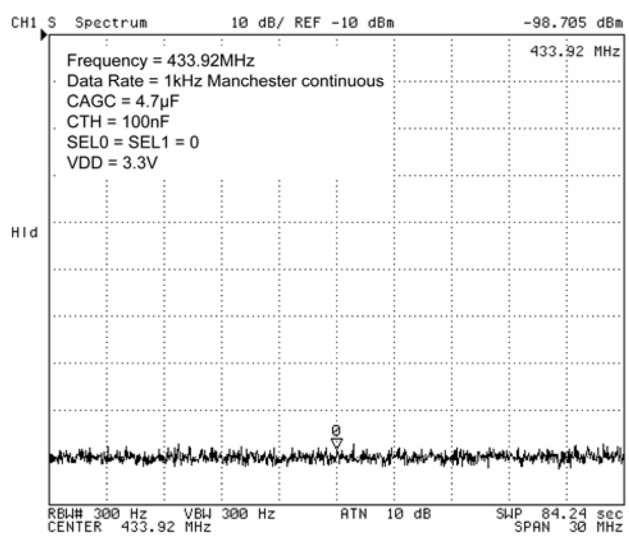
433MHz Selectivity and Bandwidth by Different Temps.



433.92MHz V/I by Temperatures



LO Leakage in RF Port



Functional Diagram

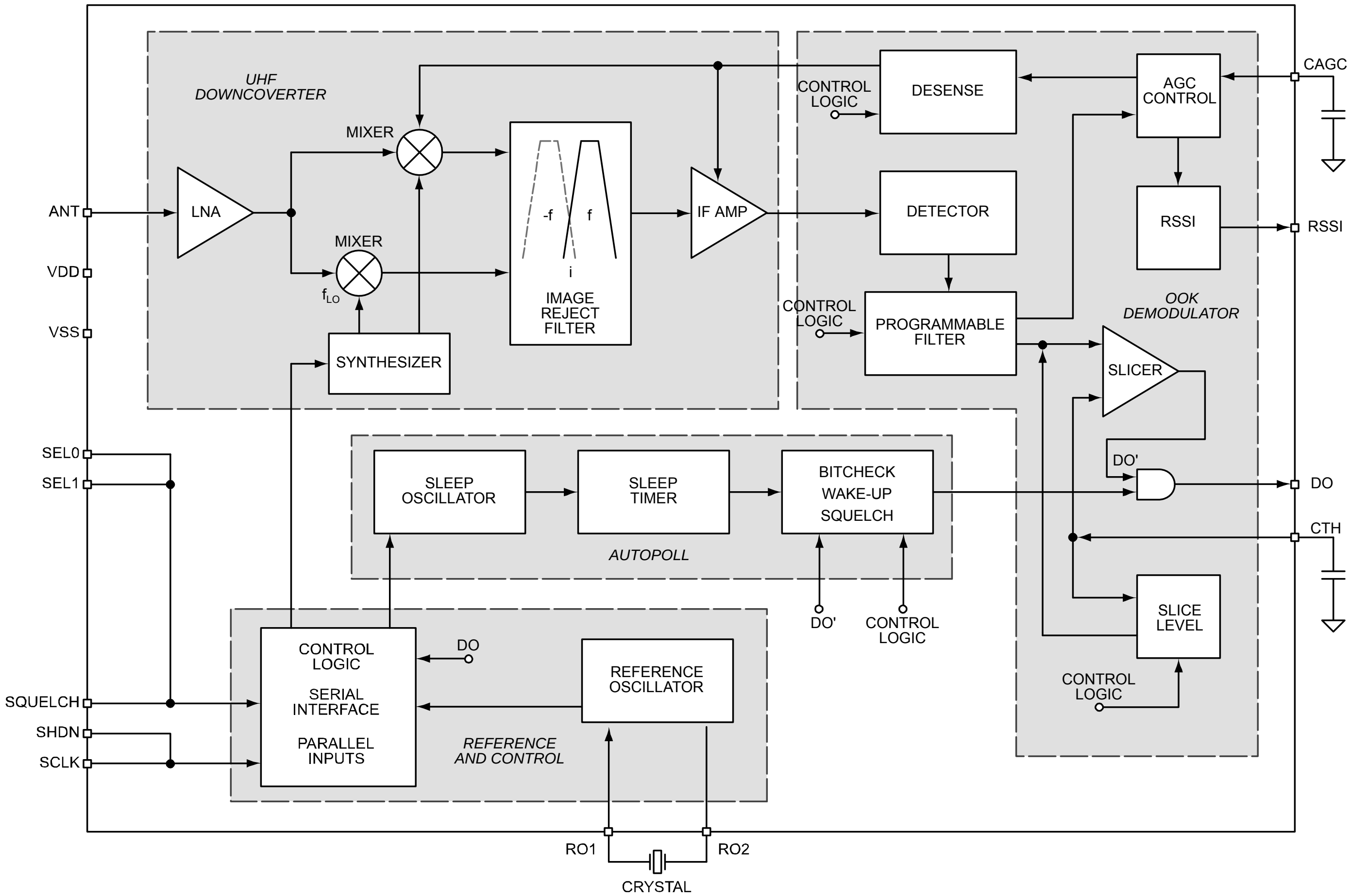


Figure 1. Simplified Block Diagram

Functional Description

The simplified block diagram, shown in Figure 1, illustrates the basic structure of the MICRF219 receiver. It is made up of four sub-blocks:

- UHF Down-converter
- OOK Demodulator
- Reference and Control logic
- Auto-poll circuitry

Outside the device, the MICRF219 receiver requires just three components to operate: two capacitors (CTH, and CAGC) and the reference frequency device (usually a quartz crystal). An additional five components are used to improve performance; a power supply decoupling capacitor, two components for the matching network, and two components for the pre-selector band-pass filter.

Receiver Operation

UHF Downconverter

The UHF down-converter has six components: LNA, mixers, synthesizer, image reject filter, band pass filter and IF amp.

LNA

The RF input signal is AC-coupled into the gate circuit of the grounded source LNA input stage. The LNA is a Cascoded NMOS amplifier. The amplified RF signal is then fed to the RF ports of two double balanced mixers.

Mixers and Synthesizer

The LO ports of the Mixers are driven by quadrature local oscillator outputs from the synthesizer block. The local oscillator signal from the synthesizer is placed on the low side of the desired RF signal to allow suppression of the image frequency at twice the IF frequency below the wanted signal. The local oscillator is set to 32 times the crystal reference frequency via a phase-locked loop synthesizer with a fully integrated loop filter.

Image-Reject Filter and Band-Pass Filter

The IF ports of the mixer produce quadrature-down converted IF signals. These IF signals are low-pass filtered to remove higher frequency products prior to the image reject filter where they are combined to reject the image frequencies. The IF signal then passes through a third order band pass filter. The IF center frequency is 1.2MHz. The IF BW is 330kHz @ 433.92MHz. This varies with RF operating frequency.

The IF BW can be calculated via direct scaling:

$$BW_{IF} = BW_{IF@433.92\ MHz} \times \left(\frac{\text{Operating Freq (MHz)}}{433.92}\right)$$

These filters are fully integrated inside the MICRF219.

After filtering, four active gain controlled amplifier stages enhance the IF signal to its proper level for demodulation.

OOK Demodulator

The demodulator section is comprised of detector, programmable low pass filter, slicer, and AGC comparator.

Detector and Programmable Low-Pass Filter

The demodulation starts with the detector removing the carrier from the IF signal. Post detection, the signal becomes base band information. The programmable low-pass filter further enhances the baseband information. There are four programmable low-pass filter BW settings: 1625Hz, 3250Hz, 6500Hz, 13000Hz for 433.92MHz operation. Low pass filter BW will vary with RF Operating Frequency. Filter BW values can be easily calculated by direct scaling. See equation below for filter BW calculation:

$$BW_{\text{Operating Freq}} = BW_{@433.92MHz} * \left(\frac{\text{Operating Freq (MHz)}}{433.92}\right)$$

It is very important to choose filter setting that fits best the intended data rate to minimize data distortion.

Demod BW is set at 13000Hz @ 433.92MHz as default (assuming both SEL0 and SEL1 pins are floating). The low pass filter can be hardware set by external pins SEL0 and SEL1.

SEL0	SEL1	Demod BW (@ 434MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

Table 1. Demodulation BW Selection

Slicer and Slicing Level

The signal, prior to the slicer, is still AM. The data slicer converts the AM signal into ones and zeros based on the threshold voltage built up in the CTH capacitor. After the slicer, the signal is ASK or OOK digital data.

The slicing threshold is default at 50%. The slicing threshold can be set via serial programming through register D5 and D6.

D5	D6	Slicing Level
1	0	Slice Level 30%
0	1	Slice Level 40%
1	1	Slice Level 50% - default
0	0	Slice Level 60%

AGC Comparator

The AGC comparator monitors the signal amplitude from the output of the programmable low-pass filter. When the output signal is less than 750mV thresh-hold, 1.5µA current is sourced into the external CAGC capacitor. When the output signal is greater than 750mV, a 15µA current sink discharges the CAGC capacitor. The voltage developed on the CAGC capacitor acts to adjust the gain of the mixer and the IF amplifier to compensate for RF input signal level variation.

Desense

Desense is a function designed to reduce the sensitivity of the MICRF219 receiver to a maximum of 45dB for training the MICRF219 receiver. This is done in order to recognize an intended transmitter. Very often, a receiver needs to learn how to recognize a particular transmitter. It is important for the receiver not to learn the signal of a stray transmitter near by. The simplest solution is to turn down the receiver gain, so the receiver only recognizes the transmitter at close range.

The de-sense function is accessible only through serial programming.

D0	D1	D2	MODE: Desense
0	X	X	No Desense - default
1	0	0	6dB Desense
1	1	0	16dB Desense
1	0	1	30dB Desense
1	1	1	42dB Desense

Reference Control

There are 2 components in Reference and Control sub-block: 1) Reference Oscillator and 2) Control Logic through parallel Inputs: SEL0, SEL1, SHDN

Reference Oscillator

The reference oscillator in the MICRF219 (Figure 2) uses a basic Pierce crystal oscillator configuration with MOS transconductor to provide negative resistance. Though the MICRF219 has build-in load capacitors for the crystal oscillator, the external load capacitors are still required for tuning it to the right frequency. R01 and R02 are external pins of the MICRF219 to connect the crystal to the reference oscillator.

Reference oscillator crystal frequency can be calculated:

$$F_{REF\ OSC} = F_{RF}/(32 + 1.1/12)$$

For 433.92 MHz, $F_{REF\ OSC}$ = 13.52127 MHz.

To operate the MICRF219 with minimum offset, crystal frequencies should be specified with 10pF loading capacitance.

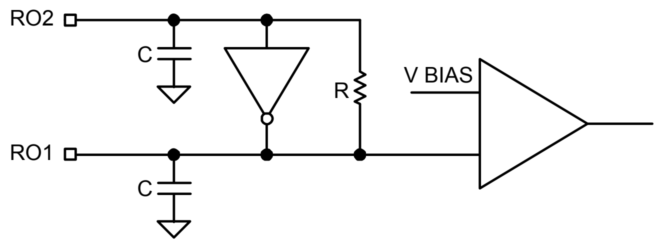


Figure 2. Reference Oscillator Circuit

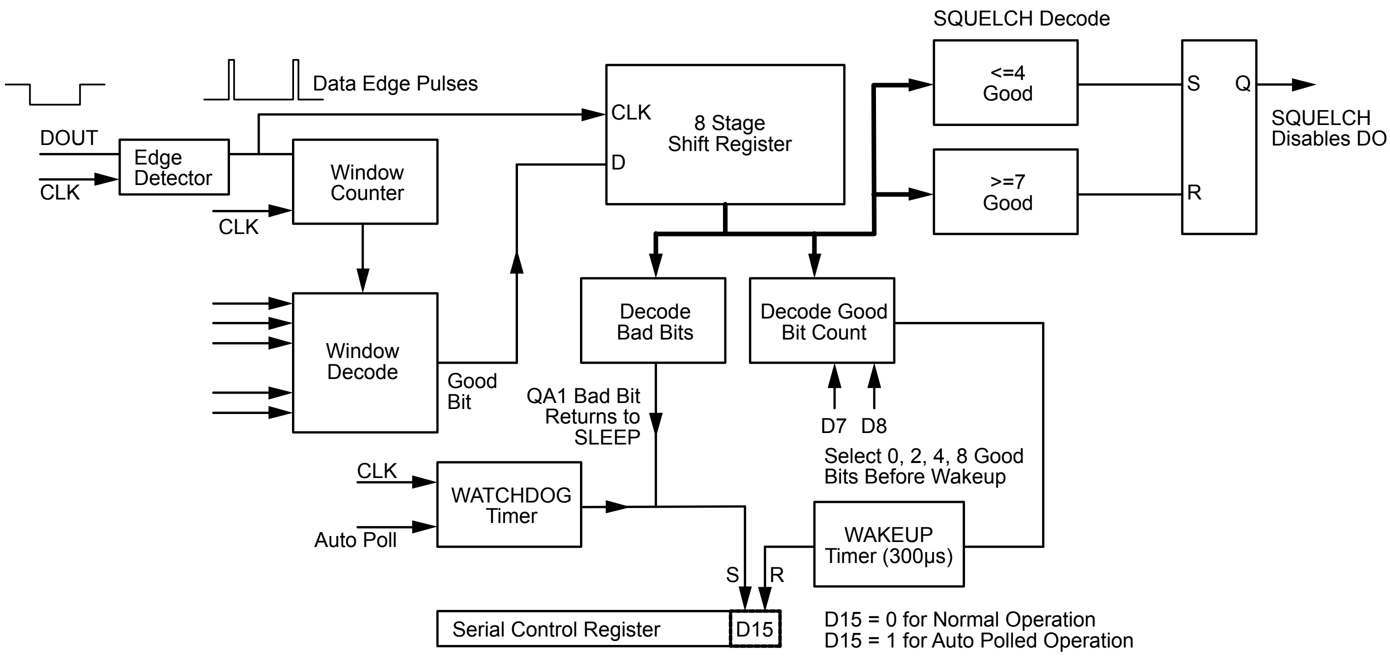


Figure 3. Autopoll, Bit-Check Block Diagram

Auto-Polling

The auto-poll block (Figure 3) contains a low power oscillator that drives the sleep timer when the rest of the device is powered down. It also contains circuits to check whether the received bits are good. Auto-polling is controlled by bit D15 in the serial register, in conjunction with bits D12, D13, D14 to set the sleep timer period. Bits D7, D8, are used for control of the bit-check operation and bits D9, D10, D11 are used to adjust the sensitivity of the bit-check action.

Auto-Polling without Bit-Checking

For simple auto-polling without bit-checking, send a serial command with bit D15 set high and bits D12, D13, D14 set to the desired sleep time. The device will go to sleep for the programmed timer duration then wake up to receive data if it is present. The device will stay awake until serial bit D15 is set low, then set high again, to enable a further sleep period. The sleep duty cycle may be controlled by the timing of serial commands.

Auto-Polling with Bit-Checking

For auto-polling with bit-checking, the serial register bits D7and D8 need to be set for the number of bits to be checked as good, before the receiver outputs data at the DO pin. The bit-check window bits D9, D10, D11 must also be set to match the data period. The shortest default window time gives the least critical bit check action. For better discrimination, the window setting may be increased up towards the normal minimum time expected between data edges. Note that a window time set longer than this will result in all bits being tested as bad and the device will remain in sleep polling mode. Now, when the serial command sets bit D15 high, the device will go to sleep for the timer period and will then awake to receive and check bits. The device will output data again at DO as soon as the programmed numbers of good RTZ bits have been received. If a bad bit is seen, the device will return to sleep mode and poll again for good bits after the sleep period. Both high and low periods are checked for each RTZ bit. The device will continue to check bits until sufficient good bits enable the device to wake up, or bad bits return the device to sleep.

Operation

Received pulse edges trigger a programmable window timer clocked by the reference frequency. If the next pulse edge falls within this window the bit is flagged as bad. Detected good bits are counted and the device will wake up once sufficient pulses have been received. Two bad pulses or a lack of pulses will cause the device to go to sleep for a further sleep timeout period.

Squelch

During normal operation, if four or less out of eight bit pulses are good, the DO output is squelched. If good bit count increases to seven or more in any eight sequential bits, squelch is disabled allowing data to output at DO pin.

Serial Interface Register Programming

Control Register Individual Truth Tables:

D0	D1	D2	MODE: Desense
0	X	X	No Desense - default
1	0	0	6dB Desense
1	1	0	16dB Desense
1	0	1	30dB Desense
1	1	1	42dB Desense

D3	D4	MODE: Demod Bandwidth (at 433.92MHz)
0	0	1625Hz
1	0	3250Hz
0	1	6500Hz
1	1	13000Hz - default

D5	D6	MODE
1	0	Slice Level 30%
0	1	Slice Level 40%
1	1	Slice Level 50% - default
0	0	Slice Level 60%

D7	D8	MODE: Bit-Check Setting
0	0	Bit-check 0 bits - default
1	0	Bit-check 2 bits
0	1	Bit-check 4 bits
1	1	Bit-check 8 bits

D9	D10	D11	MODE: Bit-Check Window Times (315 MHz)
Set D3 to			D3=1 D3=0 D3=1 D3=0
Set D4 to			D4=1 D4=1 D4=0 D4=0
0	0	0	98us, 196us, 393us, 785us
1	0	0	92us, 183us, 367us, 733us
0	1	0	85us, 170us, 341us, 681us
1	1	0	79us, 157us, 314us, 629us
0	0	1	72us, 144us, 288us, 577us
1	0	1	66us, 131us, 262us, 525us
0	1	1	59us, 118us, 236us, 473us
1	1	1	53us, 105us, 210us, 420us

D9	D10	D11	MODE: Bit-Check Window Times (433.92MHz)
Set D3 to			D3=1 D3=0 D3=1 D3=0
Set D4 to			D4=1 D4=1 D4=0 D4=0
0	0	0	71us, 143us, 285us, 570us
1	0	0	67us, 133us, 266us, 532us
0	1	0	62us, 124us, 247us, 494us
1	1	0	57us, 114us, 228us, 457us
0	0	1	52us, 105us, 209us, 419us
1	0	1	48us, 95us, 190us, 381us
0	1	1	43us, 86us, 172us, 343us
1	1	1	38us, 76us, 152us, 305us

Default State D9, D10, D11 is 111

D12	D13	D14	MODE: Sleep Time
0	0	0	10ms
1	0	0	20ms
0	1	0	40ms Default
1	1	0	80ms
0	0	1	160ms
1	0	1	320ms
0	1	1	640ms
1	1	1	1280ms

D15	MODE: Auto-Poll
0	Awake – does not poll - default
1	Auto-polls with Sleep periods

D16	Always Set This Bit to 0

SQ Pin	D17	MODE: Squelch Enable
0	0	Squelch Circuit Enabled
0	1	Squelch Circuit Disabled
1	0	Squelch Circuit Disabled (default)
1	1	Squelch Circuit Enabled

The external pin SQ can invert the setting of squelch on/off defined by register bit D17. The external pin defaults high via an internal pull-up so the squelch is off with default D17 = 0 and on if D17 = 1. Such bit logic is reversed if SQ pin is tied to low (Ground).

D18	Always Set This Bit to 1

D19	Always Set This Bit to 0

Application Information

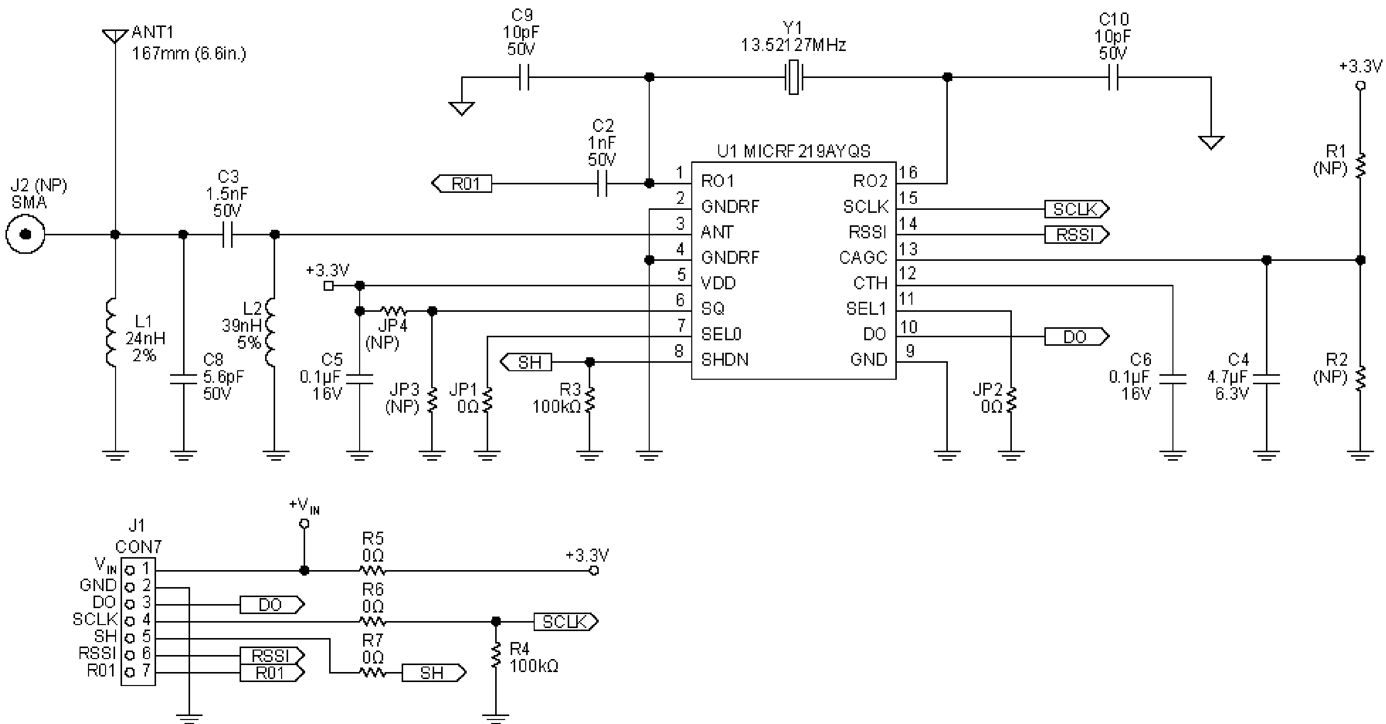


Figure 4. QR219BPF Application Example, 433.92MHz

Antenna and RF Port Connections

Figure 4 shows the schematic of the QR219BPF configured for 433.29 MHz operation. Figure 19 through Figure 23 are PCB pictures. The QR219BPF is a good starting point for the prototyping of most applications. Current design offers two antenna options: A wire antenna or 50Ω SMA antenna. The SMA connection also allows an RF signal to be injected for test or verification. To use an antenna such as a 50 Ω whip, remove the SMA and solder the whip antenna in the hole on the PCB instead. A wire of 22AWG with 167mm (6.-inch) can be used as a substitution if low cost antenna is needed.

Front-End Band Pass Filter

Components L1 and C8 form the band-pass filter at front of the receiver. Its purpose is to attenuate undesired outside band noise that degrades the receiver performance. It is calculated by the parallel resonance equation:

f = 1/(2×PI×(SQRT L1×C8))

Table 2 shows the component values for most often used frequencies.

Freq (MHz)	C8 (pF)	L1 (nH)
315.0	6.8	39
390.0	6.8	24
418.0	6.0	24
433.92	5.6	24

Table 2. Front Band-Pass Filter values for Various Frequencies

This band-pass filter can be removed if the outside band noise does not cause a problem. The MICRF219 has built-in image reject mixers which improve the selectivity significantly and reject outside band noise.

Low-Noise Amplifier Input Matching

Capacitor C3 and inductor L2 form the “L” shape input matching network. The capacitor provides additional attenuation for low-frequency outside band noise. The inductor provides additional ESD protection for the antenna pin. Two methods can be used to find these values that best matched near 50Ω. One method is done by calculating the values using the equations below and the other is using a Smith chart utility. The latter is made easier via a software plot where components are added on. In this way, the user can see the impedance moving direction for best values of C8 and L1 toward to central matching point, like WinSmith by Noble Publishing.

To calculate the matching values, one needs to know the input impedance of the device. Table 3 shows the input impedance of the MICRF219 and suggested matching values for the most often used frequencies. These suggested values may be different if the layout is not exactly the same as the one made here:

Freq (MHz)	C3 (pF)	L2(nH)	Z device (Ω)
315	1.8	68	33 - j235
390	1.5	47	23 – j199
418	1.5	43	21 – j186
433.92	1.5	39	19 – j174

Table 3. Matching Values for the Most Used Frequencies

For the frequency of 433.92MHz, the input impedance is Z = 18.6 – j174.2Ω, then the matching components are calculated by:

Equivalent parallel = B = 1/Z = 0.606 + j5.68msiemens

Rp = 1 / Re (B); Xp = 1 / Im (B)

Rp = 1.65kΩ; Xp = 176.2Ω

Q = SQRT (Rp/50 + 1)

Q = 5.831

Xm = Rp / Q

Xm = 282.98Ω

Resonance Method for L-shape Matching Network

Lc = Xp / (2×Pi×f); Lp = Xm / (2×Pi×f)

L2 = (Lc×Lp) / (Lc + Lp); C3 = 1 / (2×Pi×f×Xm)

L2 = 39.8nH

C3 = 1.3pF

Doing the same calculation example with the Smith Chart, would appear as follows,

First, one plots the input impedance of the device, (Z = 18.6 – j174.2)Ω @ 433.92MHz.(Figure 5):

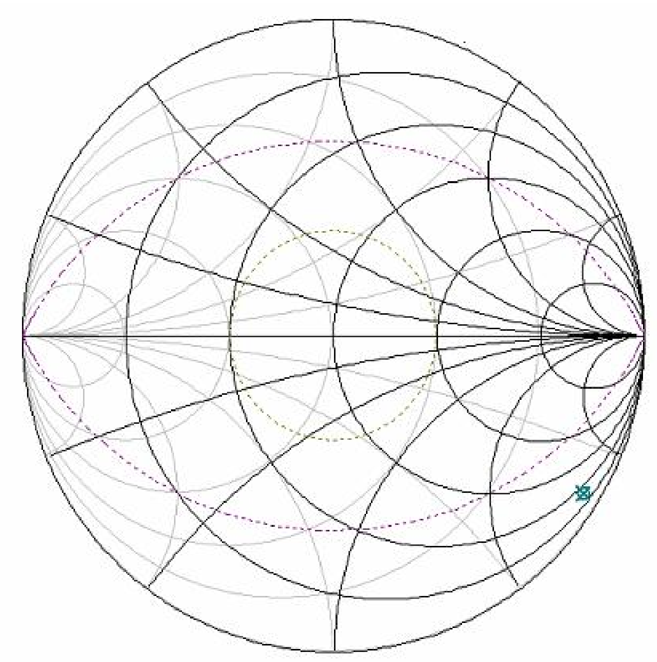


Figure 5. Device’s Input Impedance, Z = 19 – j174Ω

Second, one plots the shunt inductor (39nH) and the series capacitor (1.5pF) for the desired input impedance (Figure 6). One can then see the matching leading to the center of the Smith Chart or close to 50Ω.

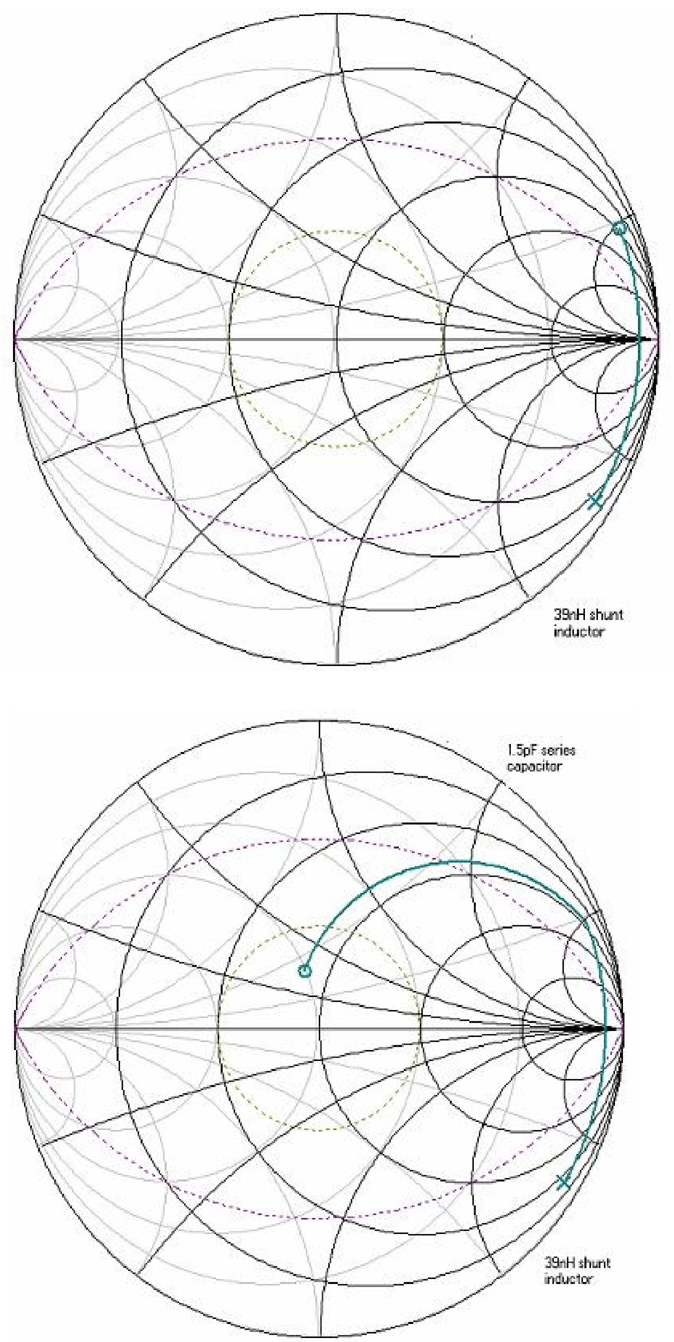


Figure 6. Plotting of Shunt Inductor and Series Capacitor

Crystal Selection

Crystal Y1 or Y1A (SMT or leaded respectively) is the reference clock for all the device internal circuits.

Crystal characteristics of 10pF load capacitance, 30ppm, ESR < 50Ω, –40ºC to +105ºC temperature range are desired. Table 4 shows Micrel's approved crystal suppliers such as (www.hib.com.br or http://www.abracon.com/) and the frequencies.

The oscillator of the MICRF219 is a Pierce-type oscillator. Good care must be taken when laying out the printed circuit board. Avoid long traces and place the ground plane on the top layer close to the REFOSC pins RO1 and RO2. When care is not taken in the layout, and the crystals used are not verified, the oscillator may take longer time to start. Time-to-good-data in the DO pin will be longer as well. In some cases, if the stray capacitance is too high (> 20pF). In this case, either the receiving central frequency will offset too much or the oscillator may not start.

The crystal frequency is calculated by REFOSC = RF Carrier/(32+(1.1/12)). The local oscillator is low-side injection (32 × 13.52127MHz = 432.68MHz), that is, its frequency is below the RF carrier frequency and the image frequency is below the LO frequency. See Figure 7. The product of the incoming RF signal and local oscillator signal will yield the IF frequency, which will be demodulated by the detector of the device.

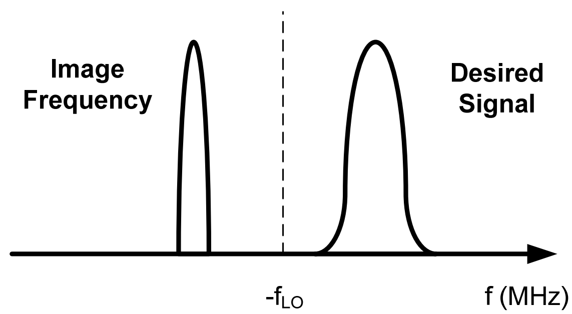


Figure 7. Low-Side Injection Local Oscillator

REFOSC (MHz)	Carrier (MHz)	HIB Part Number	Abracon Part Number
9.81563	315.0	SA-9.815630-F-10-H-30-30-X	ABLS-9.81563MHz-10J4Y
12.15269	390.0	SA-12.152690-F-10-H-30-30-X	ABLS-12.15269MHz-10J4Y
13.02519	418.0	SA-13.025190-F-10-H-30-30-X	ABLS-13.025190MHz-10J4Y
13.52127	433.92	SA-13.521270-F-10-H-30-30-X	ABLS-13.521270MHz-10J4Y

Table 4. Crystal Frequencies and Vendor Part Numbers

Demodulator Bandwidth Selection and Data Stream Optimization

JP1 and JP2 are the bandwidth selection for the demodulator bandwidth. To set it correctly, it is necessary to know the shortest pulse width of the encoded data sent in the transmitter. Similar to the example of the data profile in the Figure 7, PW2 is shorter than PW1, so PW2 should be used for the demodulator bandwidth calculation which is found by 0.65/shortest pulse width. After this value is found, the setting should be done according to Table 5. For example, if the pulse period is 100µsec, 50% duty cycle, the pulse width will be 50µsec (PW = (100µsec × 50%) / 100). Therefore, a bandwidth of 13kHz would be necessary (0.65 / 50µsec). However, if this data stream had a pulse period with a 20% duty cycle, then the bandwidth required would be 32.5kHz (0.65 / 20µsec). This would exceed the maximum bandwidth of the demodulator circuit. If one tries to exceed the maximum bandwidth, the pulse would appear stretched or wider.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum Baud Rate for 50% Duty Cycle (Hz)
Short	Short	1625	400	1250
Open	Short	3250	200	2500
Short	Open	6500	100	5000
Open	Open	13000	50	10000

Table 5. JP1 and JP2 Setting, 433.92MHz

Other frequencies will have different demodulator bandwidth limits, which is derived from the reference oscillator frequency. Table 6 and Table 7 shows the limits for the other two most used frequencies.

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum Baud Rate for 50% Duty Cycle (Hz)
Short	Short	1565	416	1204
Open	Short	3130	208	2408
Short	Open	6261	104	4816
Open	Open	12523	52	9633

Table 6. P1 and JP2 Setting, 418.0MHz

SEL0 JP1	SEL1 JP2	Demod. BW (hertz)	Shortest Pulse (µsec)	Maximum Baud Rate for 50% Duty Cycle (Hz)
Short	Short	1170	445	1123
Open	Short	2350	223	2246
Short	Open	4700	111	4493
Open	Open	9400	56	8987

Table 7. JP1 and JP2 Setting, 315MHz

AGC Capacitor and Data Slicer Threshold Capacitor Selection

Capacitors C6 and C4 are C_{TH} and C_{AGC} capacitors respectively providing a time base reference for the data pattern received. These capacitors are selected according to data profile, pulse duty cycle, dead time between two received data packets, and if the data pattern does has or not have a preamble. See Figure 8 for example of a data profile.

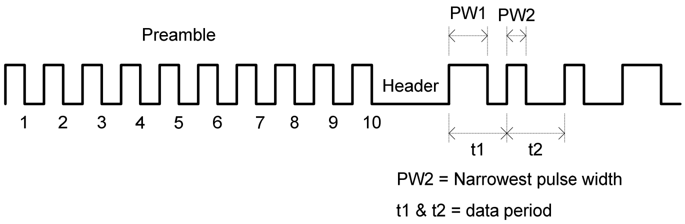


Figure 8. Example of a Data Profile

For best results, they should always be optimized for the data pattern used. As the baud rate increases, the capacitor values decrease. Table 8 shows suggested values for Manchester Encoded data, 50% duty cycle.

SEL0 JP1	SEL1 JP2	Demod. BW (Hz)	Cth	Cagc
Short	Short	1625	100nF	4.7µF
Open	Short	3250	47nF	2.2µF
Short	Open	6500	22nF	1µF
Open	Open	13000	10nF	0.47µF

Table 8. Suggested C_{TH} and C_{AGC} Values

JP3 and JP4 are jumpers selectable to high or low and used to configure the digital squelch function. When it is tied to high, there is no squelch applied to the digital circuits and the DO (data out) pin has a hash signal. When the pin is low, the DO pin activity is considerably reduced. It will have more or less than shown in the figure below depending upon the outside band noise. The penalty for using squelch is a delay in getting a good signal in the DO pin. This means that it takes longer for the data to show up. The delay is dependent upon many factors such as RF signal intensity, data profile, data rate, C_{TH} and C_{AGC} capacitor values, and outside band noise See Figure 9 and Figure 10. Please note that Squelch action is based on the Bitcheck operation and may be optimized using the Bitcheck Window serial register setting.

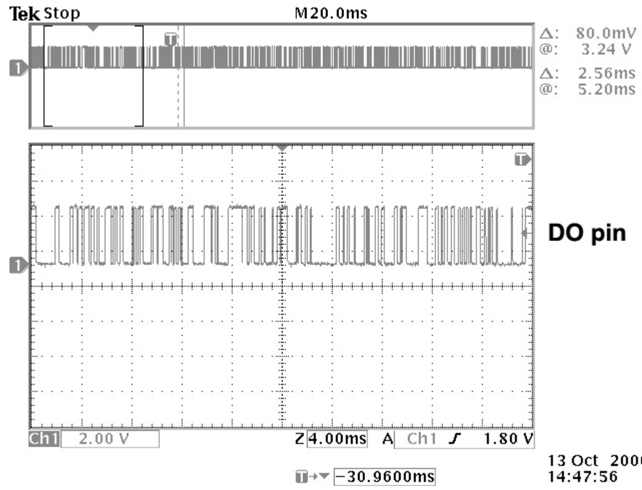


Figure 9. Data Out Pin with No Squelch (SQ = 1)

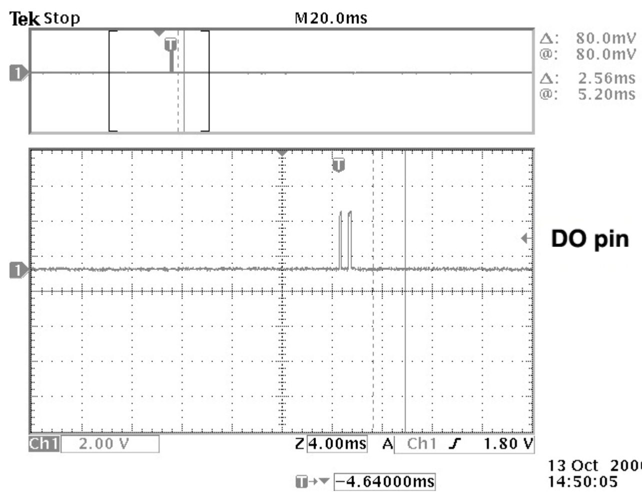


Figure 10. Data Out Pin with Squelch (SQ = 0)

Other components used are C5, which is a decoupling capacitor for the V_{DD} line; R3 for the shutdown pin (SHDN = 0, device is operation), which can be removed if that pin is connected to a microcontroller or an external switch; and R1 and R2 which form a voltage divider for the AGC pin. One can force a voltage in this AGC pin to purposely decrease the device sensitivity. Special care is needed when doing this operation, as an external control of the AGC voltage may vary from lot to lot and may not work the same in several devices.

Three other pins are worthy of comment. They are the DO, RSSI, and shutdown pins. The DO pin has a driving capability of 0.4mA. This is good enough for most of the logic family ICs on the market today. The RSSI pin provides a transfer function of the RF signal intensity versus voltage. It is very useful to determine the signal-to-noise ratio of the RF link, crude range estimate from the transmitter source and AM demodulation, which requires a low C_{AGC} capacitor value.

The shutdown pin (SHDN) is useful to save energy. Making its level close to V_{DD} (SHDN = 1), the device is not in operation. Its DC current consumption is less than 1µA (do not forget to remove R3). When toggling from high to low, there will be a time required for the device to come to steady-state mode, and a time for data to show up in the DO pin. This time will be dependent upon many things such as temperature, the crystal used, and if there is an external oscillator with faster startup time. See Figure 11 and Figure 12 or time-to-good-data on both 433.92MHz and 315MHz versions.

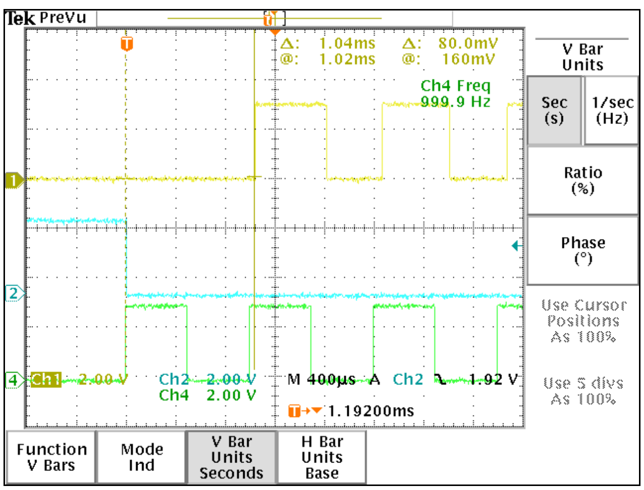


Figure 11. Time-to-Good-Data after Shutdown Cycle, 433.92MHz, Room Temperature

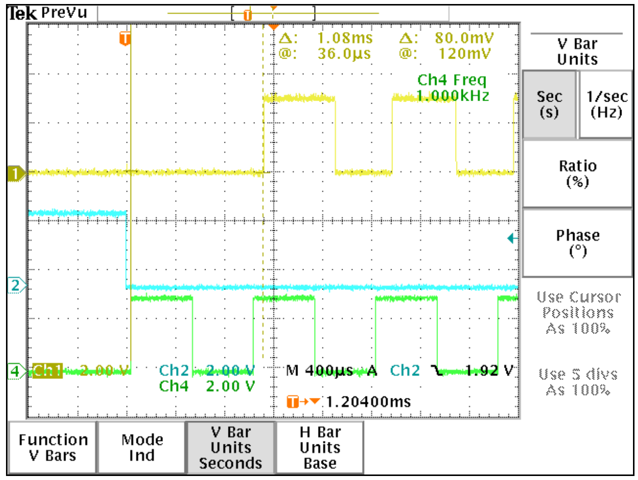


Figure 12. Time-to-Good-Data after Shutdown Cycle, 315MHz at Room Temperature

Serial Register Programming

Programming the device is accomplished by the use of pins DO and SCLK. Normally, D0 (Pin 10) is outputting data and needs to switch to an input pin made by the start sequence, as shown at Figure 13. High at the SCLK pin tri-states the DO pin, enabling the external drive into the DO pin with an initial low level. The start sequence is completed by taking SCLK low, then high while DO is low, followed by taking DO high, then low while SCLK is high. The serial interface is initialized and ready to receive the programming data.

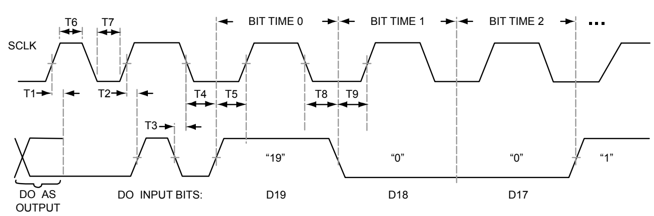


Figure 13. Serial Interface Start Sequence

Bits are serially programmed starting with the most significant bit (MSB = D19) if all bits are being programmed until the least significant bit (LSB =D0) For instance, if only the desense bits D0, D1, and D2 are being programmed, then these are the only bits that need to be programmed with the start sequence D2, D1, D0, plus the stop sequence. Or, if only the squelch bit D17 is needed, then the sequence must be from start sequence, D17 through D0 plus the stop sequence, making sure the other bits (besides D17) are programmed as needed. It is recommended that all parallel input pins (SEL0, SEL1, and SQ) be kept high when using the serial interface. After the programming bits are finished, a stop sequence (as shown in Figure 14) is required to end the mode and reestablish the DO pin as an output again. To do so, the SCLK pin is kept high while the DO pin changes from low to high, then low again, followed by the SCLK pin made low. Timing of the programming bits are not critical, but should be kept as shown below:

T1 < 0.1µs, Time from SCLK to convert DO to input pin

T6 > 0.1µs, SCLK high time

T7 > 0.1µs, SCLK low time

T2, T3, T4, T5, T8, T9, T10 > 0.1µs

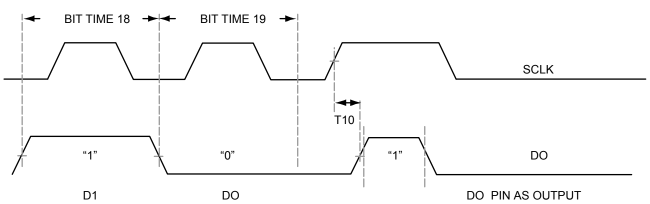


Figure 14. Serial Interface Stop Sequence

SCLK frequency should be greater than 5kHz to avoid automatic reset from internal circuitry.

Serial Interface Register Loading Examples

See Figures 15 – 17. (Channel 1 is the DO pin, and channel 2 is the SCLK pin).

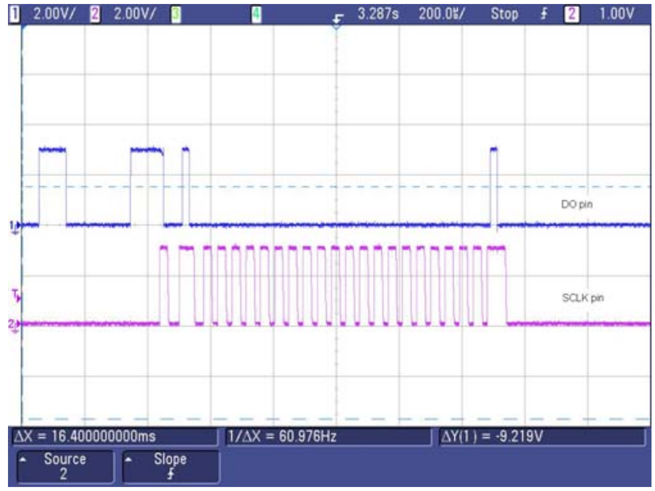


Figure 15. All Bits D19 through D0 = 0

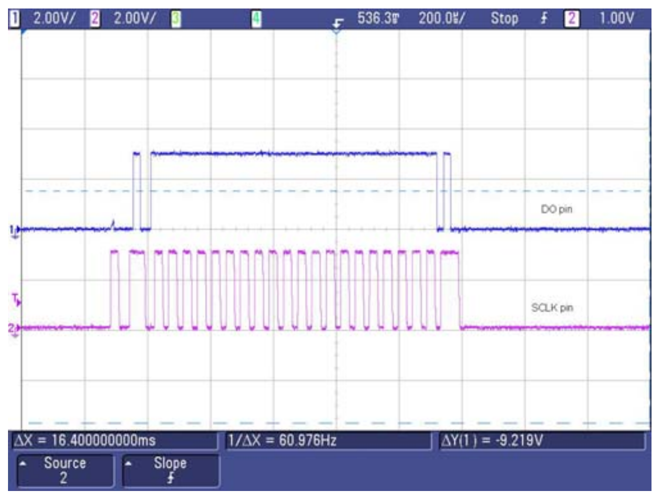


Figure 16. All Bits D19 through D0 = 1

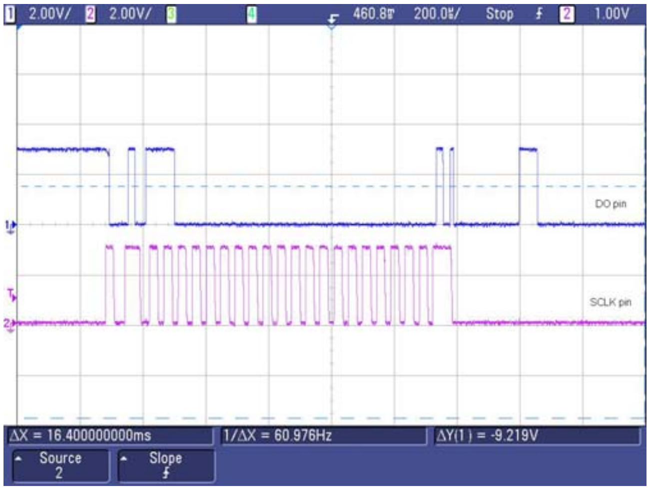


Figure 17. D19 = D18 = 1, D17 = D0 = 0

Auto-Poll Programming Example

Auto-Poll example (see Figure 18):

D0 = D1 = D2 = 0, no desense

D3 = D4 = 0, demodulator bandwidth = 1712 hertz, 1 kHz baud rate, pulse = 500μsec.

Required demodulator bandwidth is 0.65/500usec = 1300 hertz

D5 = D6 = 1, Slice level = 50%

D7 = 0, D8 = 1, bit check = 4 bits.

This is the time the device is ON checking for four consecutive valid windows.

D9 = D10 = 1, D11 = 0, data rate is 1 kHz, (500μsec pulses), window set to 433μsec (< 500 usec)

D12 = D13 = 0, D14 = 1, sleep timer set to 160msec, that is, 4 bit is ON and 160msec is OFF.

D15 = 1, device is placed in autopoll

D16 = 0, not used. Always set to 0.

D17 = 0, squelch is OFF

D18 = 1, watchdog timer is OFF

D19 = 0, no RSSI offset

From MSB to LSB (see Table 9):

D19	D18	D17	D16	D15	D14	D13	D12
0	1	0	0	1	1	0	0
D11	D10	D9	D8	D7	D6	D5	
0	1	1	1	0	1	1	
D4	D3	D2	D1	D0			
0	0	0	0	0			

Table 9. Auto-Poll Example Bit Sequence

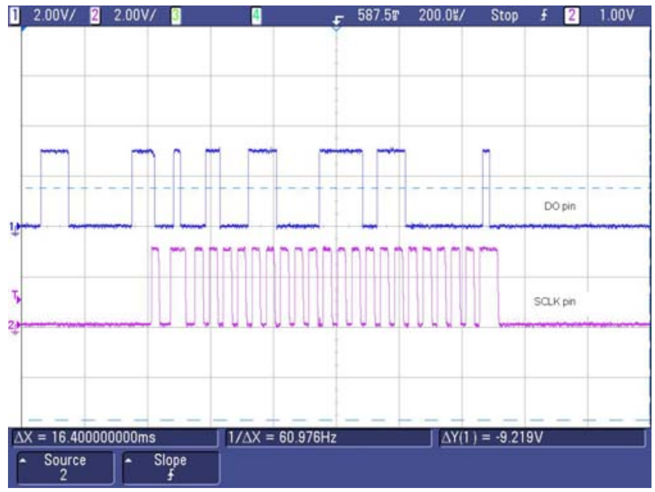


Figure 18. Autopoll Example

PCB Considerations and Layout

Figure 19 to Figure 23 show the QR219BPF PCB layout. The Gerber files provided are downloadable from Micrel Website and contain the remaining layers needed to fabricate this board. When copying or making one's own boards, make the traces as short as possible. Long traces alter the matching network and the values suggested are no longer valid. Suggested matching values may vary due to PCB variations. A PCB trace 100 mills (2.5mm) long has about 1.1nH inductance. Optimization should always be done with exhaustive range tests. Make sure the individual ground connection has a dedicated via rather then sharing a few of ground points by a single via. Sharing ground via will increase the ground path inductance. Ground plane should be solid and with no sudden interruptions. Avoid using ground plane on top layer next to the matching elements. It normally adds additional stray capacitance which changes the matching. Do not use Phenolic materials as they are conductive above 200MHz. Typically, FR4 or better materials are recommended. The RF path should be as straight as possible to avoid loops and unnecessary turns. Separate ground and V_{DD} lines from other digital or switching power circuits (such microcontroller…etc). Known sources of noise should be laid out as far as possible from the RF circuits. Avoid unnecessary wide traces which would add more distribution capacitance (between top trace to bottom GND plane) and alter the RF parameters.

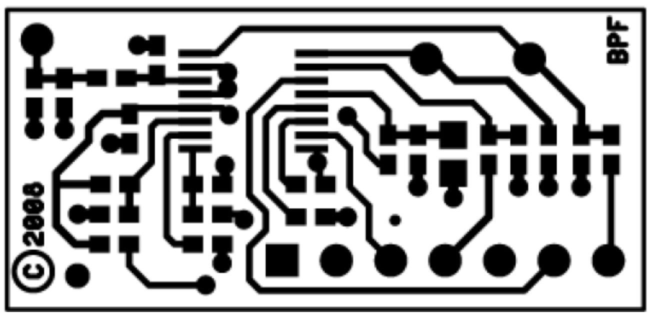


Figure 19. QR219BPF Top Layer

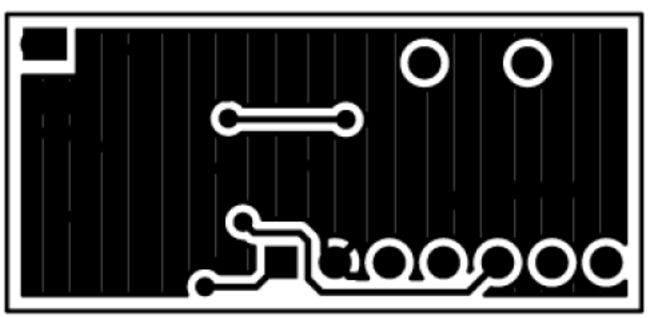


Figure 20. QR219BPF Bottom Layer

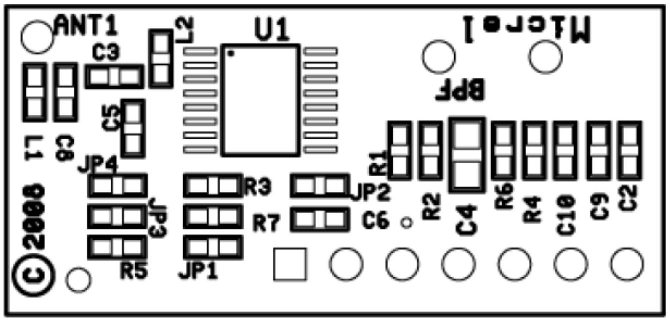


Figure 21. QR219BPF Top Silkscreen Layer

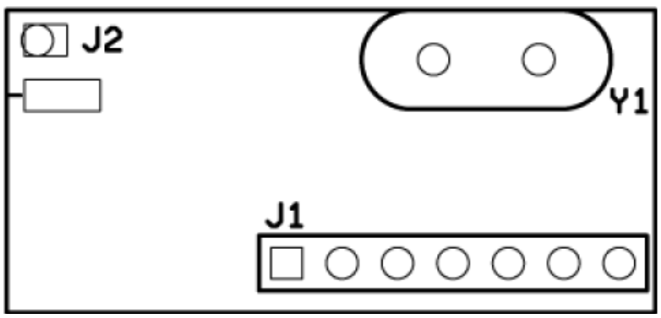


Figure 22. QR219BPF Bottom Silkscreen Layer

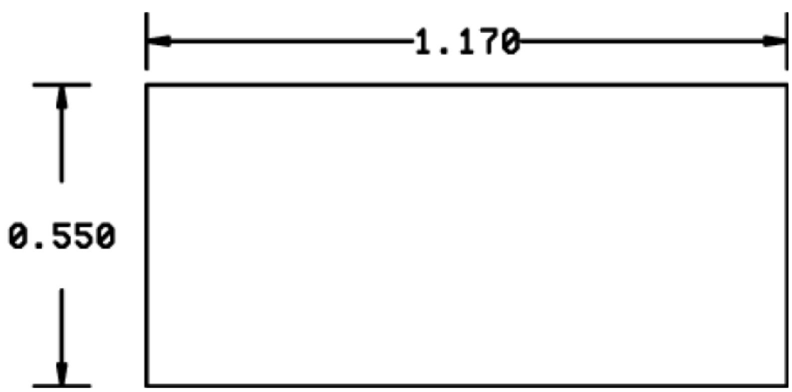


Figure 23. QR219BPF Dimensions (in inches)

QR219BPF Bill of Materials, 433.92MHz

Item	Reference	Part	Description	Qty.
1	ANT1	22AWG rigid wire	167mm (6.6”) 22AWG wire	1
2	C3	1.5pF 50V	0603 chip capacitor	1
3	C4	4.7uF 6.3V	0805 chip capacitor	1
4	C6,C5	0.1uF 16V	0603 chip capacitor	2
5	C8	5.6pF 50V	0603 chip capacitor	1
6	C10,C9	10pF 50V	0603 chip capacitor	2
7	JP1, JP2, R5, R6, R7	0ohm	0603 chip resistor	5
8	R1, R2, JP3, JP4	(np)	0603 chip resistor, not placed	4
9	J1	CON7	7 pin connector	1
10	J2	(np)	Edge mount SMA connector	1
11	L1	24nH 5%	5%, 0603 SMT inductor	1
12	L2	39nH 5%	5%, 0603 SMT inductor	1
13	R3	100kohm	0603 chip resistor	2
14	U1	MICRF219AYQS	MICRF219 chip	1
15	Y1	13.52127MHz	Crystal	1

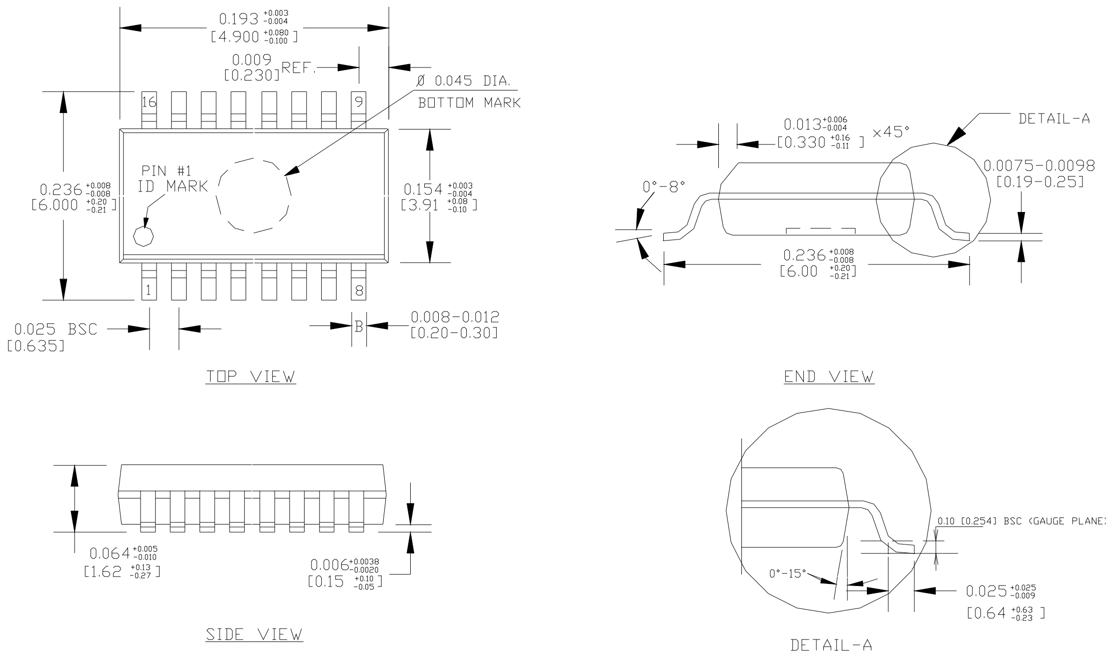
Table 10. QR219BPF Bill of Materials, 433.92MHz

QR219BPF Bill of Materials, 315MHz

Item	Reference	Part	Description	Qty.
1	ANT1	22AWG rigid wire	230mm (9.0”) 22AWG wire	1
2	C3	1.8pF 50V	0603 chip capacitor	1
3	C4	4.7µF 6.3V	0805 chip capacitor	1
4	C6,C5	0.1µF 16V	0603 chip capacitor	2
5	C8	6.8pF 50V	0603 chip capacitor	1
6	C10,C9	10pF 50V	0603 chip capacitor	2
7	JP1, JP2, R5, R6, R7	0Ω	0603 chip resistor	5
8	R1, R2, JP3, JP4	(np)	0603 chip resistor, not placed	4
9	J1	CON7	7 pin connector	1
10	J2	(np)	Edge mount SMA connector	1
11	L1	39nH 5%	5%, 0603 SMT inductor	1
12	L2	68nH 5%	5%, 0603 SMT inductor	1
13	R3	100kΩ	0603 chip resistor	2
14	U1	MICRF219AYQS	MICRF219 chip	1
15	Y1	9.81563MHz	Crystal	1

Table 11. QR219BPF Bill of Materials, 315MHz

Package Information



NOTE:
1. ALL DIMENSIONS ARE IN INCHES [MM].
2. LEAD COPLANARITY SHOULD BE 0.004" [0.10 mm] MAX.
3. MAX MISALIGNMENT BETWEEN TOP AND BOTTOM CENTER OF PACKAGE TO BE 0.004" [0.10 mm].
4. THE LEAD WIDTH, B TO BE DETERMINED AT .0075 [0.19 mm] FROM THE LEAD TIP.
5. BOTTOM MARK IS OPTIONAL, IT MAY NOT APPEAR ON THE ACTUAL UNITS.

QSOP16 Package Type (AQS16)

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