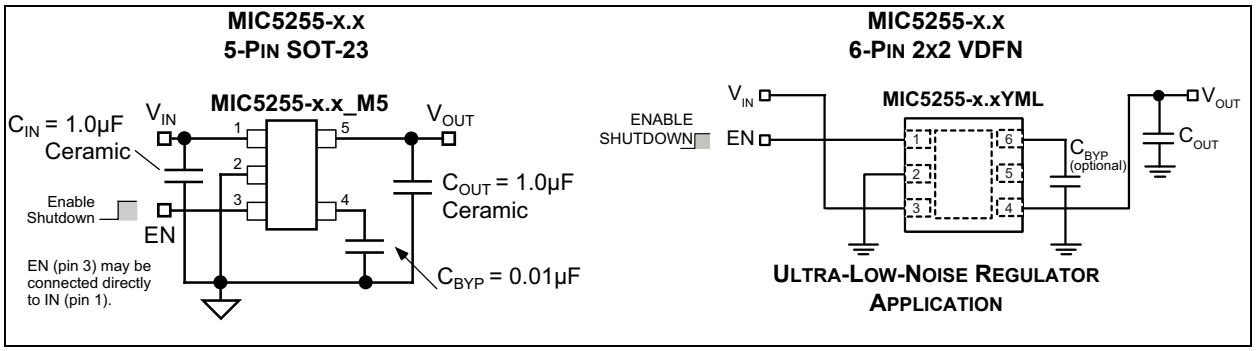
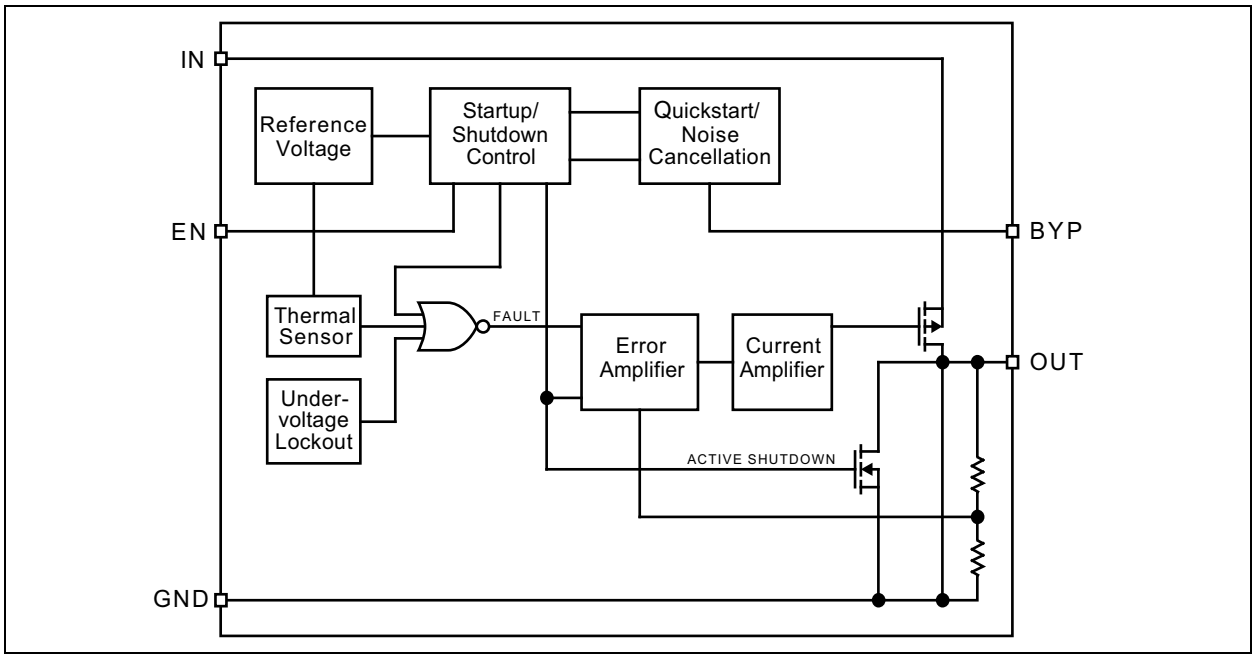
Typical Application Schematic



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) ..... 0V to +7V
Enable Voltage (V_{EN}) ..... 0V to +7V
Power Dissipation (P_D, Note 1) ..... Internally Limited
ESD Rating (Note 2) ..... 2 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) ..... +2.7V to +6V
Enable Voltage (V_{EN}) ..... 0V to V_{IN}

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown. The θ_{JA} of the MIC5255-x.xYM5 (all versions) is 235°C/W on a PC board. See the Thermal Considerations section for further details.

2: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{OUT} + 1V$, $V_{EN} = V_{IN}$; I_{OUT} = 100 µA; T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted. **(Note 1)**.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Output Voltage Accuracy	V_O	–1	—	1	%	I_{OUT} = 100 µA
		–2	—	**2**		
Line Regulation	ΔV_{LNR}	—	0.02	0.05	%/V	$V_{IN} = V_{OUT}$ + 1V to 6V
Load Regulation	ΔV_{LDR}	—	1.5	2.5	%	I_{OUT} = 0.1 mA to 150 mA; Note 2
Dropout Voltage, Note 3	$V_{IN} - V_{OUT}$	—	0.1	5	mV	I_{OUT} = 100 µA
		—	90	150		I_{OUT} = 100 mA
		—	135	200		I_{OUT} = 150 mA
		—	—	**250**		
Quiescent Current	I_Q	—	0.2	**5**	µA	$V_{EN} \le 0.4V$ (shutdown)
Ground Pin Current, Note 4	I_{GND}	—	90	150	µA	I_{OUT} = 0 mA
		—	117	—		I_{OUT} = 150 mA
Ripple Rejection	PSRR	—	60	—	dB	f = 10 Hz, C_{OUT} = 1.0 µF, C_{BYP} = 0.01 µF
		—	60	—		f = 100 Hz, $V_{IN} = V_{OUT}$ +1V
		—	50	—		f = 10 kHz, $V_{IN} = V_{OUT}$ +1V
Current Limit	I_{LIM}	160	425	—	mA	V_{OUT} = 0V
Output Voltage Noise	e_n	—	30	—	μV_{RMS}	C_{OUT} = 1.0 µF, C_{BYP} = 0.01 µF, f = 10 Hz to 100 kHz
Enable Input						
Enable Input Logic-Low Voltage	V_{IL}	—	—	**0.4**	V	V_{IN} = 2.7V to 5.5V, regulator shutdown
Enable Input Logic-High Voltage	V_{IH}	**1.6**	—	—	V	V_{IN} = 2.7V to 5.5V, regulator enabled
Enable Input Current	I_{EN}	—	0.01	—	µA	$V_{IL} \le 0.4V$, regulator shutdown
		—	0.01	—	µA	$V_{IH} \ge 1.6V$, regulator enabled
Shutdown Resistance Discharge	—	—	500	—	Ω	—
Thermal Protection						
Thermal Shutdown Temperature	—	—	150	—	°C	—
Thermal Shutdown Hysteresis	—	—	10	—	°C	—

Note 1: Specification for packaged product only.

2: Regulation is measured at constant junction temperature using low duty cycle pulse testing. Parts are tested for load regulation in the load range from 1.0 mA to 150 mA. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

3: Dropout voltage is defined as the input to output differential at which the output voltage drops 2% below its nominal value measured at 1V differential. For outputs below 2.7V, dropout voltage is the input-to-output voltage differential with the minimum input voltage 2.7V. Minimum input operating voltage is 2.7V.

4: Ground pin current is the regulator quiescent current. The total current drawn from the supply is the sum of the load current plus the ground pin current.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Operating Temperature Range	T_J	–40	—	+125	°C	Note 1
Storage Temperature	T_S	–60	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 5s
Package Thermal Resistances						
Thermal Resistance, SOT-23-5	θ_{JA}	—	235	—	°C/W	—
Thermal Resistance, 2x2 VDFN-6	θ_{JA}	—	90	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

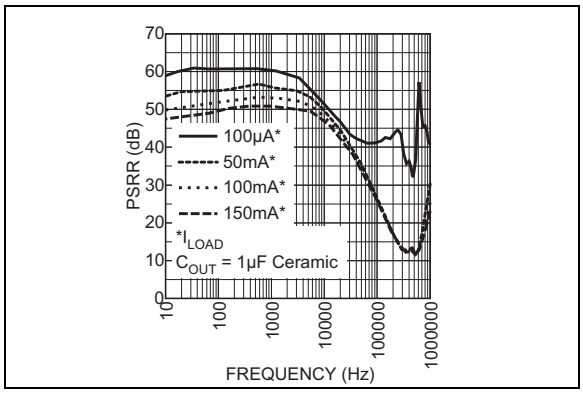


FIGURE 2-1: *Power Supply Rejection Ratio.*

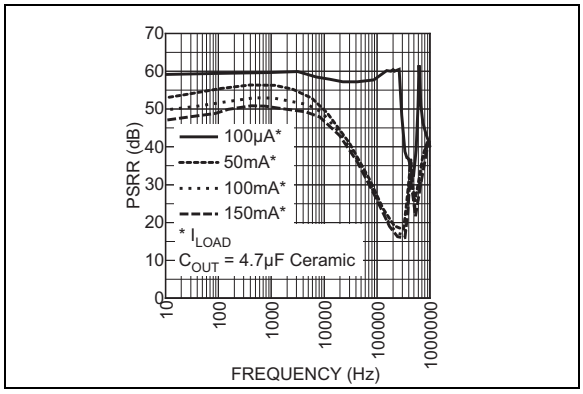


FIGURE 2-2: *Power Supply Rejection Ratio.*

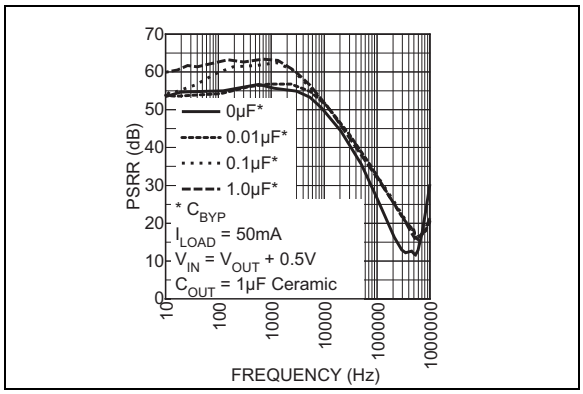


FIGURE 2-3: *Power Supply Rejection Ratio.*

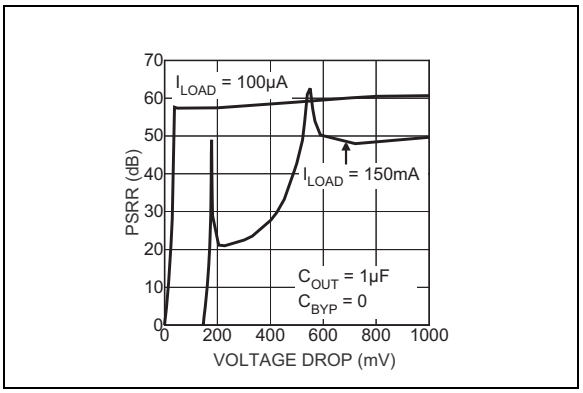


FIGURE 2-4: *PSRR vs. Voltage Drop.*

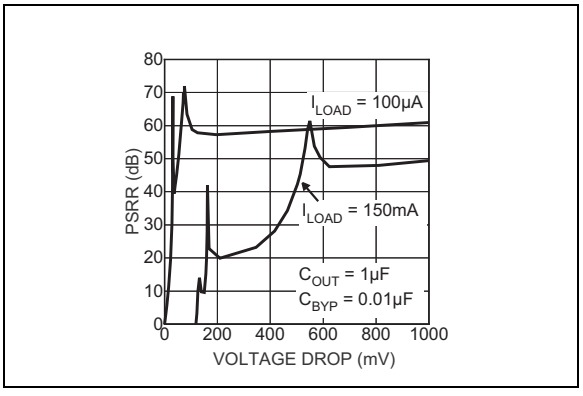


FIGURE 2-5: *PSRR vs. Voltage Drop.*

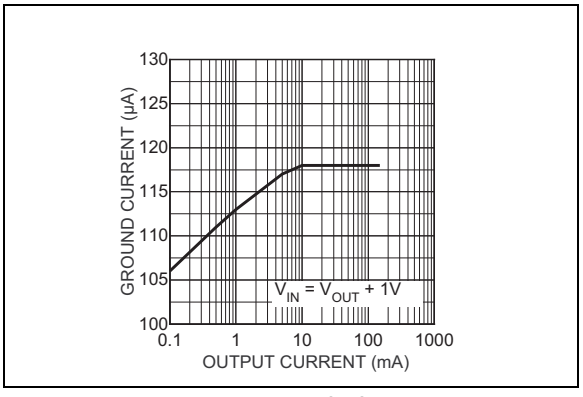


FIGURE 2-6: *Ground Pin Current.*

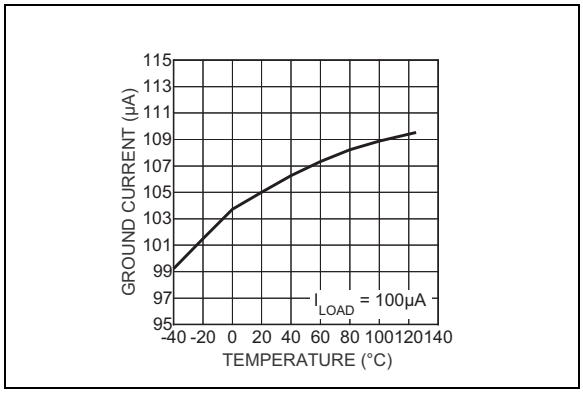


FIGURE 2-7: *Ground Pin Current.*

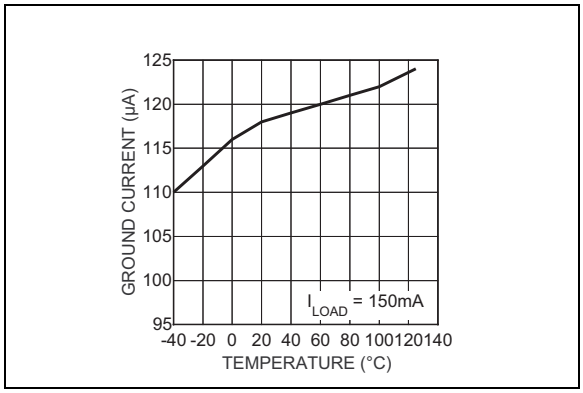


FIGURE 2-8: *Ground Pin Current.*

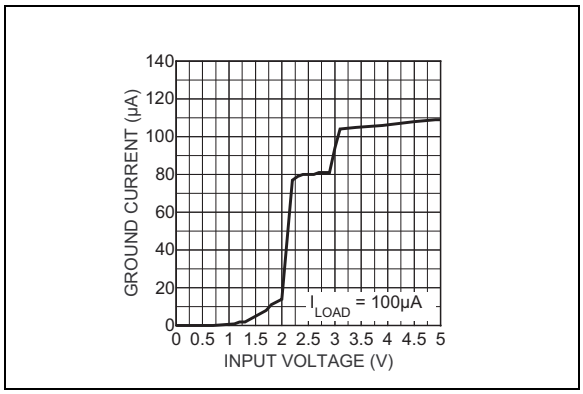


FIGURE 2-9: *Ground Pin Current.*

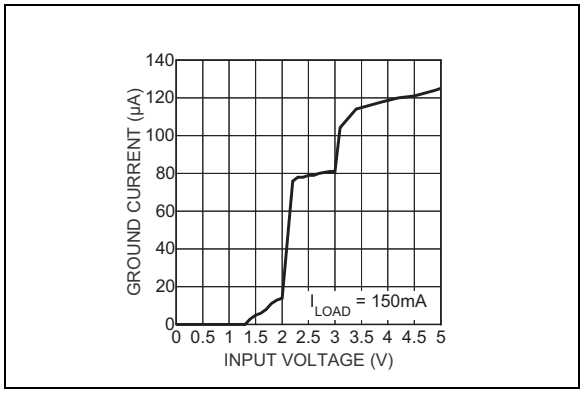


FIGURE 2-10: *Ground Pin Current.*

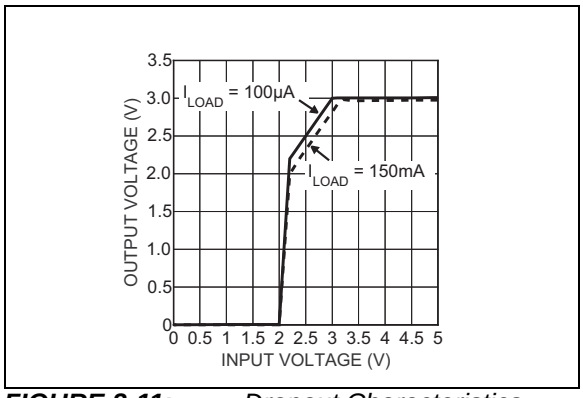


FIGURE 2-11: *Dropout Characteristics.*

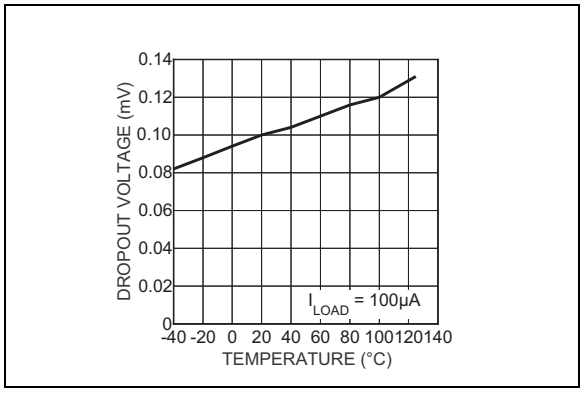


FIGURE 2-12: *Dropout Voltage.*

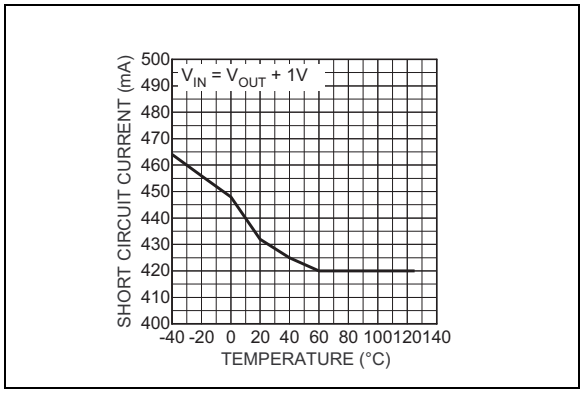


FIGURE 2-13: *Short Circuit Current*.

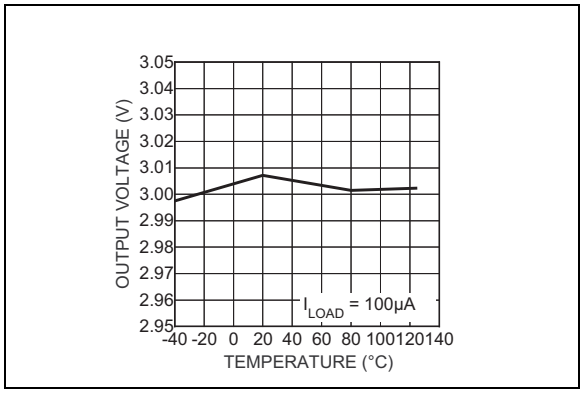


FIGURE 2-14: *Output Voltage vs. Temperature*.

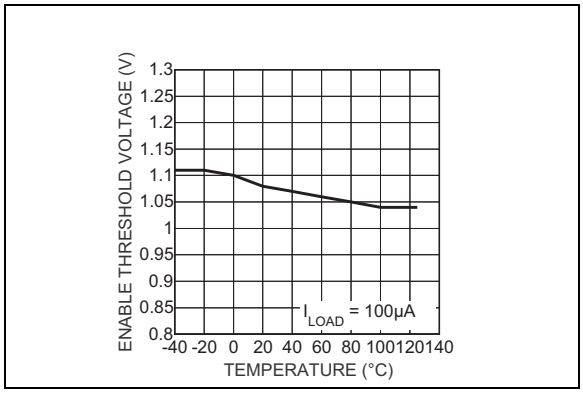


FIGURE 2-15: *Enable Threshold vs. Temperature.*

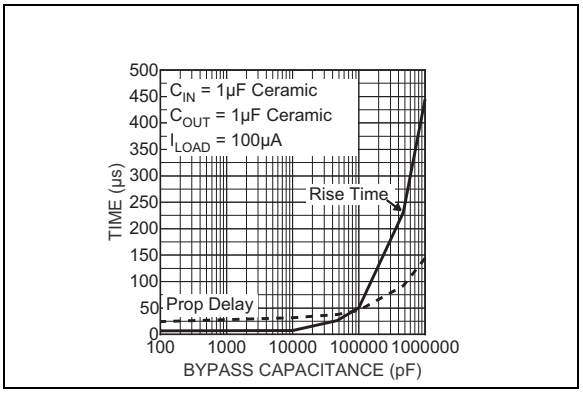


FIGURE 2-16: *Turn-On Time vs. Bypass Capacitance*.

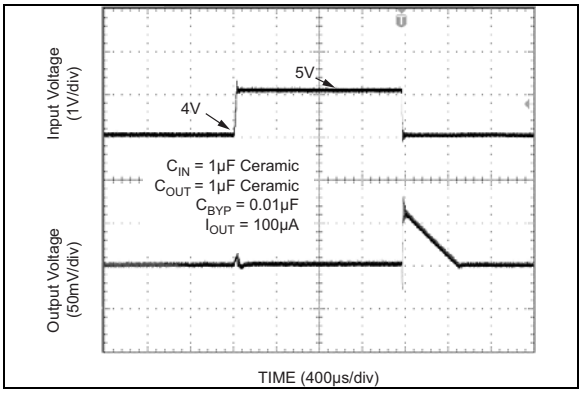


FIGURE 2-17: *Line Transient Response*.

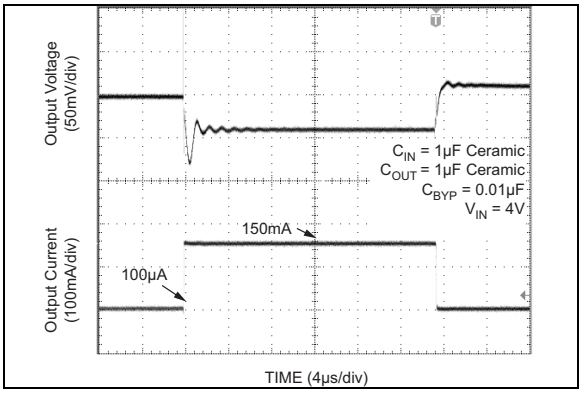


FIGURE 2-18: *Load Transient Response*.

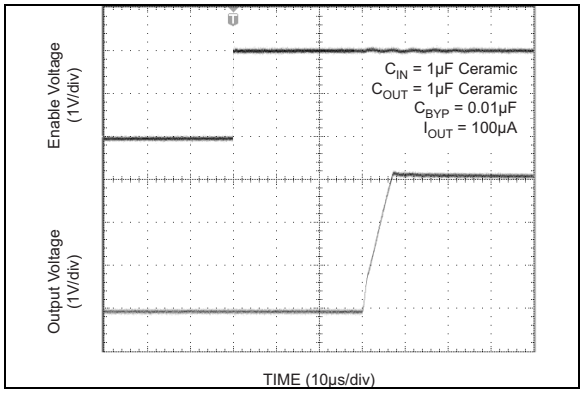


FIGURE 2-19: *Enable Pin Delay.*

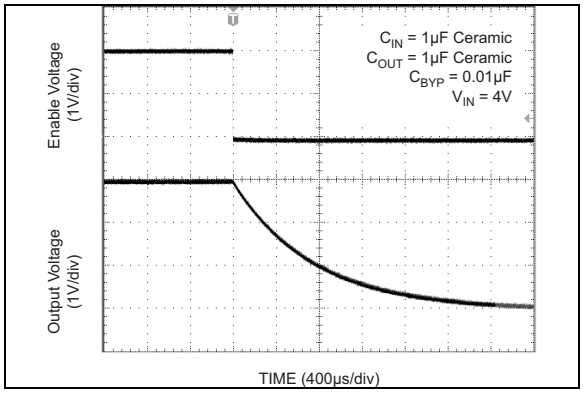


FIGURE 2-20: *Shutdown Delay.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number SOT23-5 TSOT23-5	Pin Number VDFN-6	Pin Name	Description
1	3	IN	Supply Input.
2	2	GND	Ground.
3	1	EN	Enable/Shutdown (Input): CMOS-compatible input. Logic-high = enable; logic-low = shutdown. Do not leave open.
4	6	BYP	Reference Bypass: Connect external 0.01 µF ≤ C_{BYP} ≤ 1.0 µF capacitor to GND to reduce output noise. May be left open.
5	4	OUT	Regulator Output.
—	5	NC	No internal connection.
—	EP	GND	Ground: Internally connected to the exposed pad. Connect externally to GND pin.

4.0 APPLICATION INFORMATION

4.1 Enable Shutdown

The MIC5255 comes with an active-high enable pin that allows the regulator to be disabled. Forcing the enable pin low disables the regulator and sends it into a “zero” off-mode current state. In this state, current consumed by the regulator goes nearly to zero. Forcing the enable pin high enables the output voltage. This part is CMOS and the enable pin cannot be left floating; a floating enable pin may cause an indeterminate state on the output.

4.2 Input Capacitor

The MIC5255 is a high performance, high bandwidth device. Therefore, it requires a well-bypassed input supply for optimal performance. A 1 µF capacitor is required from the input to ground to provide stability. Low-ESR ceramic capacitors provide optimal performance at a minimum of space. Additional high frequency capacitors, such as small valued NPO dielectric type capacitors, help filter out high frequency noise and are good practice in any RF-based circuit.

4.3 Output Capacitor

The MIC5255 requires an output capacitor for stability. The design requires 1 µF or greater on the output to maintain stability. The design is optimized for use with low-ESR ceramic chip capacitors. High ESR capacitors may cause high frequency oscillation. The maximum recommended ESR is 300 mΩ. The output capacitor can be increased, but performance has been optimized for a 1 µF ceramic output capacitor and does not improve significantly with larger capacitance.

X7R/X5R dielectric-type ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60%, respectively, over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic capacitor to ensure the same minimum capacitance over the equivalent operating temperature range.

4.4 Bypass Capacitor

A capacitor can be placed from the noise bypass pin to ground to reduce output voltage noise. The capacitor bypasses the internal reference. A 0.01 µF capacitor is recommended for applications that require low-noise outputs. The bypass capacitor can be increased, further reducing noise and improving PSRR. Turn-on time increases slightly with respect to bypass capacitance. A unique quick-start circuit allows the MIC5255 to drive a large capacitor on the bypass pin without significantly slowing turn-on time. Refer to the Typical Performance Curves section for performance with different bypass capacitors.

4.5 Active Shutdown

The MIC5255 also features an active shutdown clamp, which is an N-Channel MOSFET that turns on when the device is disabled. This allows the output capacitor and load to discharge, de-energizing the load.

4.6 No-Load Stability

The MIC5255 will remain stable and in regulation with no load unlike many other voltage regulators. This is especially important in CMOS RAM keep-alive applications.

4.7 Thermal Considerations

The MIC5255 is designed to provide 150 mA of continuous current in a very small package. Maximum power dissipation can be calculated based on the output current and the voltage drop across the part. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device and the following basic equation:

EQUATION 4-1:

$$P_{D(MAX)} = \left(\frac{T_{J(MAX)} - T_A}{\theta_{JA}}\right)$$

$T_{J(MAX)}$ is the maximum junction temperature of the die, 125°C, and T_A is the ambient operating temperature. θ_{JA} is layout dependent; Table 4-1 shows examples of junction-to-ambient thermal resistance for the MIC5255.

TABLE 4-1: SOT23-5 THERMAL RESISTANCE

Package	θ_{JA} Recommended Minimum Footprint	θ_{JA} 1” Square Copper Clad	θ_{JC}
SOT23-5 (M5 or D5)	235°C/W	185°C/W	145°C/W

The actual power dissipation of the regulator circuit can be determined using the equation:

EQUATION 4-2:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + V_{IN} \times I_{GND}$$

Substituting $P_{D(MAX)}$ for P_D and solving for the operating conditions that are critical to the application will give the maximum operating conditions for the regulator circuit. For example, when operating the MIC5255-3.0YM5 at +50°C with a minimum footprint layout, the maximum input voltage for a set output current can be determined as follows:

EQUATION 4-3:

$$P_{D(MAX)} = \left(\frac{125^oC - 50^oC}{235^oC/W}\right) = 319mW$$

The junction-to-ambient thermal resistance for the minimum footprint is 235°C/W, from Table 4-1. The maximum power dissipation must not be exceeded for proper operation. Using the output voltage of 3.0V and an output current of 150 mA, the maximum input voltage can be determined for the series of equations between Equation 4-4 and Equation 4-7. Because this device is CMOS and the ground current is typically 100 µA over the load range, the power dissipation contributed by the ground current is <1% and can be ignored for this calculation:

EQUATION 4-4:

$$319mW = (V_{IN} - 3.0V) \times 150mA$$

EQUATION 4-5:

$$319mW = V_{IN} \times 150mA - 450mW$$

EQUATION 4-6:

$$769mW = V_{IN} \times 150mA$$

EQUATION 4-7:

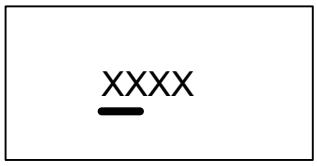
$$V_{IN(MAX)} = 5.12V$$

Therefore, a 3.0V application at 150 mA of output current can accept a maximum input voltage of 5.12V in a SOT23-5 package.

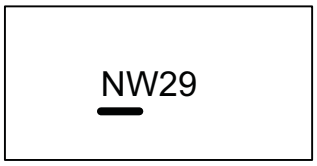
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

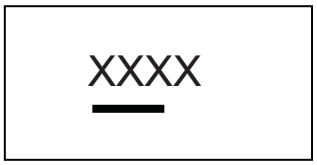
5-Pin TSOT-23*



Example

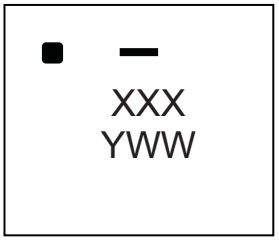


5-Pin SOT-23*

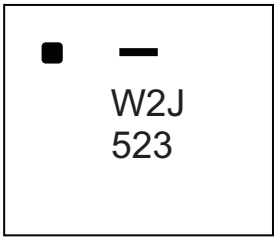


Example

6-Pin VDFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

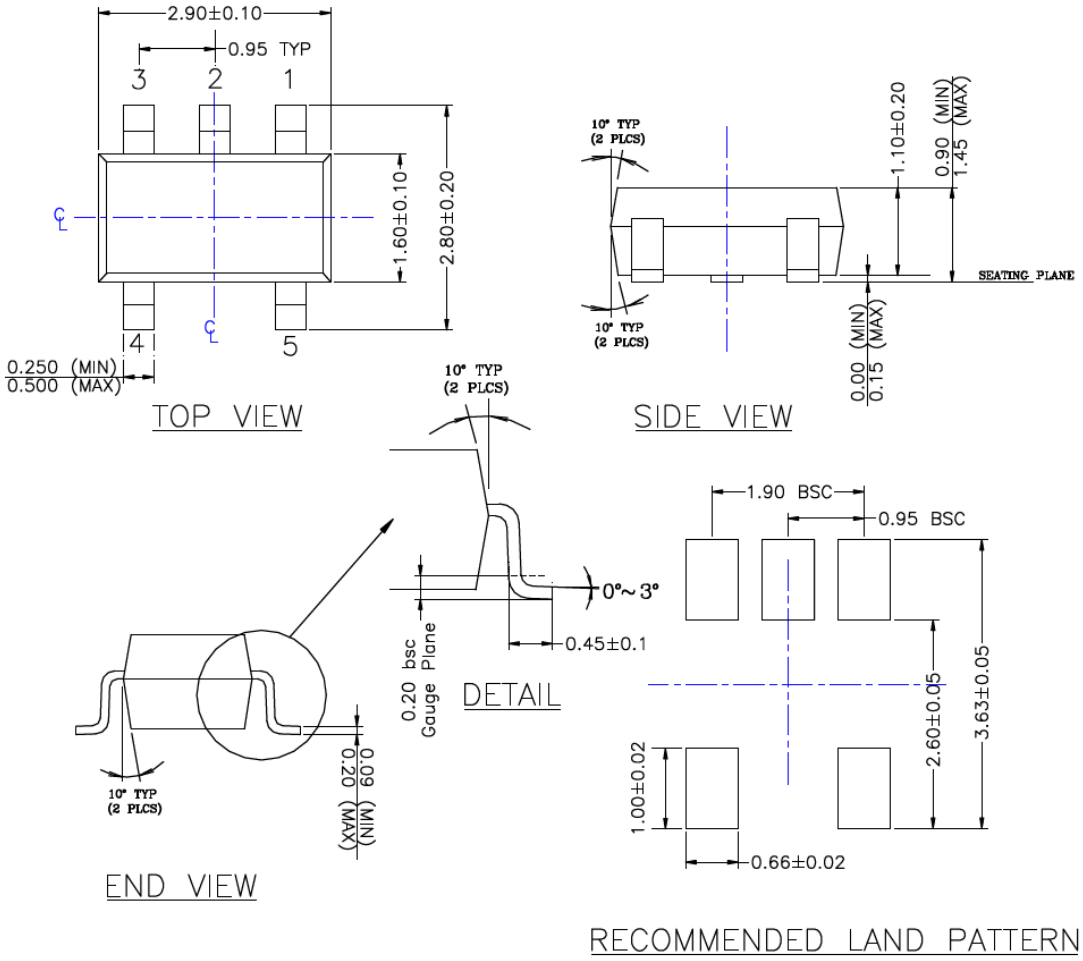
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

5-Pin SOT-23 Package Outline and Recommended Land Pattern

TITLE
5 LEAD SOT23 PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOT23-5LD-PL-1	UNIT	MM



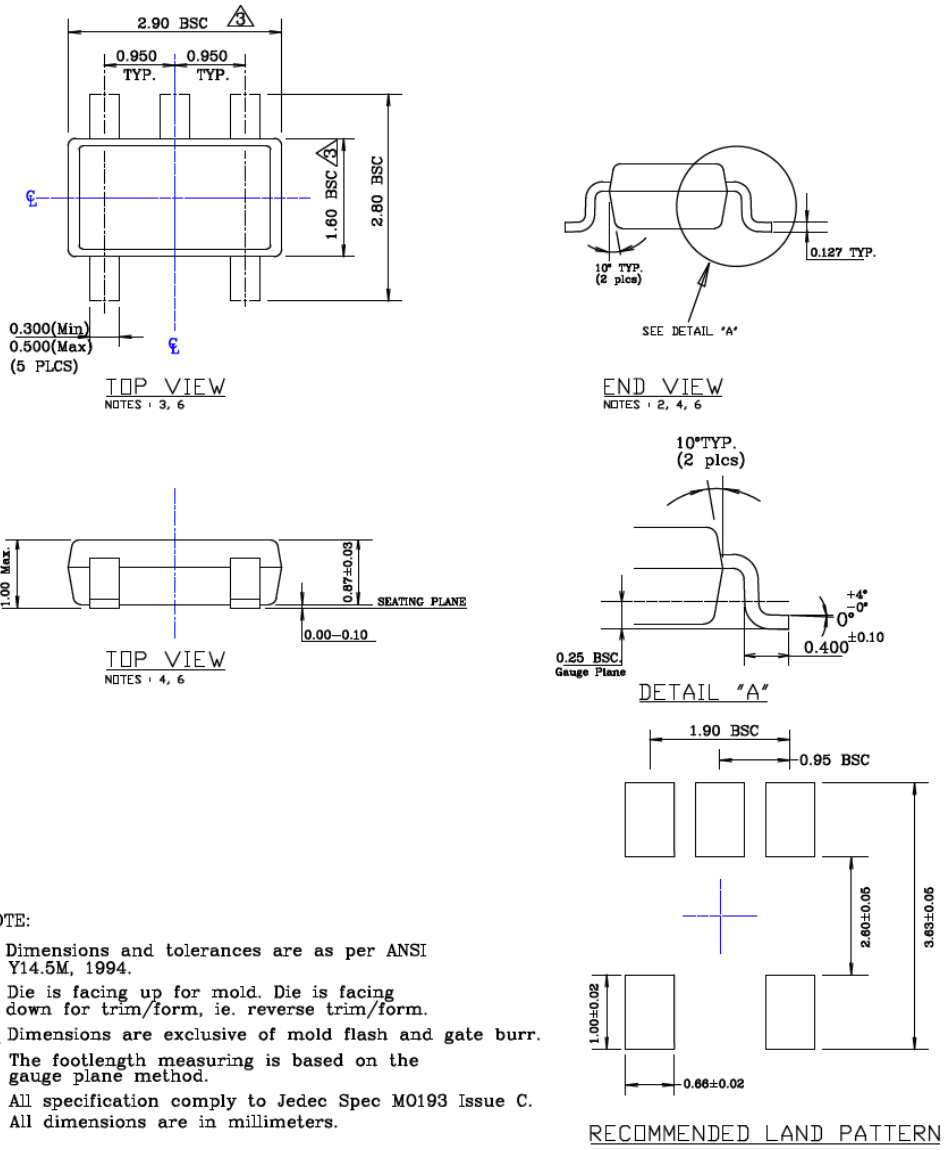
NOTE:
1. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & BURR.
2. PACKAGE OUTLINE INCLUSIVE OF SOLER PLATING.
3. DIMENSION AND TOLERANCE PER ANSI Y14.5M, 1982.
4. FOOT LENGTH MEASUREMENT BASED ON GAUGE PLANE METHOD.
5. DIE FACES UP FOR MOLD, AND FACES DOWN FOR TRIM/FORM.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

5-Pin TSOT-23 Package Outline and Recommended Land Pattern

TITLE
5 LEAD TSOT PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	TSOT-5LD-PL-1	UNIT	MM



NOTE:

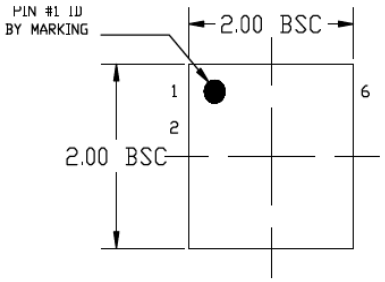
1. Dimensions and tolerances are as per ANSI Y14.5M, 1994.
2. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specification comply to Jedec Spec MO193 Issue C.
6. All dimensions are in millimeters.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

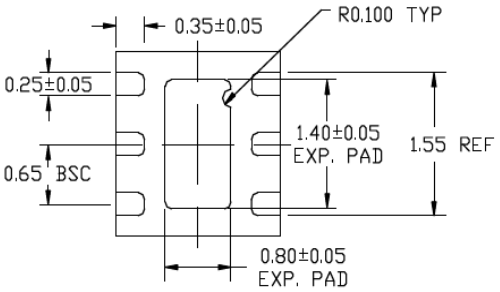
6-Pin 2 mm x 2 mm VDFN Package Outline and Recommended Land Pattern

TITLE
6 LEAD DFN 2x2mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

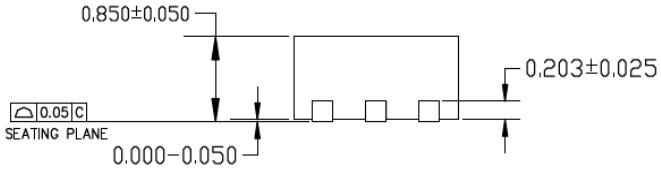
DRAWING #	DFN22-6LD-PL-1	UNIT	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



END VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.3M IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.60x0.40 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (November 2016)

- Converted Micrel document MIC5255 to Microchip data sheet DS20005661A.
- Minor text changes throughout.
- Leaded parts (B-designated) removed from data sheet.
- Voltage options updated in the Product Identification System section.
- DFN package naming updated to Microchip-standard VDFN package.
- Typical ground current updated on Page 1.
- Equation values on Page 12 updated.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	-	X.X	X	XX	-	X.X
Device		Voltage	Temperature	Package		Media Type

Device:	MIC5255:	150 mA Low Noise µCap CMOS LDO
Voltage: (Note 1, Note 2, Note 3)	2.5 = 2.8 = 3.0 = 3.2 = 3.3 =	2.5V 2.8V 3.0V 3.2V 3.3V
Temperature:	Y =	–40°C to +125°C
Package:	M5 = D5 = ML =	5-Pin SOT-23 5-Pin TSOT-23 6-Pin 2 mm x 2 mm VDFN
Media Type: (Note 4)	TR = TX =	3,000/Reel (5,000/Reel if ML package option) 3,000/Reel with Reverse Pin 1 Orientation

Note 1: Other voltage options available. Contact Microchip for details.

2: The 5-Pin TSOT package (D5) is not available in the 3.2V option.

3: The 6-Pin VDFN package (ML) is not available in 2.5V and 3.2V options.

4: The TX media type is not available with the ML package option.

Examples:

a) MIC5255-2.5YM5-TR: 150 mA Low Noise µCap CMOS LDO, 2.5V Output Voltage, –40°C to +125°C Temp. Range, 5-Pin SOT-23, 3,000/Reel

b) MIC5255-2.5YD5-TX: 150 mA Low Noise µCap CMOS LDO, 2.5V Output Voltage, –40°C to +125°C Temp. Range, 5-Pin TSOT-23, 3,000/Reel with Reverse Pin 1 Orientation

c) MIC5255-2.8YML-TR: 150 mA Low Noise µCap CMOS LDO, 2.8V Output Voltage, –40°C to +125°C Temp. Range, 6-Pin VDFN, 5,000/Reel

d) MIC5255-3.0YD5-TX: 150 mA Low Noise µCap CMOS LDO, 3.0V Output Voltage, –40°C to +125°C Temp. Range, 5-Pin TSOT-23, 3,000/Reel with Reverse Pin 1 Orientation

e) MIC5255-3.2YM5-TR: 150 mA Low Noise µCap CMOS LDO, 3.2V Output Voltage, –40°C to +125°C Temp. Range, 5-Pin SOT-23, 3,000/Reel

f) MIC5255-3.3YML-TR: 150 mA Low Noise µCap CMOS LDO, 3.3V Output Voltage, –40°C to +125°C Temp. Range, 6-Pin VDFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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