## 1.0 ELECTRICAL CHARACTERISTICS

### Maximum Ratings*

$V_{DD}$.....7.0V
All inputs and outputs w.r.t. $V_{SS}$ ..... -0.3V to $V_{DD}$ +0.3V
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-65°C to +125°C
Maximum Junction Temperature ..... 150°C
ESD protection on all pins (HBM) .....> 4 kV

***Notice:** Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, and $V_{REF}$ = 5V. Full differential input configuration (Figure 1-5) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB}$ = -40°C to +85°C **(Note 7)**. Conversion speed ($F_{SAMPLE}$) is 100 ksps with $F_{CLK}$ = 17*$F_{SAMPLE}$

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Conversion Rate** | | | | | | |
| Maximum Sampling Frequency | $F_{SAMPLE}$ | — | — | 100 | ksps | See $F_{CLK}$ specifications **(Note 8)** |
| Conversion Time | $t_{CONV}$ | | 13 | | CLK periods | |
| Acquisition Time | $t_{ACQ}$ | | 1.5 | | CLK periods | |
| **DC Accuracy** | | | | | | |
| Resolution | | | 12 data bits + sign | | bits | |
| Integral Nonlinearity | INL | —<br>— | ±0.5<br>±1 | ±1<br>±2 | LSB | MCP3301-B<br>MCP3301-C |
| Differential Nonlinearity | DNL | — | ±0.5 | ±1 | LSB | Monotonic with no missing codes over temperature |
| Positive Gain Error | | -3 | -0.75 | +2 | LSB | |
| Negative Gain Error | | -3 | -0.5 | +2 | LSB | |
| Offset Error | | -3 | +3 | +6 | LSB | |
| **Dynamic Performance** | | | | | | |
| Total Harmonic Distortion | THD | — | -91 | — | dB | **Note 3** |
| Signal to Noise and Distortion | SINAD | — | 78 | — | dB | **Note 3** |
| Spurious Free Dynamic Range | SFDR | — | 92 | — | dB | **Note 3** |
| Common-Mode Rejection | CMRR | — | 79 | — | dB | **Note 6** |
| Power Supply Rejection | PSR | — | 74 | — | dB | **Note 4** |

**Note 1:** This specification is established by characterization and not 100% tested.
**2:** See characterization graphs that relate converter performance to $V_{REF}$ level.
**3:** $V_{IN}$ = 0.1V to 4.9V @ 1 kHz.
**4:** $V_{DD}$ = 5V DC ±500 $mV_{P-P}$ @ 1 kHz, see test circuit Figure 1-4.
**5:** Maximum clock frequency specification must be met.
**6:** $V_{REF}$ = 400 mV, $V_{IN}$ = 0.1V to 4.9V @ 1 kHz
**7:** MSOP devices are only specified at 25°C and +85°C.
**8:** For slow sample rates, see **Section 5.2.1 "Maintaining Minimum Clock Speed"** for limitations on clock frequency.
**9:** 4.5V - 5.5V is the supply voltage range for specified performance


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## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, and $V_{REF}$ = 5V. Full differential input configuration (Figure 1-5) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB}$ = -40°C to +85°C **(Note 7)**. Conversion speed ($F_{SAMPLE}$) is 100 ksps with $F_{CLK}$ = 17*$F_{SAMPLE}$

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Reference Input** | | | | | | |
| Voltage Range | | 0.4 | — | $V_{DD}$ | V | **Note 2** |
| Current Drain | | —<br>— | 100<br>0.001 | 150<br>3 | µA<br>µA | <br>$\overline{CS}$ = $V_{DD}$ = 5V |
| **Analog Inputs** | | | | | | |
| Full-Scale Input Span | IN(+)-IN(-) | -$V_{REF}$ | — | $V_{REF}$ | V | |
| Absolute Input Voltage | IN(+) | -0.3 | — | $V_{DD}$ + 0.3 | V | |
| | IN(-) | -0.3 | — | $V_{DD}$ + 0.3 | V | |
| Leakage Current | | — | 0.001 | ±1 | µA | |
| Switch Resistance | $R_S$ | — | 1 | — | kΩ | See Figure 5-3 |
| Sample Capacitor | $C_{SAMPLE}$ | — | 25 | — | pF | See Figure 5-3 |
| **Digital Input/Output** | | | | | | |
| Data Coding Format | | Binary Two's Complement | | | | |
| High Level Input Voltage | $V_{IH}$ | 0.7 $V_{DD}$ | — | — | V | |
| Low Level Input Voltage | $V_{IL}$ | — | — | 0.3 $V_{DD}$ | V | |
| High Level Output Voltage | $V_{OH}$ | 4.1 | — | — | V | $I_{OH}$ = -1 mA, $V_{DD}$ = 4.5V |
| Low Level Output Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1 mA, $V_{DD}$ = 4.5V |
| Input Leakage Current | $I_{LI}$ | -10 | — | 10 | µA | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ |
| Output Leakage Current | $I_{LO}$ | -10 | — | 10 | µA | $V_{OUT}$ = $V_{SS}$ or $V_{DD}$ |
| Pin Capacitance | $C_{IN}$, $C_{OUT}$ | — | — | 10 | pF | $T_{AMB}$ = 25°C, f = 1 MHz, **Note 1** |
| **Timing Specifications** | | | | | | |
| Clock Frequency **(Note 8)** | $F_{CLK}$ | 0.085 | — | 1.7 | MHz | $V_{DD}$ = 5V, $F_{SAMPLE}$ = 100 ksps |
| Clock High Time | $t_{HI}$ | 275 | — | — | ns | **Note 5** |
| Clock Low Time | $t_{LO}$ | 275 | — | — | ns | **Note 5** |
| $\overline{CS}$ Fall To First Rising CLK Edge | $t_{SUCS}$ | 100 | — | — | ns | |
| CLK Fall To Output Data Valid | $t_{DO}$ | — | — | 125<br>200 | ns<br>ns | $V_{DD}$ = 5V, see Figure 1-2<br>$V_{DD}$ = 2.7V, see Figure 1-2 |
| CLK Fall To Output Enable | $t_{EN}$ | — | — | 125<br>200 | ns<br>ns | $V_{DD}$ = 5V, see Figure 1-2<br>$V_{DD}$ = 2.7V, see Figure 1-2 |
| $\overline{CS}$ Rise To Output Disable | $t_{DIS}$ | — | — | 100 | ns | See test circuits, Figure 1-2; **Note 1** |
| $\overline{CS}$ Disable Time | $t_{CSH}$ | 580 | — | — | ns | |
| $D_{OUT}$ Rise Time | $t_R$ | — | — | 100 | ns | See test circuits, Figure 1-2; **Note 1** |
| $D_{OUT}$ Fall Time | $t_F$ | — | — | 100 | ns | See test circuits, Figure 1-2; **Note 1** |

**Note 1:** This specification is established by characterization and not 100% tested.
**2:** See characterization graphs that relate converter performance to $V_{REF}$ level.
**3:** $V_{IN}$ = 0.1V to 4.9V @ 1 kHz.
**4:** $V_{DD}$ = 5V DC ±500 $mV_{P-P}$ @ 1 kHz, see test circuit Figure 1-4.
**5:** Maximum clock frequency specification must be met.
**6:** $V_{REF}$ = 400 mV, $V_{IN}$ = 0.1V to 4.9V @ 1 kHz
**7:** MSOP devices are only specified at 25°C and +85°C.
**8:** For slow sample rates, see **Section 5.2.1 "Maintaining Minimum Clock Speed"** for limitations on clock frequency.
**9:** 4.5V - 5.5V is the supply voltage range for specified performance



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## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, and $V_{REF}$ = 5V. Full differential input configuration (Figure 1-5) with fixed common mode voltage of 2.5V. All parameters apply over temperature with $T_{AMB}$ = -40°C to +85°C **(Note 7)**. Conversion speed ($F_{SAMPLE}$) is 100 ksps with $F_{CLK}$ = 17*$F_{SAMPLE}$

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Power Requirements** | | | | | | |
| Operating Voltage | $V_{DD}$ | 4.5 | — | 5.5 | V | **Note 9** |
| Operating Current | $I_{DD}$ | —<br>— | 300<br>200 | 450<br>— | µA | $V_{DD}$ , $V_{REF}$ = 5V, $D_{OUT}$ unloaded<br>$V_{DD}$, $V_{REF}$ = 2.7V, $D_{OUT}$ unloaded |
| Standby Current | $I_{DDS}$ | — | 0.05 | 1 | µA | $\overline{CS}$ = $V_{DD}$ = 5.0V |
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistance** | | | | | | |
| Thermal Resistance, 8L-MSOP | $\theta_{JA}$ | — | 206 | — | °C/W | |
| Thermal Resistance, 8L-PDIP | $\theta_{JA}$ | — | 85 | — | °C/W | |
| Thermal Resistance, 8L-SOIC | $\theta_{JA}$ | — | 163 | — | °C/W | |

**Note 1:** This specification is established by characterization and not 100% tested.
**2:** See characterization graphs that relate converter performance to $V_{REF}$ level.
**3:** $V_{IN}$ = 0.1V to 4.9V @ 1 kHz.
**4:** $V_{DD}$ = 5V DC ±500 $mV_{P-P}$ @ 1 kHz, see test circuit Figure 1-4.
**5:** Maximum clock frequency specification must be met.
**6:** $V_{REF}$ = 400 mV, $V_{IN}$ = 0.1V to 4.9V @ 1 kHz
**7:** MSOP devices are only specified at 25°C and +85°C.
**8:** For slow sample rates, see **Section 5.2.1 "Maintaining Minimum Clock Speed"** for limitations on clock frequency.
**9:** 4.5V - 5.5V is the supply voltage range for specified performance

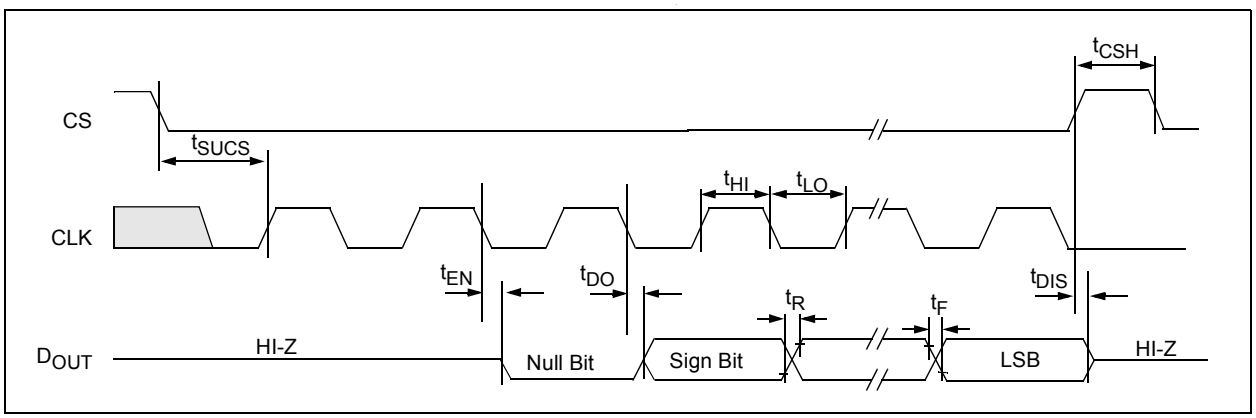


***FIGURE 1-1:*** *Timing Parameters.*


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## 1.1 Test Circuits

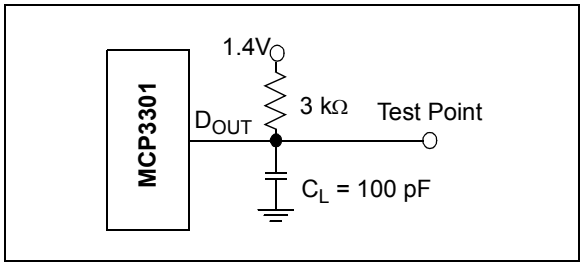
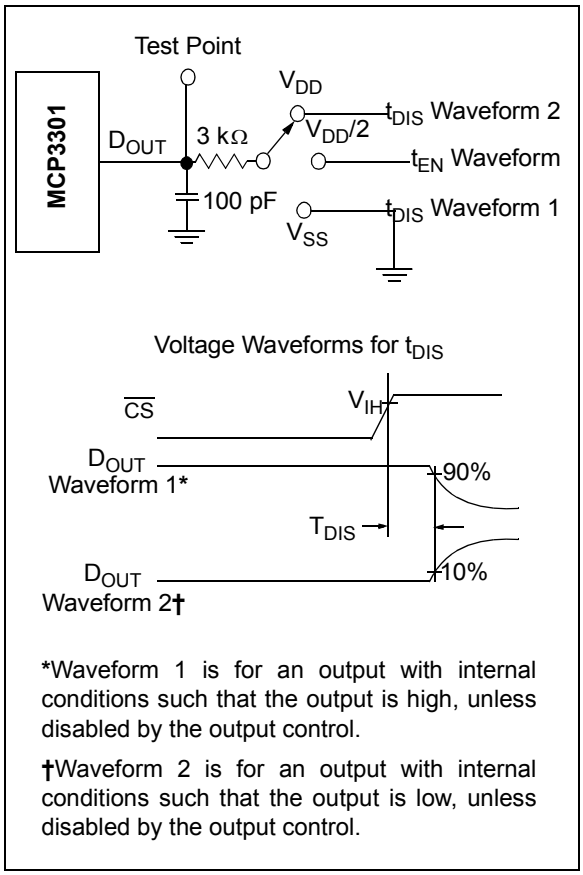



***FIGURE 1-2:*** *Load Circuit for $t_R$, $t_F$, $t_{DO}$.*




*Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.

†Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.

***FIGURE 1-3:*** *Load Circuit for $T_{DIS}$ and $T_{EN}$.*

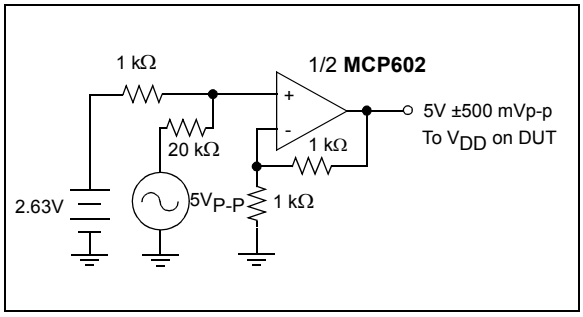



***FIGURE 1-4:*** *Power Supply Sensitivity Test Circuit (PSRR).*

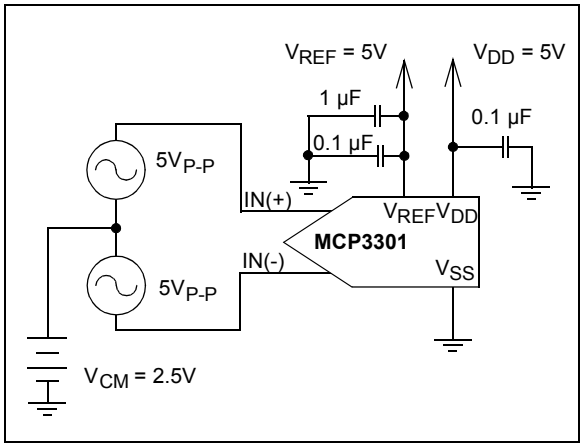



***FIGURE 1-5:*** *Full Differential Test Configuration Example.*

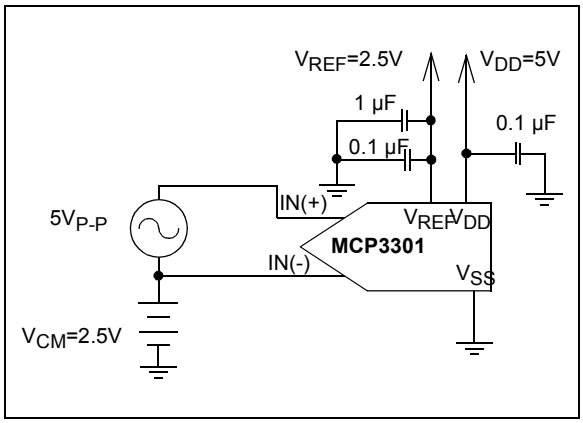



***FIGURE 1-6:*** *Pseudo Differential Test Configuration Example.*



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## 2.0 TYPICAL PERFORMANCE CURVES

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |
|---|---|

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

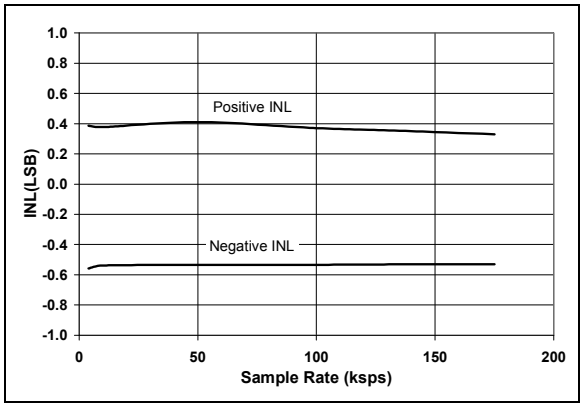


***FIGURE 2-1:*** *Integral Nonlinearity (INL) vs. Sample Rate.*

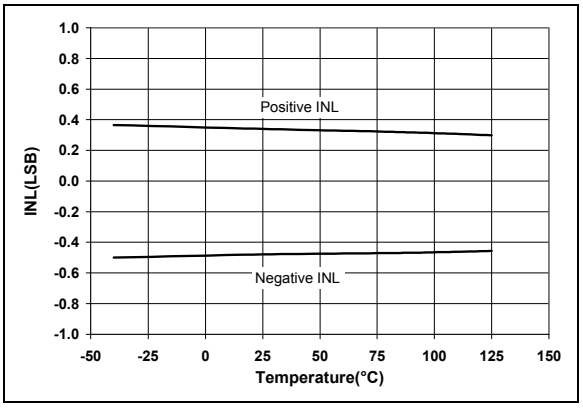


***FIGURE 2-4:*** *Integral Nonlinearity (INL) vs. Temperature.*

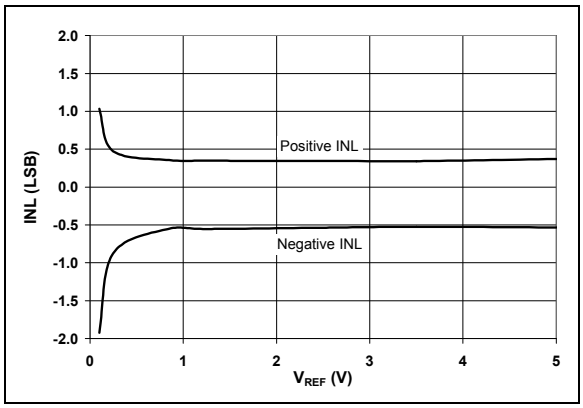


***FIGURE 2-2:*** *Integral Nonlinearity (INL) vs. $V_{REF}$.*

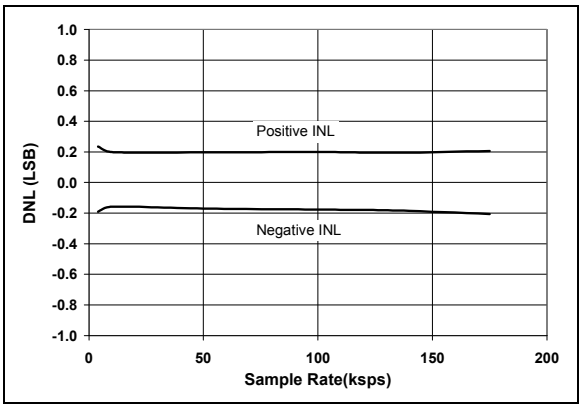


***FIGURE 2-5:*** *Differential Nonlinearity (DNL) vs. Sample Rate.*

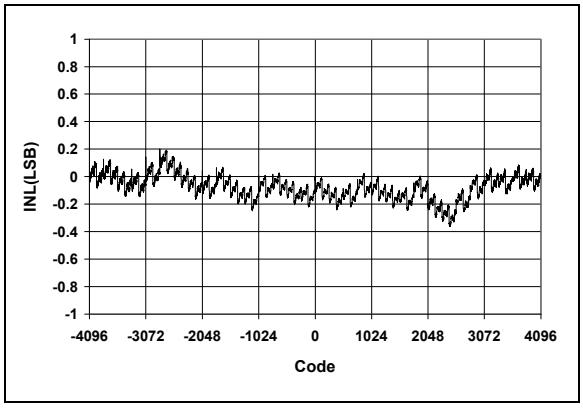


***FIGURE 2-3:*** *Integral Nonlinearity (INL) vs. Code (Representative Part).*

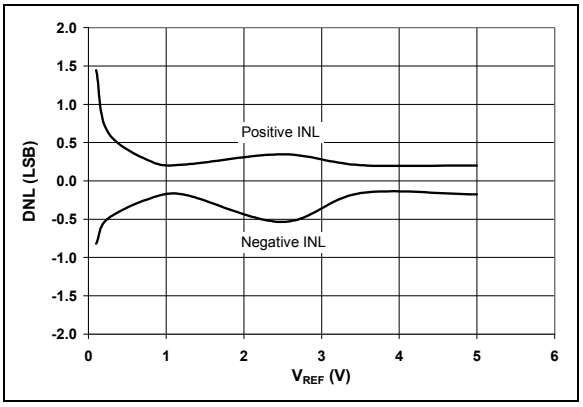


***FIGURE 2-6:*** *Differential Nonlinearity (DNL) vs. $V_{REF}$.*


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**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

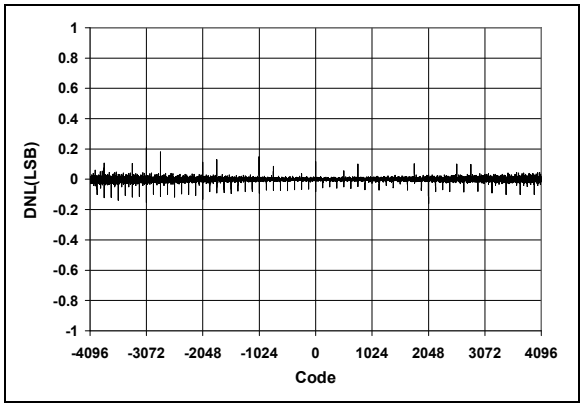


***FIGURE 2-7:*** *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

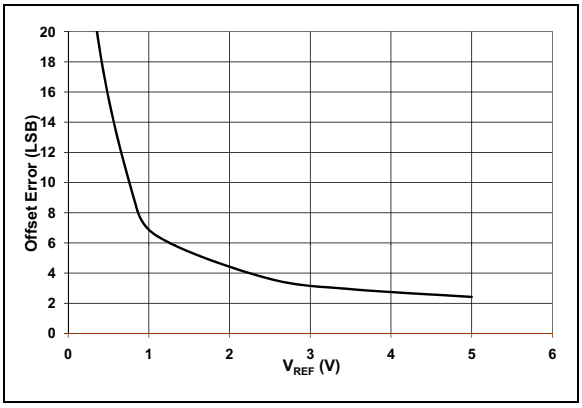


***FIGURE 2-10:*** *Offset Error vs. $V_{REF}$.*

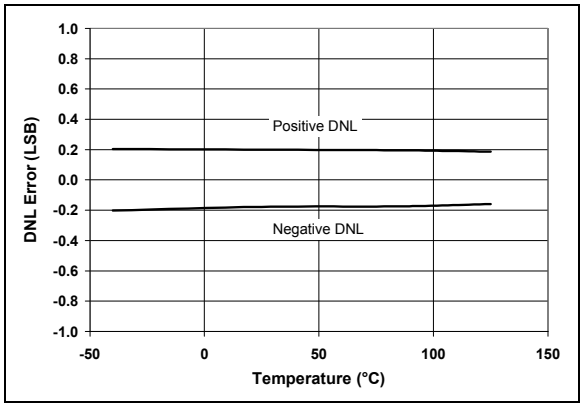


***FIGURE 2-8:*** *Differential Nonlinearity (DNL) vs. Temperature.*

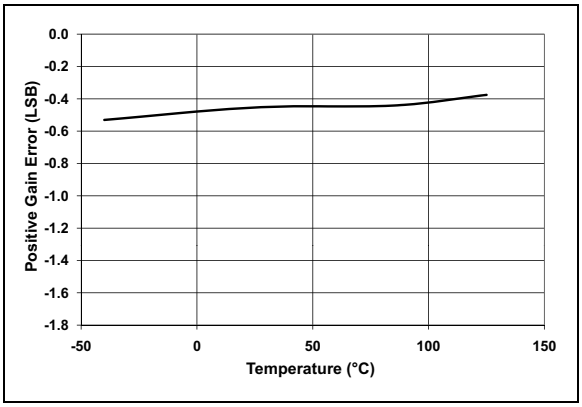


***FIGURE 2-11:*** *Positive Gain Error vs. Temperature.*

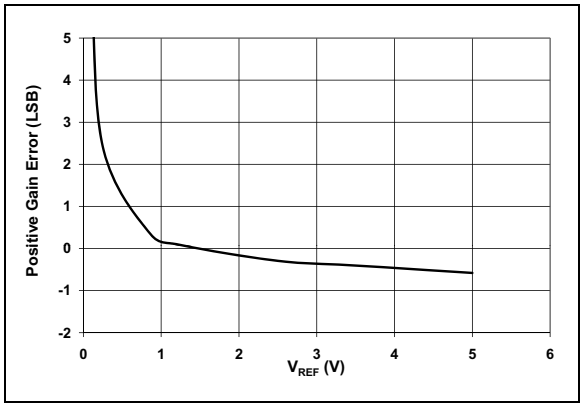


***FIGURE 2-9:*** *Positive Gain Error vs. $V_{REF}$.*

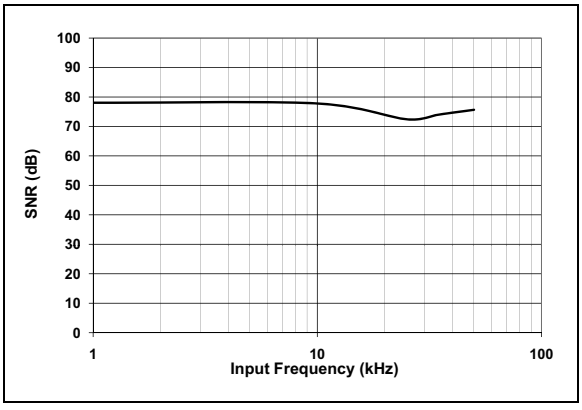


***FIGURE 2-12:*** *Signal to Noise Ratio (SNR) vs. Input Frequency.*



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**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

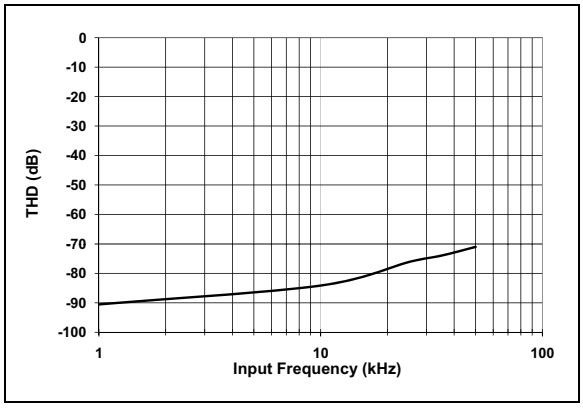


***FIGURE 2-13:*** *Total Harmonic Distortion (THD) vs. Input Frequency.*

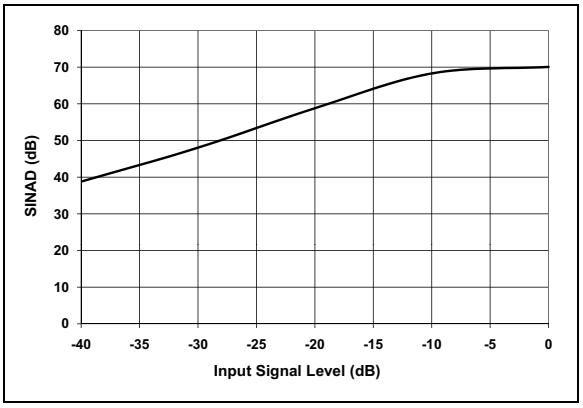


***FIGURE 2-16:*** *Signal to Noise and Distortion (SINAD) vs. Input Signal Level.*

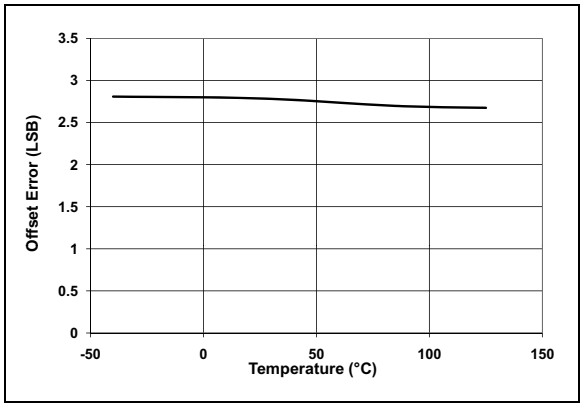


***FIGURE 2-14:*** *Offset Error vs. Temperature.*

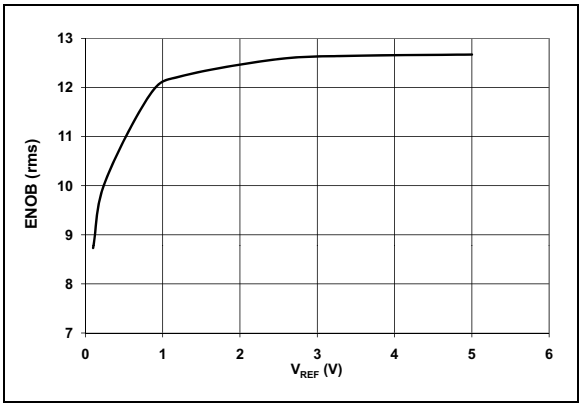


***FIGURE 2-17:*** *Effective Number of Bits (ENOB) vs. $V_{REF}$.*

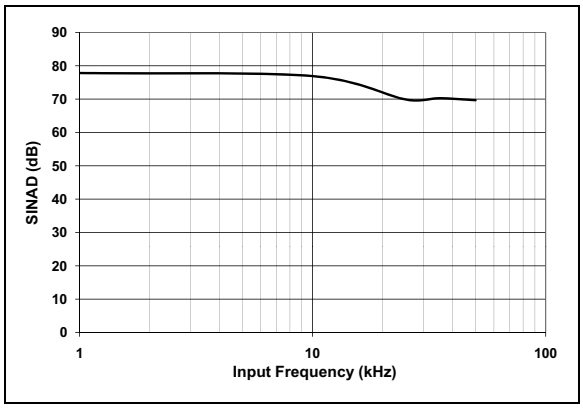


***FIGURE 2-15:*** *Signal to Noise and Distortion (SINAD) vs. Input Frequency.*

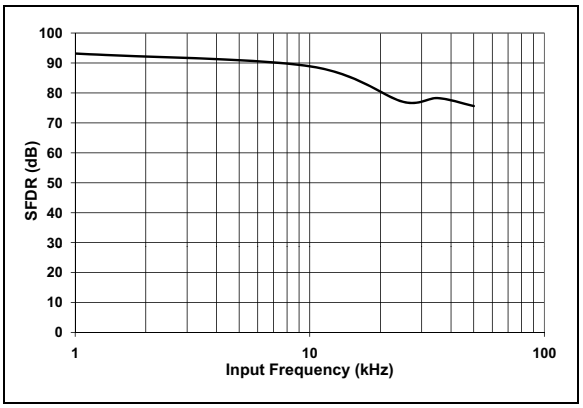


***FIGURE 2-18:*** *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*


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**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

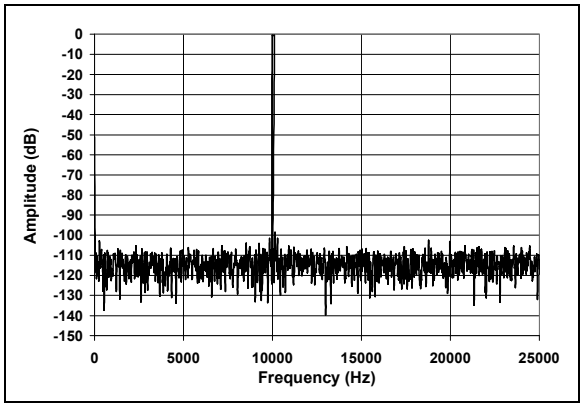


***FIGURE 2-19:*** *Frequency Spectrum of 10 kHz Input (Representative Part).*

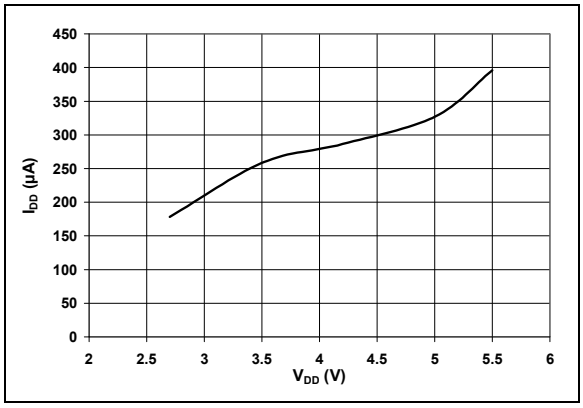


***FIGURE 2-22:*** *$I_{DD}$ vs. $V_{DD}$.*

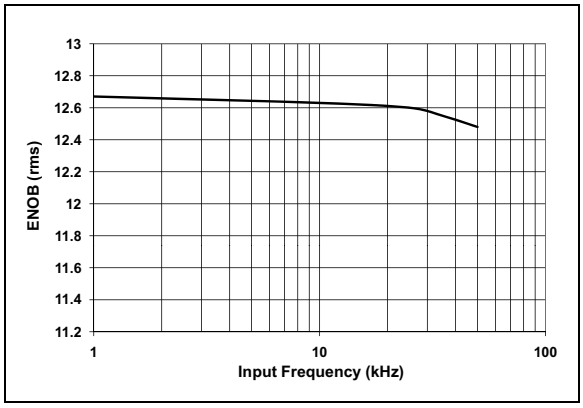


***FIGURE 2-20:*** *Effective Number of Bits (ENOB) vs. Input Frequency.*

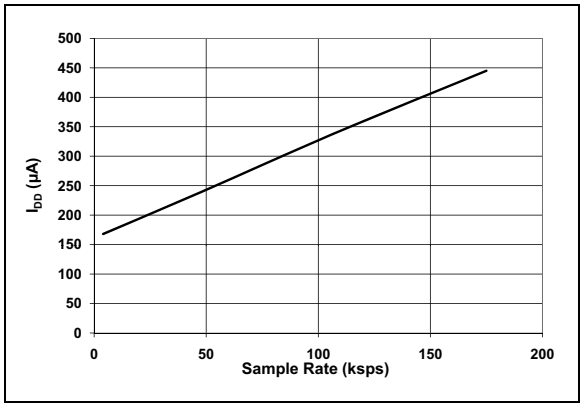


***FIGURE 2-23:*** *$I_{DD}$ vs. Sample Rate.*

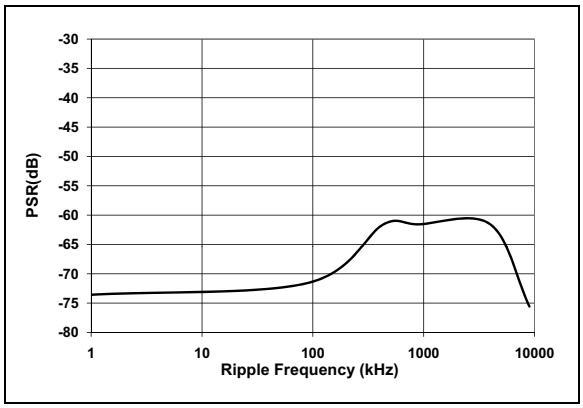


***FIGURE 2-21:*** *Power Supply Rejection (PSR) vs. Ripple Frequency. A 0.1 µF bypass capacitor is connected to the $V_{DD}$ pin.*

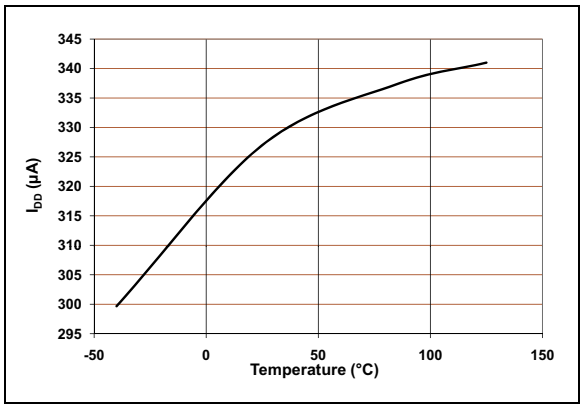


***FIGURE 2-24:*** *$I_{DD}$ vs. Temperature.*



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**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

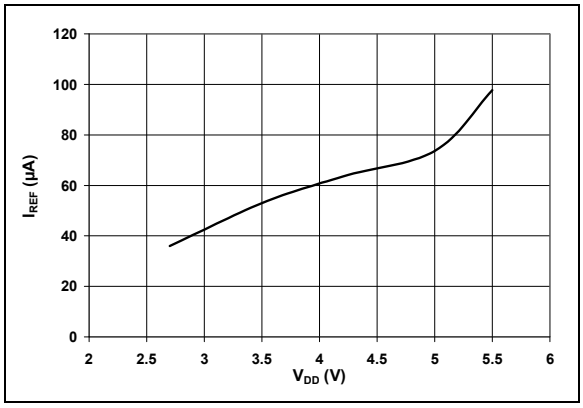


***FIGURE 2-25:*** *$I_{REF}$ vs. $V_{DD}$.*

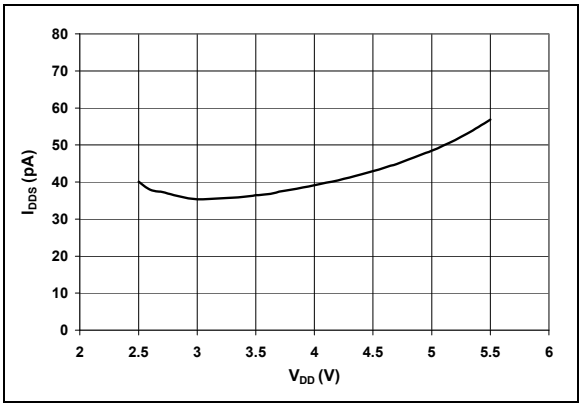


***FIGURE 2-28:*** *$I_{DDS}$ vs. $V_{DD}$.*

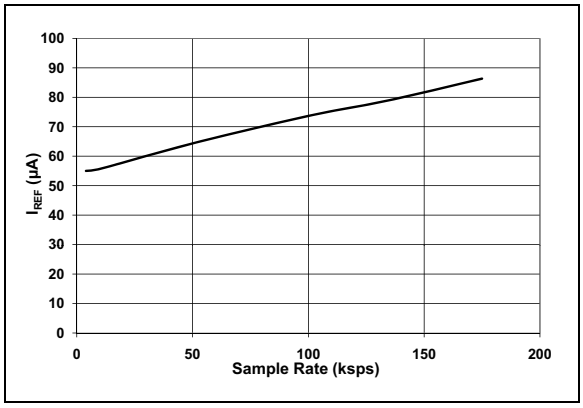


***FIGURE 2-26:*** *$I_{REF}$ vs. Sample Rate.*

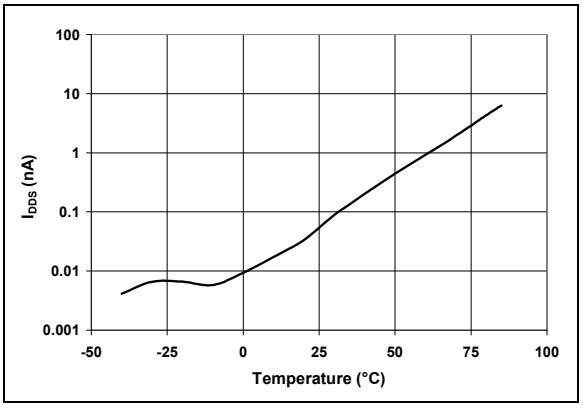


***FIGURE 2-29:*** *$I_{DDS}$ vs. Temperature.*

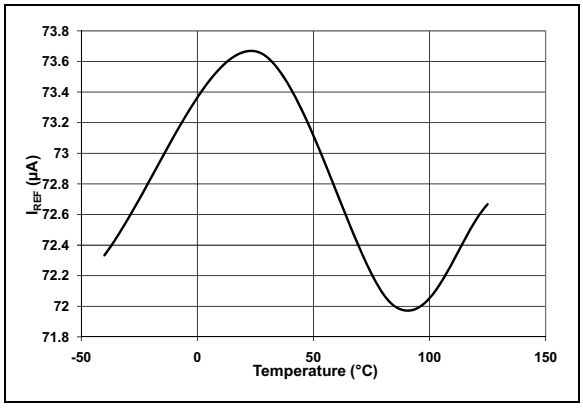


***FIGURE 2-27:*** *$I_{REF}$ vs. Temperature.*

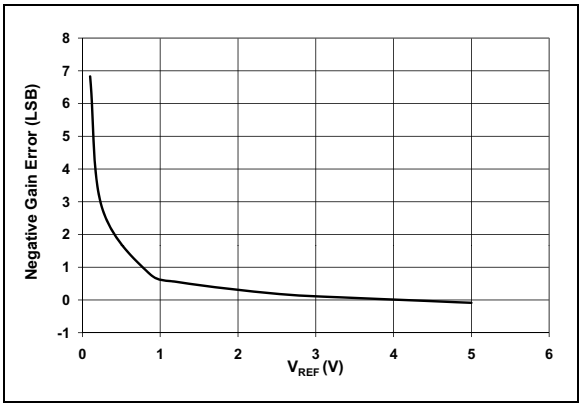


***FIGURE 2-30:*** *Negative Gain Error vs. Reference Voltage.*


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**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, Full differential input configuration, $V_{SS} = 0V$, $F_{SAMPLE} = 100$ ksps, $F_{CLK} = 17*F_{SAMPLE}$, $T_A = 25°C$.

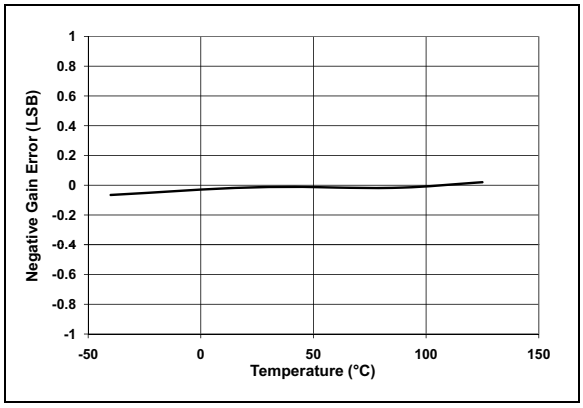


***FIGURE 2-31:*** *Negative Gain Error vs. Temperature.*

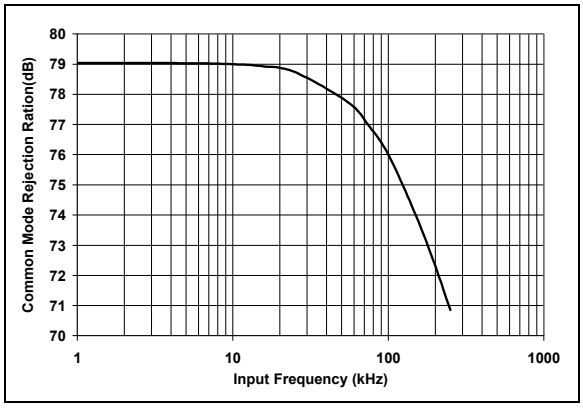


***FIGURE 2-32:*** *Common Mode Rejection vs. Frequency.*



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## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| MSOP, PDIP, SOIC | Name | Function |
|---|---|---|
| 1 | $V_{REF}$ | Reference Voltage Input |
| 2 | IN(+) | Positive Analog Input |
| 3 | IN(-) | Negative Analog Input |
| 4 | $V_{SS}$ | Ground |
| 5 | $\overline{CS}$/SHDN | $\overline{\text{Chip Select}}$ / Shutdown Input |
| 6 | $D_{OUT}$ | Serial Data Out |
| 7 | CLK | Serial Clock |
| 8 | $V_{DD}$ | +4.5V to 5.5V Power Supply |

### 3.1 Voltage Reference ($V_{REF}$)

This input pin provides the reference voltage for the device, which determines the maximum range of the analog input signal and the LSB size.

The LSB size is determined by the equation shown below. As the reference input is reduced, the LSB size is reduced accordingly.

**EQUATION**

$$\text{LSB Size} = \frac{2 \times V_{REF}}{8192}$$

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the accuracy of the ADC conversion results.

### 3.2 Positive Analog Input (IN+)

This pin has an absolute voltage range of $V_{SS}$-0.3V to $V_{DD}$+0.3V. The full scale input range is defined as the absolute value of (IN+) - (IN-).

### 3.3 Negative Analog Input (IN-)

This pin has an absolute voltage range of $V_{SS}$-0.3V to $V_{DD}$+0.3V. The full scale input range is defined as the absolute value of (IN+) - (IN-).

### 3.4 Ground Connection ($V_{SS}$)

If an analog ground plane is available, it is recommended that this device be tied to the analog ground plane in the circuit. See **Section 5.6 "Layout Considerations"**, for more information regarding circuit layout.

### 3.5 $\overline{\text{Chip Select}}$/Shutdown ($\overline{CS}$/SHDN)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low. This pin will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions and cannot be tied low for multiple conversions. See Figure 6-2 for serial communication protocol.

### 3.6 Serial Data Output ($D_{OUT}$)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place. See Figure 6-2 for serial communication protocol.

### 3.7 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion, as well as to clock out each bit of the conversion as it takes place. See **Section 5.2 "Driving the Analog Input"** for constraints on clock speed, and Figure 6-2 for serial communication protocol.

### 3.8 Power Supply ($V_{DD}$)

The device can operate from 2.7V to 5.5V, but the performance is applicable from a 4.5V to 5.5V supply range. To ensure accuracy, a 0.1 µF ceramic bypass capacitor should be placed as close as possible to the pin. See **Section 5.6 "Layout Considerations"** for more information regarding circuit layout.


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## 4.0 DEFINITION OF TERMS

**Bipolar Operation -** This applies to either a differential or single-ended input configuration, where both positive and negative codes are output from the A/D converter. Full bipolar range includes all 8192 codes. For bipolar operation on a single-ended input signal, the A/D converter must be configured to operate in pseudo differential mode.

**Unipolar Operation -** This applies to either a single-ended or differential input signal where only one side of the device transfer is being used. This could be either the positive or negative side, depending on which input (IN+ or IN-) is being used for the DC bias. Full unipolar operation is equivalent to a 12-bit converter.

**Full Differential Operation -** Applying a full differential signal to both the IN(+) and IN(-) inputs is referred to as *full differential operation*. This configuration is described in Figure 1-5.

**Pseudo-Differential Operation -** Applying a single-ended signal to only one of the input channels with a bipolar output is referred to as *pseudo differential operation*. To obtain a bipolar output from a single-ended input signal the inverting input of the A/D converter must be biased above $V_{SS}$. This operation is described in Figure 1-6.

**Integral Nonlinearity -** The maximum deviation from a straight line passing through the endpoints of the bipolar transfer function is defined as the maximum *integral nonlinearity* error. The endpoints of the transfer function are a point 1/2 LSB above the first code transition (0x1000) and 1/2 LSB below the last code transition (0x0FFF).

**Differential Nonlinearity -** The difference between two measured adjacent code transitions and the 1 LSB ideal is defined as *differential nonlinearity*.

**Positive Gain Error -** This is the deviation between the last positive code transition (0x0FFF) and the ideal voltage level of $V_{REF}$-1/2 LSB, after the bipolar offset error has been adjusted out.

**Negative Gain Error -** This is the deviation between the last negative code transition (0X1000) and the ideal voltage level of $-V_{REF}$-1/2 LSB, after the bipolar offset error has been adjusted out.

**Offset Error -** This is the deviation between the first positive code transition (0x0001) and the ideal 1/2 LSB voltage level.

**Acquisition Time -** The *acquisition time* is defined as the time during which the internal sample capacitor is charging. This occurs for 1.5 clock cycles of the external CLK as defined in Figure 6-2.

**Conversion Time -** The *conversion time* occurs immediately after the *acquisition time*. During this time, successive approximation of the input signal occurs as the 13-bit result is being calculated by the internal circuitry. This occurs for 13 clock cycles of the external CLK as defined in Figure 6-2.

**Signal to Noise Ratio -** *Signal to Noise Ratio (SNR)* is defined as the ratio of the signal to noise measured at the output of the converter. The signal is defined as the rms amplitude of the fundamental frequency of the input signal. The noise value is dependant on the device noise as well as the quantization error of the converter and is directly affected by the number of bits in the converter. The *theoretical* signal to noise ratio limit based on quantization error only for an N-bit converter is defined as:

**EQUATION**

$$SNR = (6.02N + 1.76)dB$$

For a 13-bit converter, the theoretical SNR limit is 80.02 dB.

**Total Harmonic Distortion -** *Total Harmonic Distortion (THD)* is the ratio of the rms sum of the harmonics to the fundamental, measured at the output of the converter. For the MCP3301, it is defined using the first 9 harmonics, as shown in the following equation:

**EQUATION**

$$THD(\text{-dB}) = -20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_8^2 + V_9^2}}{V_1^2}$$

Here $V_1$ is the rms amplitude of the fundamental and $V_2$ through $V_9$ are the rms amplitudes of the second through ninth harmonics.

**Signal-to-Noise plus Distortion (SINAD) -** Numerically defined, *SINAD* is the calculated combination of SNR and THD. This number represents the dynamic performance of the converter, including any harmonic distortion.

**EQUATION**

$$SINAD(dB) = 20\log\sqrt{10^{(SNR/10)} + 10^{-(THD/10)}}$$

**Effectlve Number of Bits -** *Effective Number of Bits (ENOB)* states the relative performance of the ADC in terms of its resolution. This term is directly related to SINAD by the following equation:

**EQUATION**

$$ENOB(N) = \frac{SINAD - 1.76}{6.02}$$

For SINAD performance of 78 dB, the effective number of bits is 12.66.

**Spurious Free Dynamic Range -** *Spurious Free Dynamic Range (SFDR)* is the ratio of the rms value of the fundamental to the next largest component in the output spectrum of the ADC. This is, typically, the first harmonic, but could also be a noise peak.



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## 5.0 APPLICATIONS INFORMATION

### 5.1 Conversion Description

The MCP3301MCP3301 A/D converter employs a conventional SAR architecture. With this architecture, the potential between the IN+ and IN- inputs are simultaneously sampled and stored with the internal sample circuits for 1.5 clock cycles ($t_{ACQ}$). Following this sample time, the input hold switches of the converter open and the device uses the collected charge to produce a serial 13-bit binary two's complement output code. This conversion process is driven by the external clock and must include 13 clock cycles, one for each bit. During this process, the most significant bit (MSB) is output first. This bit is the sign bit and indicates whether the IN+ input or the IN- input is at a higher potential.

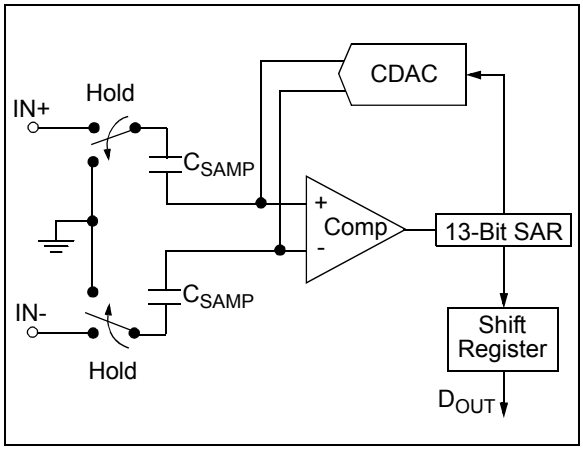


***FIGURE 5-1:*** *Simplified Block Diagram.*

### 5.2 Driving the Analog Input

The analog input of the MCP3301 is easily driven either differentially or single ended. Any signal that is common to the two input channels will be rejected by the common mode rejection of the device. During the charging time of the sample capacitor, a small charging current will be required. For low source impedances, this input can be driven directly. For larger source impedances, a larger acquisition time will be required, due to the RC time constant that includes the source impedance. For the A/D Converter to meet specification, the charge holding capacitor ($C_{SAMPLE}$) must be given enough time to acquire a 13-bit accurate voltage level during the 1.5 clock cycle acquisition period.

An analog input model is shown in Figure 5-3. This model is accurate for an analog input, regardless of whether it is configured as a single-ended input or the IN+ and IN- input in differential mode. In this diagram, it is shown that the source impedance ($R_S$) adds to the internal sampling switch ($R_{SS}$) impedance, directly affecting the time that is required to charge the capacitor ($C_{SAMPLE}$). Consequently, a larger source impedance with no additional acquisition time increases the offset, gain, and integral linearity errors of the conversion. To overcome this, a slower clock speed can be used to allow for the longer charging time. Figure 5-2 shows the maximum clock speed associated with source impedances.

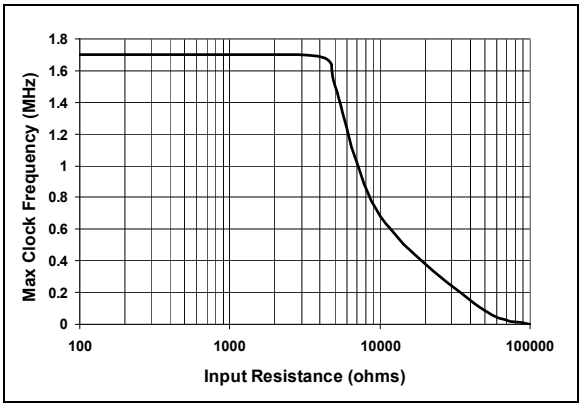


***FIGURE 5-2:*** *Maximum Clock Frequency vs. Source Resistance ($R_S$) to maintain ±1 LSB INL.*


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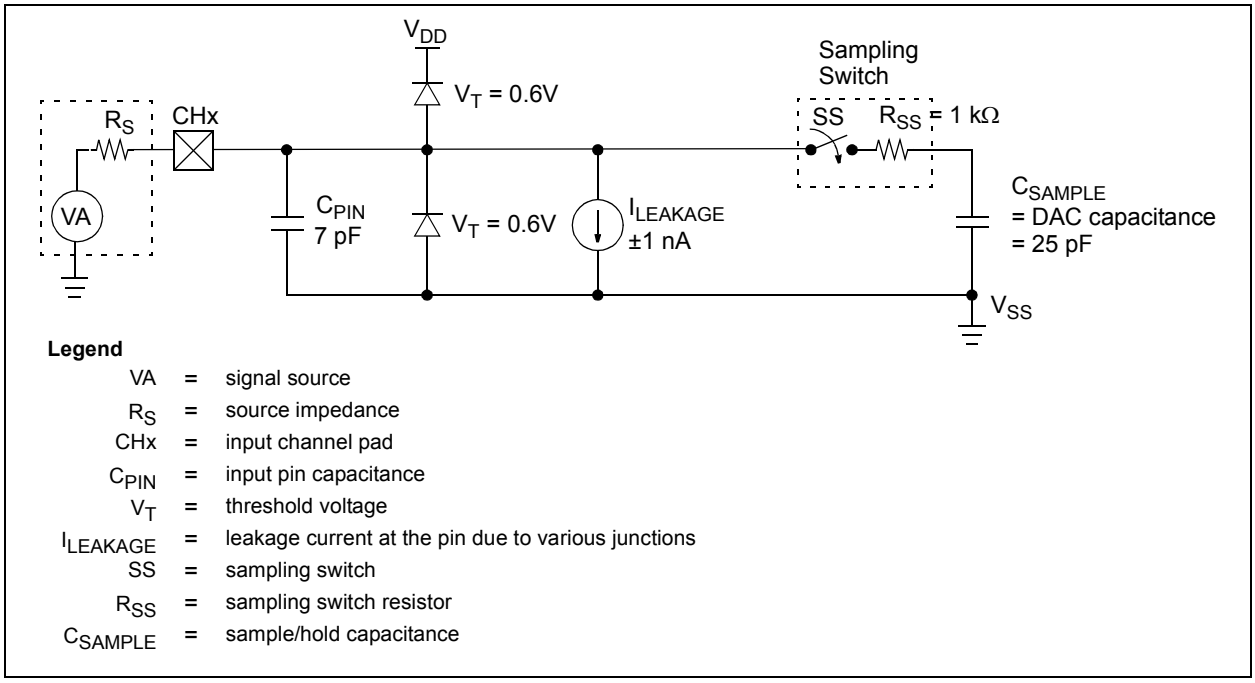


***FIGURE 5-3:*** *Analog Input Model.*

### 5.2.1 MAINTAINING MINIMUM CLOCK SPEED

When the MCP3301 initiates, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. For MCP3301 devices, the recommended minimum clock speed during the conversion cycle ($t_{CONV}$) is 85 kHz. Failure to meet this criteria may introduce linearity errors into the conversion outside the rated specifications. It should be noted that, during the entire conversion cycle, the A/D converter does not have requirements for clock speed or duty cycle, as long as all timing specifications are met.

## 5.3 Biasing Solutions

For pseudo-differential bipolar operation, the biasing circuit shown in Figure 5-4 shows a single-ended input AC coupled to the converter. This configuration will give a digital output range of -4096 to +4095. With the 2.5V reference, the LSB size is equal to 610 µV.

Although the ADC is not production tested with a 2.5V reference as shown, linearity will not change more than 0.1 LSB. See Figure 2-2 and Figure 2-6 for INL and DNL errors versus $V_{REF}$ at $V_{DD}$ = 5V. A trade-off exists between the high-pass corner and the acquisition time. The value of C will need to be quite large in order to bring down the high-pass corner. The value of R needs to be 1 kΩ or less, since higher input impedances require additional acquisition time.

Using the values in Figure 5-4, we have a 100 Hz corner frequency. See Figure 5-2 for the relationship between input impedance and acquisition time.

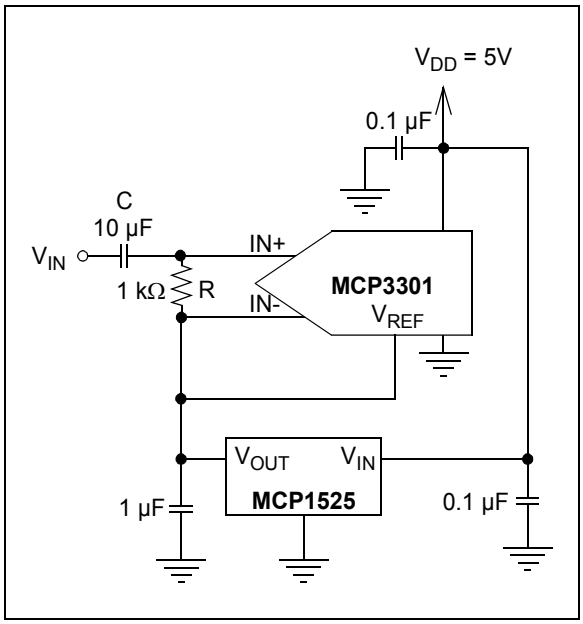


***FIGURE 5-4:*** *Pseudo-differential biasing circuit for bipolar operation.*



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Using an external operational amplifier on the input allows for gain and buffers the input signal from the input to the ADC, allowing for a higher source impedance. This circuit is shown in Figure 5-5.

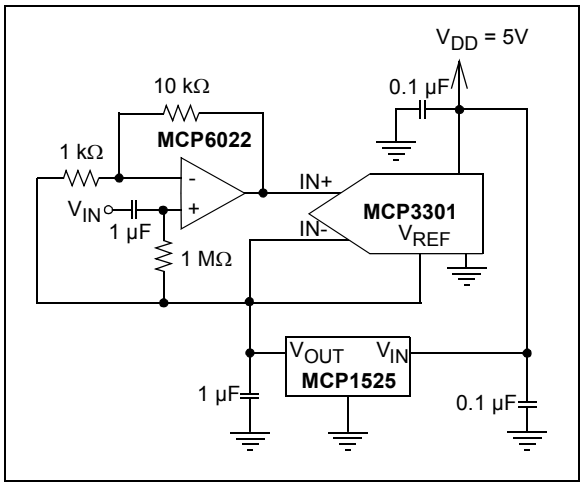


***FIGURE 5-5:*** *Adding an amplifier allows for gain and also buffers the input from any high impedance sources.*

This circuit shows that some headroom will be lost due to the amplifier output not being able to swing all the way to the rail. An example would be for an output swing of 0V to 5V. This limitation can be overcome by supplying a $V_{REF}$ that is slightly less than the common mode voltage. Using a 2.048V reference for the A/D converter, while biasing the input signal at 2.5V solves the problem. This circuit is shown in Figure 5-6.

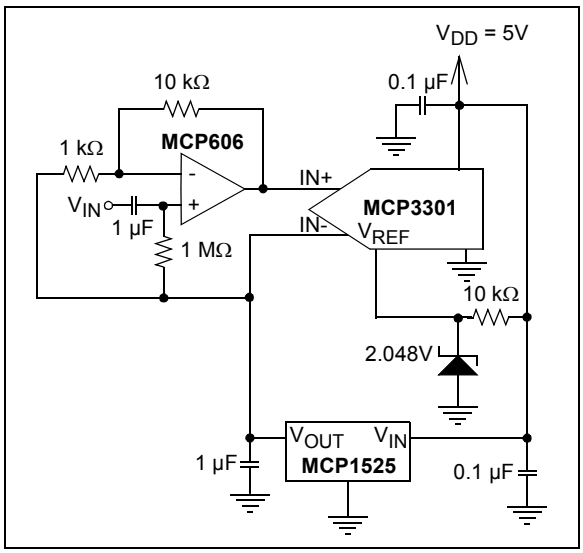


***FIGURE 5-6:*** *Circuit solution to overcome amplifier output swing limitation.*

## 5.4 Common Mode Input Range

The *common mode input range* has no restriction and is equal to the absolute input voltage range: $V_{SS}$ -0.3V to $V_{DD}$ + 0.3V. However, for a given $V_{REF}$, the common mode voltage has a limited swing if the entire range of the A/D converter is to be used. Figure 5-7 and Figure 5-8 show the relationship between $V_{REF}$ and the common mode voltage. A smaller $V_{REF}$ allows for wider flexibility in a common mode voltage. $V_{REF}$ levels, down to 400 mV, exhibit less than 0.1 LSB change in INL and DNL.

For characterization graphs that show this performance relationship, see Figure 2-2 and Figure 2-6.

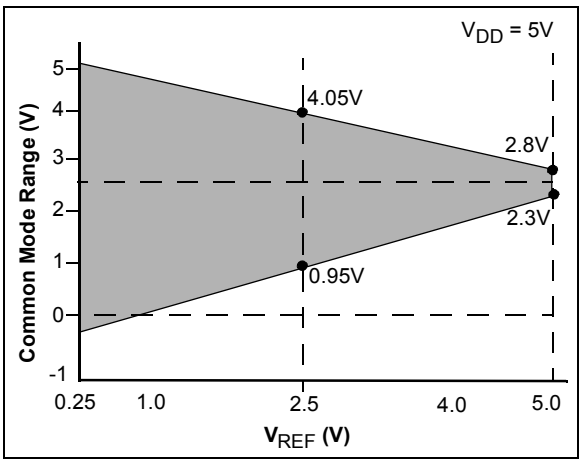


***FIGURE 5-7:*** *Common Mode Range of Full Differential input signal versus $V_{REF}$.*

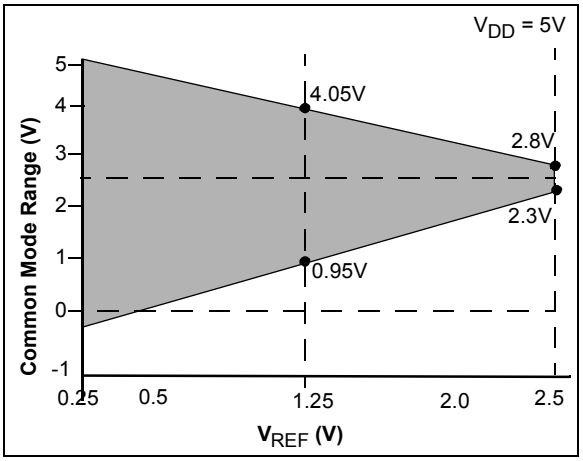


***FIGURE 5-8:*** *Common Mode Range versus $V_{REF}$ for Pseudo Differential Input.*


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## 5.5 Buffering/Filtering the Analog Inputs

Inaccurate conversion results may occur if the signal source for the A/D converter is not a low impedance source. Buffering the input will solve the impedance issue. It is also recommended that an analog filter be used to eliminate any signals that may be aliased back into the conversion results. Using an op amp to drive the analog input of the MCP3301 is illustrated in Figure 5-9. This amplifier provides a low impedance source for the converter input and low pass filter, which eliminates unwanted high frequency noise. Values shown are for a 10 Hz Butterworth Low pass filter.

Low pass (anti-aliasing) filters can be designed using Microchip's interactive FilterLab® software. FilterLab will calculate capacitor and resistor values as well as determine the number of poles that are required for the application. For more information on filtering signals, see AN-699 *"Anti-Aliasing Analog Filters for Data Acquisition Systems*".

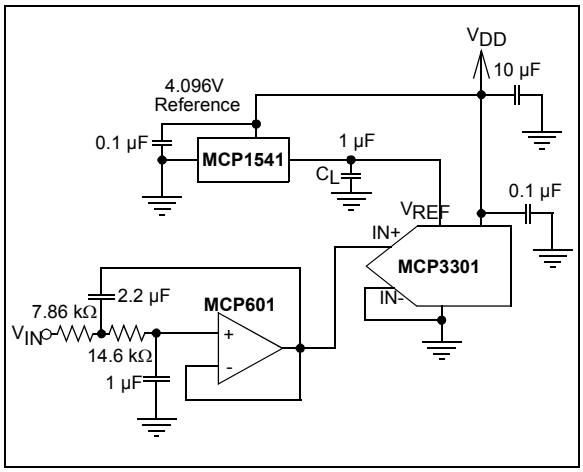


***FIGURE 5-9:*** *The MCP601 Operational Amplifier is used to implement a 2nd order anti-aliasing filter for the signal being converted by the MCP3301.*

## 5.6 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor from $V_{DD}$ to ground should always be used with this device and should be placed as close as possible to the device pin. A bypass capacitor value of 0.1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board with no traces running underneath the device or bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing $V_{DD}$ connections to devices in a "star" configuration can also reduce noise by eliminating current return paths and associated errors (Figure 5-10). For more information on layout tips when using the MCP3301 or other ADC devices, refer to AN-688 *"Layout Tips for 12-Bit A/D Converter Applications"*.

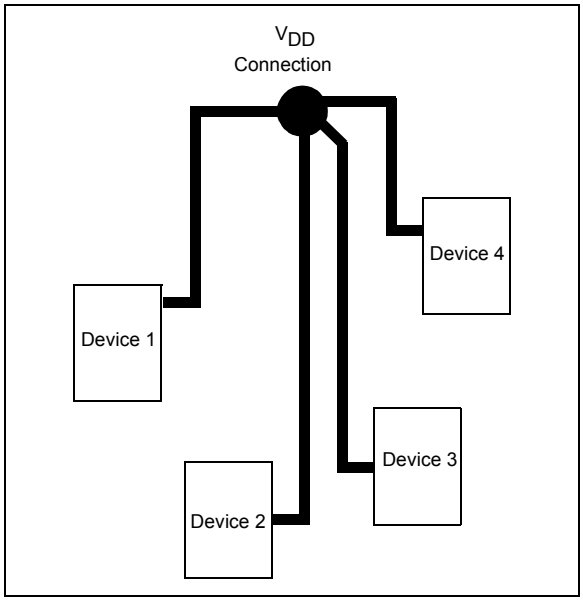


***FIGURE 5-10:*** *$V_{DD}$ traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.MCP3301*



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# 6.0 SERIAL COMMUNICATIONS

## 6.1 Output Code Format

The output code format is a binary two's complement scheme with a leading sign bit that indicates the sign of the output. If the IN+ input is higher than the IN- input, the sign bit will be a zero. If the IN- input is higher, the sign bit will be a '1'.

The diagram shown in Figure 6-1 shows the output code transfer function. In this diagram, the horizontal axis is the analog input voltage and the vertical axis is the output code of the ADC. It shows that when IN+ is equal to IN-, both the sign bit and the data word are zero. As IN+ gets larger, with respect to IN-, the sign bit is a zero and the data word gets larger. The full scale output code is reached at +4095 when the input [(IN+) - (IN-)] reaches $V_{REF}$ - 1 LSB. When IN- is larger than IN+, the two's complement output codes will be seen with the sign bit being a one. Some examples of analog input levels and corresponding output codes are shown in Table 6-1.

**TABLE 6-1: BINARY TWO'S COMPLEMENT OUTPUT CODE EXAMPLES.**

| Analog Input Levels | | Sign Bit | Binary Data | Decimal DATA |
|---|---|---|---|---|
| Full Scale Positive | (IN+)-(IN-) = $V_{REF}$-1 LSB | 0 | 1111 1111 1111 | +4095 |
| | (IN+)-(IN-) = $V_{REF}$-2 LSB | 0 | 1111 1111 1110 | +4094 |
| | IN+ = (IN-) +2 LSB | 0 | 0000 0000 0010 | +2 |
| | IN+ = (IN-) +1 LSB | 0 | 0000 0000 0001 | +1 |
| | IN+ = IN- | 0 | 0000 0000 0000 | 0 |
| | IN+ = (IN-) - 1 LSB | 1 | 1111 1111 1111 | -1 |
| | IN+ = (IN-) - 2 LSB | 1 | 1111 1111 1110 | -2 |
| | $IN^+ - IN^- = V_{REF}$+1 LSB | 1 | 0000 0000 0001 | -4095 |
| Full Scale Negative | $IN^+ - IN^- = -V_{REF}$ | 1 | 0000 0000 0000 | -4096 |


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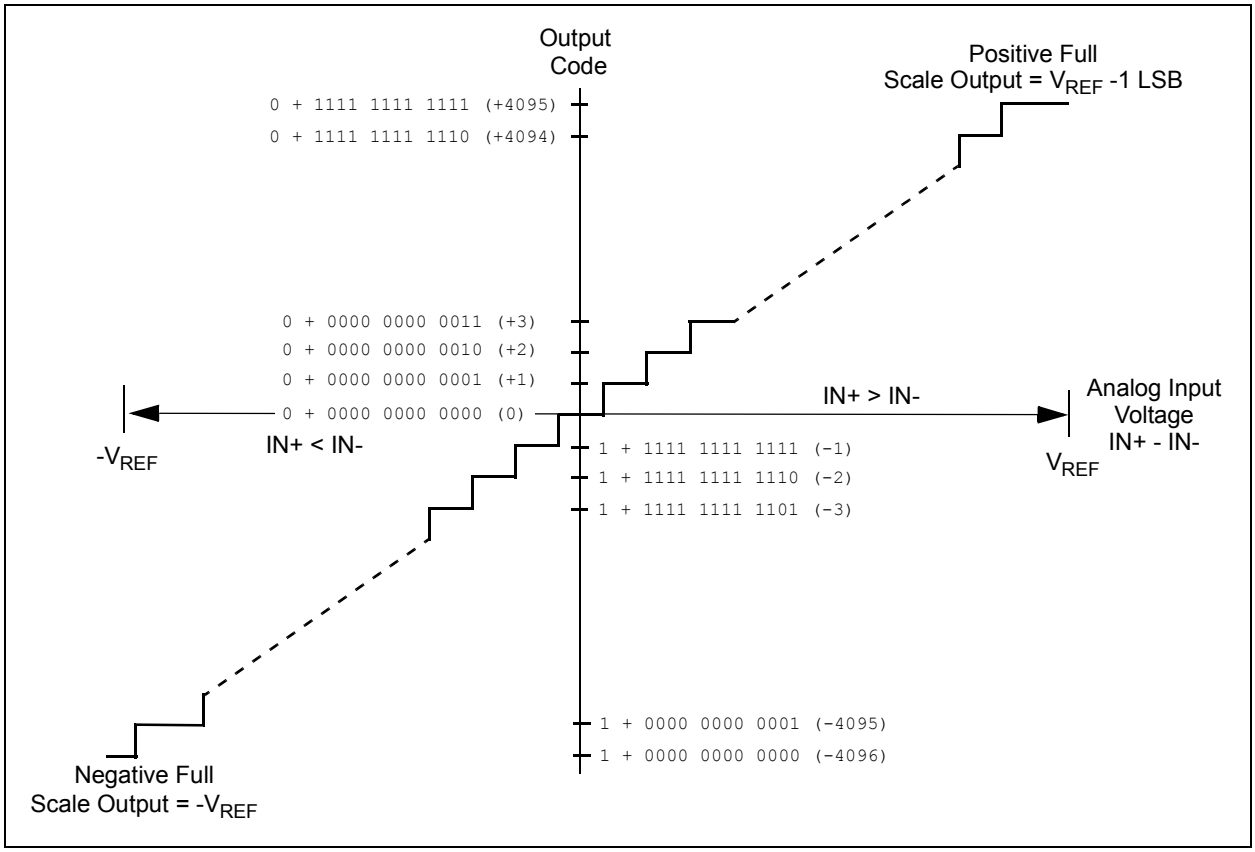


***FIGURE 6-1:*** *Output Code Transfer Function.*



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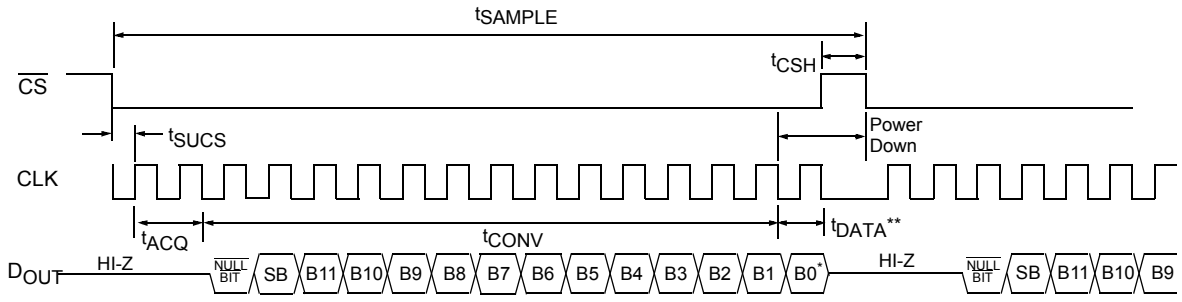
## 6.2 Communicating with the MCP3301

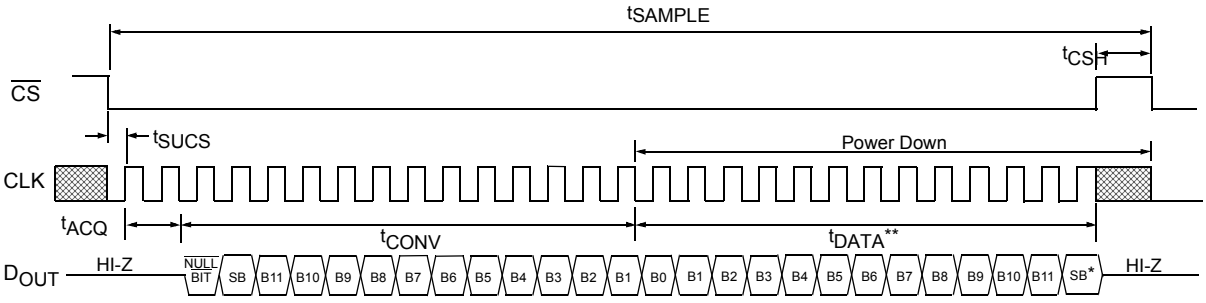
Communication with the device is completed using a standard SPI compatible serial interface. Initiating communication with the MCP3301 begins with the $\overline{CS}$ going low. If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The device will begin to sample the analog input on the first rising edge of CLK after $\overline{CS}$ goes low. The sample period will end in the falling edge of the second clock, at which time the device will output a low null bit. The next 13 clocks will output the result of the conversion with the sign bit first, followed by the 12 remaining data bits, as shown in Figure 6-2. Data is always output from the device on the falling edge of the clock. If all 13 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, the device will output the conversion result LSB first, as shown in Figure 6-3. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.




* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the ADC will output LSB first data, followed by zeros indefinitely. See Figure 6-2 below.

** $t_{DATA}$: during this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

***FIGURE 6-2:*** *Communication with MCP3301 (MSB first Format).*




* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the ADC will output zeros indefinitely.

** $t_{DATA}$: during this time, the bias current and the comparator power down and the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

***FIGURE 6-3:*** *Communication with MCP3301 (LSB first Format).*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## 6.3 Using the MCP3301 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to clock out eight bits at a time. Using a hardware SPI port with the MCP3301 is very easy because each conversion requires 16 clocks. For example, Figure 6-4 and Figure 6-5 show how the MCP3301 can be interfaced to a microcontroller with a standard SPI port. Since the MCP3301 always clocks data out on the falling edge of clock, the MCU SPI port must be configured to match this operation. SPI Mode 0,0 (clock idles low) and SPI Mode 1,1 (clock idles high) are both compatible with the MCP3301. Figure 6-4 depicts the operation shown in SPI Mode 0,0, which requires that the CLK from the microcontroller idles in the 'low' state. As shown in the diagram, the sign bit is clocked out of the ADC on the falling edge of the third clock pulse, followed by the remaining 12 data bits (MSB first). Once the first eight clocks have been sent to the device, the microcontroller's receive buffer will contain two unknown bits (for the first two clocks, the output is high impedance), followed by the null bit, the sign bit and the highest order four bits of the conversion. After the second eight clocks have been sent to the device, the MCU receive register will contain the lowest order 8 data bits. Notice that, on the falling edge of clock 16, the ADC has begun to shift out LSB first data.

Figure 6-5 shows the same scenario in SPI Mode 1,1, which requires that the clock idles in the high state. As with mode 0,0, the ADC outputs data on the falling edge of the clock and the MCU latches data from the ADC in on the rising edge of the clock.

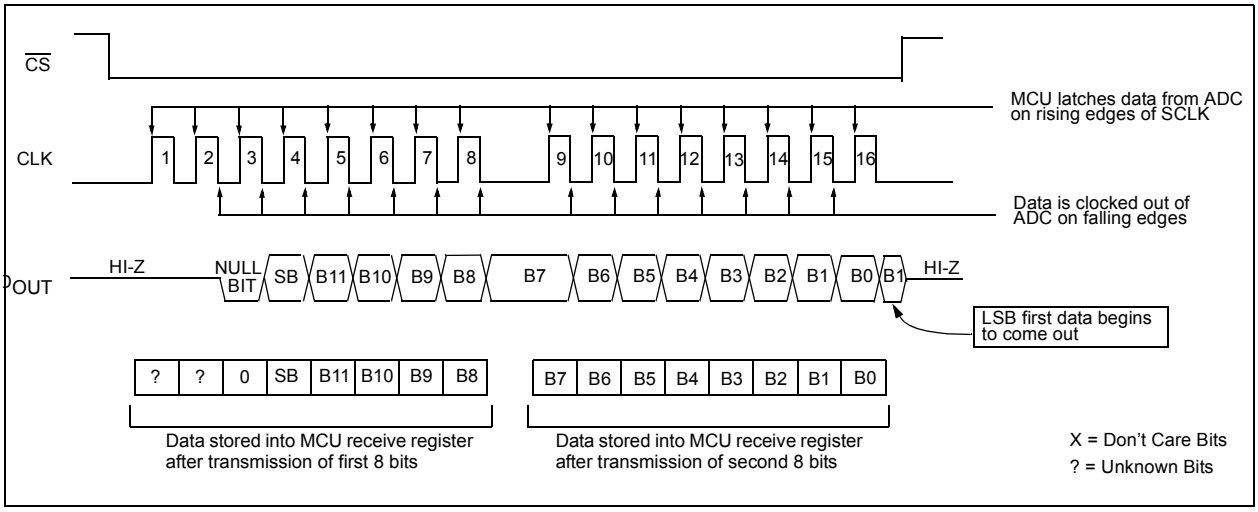


***FIGURE 6-4:*** *SPI Communication with the MCP3301 using 8-bit segments (Mode 0,0: SCLK idles low).*

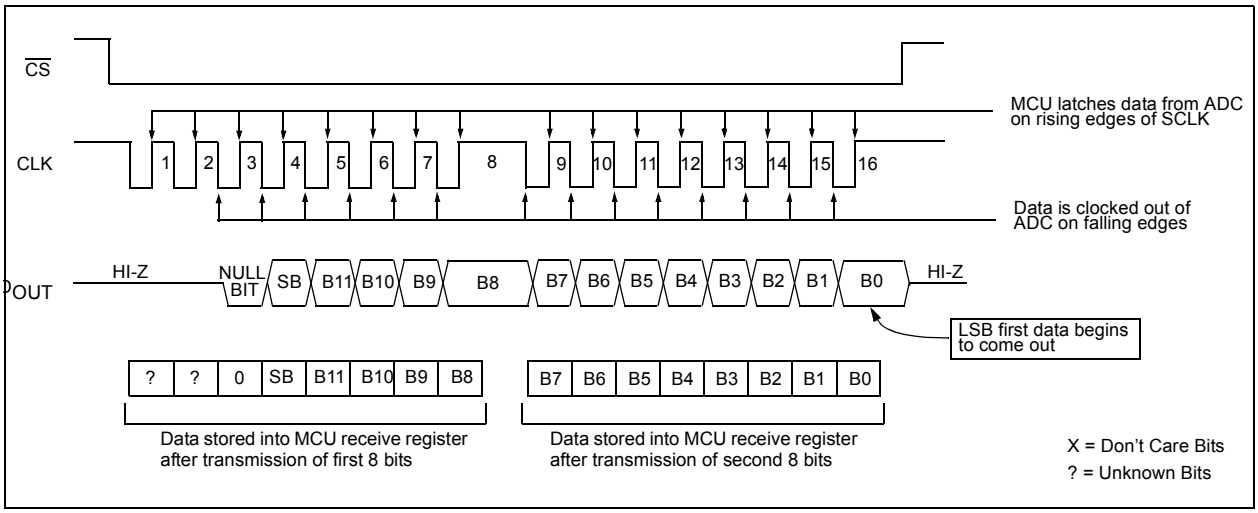


***FIGURE 6-5:*** *SPI Communication with the MCP3301 using 8-bit segments (Mode 1,1: SCLK idles high).*



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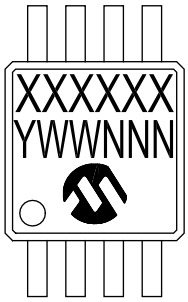
## 7.0 PACKAGING INFORMATION

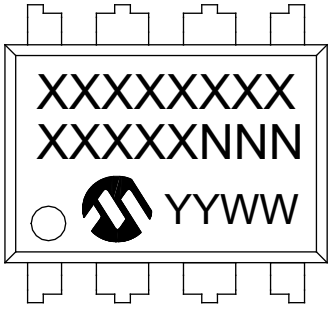
### 7.1 Package Marking Information

8-Lead MSOP (3x3 mm)

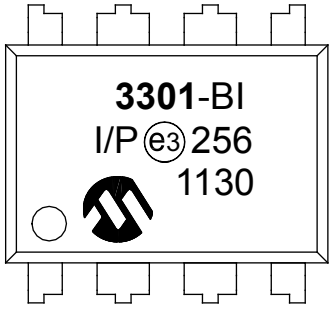



Example

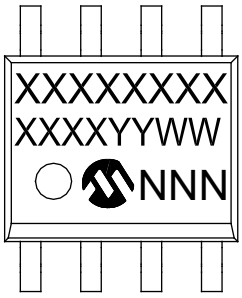
8-Lead PDIP (300 mil)



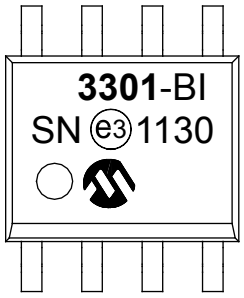

Example




8-Lead SOIC (3.90 mm)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.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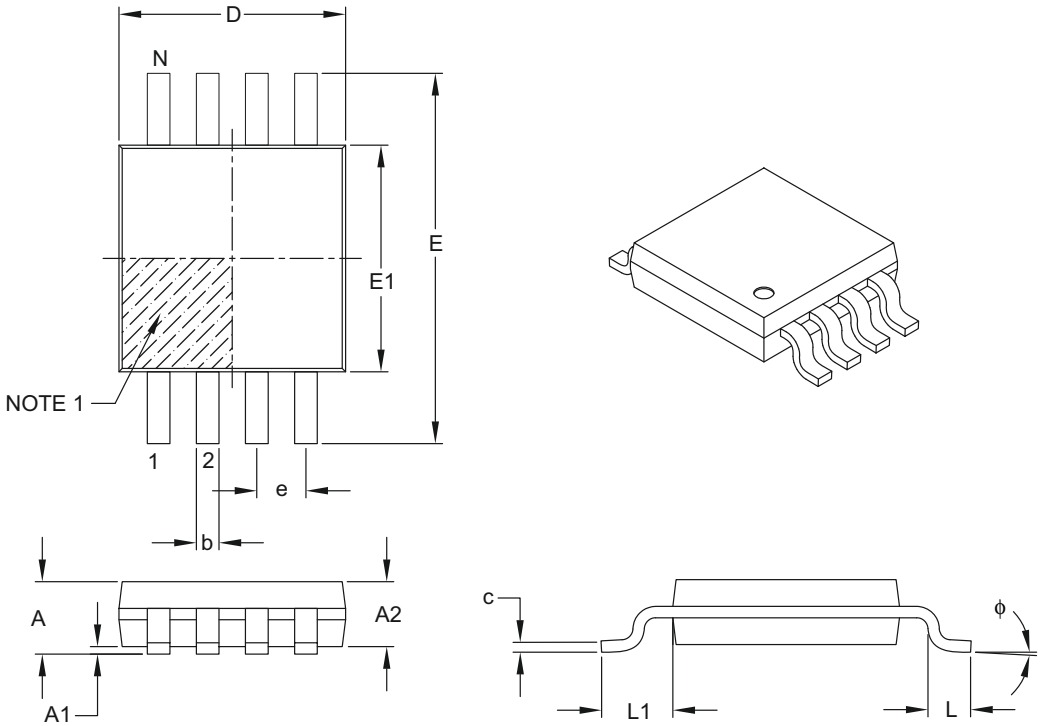
## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 1.10 |
| Molded Package Thickness | A2 | 0.75 | 0.85 | 0.95 |
| Standoff | A1 | 0.00 | – | 0.15 |
| Overall Width | E | | 4.90 BSC | |
| Molded Package Width | E1 | | 3.00 BSC | |
| Overall Length | D | | 3.00 BSC | |
| Foot Length | L | 0.40 | 0.60 | 0.80 |
| Footprint | L1 | | 0.95 REF | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.08 | – | 0.23 |
| Lead Width | b | 0.22 | – | 0.40 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B



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## 8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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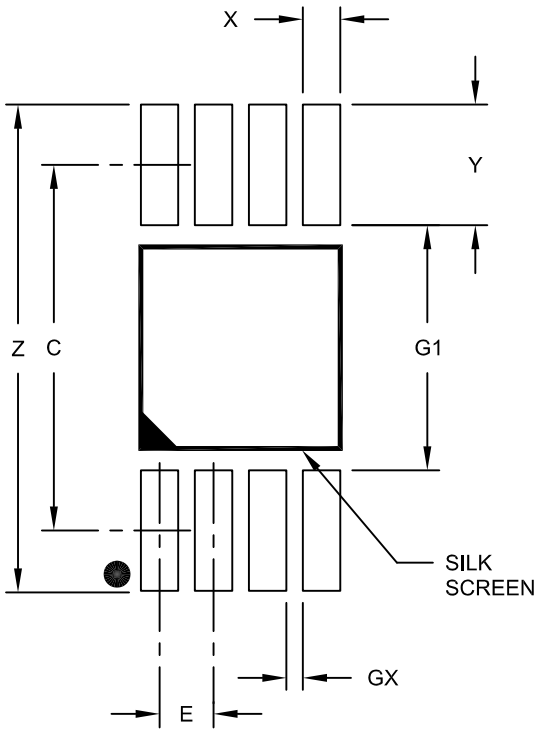


RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Contact Pad Spacing | C | | 4.40 | |
| Overall Width | Z | | | 5.85 |
| Contact Pad Width (X8) | X1 | | | 0.45 |
| Contact Pad Length (X8) | Y1 | | | 1.45 |
| Distance Between Pads | G1 | 2.95 | | |
| Distance Between Pads | GX | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A


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## 8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

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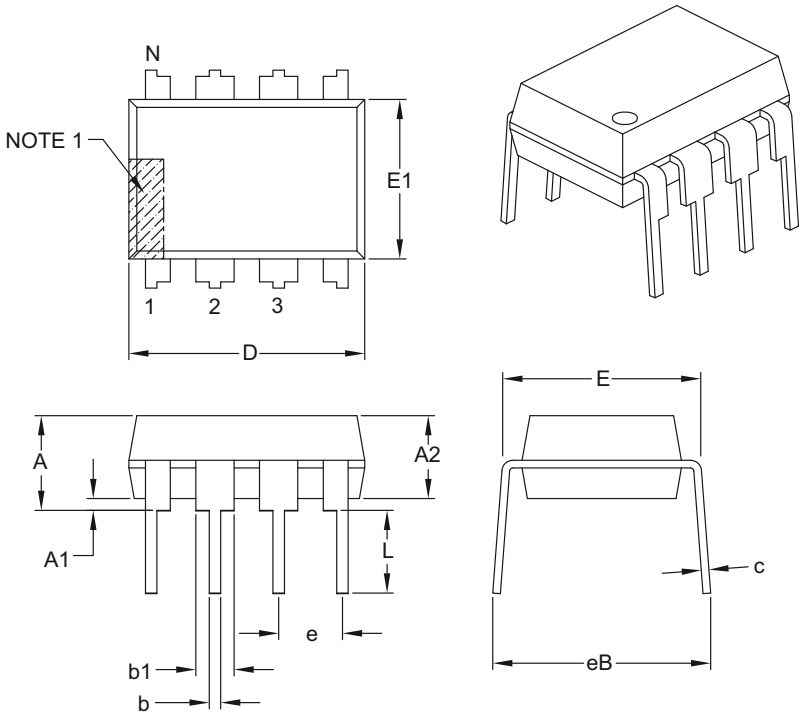


| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .348 | .365 | .400 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B



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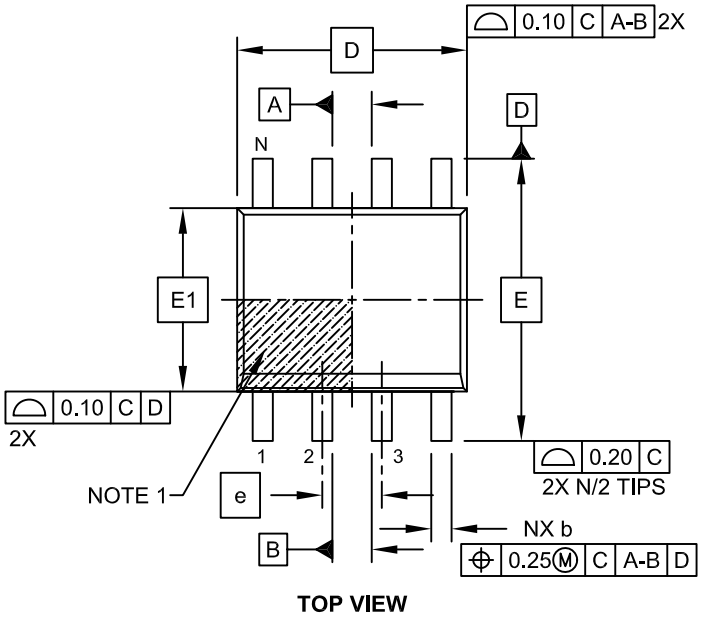
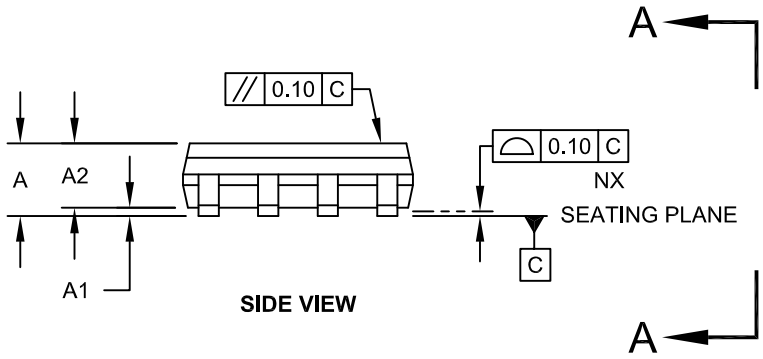
### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

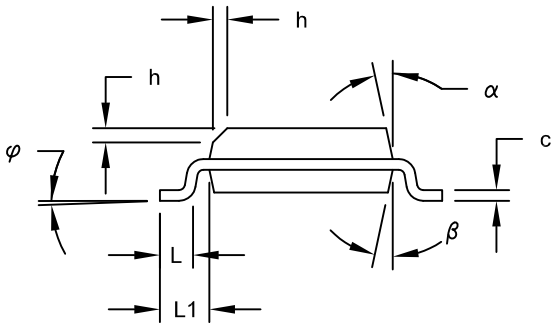
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW




VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2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## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

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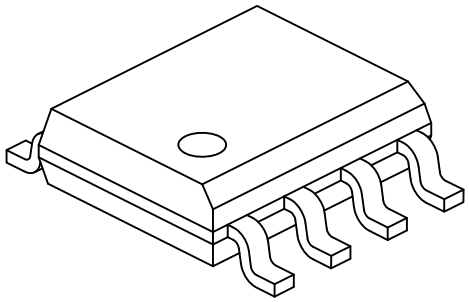

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 8 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | | 6.00 BSC | |
| Molded Package Width | E1 | | 3.90 BSC | |
| Overall Length | D | | 4.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.04 REF | |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2



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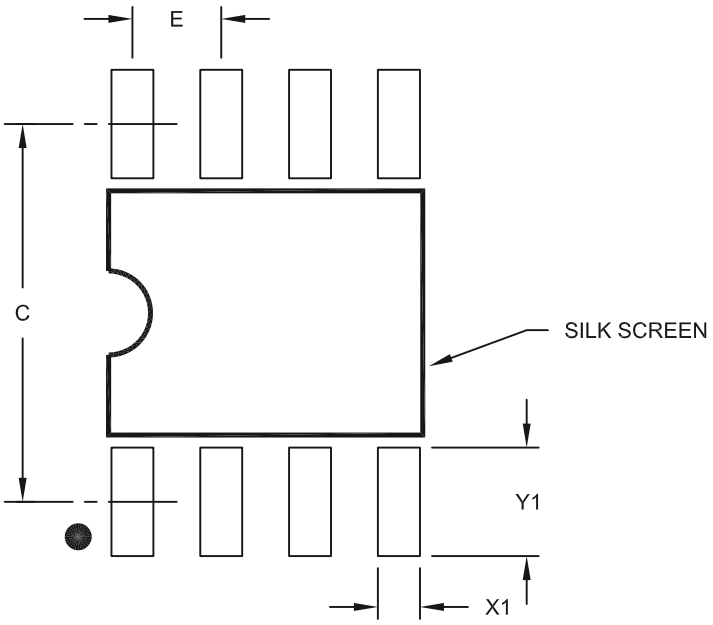
### 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 1.27 BSC | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

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# APPENDIX A: REVISION HISTORY

## Revision E (November 2011)

Updated **Product Identification System**.

Corrected MSOP marking drawings.

Updated Package Specification Drawings with new additions.

## Revision D (April 2011)

The following is the list of modifications:

1. Updated the content to illustrate that the devices now have tested specifications in the 4.5V to 5.5V supply range.
2. Removed figures 2-4 to 2-6, 2-10 to 2-12, 2-16 and 2-17.

## Revision C (January 2007)

This revision includes updates to the packaging diagrams.

## Revision B (February 2002)

Undocumented changes.

## Revision A (December 2001)

Original Release of this Document.



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## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact the local Microchip sales office.

| PART NO. | X | X | /XX |
|---|---|---|---|
| Device | Grade | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP3301: | 13-Bit Serial A/D Converter |
| | MCP3301T: | 13-Bit Serial A/D Converter (Tape and Reel) |
| Grade: | B = | ±1 LSB INL |
| | C = | ±2 LSB INL |
| Temperature Range: | I = | -40°C to +85°C |
| Package: | MS = | Plastic MSOP, 8-lead |
| | P = | Plastic DIP (300 mil Body), 8-lead |
| | SN = | Plastic SOIC (150 mil Body), 8-lead |

**Examples:**

a) MCP3301-BI/P: ±1 LSB INL, Industrial Temperature, PDIP package

b) MCP3301-BI/SN: ±1 LSB INL, Industrial Temperature, SOIC package

c) MCP3301-CI/MS: ±2 LSB INL, Industrial Temperature, MSOP package


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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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