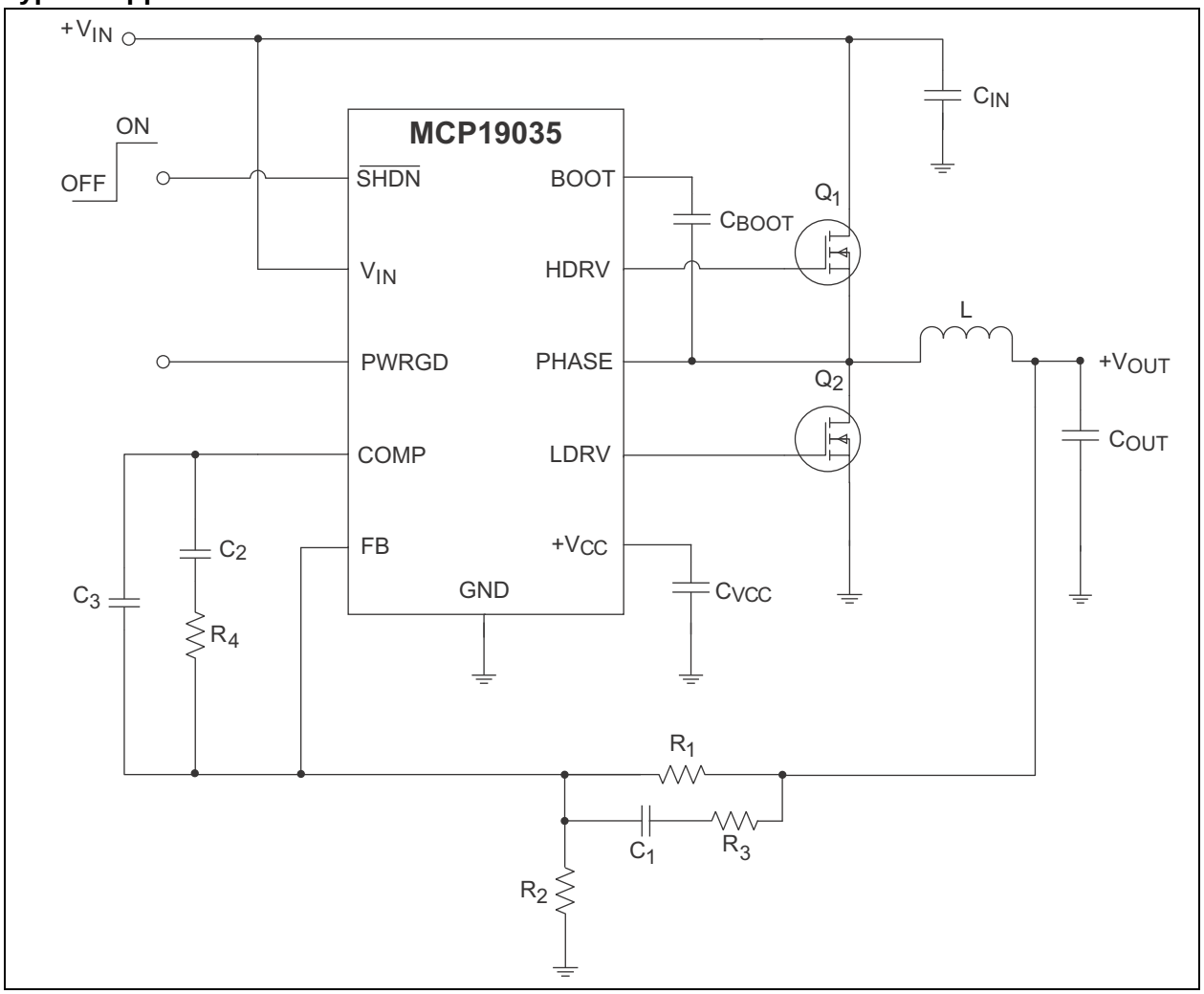
Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} - V_{GND} ..... -0.3V to +32V
V_{BOOT} ..... -0.3V to +37V
VHDRV, HDRV Pin ..... $+V_{PHASE}$ -0.3V to V_{BOOT}+0.3V
VLDRV, LDRV Pin ..... + (V_{GND}-0.3V) to (V_{CC}+0.3V)
Max. Voltage on Any Pin ..... + (V_{GND}-0.3V) to (V_{CC}+0.3V)
Storage Temperature ..... -65°C to +150°C
Maximum Junction Temperature ..... +150°C
ESD protection on all pins (HBM) ..... 2 kV
ESD protection on all pins (MM) 200V

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, C_{IN} = 1.0 µF, T_A = +25°C (for typical values), T_A = -40°C to +125°C (for minimum and maximum).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Inputs						
Input Voltage Range	V_{IN}	4.5	—	30	V	
UVLO (V_{IN} Rising)	$UVLO_{ON}$	4	4.2	4.4	V	
UVLO (V_{IN} Falling)	$UVLO_{OFF}$	3.4	3.6	3.8	V	
UVLO Hysteresis	$UVLO_{HYST}$	—	600	—	mV	
Input Quiescent Current	$I(V_{IN})$	—	6	8	mA	
Shutdown Current	I_{IN_SHDN}	—	25	50	µA	$\overline{SHDN}$ = GND. Internal Voltage Regulator is also disabled
Linear Regulator						
Output Voltage	V_{CC}	4.875	5	5.125	V	6V ≤ V_{IN} < 30V
Output Current	$I_{VCC-OUT}$	50	—		mA	6.5V ≤ V_{IN} < 30V, **Note 2**
Short-Circuit Output Current	$I_{VCC-OUT\_SC}$	—	—	100	mA	V_{IN} = 6V, R_{LOAD} < 0.1Ω
Load Regulation		—	0.1	—	%	**Note 1**
Line Regulation		—	0.05	—	%	**Note 1**
Dropout Voltage		—	0.75	1.3	V	I_{VCC_OUT} = 50 mA
Power Supply Rejection Ratio	PSRR	—	70	—	dB	f ≤ 1000 Hz, I_{VCC_OUT} = 50 mA C_{IN} = 0 µF, $C_{VCC-OUT}$ = 4.7 µF, **Note 1**
Internal Oscillator						
Switching Frequency	F_{SW}	255	300	345	kHz	2 options, see **Section 4.4, Internal Oscillator**
		510	600	690	kHz	
Ramp Signal Amplitude	V_{RAMP}	0.9	1	1.1	V_{PP}	**Note 1**
Reference Voltage						
Reference Voltage Generator	V_{REF}	585	600	615	mV	

Note 1: Ensured by design. Not production tested.
2: Limited by the maximum power dissipation of the case.
3: Possibility to be adjusted for high volumes.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, C_{IN} = 1.0 µF, T_A = +25°C (for typical values), T_A = -40°C to +125°C (for minimum and maximum).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Error Amplifier						
Gain Bandwidth Product	GBP	6.5	10	—	MHz	**Note 1**
Open Loop Gain	A_{OL}	70	80	—	dB	**Note 1**
Input Offset Voltage	V_{OS}	-5	0.1	5	mV	**Note 1**
Input Bias Current (FB Pin)	I_{BIAS}	—	—	5	nA	**Note 1**
Error Amplifier Sink Current	I_{SINK}	—	5	—	mA	**Note 1**
Error Amplifier Source Current	I_{SOURCE}	—	5	—	mA	**Note 1**
PWM Section						
Maximum Duty Cycle	DC_{MAX}	85	—	—	%	**Note 1**
Minimum ON time	$t_{ON(MIN)}$	50	—	100	ns	6V ≤ V_{IN} < 30V, **Note 1**
Soft Start						
Soft Start Time	t_{SS}	—	8	—	ms	
Shutdown						
Logic Low-to-High Threshold	$SHDN_{HI}$	0.85	—	—	V	4.5V ≤ V_{IN} < 30V, V_{CC} goes from 0V to 5V
Logic High-to-Low Threshold	$SHDN_{LO}$	—	—	0.4	V	4.5V ≤ V_{IN} < 30V, V_{CC} goes from 5V to 0V
Power Good						
Power Good Threshold High	PG_{TH-H}	—	93	96	% of V_{REF}	
Power Good Threshold Low	PG_{TH-LOW}	88	90	—	% of V_{REF}	
Power Good Threshold Hysteresis	PG_{TH-HYS}	—	3	—	% of V_{REF}	
Power Good Delay	$t_{PG-DELAY}$	—	150	—	us	V_{FB} = (PG_{TH-HI} + 100 mV) to (PG_{TH-LOW} – 100 mV)
Power Good Active Time-Out Period	$t_{PG-TIME-OUT}$	—	120	—	ms	V_{FB} = (PG_{TH-HI} – 100 mV) to (PG_{TH-HI} + 100 mV)
MOSFET Drivers						
High-Side Driver Pull-up Resistance	$R_{HI-SOURCE}$	—	2	3.5	Ω	V_{BOOT} – V_{PHASE} = 4.5V, I_{HDRV} = 100 mA, **Note 1**
High-Side Driver Pull-Down Resistance	$R_{HI-SINK}$	—	2	3.5	Ω	V_{BOOT} – V_{PHASE} = 4.5V, I_{HDRV} = 100 mA, **Note 1**
Low-Side Driver Pull-Up Resistance	$R_{LO-SOURCE}$	—	2	3.5	Ω	V_{CC} = 5V, **Note 1**
Low-Side Driver Pull-Down Resistance	$R_{LO-SINK}$	—	1	2.5	Ω	V_{CC} = 5V, **Note 1**
HDRV Rise Time	t_{RH}	—	15	35	ns	C_{LOAD} = 1.0 nF, **Note 1**
HDRV Fall Time	t_{FH}	—	15	35	ns	C_{LOAD} = 1.0 nF, **Note 1**
LDRV Rise Time	t_{RL}	—	10	25	ns	C_{LOAD} = 1.0 nF, **Note 1**

Note 1: Ensured by design. Not production tested.

2: Limited by the maximum power dissipation of the case.

3: Possibility to be adjusted for high volumes.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, F_{SW} = 300 kHz, C_{IN} = 1.0 µF, T_A = +25°C (for typical values), T_A = -40°C to +125°C (for minimum and maximum).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
LDRV Fall Time	t_{FL}	—	10	25	ns	C_{LOAD} = 1.0 nF, **Note 1**
Dead Time	t_{DT}	20	—	—	ns	Two Dead-Time options, see **Section 5.2.2, Dead Time Selection**, **Note 1**
		—	12	—		
Short Circuit Protection						
High-Side Over Current Threshold Voltage	OC_{TH-HI}	430	480	530	mV	**Note 1**, V_{CBOOT} = 5V
Low-Side Over Current Threshold Voltage	OC_{TH-LO}	130	180	230	mV	**Note 1**, **Note 3**
Minimum Pulse Width During Short Circuit	t_{SS-MIN}	—	800	—	ns	**Note 1**
Off-Time Between Restart Attempts (Hick-Up Time)	t_{SS-HT}	30	60	—	ms	**Note 1**
Thermal Shutdown						
Thermal Shutdown	TSHD	—	150	—	°C	**Note 1**
Thermal Shutdown Hysteresis	TSHD_HYS	—	15	—	°C	**Note 1**

Note 1: Ensured by design. Not production tested.

2: Limited by the maximum power dissipation of the case.

3: Possibility to be adjusted for high volumes.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, V_{IN} = 6.0V to 30V, F_{SW} = 300 kHz

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Maximum Junction Temperature	T_{J-MAX}	—	—	+150	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 10L-3x3 DFN	θ_{JA}	—	53.3	—	°C/W	Typical 4-Layer board with interconnecting vias

NOTES:

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 300 kHz, C_{VCC} = 4.7 uF.

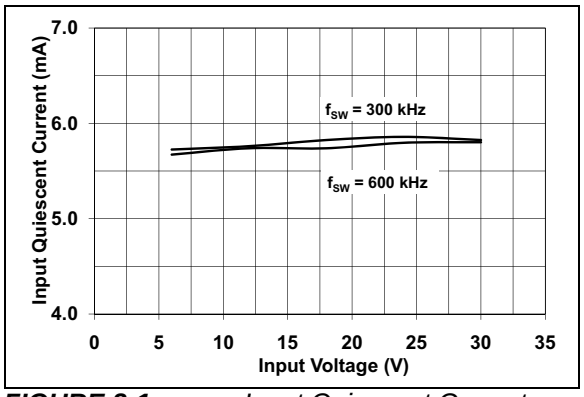


FIGURE 2-1: *Input Quiescent Current vs. Input Voltage.*

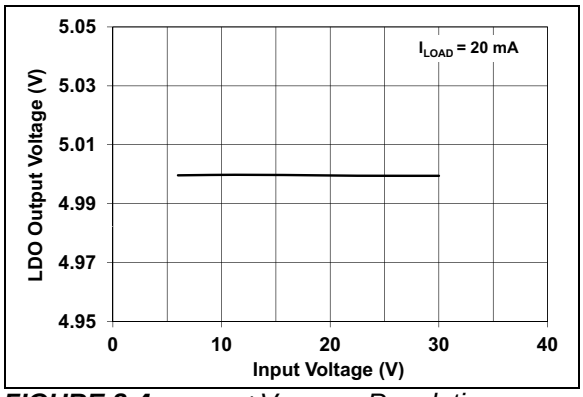


FIGURE 2-4: *+V_{CC-OUT} Regulation vs. Input Voltage.*

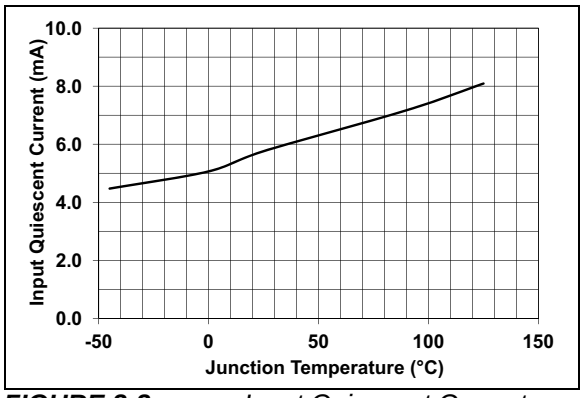


FIGURE 2-2: *Input Quiescent Current vs. Temperature.*

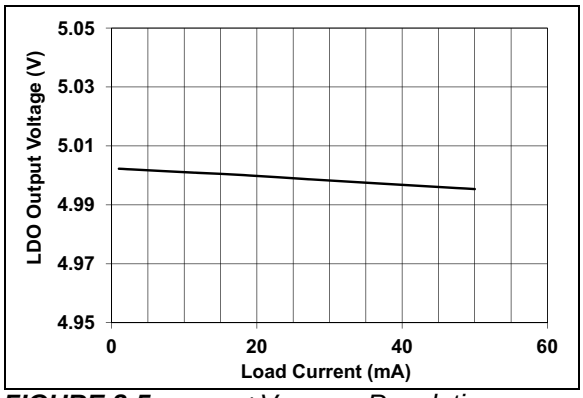


FIGURE 2-5: *+V_{CC-OUT} Regulation vs. Load Current.*

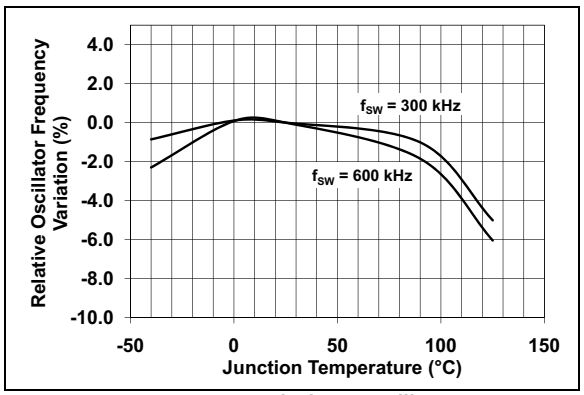


FIGURE 2-3: *Relative Oscillator Frequency Variation vs. Temperature.*

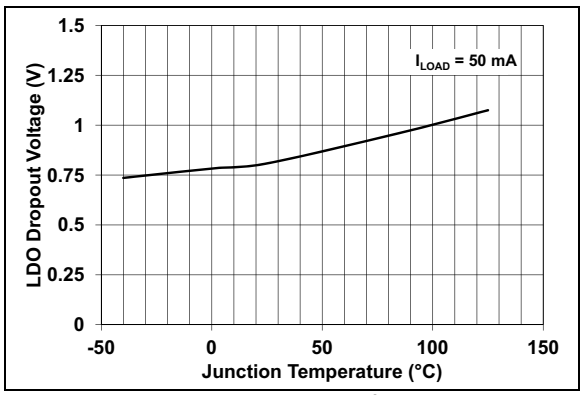


FIGURE 2-6: *LDO Regulator Dropout Voltage vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 300 kHz, C_{VCC} = 4.7 uF.

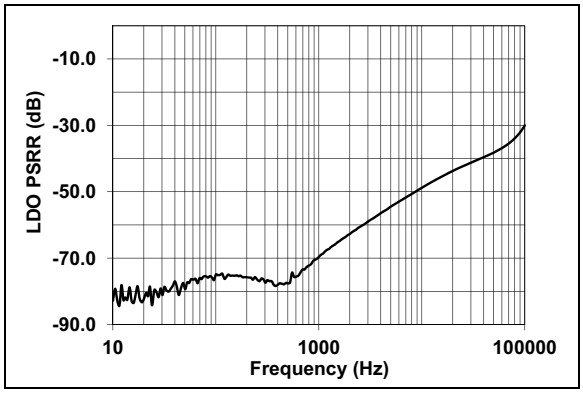


FIGURE 2-7: *+V_{CC-OUT} LDO PSRR vs. Frequency.*

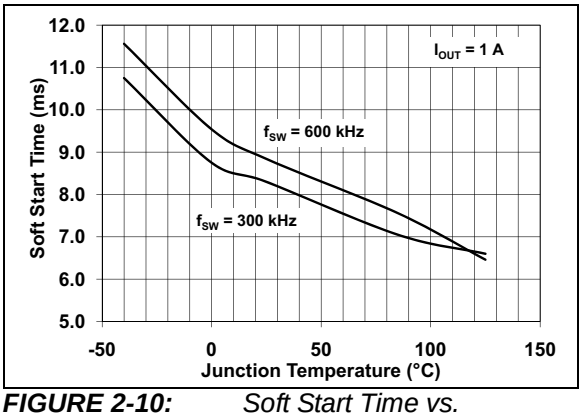


FIGURE 2-10: *Soft Start Time vs. Temperature.*

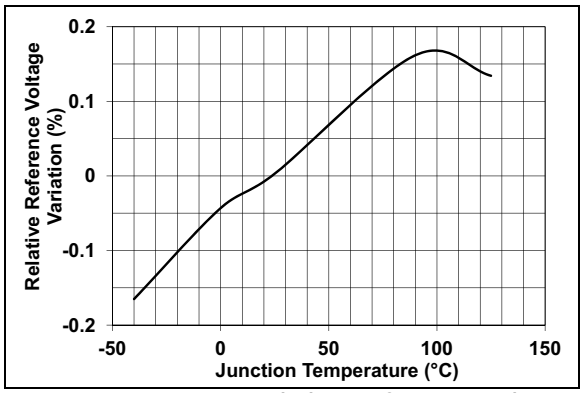


FIGURE 2-8: *Relative Reference Voltage Variation vs. Temperature.*

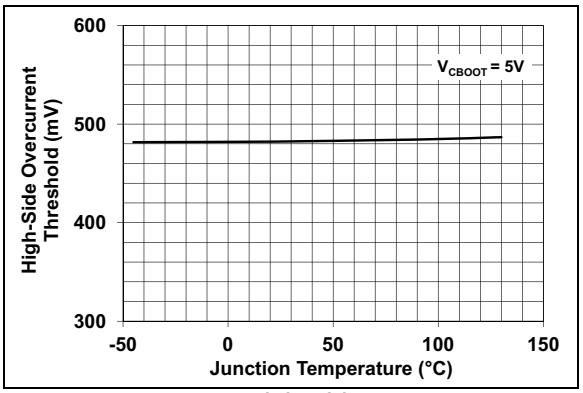


FIGURE 2-11: *High-Side Overcurrent Threshold vs. Temperature.*

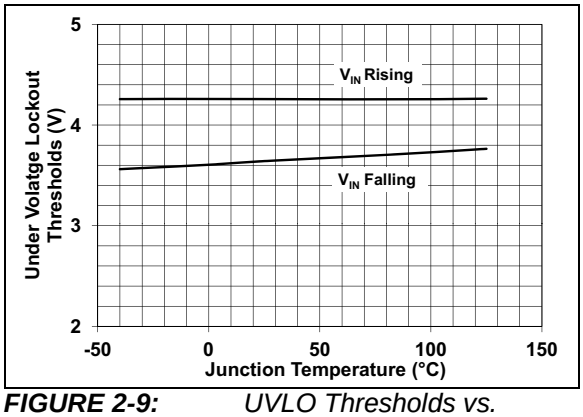


FIGURE 2-9: *UVLO Thresholds vs. Temperature.*

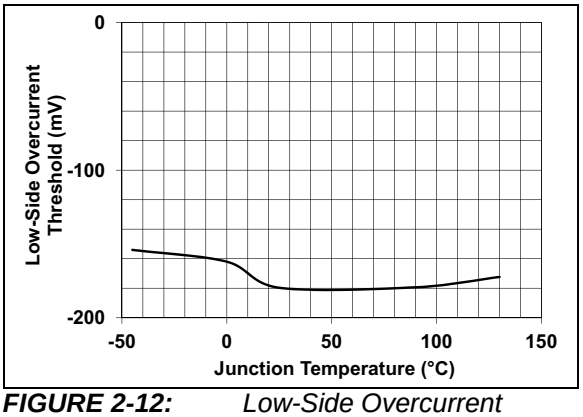


FIGURE 2-12: *Low-Side Overcurrent Threshold vs. Temperature.*

Note: Unless otherwise indicated, T_A = +25°C, V_{IN} = 12V, V_{OUT} = 1.8V, f_{SW} = 300 kHz, C_{VCC} = 4.7 uF.

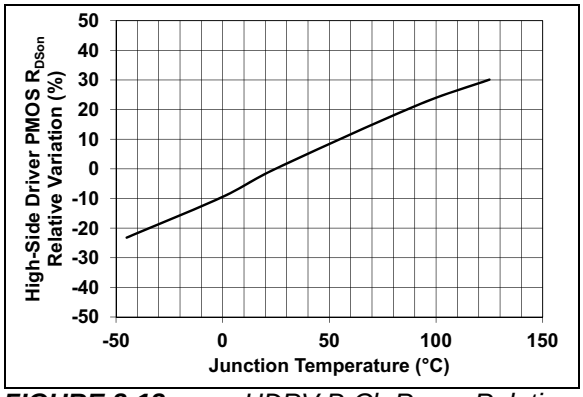


FIGURE 2-13: *HDRV P-Ch R_{DSon} Relative Variation vs. Temperature.*

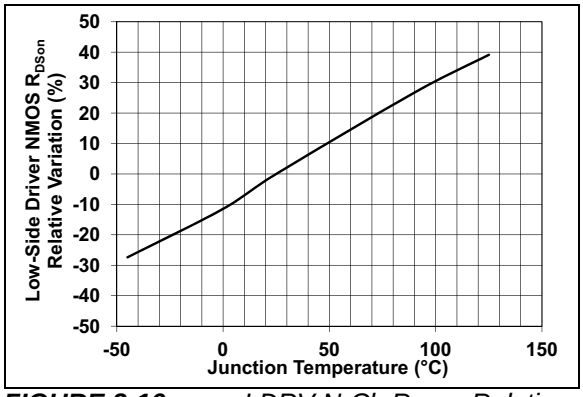


FIGURE 2-16: *LDRV N-Ch R_{DSon} Relative Variation vs. Temperature*

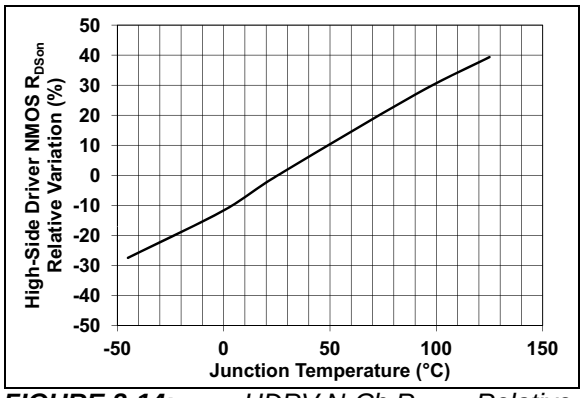


FIGURE 2-14: *HDRV N-Ch R_{DSon} Relative Variation vs. Temperature.*

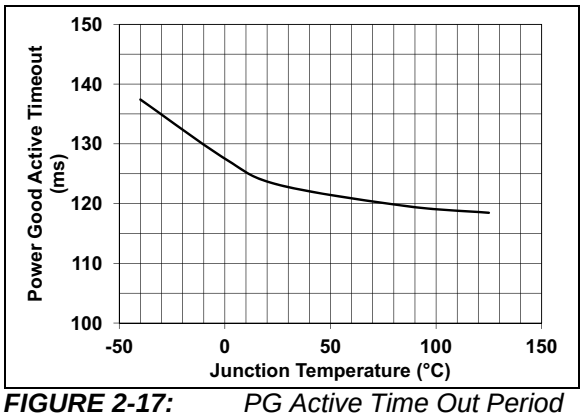


FIGURE 2-17: *PG Active Time Out Period vs. Temperature.*

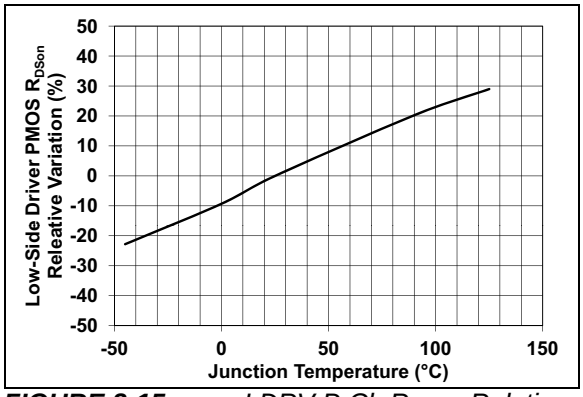


FIGURE 2-15: *LDRV P-Ch R_{DSon} Relative Variation vs. Temperature.*

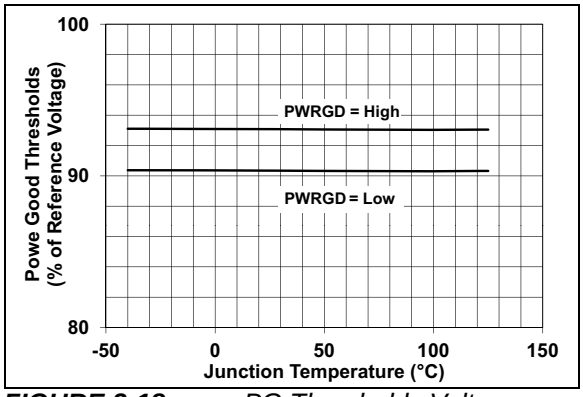


FIGURE 2-18: *PG Thresholds Voltage vs. Temperature.*

NOTES:

3.0 PIN DESCRIPTION

Description of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTION TABLE

MCP19035 3 x 3 DFN	Symbol	Description
1	$\overline{SHDN}$	Device shutdown input pin
2	FB	Feedback voltage input pin
3	COMP	Internal error amplifier output pin
4	V_{IN}	Input voltage pin
5	PWRGD	Power good pin
6	$+V_{CC}$	+5.0V output voltage pin
7	LDRV	Lower gate drive output pin
8	BOOT	Floating bootstrap supply pin
9	PHASE	Switching node pin
10	HDRV	Upper gate drive output pin
11	EP	Exposed Thermal Pad, must be connected to GND

3.1 Shutdown Input Pin ($\overline{SHDN}$)

This pin enables or disables the MCP19035 device. When logic “High” is applied to this pin, the device is enabled. A logic “Low” will disable the device. When the device is disabled, both the LDRV and HDRV pins are held low. The internal LDO regulator is also disabled when the $\overline{SHDN}$ pin is pulled low. Do not let this pin float. If not used, connect to V_{IN} using a 100 kΩ resistor.

3.2 Feedback Voltage Input Pin (FB)

This is the internal error amplifier’s negative input, and is used to sense the output voltage. The positive input to the amplifier is connected to the internal reference voltage.

3.3 Internal Error Amplifier Pin (COMP)

This is the output of the internal error amplifier. The compensation network is connected between this pin and the FB pin.

3.4 Input Voltage Pin (V_{IN})

This pin is the input power for the controller. A bypass capacitor must be connected between this pin and the GND pin. The input of an internal voltage regulator (LDO) is connected to this pin to generate the +5V V_{CC} used for internal circuitry bias.

3.5 Power Good Pin (PWRGD)

The power good pin is an open drain output. This pin is pulled low when the output is 90% less than the typical value. Connect this pin to $+V_{CC}$ pin through a pull-up resistor. The recommended value for the pull-up resistor is 100 kΩ.

3.6 LDO Output Voltage Pin ($+V_{CC}$)

This pin is the output of the internal voltage regulator (LDO). The internal circuitry of the controller is powered from this pin (+5.0V). External low noise loads can be powered from this pin, but the sum of the external load current and the internal circuitry current should not exceed 50 mA. A 4.7 µF ceramic capacitor must be connected between this pin and GND.

3.7 Lower Gate Pin (LDRV)

This pin is the drive output for the low-side N-Channel MOSFET (synchronous rectifier). The LDRV drive is capable of sourcing 1A and sinking 1.5A.

3.8 Bootstrap Supply Pin (BOOT)

The BOOT pin is the floating bootstrap power supply pin for the high-side MOSFET gate driver. A capacitor connected between this pin and the PHASE pin provides the necessary charge to turn on the external high-side MOSFET.

3.9 Switching Node Pin (PHASE)

This pin provides a return path for the high-side gate driver. It also provides a path for the charging of the BOOT capacitor, used while turning on the high-side MOSFET. This pin also senses the switching transition to eliminate cross conduction (shoot-through).

3.10 Upper Gate Drive Pin (HDRV)

This pin is the high-side N-channel MOSFET (control transistor) gate drive output. The HDRV drive is capable of sourcing and sinking 1A.

3.11 Exposed Thermal Pad (EP)

Analog ground and power ground are both connected to this pin.

4.0 DETAILED DESCRIPTION

4.1 Device Overview

The MCP19035 family of devices are high-performance controllers providing all the necessary functions to construct a high-performance DC/DC converter, while keeping costs and design effort to a minimum:

- Support for pre-biased outputs eliminates concerns about damaging sensitive loads during startup.
- Strong gate drivers for the high-side and rectifier N-Channel MOSFETs decrease switching losses, yielding increases in efficiency.
- Adaptive gate drive timing prevents shoot-through and minimizes body diode conduction in the synchronous rectifier MOSFET, which also increases the efficiency.
- Dead-Time optimization options of the MCP19035 assist in improving the power conversion efficiency, when used with high-speed, low Figure of Merit MOSFETs.
- Overcurrent protection circuits in both high and low-side switches, and a short circuit hiccup-recovery mode increase design flexibility and minimize power dissipation in the event of prolonged output faults.
- The dedicated $\overline{\text{SHDN}}$ pin allows the converter to be placed in a low quiescent current state.
- Internal fixed converter switching frequency and soft-start reduce the external component count, simplifying design and layout, as well as reducing footprint and size.
- The 3 mm × 3 mm DFN package size also minimizes the overall converter footprint.

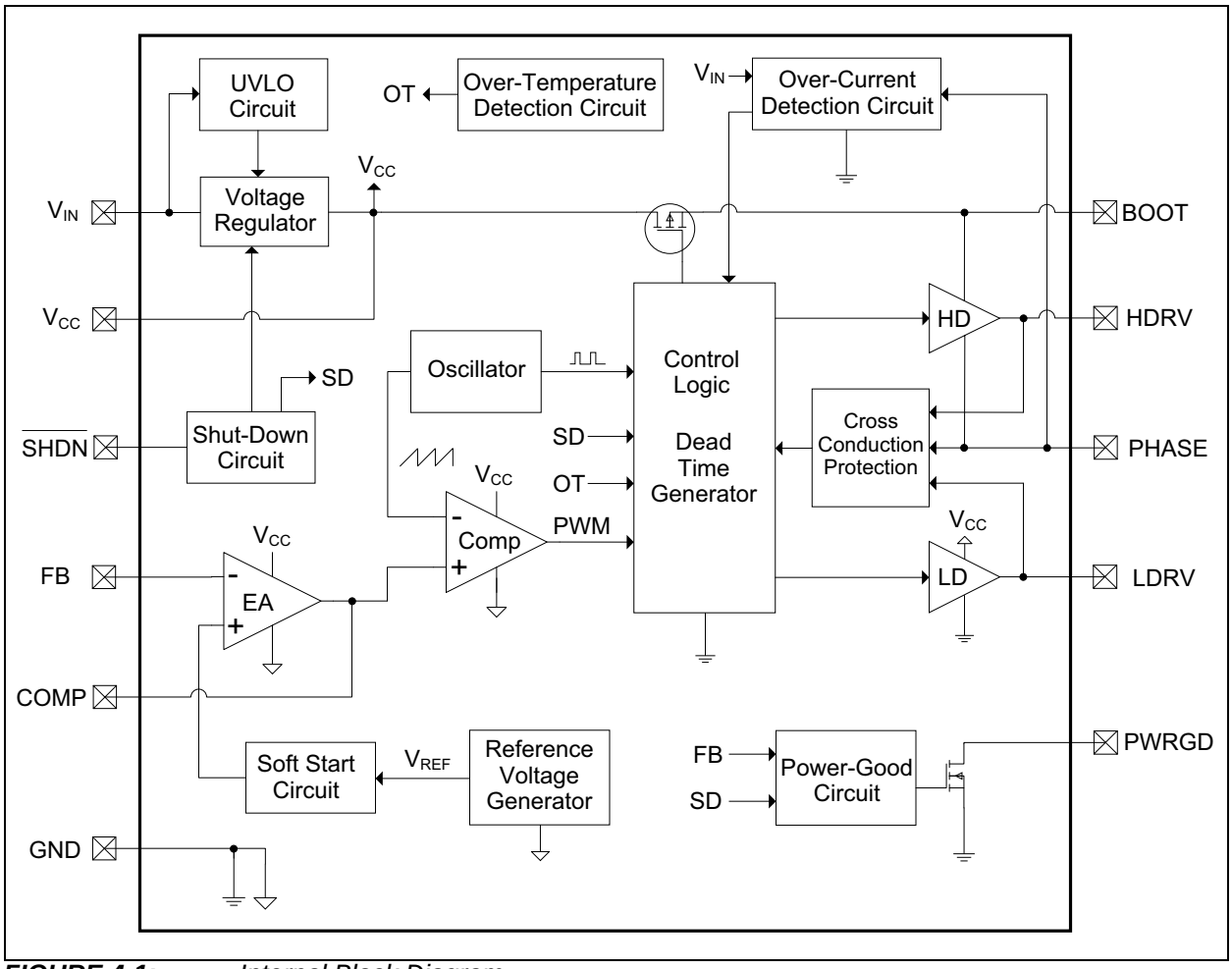


FIGURE 4-1: *Internal Block Diagram.*

4.2 PWM Circuitry

The MCP19035 controller implements a fixed frequency, voltage-mode control scheme. The internal PWM generator is comprised of an oscillator, error amplifier, high-speed comparator and a latch. The error amplifier generates the control voltage by amplifying the difference between voltage reference (600 mV, internally generated) and the voltage of the FB pin (feedback voltage). This control voltage is compared by the high-speed comparator to an artificially generated ramp signal; the result is a PWM signal. An SR latch (Set-Reset flip-flop) is used to prevent the PWM circuitry from turning on the external switch until the beginning of the next clock cycle.

An external Compensation Network (Type-II or Type-III) must be used to stabilize the control system.

4.3 Internal Reference Voltage V_{REF}

An integrated, precision voltage reference is provided by the MCP19035. An external resistor divider is used to program the converter's output voltage. The nominal value of this internal reference voltage is 600 mV.

4.4 Internal Oscillator

The MCP19035 device provides two switching frequency options: 300 kHz and 600 kHz.

4.5 Under Voltage Lockout Circuit (UVLO)

An integrated Under Voltage Lockout Circuit (UVLO) prevents the converter from starting until the input voltage is high enough for normal operation. The converter will typically start at 4.2V and operate down to 3.6V. Hysteresis is added to prevent starting and stopping during startup, as a result of loading the input voltage source.

4.6 Shutdown Input

The Shutdown input pin ($\overline{SHDN}$) is used to enable and disable the controller. When the $\overline{SHDN}$ pin is pulled low, the MCP19035 is placed in Shutdown mode. During Shutdown, most of the internal circuits (including the LDO) are disabled, to minimize current consumption.

A 100 kΩ pull-up resistor is recommended between the $\overline{SHDN}$ pin and V_{IN} pin. Note that the $\overline{SHDN}$ input is a high-impedance pin. Noise generated by the circuits located near this pin may inadvertently shut down the controller. To improve the noise immunity of this input pin, we recommend placing a small capacitor between GND and $\overline{SHDN}$, or decrease the value of the pull-up resistor. The Shutdown input pin should not be left floating.

4.7 Power Good Output (PWRGD)

This open drain output provides an indication that the output voltage is 92% (typical) of its regulated value. This output is also low for other existing conditions that signal the possibility that the output of the power supply is out of regulation. The conditions are:

- Feedback pin (FB) voltage differs more than ±8% from its nominal value (600 mV)
- Soft-start period is active
- Undervoltage condition detected
- Overcurrent condition detected, on either the High Side or Low Side
- Die temperature is above the thermal shutdown threshold (+150°C)

The active high power good signal has a fixed time delay of approximately 120 ms ($t_{PG-TIMEOUT}$). There is typically a 150 µs delay ($t_{PG-DELAY}$) on the power good signal high-to-low transition.

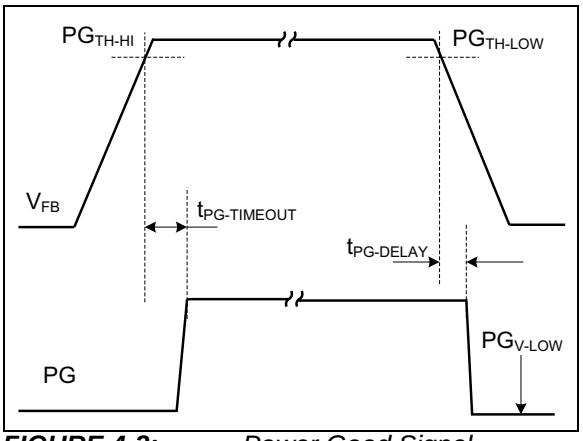


FIGURE 4-2: *Power Good Signal.*

4.8 Internal Voltage Regulator (LDO)

The MCP19035 controller offers an internal 5V Low Dropout Voltage Regulator. This regulator provides the bias voltage for all internal circuits. A ceramic capacitor (4.7 µF minimum) must be connected between the output of this LDO (V_{CC} pin) and ground (GND pin) for stable operation.

An external low noise load may be powered from this regulator, but the total current consumed from the LDO output (internal circuitry of MCP19035 + external load) should not exceed 50 mA. The internal circuitry of the MCP19035 consume approximately 5 mA. The total amount of current available to power the external load can be estimated from Equation 4-1:

EQUATION 4-1:

$$I_{External\ Load} = 50\ mA - f_{SW} \times (Q_{G(High\ Side)} + Q_{G(Low\ Side)}) - 5\ mA$$

Where:

- $I_{External\ Load}$ = Current Available for powering the External Load
- f_{SW} = Switching Frequency (300 kHz or 600 kHz)
- $Q_{G(High\ Side)}$ = Total Gate Charge of the High-Side MOSFET at 4.5V V_{GS}
- $Q_{G(Low\ Side)}$ = Total Gate Charge of the Low-Side MOSFET at 4.5V V_{GS}

This LDO dissipates power within the MCP19035. To avoid tripping the Overtemperature Protection Circuit, the designer must ensure that the maximum die temperature is below +125°C under worst case conditions (i.e. high input voltage). For further information regarding the maximum dissipated power for LDOs, see Microchip's AN761 and AN792 application notes.

The LDO is protected against overload and short-circuit conditions. Consistent performance of the internal MOS drivers is ensured by monitoring the LDO output voltage; if the voltage is lower than 3.3V typical, the chip will enter in Shut-Down mode to prevent damage to the external MOSFETs.

4.9 Internal MOSFET Drivers

Internal MOSFET drivers are capable of driving external, "Logic Level" (+5V) MOSFETs.

The Low-Side Driver (LDRV) is referenced to the GND pin and is capable of sourcing 1A and sinking 1.5A.

The High-Side Driver (HDRV) is floating and capable of sourcing and sinking 1A. This driver is powered from an external bootstrap capacitor.

The drivers have non-overlapping timing that is governed by an adaptive delay circuit to minimize body diode conduction in the synchronous rectifier.

For the optimized Dead Time version of the MCP19035, the adaptive delay circuit is disabled and the Dead Time has a fixed value.

4.10 Overcurrent Protection

Overcurrent protection is accomplished by monitoring the voltage across the external MOSFETs when they are ON (conducting).

For the high-side overcurrent protection, when the sensed voltage drop across the high-side MOSFET is greater than the high-side overcurrent threshold voltage, the high-side MOSFET is immediately turned off and the high-side overcurrent counter is incremented by one. On the next cycle, if the high-side overcurrent threshold voltage is not exceeded, the high-side overcurrent counter is decreased by one count. If the high-side overcurrent counter reaches a count of 7, a fault condition exists and the MCP19035 turns off both external MOSFETs.

After a 60 ms delay, the MCP19035 will attempt to restart. If during the next cycle, a high-side overcurrent threshold voltage is measured across the high-side MOSFET, a fault is again declared and both external MOSFETs are turned off for another 60 ms. However, if after the attempted restart a high-side overcurrent threshold voltage is not measured across the high-side MOSFET, the high-side overcurrent counter is decreased by one and the MCP19035 continues to operate until the high-side overcurrent counter reaches a count of 7.

The low-side overcurrent protection behaves much the same way as the high-side overcurrent protection. The difference is that the low-side MOSFET is not immediately turned off when a low-side overcurrent threshold voltage is measured. It remains on until the next cycle begins.

For the low-side overcurrent protection, when the sensed voltage drop across the low-side MOSFET is greater than the low-side overcurrent threshold voltage specified, a low-side overcurrent counter is incremented by one count. On the next cycle, if the low-side over current threshold voltage is not exceeded, the low-side overcurrent counter is decreased by one. If the low-side overcurrent counter reaches a count of 7, a fault condition exists and the MCP19035 turns off both external MOSFETs. After a 60 ms delay, the MCP19035 device will attempt to restart. If during the next cycle, a low-side overcurrent threshold voltage is measured across the low-side MOSFET, a fault is again declared and both external MOSFETs are turned off for another 60 ms. However, if after the attempted restart a low-side overcurrent threshold voltage is not measured across the low-side MOSFET, the low-side overcurrent counter is decreased by one and the MCP19035 continues to operate until the low-side overcurrent counter reaches a count of 7.

The voltage threshold for high-side overcurrent protection circuit is fixed, 480 mV typical. The high-side voltage threshold will also depend on the value of the voltage across the bootstrap circuit capacitor, and will decrease when this voltage decreases. This will ensure that the high-side protection will avoid a failure of the MOSFET when the bootstrap voltage is low and the switching losses are high. This threshold will provide a cycle-by-cycle protection in case of short circuit, but it should not be used to provide a precise current limit for the converter. An estimation of the current that flows in the high-side MOSFET during short circuit can be found using Equation 4-2. Note that, due to the leading edge blanking time, this current also depends on the inductor's ripple current. To avoid false triggering of the high-side overcurrent protection circuit during transients, it is highly recommended to choose a MOSFET that will provide a threshold at least four times higher than the maximum output current of the converter.

EQUATION 4-2: PEAK CURRENT FOR HIGH-SIDE MOSFET

$$I_{HS\ MOS} = \frac{V_{OC\ HS}}{R_{DSON}}$$

Where:

- $I_{HS\ MOS}$ = Current that passes through the High-Side MOSFET
- $V_{OC\ HS}$ = Threshold Voltage for High-Side Overcurrent Protection Circuit (480 mV)
- R_{DSON} = ON Resistance of the High-Side MOSFET

The voltage threshold for the low-side overcurrent protection circuit is fixed, 180 mV typical. Different values for this threshold (from 100 mV to 300 mV) are available on request. An estimation of the current that flows on the low-side MOSFET during short circuit is realized using Equation 4-3. Note that, due to the leading edge blanking time, this current also depends on the inductor's ripple current. To avoid false triggering of the low-side over current protection circuit during transients, it is highly recommended to choose a MOSFET that will provide a threshold at least two times higher than the maximum output current of the converter.

EQUATION 4-3:

$$I_{LS\ MOS} = \frac{V_{OC\ LS}}{R_{DSON}}$$

Where:

- $I_{LS\ MOS}$ = Current that passes through the Low-Side MOSFET
- $V_{OC\ LS}$ = Threshold Voltage for Low-Side Overcurrent Protection Circuit (180 mV)
- R_{DSON} = ON Resistance of the Low-Side MOSFET

To avoid a false trigger of the overcurrent circuit, a leading edge blanking circuit is present on both the high and low-side measurements. Due to this blanking time, the accuracy of the overcurrent circuit may be impacted if the converter operates at higher duty cycles (more than 85%), or if the inductor's current ripple is very high (i.e. the inductor is saturated by the excessive current).

4.11 Soft Start

To control the output voltage during start-up, the MCP19035 uses a soft-start circuit that allows the output voltage of the system to monotonically increase. The soft start circuitry allows the output voltage to rise up to the desired regulation limit, typically within 8 ms. The soft start circuit is enabled each time the MCP19035 starts. This includes initial start-up, start-up from toggling the $\overline{SHDN}$ pin, start-up after thermal shutdown, or start-up after an overcurrent condition.

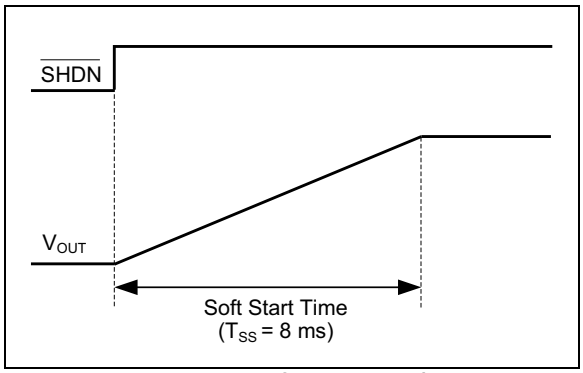


FIGURE 4-3: *Soft Start-up Diagram.*

4.12 Pre-Bias Load Start-up

A special start-up sequence will prevent any current to be sourced from the output in case of a pre-biased load. This is accomplished by monitoring the FB pin and internal reference voltages. If the positive input to the Error Amplifier (internal reference voltage) is greater than the feedback voltage (voltage present at FB pin), the controller will drive the low-side MOSFET (synchronous rectifier) with a reduced duty cycle. This sequence ensures a smooth output voltage transition without sinking any current from the pre-biased external load.

Note:	Do not use a low impedance source to back-drive the output voltage during the pre-bias state. There is no protection mechanism for positive current flow in the synchronous rectifier MOSFET. The converter can reverse the energy flow (becoming a Boost converter) if the input voltage is accidentally disconnected.

NOTES:

5.0 APPLICATION INFORMATION

5.1 Typical Applications

The MCP19035 synchronous buck controller operates over an input voltage range up to a maximum of 30V. The output current capability depends only on the external MOSFET's selection and can also be very high, typically up to 20A.

Typical applications include POL modules for powering DSPs, FPGAs and ASICs, and, in general, any step-down voltage conversion (from maximum 30V input voltage) for medium-to-high output current loads.

5.2 Design Procedure

To simplify this design process, an Excel®-based design tool is available to support typical applications. This tool is available on the MCP19035 product web site. Refer to AN1452 – *"Using the MCP19035 Synchronous Buck Converter Design Tool"* for further details.

5.2.1 SWITCHING FREQUENCY AND THE MAXIMUM CONVERSION RATIO

The MCP19035 controller provides two options for the switching frequency: 300 kHz and 600 kHz. In general, choosing a higher switching frequency allows the use of smaller size components (i.e. inductor and filtering capacitors), but increases the switching losses. The 300 kHz switching frequency is recommended for applications requiring output currents up to 20A. For applications requiring output currents up to 10A, the recommended switching frequency is 600 kHz.

Due to the minimum "On Time" for the high-side MOSFET driver (70 ns typical), the maximum conversion ratio must be limited to 20:1.

5.2.2 DEAD TIME SELECTION

Dead Time will affect the maximum obtainable efficiency of the converter. Selecting the Dead Time depends on the external MOSFETs' parameters. Lower Figure of Merit (FOM) transistors will permit the use of shorter Dead Times. This may increase the converter efficiency by up to 2%.

Low Figure of Merit transistors allow the user to select a low value for Dead Time (typical 12 ns) without causing a shoot-through phenomenon. For low-FOM transistors, the MCP19035 version with fixed 12 ns Dead Time is recommended.

For typical medium Figure of Merit transistors, the MCP19035 version with the adaptive Dead-Time generator is recommended.

5.2.3 INDUCTOR SELECTION

The output inductor is responsible for smoothing the square wave created by the switching action and for controlling the output current ripple (ΔI_{OUT}). There is a trade off between efficiency and load transient response time when the value of the inductor is chosen. The smaller the inductance, the quicker the converter can respond to transients in the load current. However, a smaller inductor requires a higher switching frequency to maintain the same level of output current ripple. Remember that increasing the switching frequency will also increase the switching losses in the MOSFETs.

A good compromise for the inductor current ripple is 30% of the output current. The value of the inductor is calculated in Equation 5-1:

EQUATION 5-1: INDUCTOR VALUE

$$L = \left(V_{IN_{MAX}} - V_{OUT}\right) \times \frac{V_{OUT}}{V_{IN_{MAX}}} \times \frac{1}{f_{SW}} \times \frac{1}{0.3 \times I_{OUT_{MAX}}}$$

The peak current in the inductor is determined in Equation 5-2:

EQUATION 5-2: INDUCTOR PEAK CURRENT

$$I_{L_{PEAK}} = I_{OUT_{MAX}} + \frac{0.3 \times I_{OUT_{MAX}}}{2}$$

EQUATION 5-3: INDUCTOR RMS CURRENT

$$I_{L_{RMS}} = \sqrt{I_{OUT}^2 + \frac{I_{Ripple}}{3}^2}$$

Additional care must be taken when selecting an inductor:

- Choose an inductor that has a saturation current larger than the calculated peak current. The tolerance of the inductor must also be considered (typically 20%).
- To minimize the conduction losses, choose an inductor with the lowest possible DC resistance. The maximum DC resistance specified in the data sheet will ensure the worst-case component specification.
- There are many magnetic materials available for inductor core: ferrite, iron powder and composite materials. The ferrite offers the lowest core losses, but the saturation characteristic is "hard" (i.e. the inductance drops rapidly after the current reaches the saturation level). The losses of iron powder or composite material cores are higher than ferrite, but the saturation characteristic is "soft", making it more suitable for voltage mode control converter, including the MCP19035.

5.2.4 INPUT CAPACITOR SELECTION

The input capacitor is responsible for providing a low impedance voltage source for the step-down converter. This capacitor must be able to sustain high ripple current, a consequence of the discontinuous input current of the buck converter. A low equivalent series resistance capacitor (ESR), preferably ceramic, is recommended. For wide temperature range applications, a multi-layer X7R dielectric is recommended, while for applications with limited temperature range, a multi-layer X5R dielectric is acceptable. A higher ESR will produce a higher voltage ripple and higher power losses. The capacitor voltage rating must be higher than the maximum operating input voltage of the converter.

The minimum capacitance is determined in Equation 5-4:

EQUATION 5-4: MINIMUM CAPACITANCE FOR INPUT CAPACITOR

$$C_{IN\_MIN} = \frac{I_{OUT} \times D \times (1-D)}{f_{SW} \times (V_{Ripple} - D \times I_{OUT} \times ESR)}$$

Where:

- C_{IN_MIN} = Minimum Capacitance of the Input Capacitor (in Farad)
- I_{OUT} = Output Current (A)
- D = Duty Cycle (for worst case this is 0.5)
- f_{SW} = Switching Frequency (Hz)
- V_{Ripple} = Input Voltage Ripple (usually between 0.1V and 0.5V)
- ESR = Equivalent Series Resistance of the Capacitor (in Ohm)

The maximum ripple current in the input capacitor occurs when the duty cycle is 50%. This must be considered worst case for calculating the input capacitor.

The RMS current in the input capacitor is estimated with Equation 5-5:

EQUATION 5-5: RMS CURRENT IN THE INPUT CAPACITOR

$$I_{RMS(C_{IN})} = \left(I_{OUT} + \frac{I_{Ripple}}{12}\right)\sqrt{D} - \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN}}\right)$$

The input capacitor must be rated to sustain this RMS current without considerable losses.

5.2.5 OUTPUT CAPACITOR SELECTION

The output capacitor is responsible for smoothing the output voltage. It also plays an important role in the stability of the control system. The voltage ripple across the output capacitor is the sum of ripple voltages due to the Equivalent Series Resistance (ESR) and the voltage sag due to the load current that must be supplied by the capacitor as the inductor is discharged. A low ESR capacitor, preferably ceramic, is recommended. For wide temperature range applications, a multi-layer X7R dielectric is recommended, while for applications with limited temperature range, a multi-layer X5R dielectric is acceptable.

The output voltage ripple is estimated in Equation 5-6:

EQUATION 5-6: OUTPUT VOLTAGE RIPPLE

$$V_{Ripple} = I_{Ripple} \times \left(ESR + \frac{1}{8 \times C_{OUT} \times f_{SW}}\right)$$

Where:

- I_{Ripple} = Inductor Current Ripple (A)
- V_{Ripple} = Output Voltage Ripple (V)
- C_{OUT} = Output Capacitor (F)
- ESR = Equivalent Series Resistance of the Output Capacitor (Ohm)

Minimum capacitance value is calculated according to the demand of the load transient response. During a transient load current, the excessive energy stored by the inductor must be absorbed by the output capacitor until the control loop sets the proper duty cycle. Equation 5-7 calculates the minimum value for the output capacitor value:

EQUATION 5-7: OUTPUT CAPACITOR MINIMUM VALUE

$$C_{OUT} = \frac{L \times \left|I_{OH}^2 - I_{OL}^2\right|}{\left|V_f^2 - V_{OUT}^2\right|}$$

Where:

- I_{OH} = Final Value of the Output Current
- I_{OL} = Initial Value of the Output Current
- V_{OUT} = Initial Output Voltage
- V_f = Final Output Voltage

For applications that require low output voltage overshoot during a step load, the value of the output capacitor can become very large. In this case, it is recommended to mix ceramic capacitors with aluminum or polymer electrolytic capacitors to reach the recommended value.

5.2.6 MOSFETS SELECTION

Choosing the right MOSFET is a critical part of the design for a switching regulator. Their performance will directly impact the efficiency and reliability of the regulator.

The MCP19035 synchronous buck controller offers an integrated, logic-level MOSFET driver, and is capable of supplying 5V to drive the MOSFET gates. As a result, logic-level MOSFETs must be used. Suitable MOSFETs should meet the requirement of voltage and current rating.

A key parameter for evaluating the MOS transistor performance is the Figure of Merit. For a given MOSFET, this is defined as the product between the Total Gate Charge (Q_G) and $R_{DS(ON)}$ (see Equation 5-8).

EQUATION 5-8: FIGURE OF MERIT

$$FOM = Q_{G(Tot)} \times R_{DS_{(ON)}}$$

A lower FOM value means a higher-performance MOS transistor.

For the high-side MOSFET, power losses consist of both switching and conduction losses. Conduction losses are high when the duty cycle of the converter is high. The conduction loss of the high-side MOSFET can be estimated by multiplying the $R_{DS(ON)}$ with the RMS value of the current that passes through the transistor (see Equation 5-9).

EQUATION 5-9: RMS VALUE FOR HIGH-SIDE CURRENT

$$I_{RMS\ High\text{-}Side} = \sqrt{D \times \left(I_{OUT}^2 + \frac{I_{Ripple}^2}{12} \right)}$$

Where:

- D = Duty Cycle
- I_{OUT} = Output Current (A)
- I_{Ripple} = Current Ripple in the Inductor (typically 30% of the maximum output current) (A)

The conduction losses for high-side MOS transistor are estimated in Equation 5-10:

EQUATION 5-10: CONDUCTION LOSSES FOR HIGH-SIDE MOSFET

$$P_{COND\ High\text{-}Side} = I_{RMS\ High\text{-}Side}^2 \times R_{DS(on)HS(max)}$$

The switching losses are more difficult to calculate, since they depend on many parameters. Equation 5-11 shows an estimation of these losses:

EQUATION 5-11: SWITCHING LOSSES FOR HIGH-SIDE MOSFET

$$P_{SW\ High\text{-}Side} = \left(\frac{V_{IN} \times I_{OUT}}{2} \right) \times (t_{s(HL)} + t_{s(LH)}) \times f_{SW}$$

Where:

- V_{IN} = Input Voltage (V)
- I_{OUT} = Output Current (A)
- f_{SW} = Switching Frequency (Hz)
- $t_{s(HL)}$ = MOSFET Switching Time (High-to-Low transition) (s)
- $t_{s(LH)}$ = MOSFET Switching Time (Low-to-High transition) (s)

The $t_{s(HL)}$ and $t_{s(LH)}$ times can be estimated using the following equations:

EQUATION 5-12:

$$t_{s(HL)} = \frac{Q_{G(Total)}}{I_{DRV_{Sink}}}$$

$$t_{s(LH)} = \frac{Q_{G(Total)}}{I_{DRV_{Source}}}$$

Where:

- $Q_{G(Total)}$ = High-side MOSFET Total Gate Charge
- $I_{DRVSink}$ = Sink Peak Current for High-Side Driver (typical 1A)
- $I_{DRVSource}$ = Source Peak Current for High-Side Driver (typical 1A)

The total power losses for the high-side MOSFET can be calculated with Equation 5-13:

EQUATION 5-13: TOTAL POWER LOSSES FOR HIGH-SIDE MOSFET

$$P_{Loss\ High\text{-}Side} = P_{COND\ High\text{-}Side} + P_{SW\ High\text{-}Side}$$

For applications that operate with low duty cycle (lower than 30%) or high input voltage, the power losses for the high-side transistor are mainly switching losses. For these applications, it is recommended to choose a MOSFET that offers a low Total Gate Charge.

For applications that operate with duty cycles higher than 50%, the power losses for the high-side transistor are mainly conduction losses. For these applications, choose a MOSFET that has a low $R_{DS(on)}$.

The low-side MOSFET (synchronous rectifier) is “soft-commutated” by the energy stored in the inductor , thus reducing the switching losses. For the low-side transistor, the power losses mainly consist of conduction losses, body diode conduction losses and body diode reverse recovery losses.

Similarly to the high-side, the RMS current that pass through the low-side MOSFET is calculated using Equation 5-14:

EQUATION 5-14: RMS CURRENT FOR LOW-SIDE MOSFET

$$I_{RMS\ Low\text{-}Side} = \sqrt{(1-D) \times \left(I_{OUT}^{2} + \frac{I_{Ripple}^{2}}{12} \right)}$$

Where:

D = Duty Cycle

I_{OUT} = Output Current (A)

I_{Ripple} = Current Ripple in the Inductor (typically 30% of the maximum output current) (A)

The conduction losses for low-side MOS transistor are estimated in Equation 5-15:

EQUATION 5-15: CONDUCTION LOSSES FOR LOW-SIDE TRANSISTOR

$$P_{COND\ Low\text{-}Side} = I_{RMS\ Low\text{-}Side}^{2} \times R_{DS(on)LS(max)}$$

The body diode conduction loss is calculated in Equation 5-16:

EQUATION 5-16: BODY DIODE CONDUCTION LOSSES

$$P_{LOSS\ BD} = I_{OUT} \times V_F \times t_{BD} \times f_{SW}$$

Where:

V_F = Forward Voltage of the Body Diode (V)

t_{BD} = Total Conduction Time for Body Diode (s)

The body diode recovery time losses will be calculated using Equation 5-17:

EQUATION 5-17: BODY DIODE REVERSE RECOVERY LOSSES

$$P_{RR} = \frac{Q_{RR} \times V_{IN} \times f_{SW}}{2}$$

Where:

Q_{RR} = Reverse Recovery Charge of the Body Diode (C)

The total power loss for the low-side MOSFET can now be estimated by summing the power losses in Equation 5-18:

EQUATION 5-18: TOTAL POWER LOSS FOR LOW-SIDE MOSFET (SR)

$$P_{Loss\ Low\text{-}Side} = P_{COND\ Low\text{-}Side} + P_{LOSS\ BD} + P_{RR}$$

The conduction losses are the dominant part of the total losses for the low-side transistor; choose a MOSFET with a low $R_{DS(on)}$.

The body diode conduction and reverse recovery losses can be greatly minimized by reducing the Dead Times necessary to prevent the shoot-through. This can be achieved by choosing transistors that have a very low Figure of Merit (FOM) MOSFET for both sides.

5.2.7 BOOTSTRAP CAPACITOR SELECTION

The selection of the bootstrap capacitor is based upon the total gate charge of the high-side power MOSFET and the allowable droop in gate drive voltage while the high-side power MOSFET is conducting (see Equation 5-19).

EQUATION 5-19: BOOTSTRAP CAPACITOR

$$C_{BOOT} = \frac{Q_{G(Total)}}{\Delta V_{DROOP}}$$

Where:

$Q_{G(Total)}$ = High-side MOSFET Total Gate Charge (C)

ΔV_{DROOP} = Allowable Gate Drive Voltage Droop (V)

It is recommended that the voltage droop does not exceed 50 mV. A low ESR, ceramic capacitor, rated at least 16 V_{DC}, is recommended.

5.2.8 FEEDBACK LOOP COMPENSATION

Since the MCP19035 implements a Voltage-Mode PWM control, a Type-III compensation network is recommended. Correct placing of poles and zeros require analysis of the Bode plots for the buck converter power train.

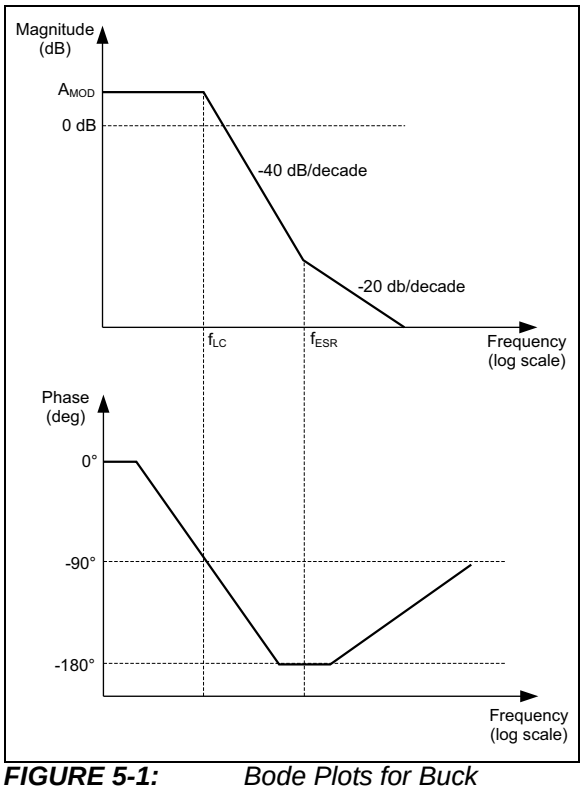


FIGURE 5-1: *Bode Plots for Buck Converter Power Train (Representation Using Asymptotes).*

The power train of a buck converter that uses voltage mode control is a second order system. At the LC resonance frequency, a double pole occurs; this pole will “push” the gain down with a slope of -40db/decade. This double pole also introduces a phase lag of -180°. The compensation network must counteract the effects of this double pole in order to achieve the stability of the system.

The Equivalent Series Resistance (ESR) of the output capacitor introduces a zero that “pushes” the gain and phase up again. This zero helps the stability of the system if it occurs before the phase reaches the critical point of -180°. However, due to the performance criteria (output voltage ripple, efficiency), the application requires the use of low ESR capacitors. For capacitors that have very low ESR (ceramic capacitors), this zero occurs at high frequency, where the phase reaches the critical point.

The frequencies for pole and zero are determined using Equation 5-20:

EQUATION 5-20: POLE AND ZERO FREQUENCIES

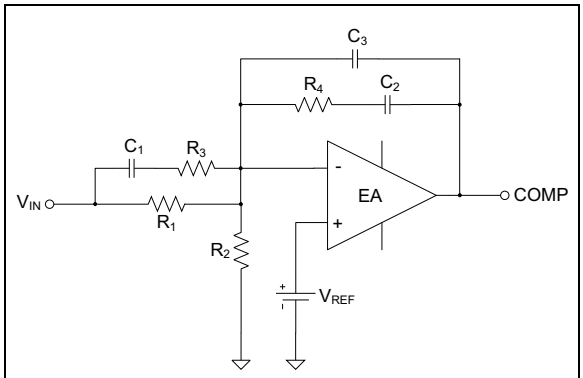
$$f_{LC} = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

EQUATION 5-21: PWM MODULATOR GAIN

$$A_{MOD} = 20 \times \log\frac{V_{IN}}{\Delta V_{RAMP}} = 20 \times \log V_{IN}$$

The Type-III compensation network is represented in Figure 5-2:



Where:

$$G(s) = \frac{R_1 + R_3}{R_1 \times R_3 \times C_1} \times \frac{\left(s + \frac{1}{R_4 \times C_2}\right) \times \left(s + \frac{1}{(R_1 \times R_3) \times C_1}\right)}{s \times \left(s + \frac{(C_2 + C_3)}{R_4 \times C_2 \times C_3}\right) \times \left(s + \frac{1}{R_3 \times C_1}\right)}$$

FIGURE 5-2: *Type-III Compensation Network.*

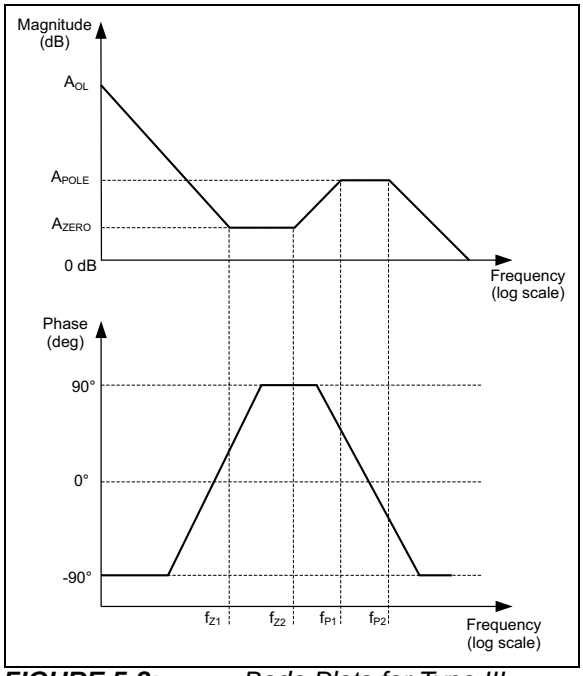


FIGURE 5-3: *Bode Plots for Type III Compensation Network (Representation Using Asymptotes).*

Assuming $C_3 \ll C_2$ and $R_3 \ll R_1$, the pole and zero frequencies can be calculated using Equation 5-22:

EQUATION 5-22: POLE AND ZERO FREQUENCIES OF THE COMPENSATION NETWORK

$$f_{Z1} = \frac{1}{2\pi \times (R_1 + R_3) \times C_1} \cong \frac{1}{2\pi \times R_1 \times C_1}$$

$$f_{Z2} = \frac{1}{2\pi \times R_4 \times C_2}$$

$$f_{P1} = \frac{1}{2\pi \times R_4 \times \left(\frac{C_2 \times C_3}{C_2 + C_3}\right)} \cong \frac{1}{2\pi \times R_4 \times C_3}$$

$$f_{P2} = \frac{1}{2\pi \times R_3 \times C_1}$$

EQUATION 5-23: ZERO GAIN

$$A_{ZERO} = 20 \times \log \frac{R_4}{R_1}$$

EQUATION 5-24: POLE GAIN

$$A_{POLE} = 20 \times \log \frac{R_4 \times (R_1 + R_3)}{R_1 \times R_3}$$

The Type-III compensation network provides two zeros and three poles (including origin pole), pushing the cross-over frequency as high as possible, and boosts the phase margin of the system to greater than 45°. A higher bandwidth yields a faster load transient response. The faster transient response results in a smaller output voltage overshoot.

The procedure for placing the poles and zeros to achieve the optimum phase margin are presented below:

1. Determine the frequency of the double pole (LC pole) and ESR zero using Equation 5-20.
2. Choose resistor R_1 (usually between 10 kΩ and 100 kΩ). This value is a compromise between high values for additional capacitors (higher cost) and possible noise induced problems.
3. Resistor R_2 is calculated using Equation 5-25:

EQUATION 5-25: FEEDBACK RESISTOR DIVIDER

$$R_2 = \frac{V_{REF} \times R_1}{V_{OUT} - V_{REF}} = \frac{0.6 \times R_1}{V_{OUT} - 0.6}$$

4. Choose the crossover frequency of the compensated system. This frequency is recommended to be between 1/10th and 1/5th of the switching frequency (f_{SW}). A higher crossover frequency will improve the transient response, but will decrease the phase margin. For most of the applications, the crossover frequency is set around 1/10th of switching frequency. This is a reasonable compromise between simplifying the design of the compensation loop and achieving a fast transient response. Since the frequency of the ESR zero is much higher than LC resonant frequency, the gain of the power train can be typically approximated at the crossover frequency, using Equation 5-26:

EQUATION 5-26: POWER TRAIN GAIN AT CROSSOVER FREQUENCY

$$A_{PT_{CO}} = A_{MOD} - 40 \times \log\left(\frac{f_{CO}}{f_{LC}}\right)$$

The compensated error amplifier must have a gain equal to A_{PTco} at crossover frequency (f_{CO}). Typically, this crossover frequency occurs between F_{Z2} and F_{P1} (see Figure 5-3).

5. The first zero of the compensation network must be placed at the f_{LC} frequency. The capacitor C_1 is calculated using Equation 5-27:

EQUATION 5-27: CAPACITOR C_1

$$C_1 = \frac{\sqrt{L \times C_{OUT}}}{R_1}$$

6. The value of the resistor R_4 is estimated using Equation 5-28:

EQUATION 5-28: RESISTOR R_4

$$R_4 = \frac{f_{CO}}{f_{LC}} \times \frac{1}{V_{IN}} \times R_1$$

Where:

f_{CO} = cross-over frequency for the compensated system (usually 1/10th of f_{SW})

7. The second zero of the compensation network must be placed at half of the f_{LC} frequency. The value of the capacitor C_2 is calculated in Equation 5-29:

EQUATION 5-29: CAPACITOR C_2

$$C_2 = 2 \times \frac{\sqrt{L \times C_{OUT}}}{R_4}$$

8. The first pole of the compensation network must be placed at f_{SW}. The value of C_3 is calculated in Equation 5-30:

EQUATION 5-30: CAPACITOR C_3

$$C_3 = \frac{1}{2 \times \pi \times R_4 \times f_{SW}}$$

9. The second pole of the compensation network must be placed at half of the f_{SW} .The value for resistor R_3 is calculated in Equation 5-31:

EQUATION 5-31: RESISTOR R_3

$$R_3 = \frac{1}{\pi \times C_1 \times f_{SW}}$$

The compensation circuit can be simulated with any available simulator. The values of the components can be adjusted to meet the initial design parameters (crossover frequency and phase margin). It is also necessary to ensure that the gain of the compensation circuit does not exceed the gain of the error amplifier. Due to the interactions between poles and zeros, it is highly recommended to use the design tool provided by Microchip Technology Inc. to design and analyze the compensation network.

5.3 Operation with Low Input Voltages

If the application requires an input voltage below 5.5V, it is recommended to use the alternative schematic depicted in Figure 5-4.

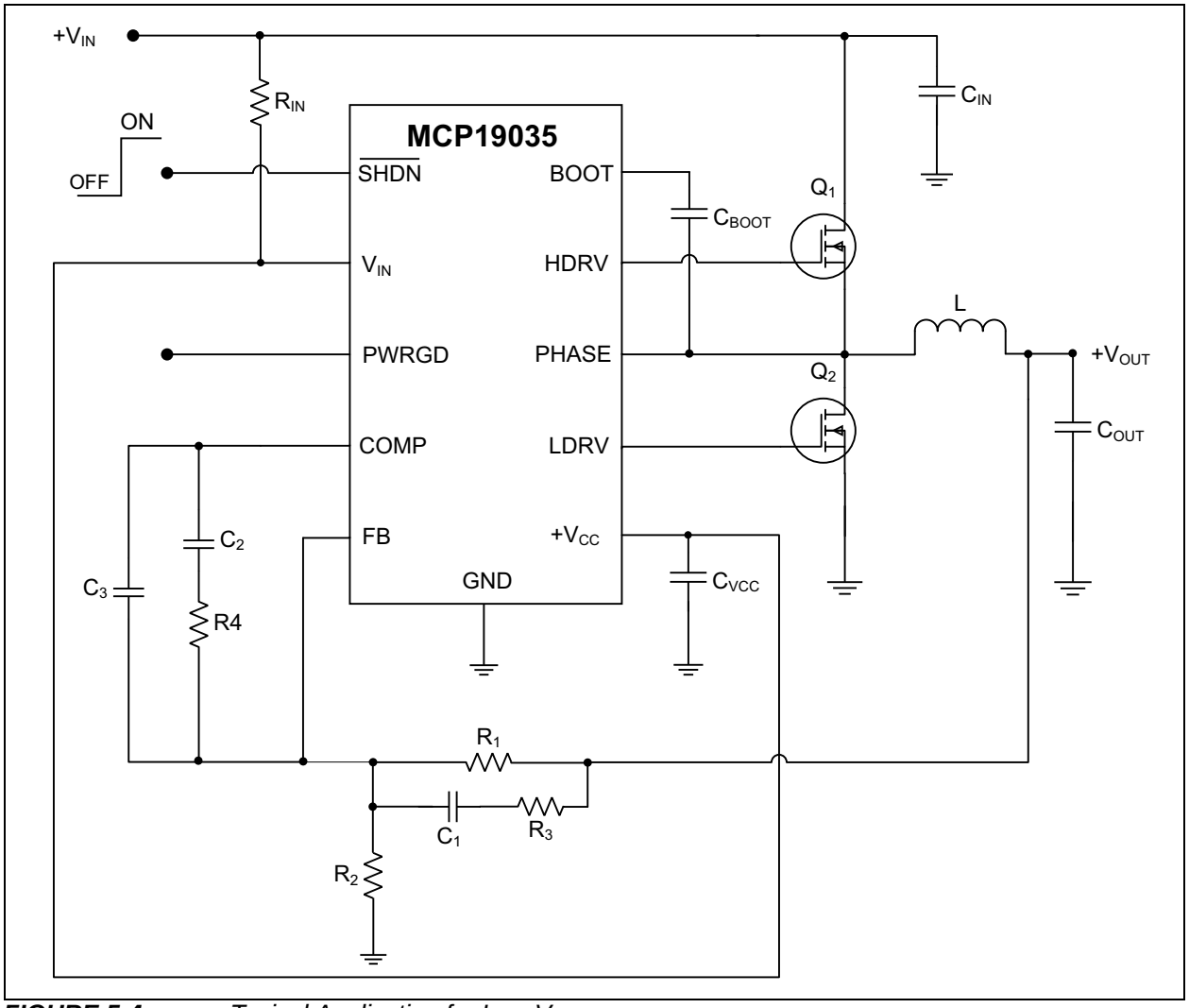


FIGURE 5-4: *Typical Application for Low V_{IN}.*

This connection avoids the voltage drop on the internal voltage regulator, ensuring the correct driving of the MOSFETs at low input voltage.

Additional care must be exercised when this alternative schematic is used to minimize the input voltage ripple/noise. The internal circuitry of the MCP19035 may be affected by the ripple/noise present on the V_{CC} pin. The R_{IN} resistor together with C_{VCC} capacitor form a low-pass filter for the bias voltage (V_{CC} voltage). The recommended value range for this resistor is between 2.2Ω and 10Ω.

6.0 DESIGN EXAMPLE

This example illustrates the step-by-step design procedure for a 12V to 1.8V synchronous buck converter using the MCP19035 controller. To minimize the design effort, Microchip provides a design tool that is used to calculate the component values. See AN1452 - *"Using the MCP19035 Synchronous Buck Converter Design Tool"* for further details (DS01452).

The electrical parameters are detailed in Table 6-1.

TABLE 6-1: DESIGN EXAMPLE ELECTRICAL SPECIFICATION

Parameter	Test Conditions	Min	Nominal	Max	Unit
Input Voltage (V_{IN})		8	12	14	V
Output Voltage (V_{OUT})	$0 \le I_{OUT} \le 15A$	—	1.8	—	V
Line Regulation	$8.0V \le V_{IN} \le 14V$	—	—	0.5	%
Load Regulation	$0A \le I_{OUT} \le 15A$	—	—	0.5	%
Output ripple (V_{OUT_RIPPLE})	I_{OUT} = 15A	—	—	30	mV
Input ripple (V_{IN_RIPPLE})	I_{OUT} = 15A	—	—	0.3	V
Output overshoot	Step from 3.75A to 11.25A	—	—	100	mV
Output undershoot	Step from 11.25A to 3.75A	—	—	100	mV
Output current (I_{OUT})		0	—	15	A
Efficiency	V_{IN} = 12V, I_{OUT} = 10A	90	—	—	%

6.0.1 INDUCTOR SELECTION

The inductor must be sized for a typical ripple current that is around 30% of maximum output current. The inductor value calculated with Equation 5-1 is 1.16 µH. To compensate against component tolerance, choose the next higher standard value 1.5 µH (typically 20% for high current inductors).

The peak current in the inductor can be calculated with Equation 5-2, its value being 17.25A. The inductor must sustain, without saturating, this peak current. To maintain low-conduction losses, the DC resistance of the inductor must be as low as possible. Table 6-2 shows some suitable inductors for this application.

TABLE 6-2: SUITABLE INDUCTORS FROM VARIOUS VENDORS

Vendor	Part Number	Inductance (µH)	DCR (mΩ)	I_{SAT} (A)
Coilcraft®	XAL1010-152MEB	1.5	1.76	36.6
Wurth Elektronik®	7443320150	1.5	2.1	27
TDK - EPC®	B82559A0142A013	1.4	1.5	22
Bourns®	SRP1270-1R5M	1.5	2.1	48

6.0.2 INPUT CAPACITOR SELECTION

The converter operates with a maximum duty cycle of 22.5%. A ceramic capacitor (X7R dielectric) with a 10 mΩ ESR (typical) will be used. The minimum capacitance for input capacitor, calculated in Equation 5-4, is 32.7 µF. Use two standard 22 µF capacitors (X7R) rated at 25V_{DC} in parallel.

6.0.3 OUTPUT CAPACITOR SELECTION

Based on a step load from 25% to 75% of the maximum output current, the minimum value for the output capacitor can be determined with Equation 5-7. The minimum value is 456 µF. Choose the next higher standard value (500 µF). The ESR of the output capacitor will strongly affect the output voltage ripple. Use five 100 µF standard ceramic capacitors (X7R or X5R dielectric) rated at 6.3V_{DC} in parallel. The estimated final value of the ESR is lower than 5 mΩ. The output voltage ripple is now estimated with Equation 5-6.

6.0.4 MOSFETS SELECTION

Before the MOSFET selection, the total losses of the converter should be estimated. For this application, the input power can be estimated using Equation 6-1:

EQUATION 6-1: INPUT POWER

$$P_{IN} = \frac{U_{OUT} \times I_{OUTmax}}{Eff}$$

The total power losses are estimated in Equation 6-2:

EQUATION 6-2: TOTAL CONVERTER LOSSES

$$P_{LOSS} = P_{IN} - P_{OUT}$$

To achieve the efficiency goal (90%), the total power losses must be lower than 2W at 10A output current. Table 6-3 shows how these losses are distributed over the converter components. The power losses distribution varies with the design parameters. As a rule of thumb, for designs that have higher conversion ratio (low duty cycles), the losses for the high-side MOSFET are mainly switching losses. For the low side, most of the losses will be the conduction losses.

TABLE 6-3: ESTIMATION OF THE POWER LOSSES DISTRIBUTION

Component	Losses (%)
High-Side MOSFET	36
Low-Side MOSFET	40
Inductor	10
Input Capacitor	2
Output Capacitor	1
PWM Controller	10
Traces DC Resistance	1

An important part of the total power losses (over 75%) are dissipated by the MOSFETs.

For the high-side MOSFET, the total amount of losses (conduction and switching losses) should not exceed 0.72W. This design has a higher conversion ratio (greater than 7:1), thus most of the losses of the high-side MOSFET will be switching losses. As a rule of thumb, the switching losses will be considered to be 70% of the total losses.

The conduction losses for the high-side MOSFET are estimated in Equation 5-10. High-side MOSFET conduction losses are high at low input voltages. The maximum $R_{DS(on)}$ for the high-side MOSFET is:

EQUATION 6-3: MAXIMUM HIGH-SIDE $R_{DS(ON)}$

$$R_{DS(on)} = \frac{P_{LOSS\ High-Side}}{I_{RMS\ High-Side}^{2}} \times 0.3$$

For this design, where $I_{RMS\ High-Side}$ = 3.9A at 12V input voltage and 10A output current, the high-side MOSFET should have a $R_{DS(On)}$ lower than 14 mΩ.

For the high-side MOSFET, most of the losses are switching losses (70%). The maximum total gate charge for the high-side MOSFET is:

EQUATION 6-4: MAXIMUM TOTAL GATE CHARGE FOR THE HIGH-SIDE MOSFET

$$Q_{G(Total)} = \frac{P_{LOSS\ High-Side}}{V_{IN(Max)} \times I_{OUT} \times f_{SW}} \times 0.7$$

The maximum Total Gate Charge ($Q_{G(Total)}$) at 4.5V V_{GS} should be lower than 12 nC (calculated for 10A output current).

For the low-side MOSFET, losses are mainly conduction losses. As a rule of thumb, the conduction losses are considered to be 85% of the total losses. For this design, the maximum power losses (estimated at 12V input voltage and 10A output current) for low-side should be lower than 0.9W. Estimate the maximum $R_{DS(On)}$ for the low-side MOSFET using Equation 6-5:

EQUATION 6-5: MAXIMUM $RD_{(ON)}$ OF LOW-SIDE MOSFET

$$R_{DS(on)} = \frac{P_{LOSS\ Low-Side}}{I_{RMS\ Low-Side}^{2}} \times 0.85$$

In this design, $I_{RMS\ Low-Side}$ = 9.3A at 12V input voltage, 10A output current and the maximum $R_{DS(On)}$ for low-side MOSFET = 7.8 mΩ.

For this design, Microchip's MCP87050 and MCP87022 high-performance MOSFETs can be used. Calculate the total losses introduced by these transistors using the provided equations. For the high-side MOSFET (MCP87050), the total loss is 0.66W. The low-side MOSFET (MCP87022) will dissipate a 0.3W loss.

6.0.5 BOOTSTRAP CAPACITOR SELECTION

From Equation 5-19, the value of the Bootstrap Capacitor should be higher than 276 nF. Choose the standard value 330 nF ceramic capacitor (X7R) rated at 16 V_{DC}.

6.0.6 DEAD TIME (DT) SELECTION

The MOSFET used in this design has a low Figure of Merit parameter. The overall efficiency of the converter can be improved by choosing the MCP19035 with optimized Dead Time.

6.0.7 OVERCURRENT PROTECTION THRESHOLDS

The MCP19035 controller provides two fixed threshold for high and low-side overcurrent protection circuits. These thresholds are 480 mV (typical) for high-side and 180 mV (typical) for the low-side. The peak current for the high-side is:

EQUATION 6-6: MAXIMUM PEAK CURRENT FOR A HIGH-SIDE MOSFET

$$I_{MAX_{HS}} = \frac{0.48}{R_{DS(on)HS}}$$

For this design, the maximum peak current that flows into the high-side MOSFET is 87A.

The peak current for the low-side MOSFET is:

EQUATION 6-7: MAXIMUM PEAK CURRENT FOR A LOW-SIDE MOSFET

$$I_{MAX_{LS}} = \frac{0.18}{R_{DS(on)LS}}$$

For this design, the maximum peak current that flows into the low-side MOSFET is 81A.

6.0.8 FEEDBACK LOOP COMPENSATION

For this design, the crossover frequency is 30 kHz, while the resonant frequency of LC tank is 5.88 kHz. With these parameters, and following the design procedure described in **Section 5.2, Design Procedure**, the value for compensation network components can be calculated.

TABLE 6-4: COMPENSATION NETWORK COMPONENTS

Component	Value	Standard Value
R_1	20 kΩ	20 kΩ
R_2	10 kΩ	10 kΩ
R_3	0.774 kΩ	0.75 kΩ
R_4	8.6 kΩ	8.2 kΩ
C_1	1.37 nF	1.2 nF
C_2	6.36 nF	6.8 nF
C_3	61 pF	68 pF

The components used for the compensation network must be of good quality and tolerance. The recommended dielectric for capacitors is C0G and the tolerance 5%. The recommended tolerance for resistors is 1%.

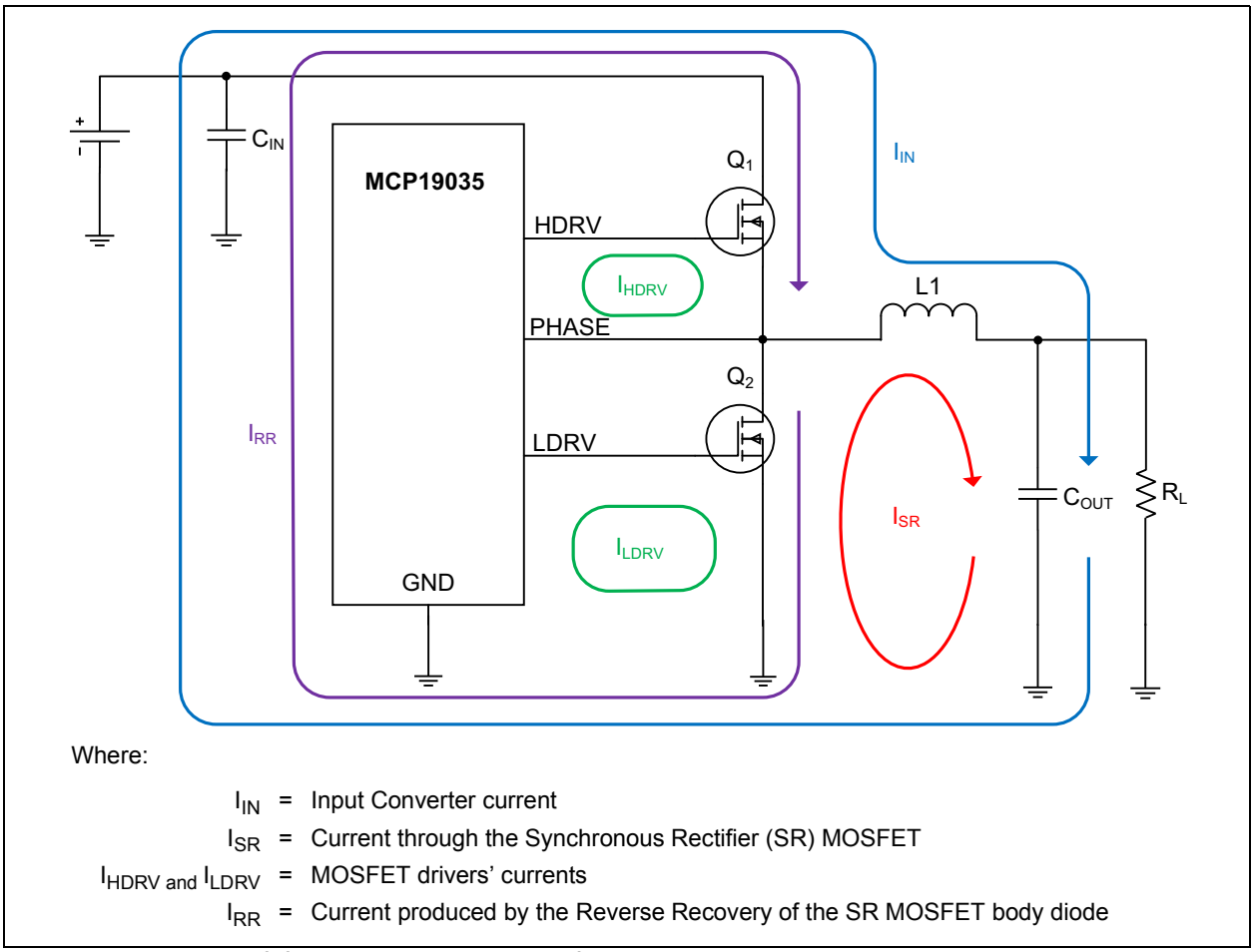
6.0.9 LAYOUT RECOMMENDATIONS

Good printed circuit board layout techniques are important to any switching circuitry, and switching power supplies are no different. Here are the guidelines for the PCB layout:

- The exposed pad of MCP19035 DFN case is the only connection to the internal device ground. Connect this pad directly to the board ground plane.
- Place at least four vias in the exposed pad land to help remove heat from the device.
- Use separate grounds for power and signal paths. Keep high current paths away from sensitive components and nodes (ex. feedback and compensation network components).
- Four layer PCBs are highly recommended to obtain optimum results regarding noise/EMI. Use an internal layer as ground plane.

- For double layer boards, a single ground plane (usually the bottom) is recommended.
- Use short, wide traces for the MOSFET's gate drive connection (LDRV and HDRV signals).
- Place the main MOSFET (control/high-side MOSFET) as close as possible to the input capacitors.
- Minimize the connections between MOSFETs, the inductor and the MCP19035 case (PHASE node). Place this node over a ground plane to minimize the radiated noise.
- Place the compensation network components near the MCP19035 case and connect these components to a low noise ground (signal ground).
- Locate the V_{IN} decoupling capacitor close to the MCP19035 case.
- Locate the Bootstrap Circuit capacitor close to the MCP19035 case.
- Minimize the area of high frequency current loops.

Figure 6-1 helps the PCB designer to identify the main high frequency current paths for the Synchronous Buck Converter.



Where:

I_{IN} = Input Converter current

I_{SR} = Current through the Synchronous Rectifier (SR) MOSFET

I_{HDRV} and I_{LDRV} = MOSFET drivers' currents

I_{RR} = Current produced by the Reverse Recovery of the SR MOSFET body diode

FIGURE 6-1: *High Frequency Current Paths.*

All these currents contain high-frequency components and can produce EMI. Minimizing the area of these loops will reduce the radiated noise.

The Reverse Recovery of the SR MOSFET Body Diode current is an important source of noise and EMI. This current, although very short (less than 10 ns), can easily reach a few hundred amps, especially when using low ESR capacitors for input bypass and very fast MOSFETs for switching transistors. If this current passes through a path that has a high inductance, it will produce an intense voltage ringing.

For noise sensitive applications (for example, RF applications) the excessive voltage ringing in the PHASE node produced by Reverse Recovery of SR MOSFET Body Diode can be reduced by placing a low-value resistor in series with the bootstrap capacitor. This resistor will slow down the high-side MOSFET during low-to-high transition, reducing the slew rate of the SW node signal. The recommended value for this resistor is between 2.2Ω and 10Ω, and should be determined by lab measurements. The penalty of including this resistor is an efficiency reduction. It should, however, be no more than 0.5%.

Figures 6-2 and 6-3 show the difference between PHASE node voltage with and without this resistor.

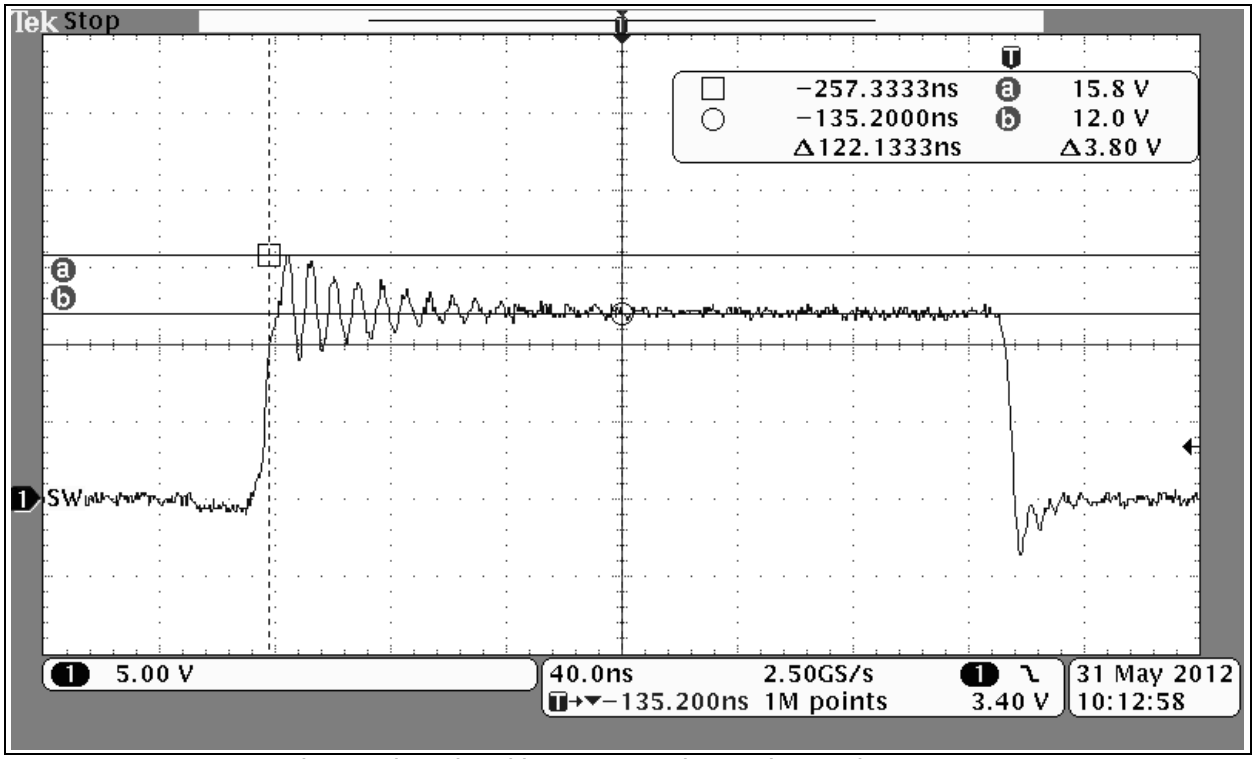


FIGURE 6-2: *SW (PHASE) Node With Boot Capacitor Series Resistor.*

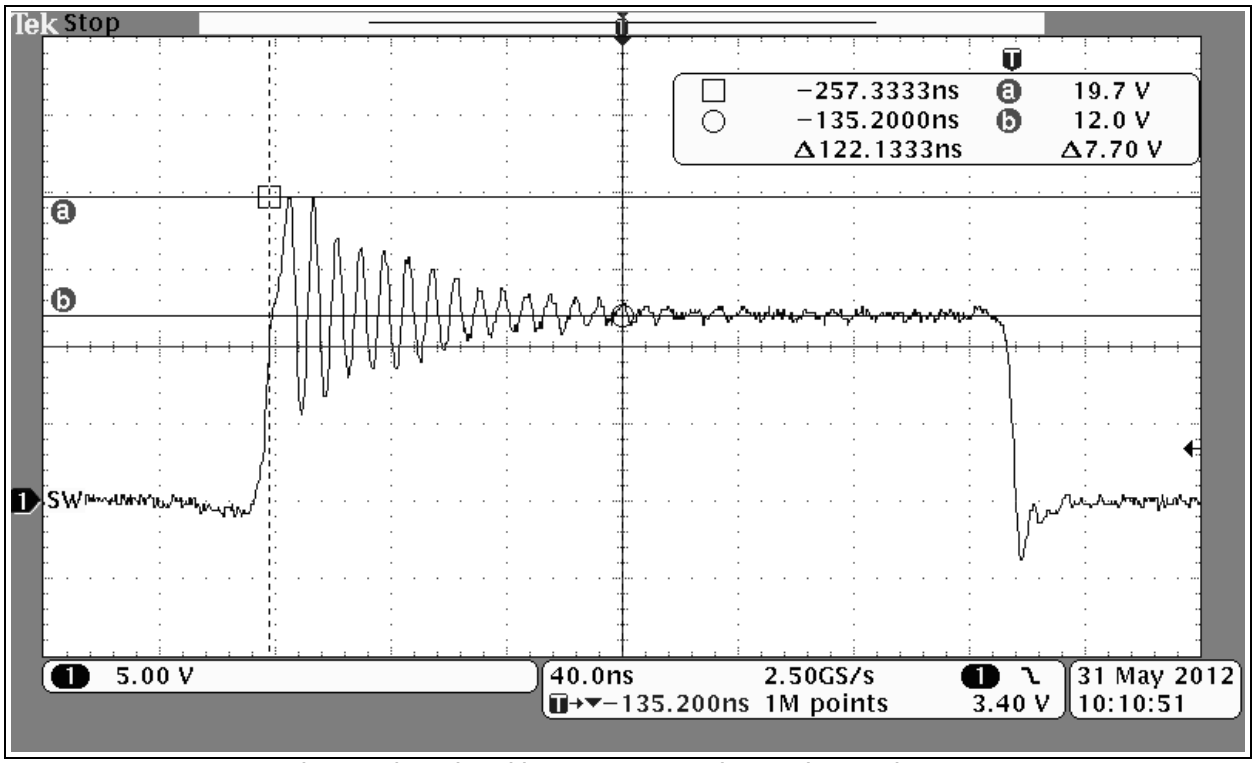


FIGURE 6-3: *SW (PHASE) Node Without Boot Capacitor Series Resistor.*

6.0.10 SCHEMATIC AND BILL OF MATERIALS

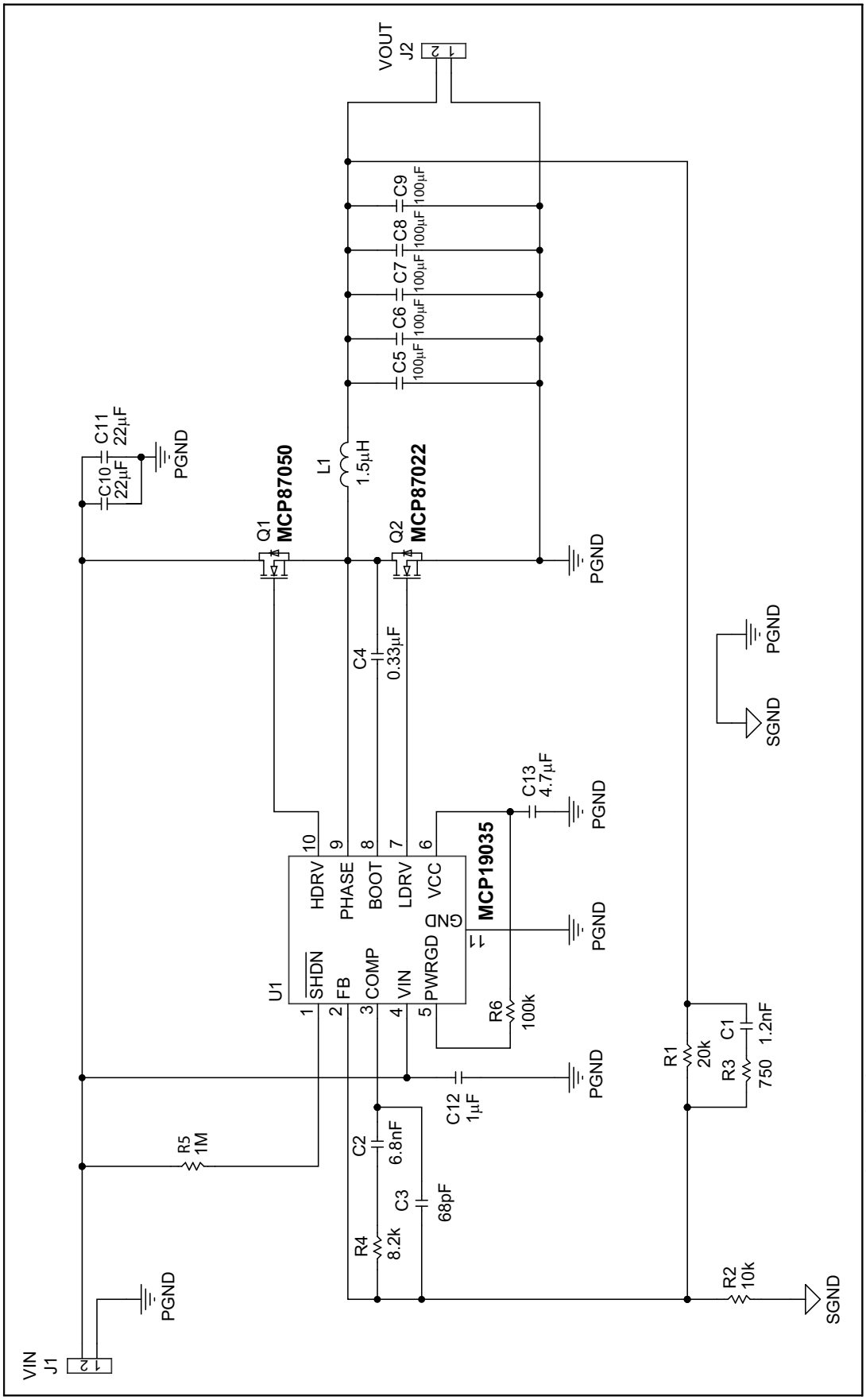


FIGURE 6-4: *Schematic Diagram.*

TABLE 6-5: BILL OF MATERIALS

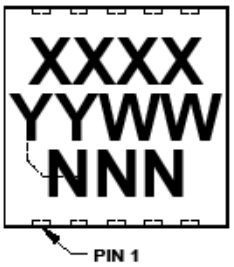
Qty	Reference	Value	Manufacturer	Manufacturer Part Number	Description
1	C1	1.2 nF	KEMET® Electronic Corp.	C0603C122J1GACTU	Cap. Ceramic 1200 PF 100V 5% NP0 0603
1	C2	6.8 nF	KEMET Electronic Corp.	C0603C682J5GACTU	Cap. Ceramic 6800 PF 50V 5% NP0 0603
1	C3	68 pF	KEMET Electronic Corp.	C0603C680J1GACTU	Cap. Ceramic 68 PF 100V 5% NP0 0603
1	C4	0.33 µF	MURATA Electronics®	GRM188R71C334KA01D	Cap. Ceramic 0.33 µF16V 10% X7R 0603
5	C5, C6, C7, C8, C9	100 µF	TDK® Corporation	C3225X5R0J107M	Cap. Ceramic 100 µF 6.3V 20% X5R 1210
2	C10, C11	22 µF	MURATA Electronics	GRM32ER71E226KE15L	Cap. Ceramic 22 µF 25V 10% X7R 1210
1	C12	1 µF	TDK Corporation	CGA4J3X7R1V105K	Cap. Ceramic 1 µF 35V 10% X7R 0805
1	C13	4.7 µF	TDK Corporation	C2012X5R1E475K	Cap. Ceramic 4.7 µF 25V X5R 0805
2	J1, J2		On-Shore Technology Inc.	ED120/2DS	Terminal Block 5.08 mm Vert. 2 POS
1	L1	1.5 µH	Wurth Electronik Group	7443320150	Inductor Power 1.5 µH 19.5A SMD
1	Q1		Microchip Technology Inc.	**MCP87050T-U/MF**	High-Speed N-Channel Power MOSFET, 5x6 mm PDFN
1	Q2		Microchip Technology Inc.	**MCP87022T-U/MF**	High-Speed N-Channel Power MOSFET, 5x6 mm PDFN
1	R1	20 kΩ	Panasonic® - ECG	ERJ-3EKF2002V	Res. 20k Ohm 1/10W 1% 0603 SMD
1	R2	10 kΩ	Panasonic - ECG	ERJ-3GEYJ103V	Res. 10k Ohm 1/10W 5% 0603 SMD
1	R3	750Ω	Vishay®/Dale Intertechnology	CRCW0603750RFKEA	Res. 750 OHM 1/10W 1% 0603 SMD
1	R4	8.2 kΩ	Panasonic - ECG	ERJ-3EKF8201V	Res. 8.2k Ohm 1/10W 1% 0603 SMD
1	R5	1 MΩ	Panasonic - ECG	ERJ-3EKF1004V	Res. 1M Ohm 1/10W 1% 0603 SMD
1	R6	100 kΩ	Panasonic - ECG	ERJ-3EKF1003V	Res. 100k Ohm 1/10W 1% 0603 SMD
1	U1		Microchip Technology Inc.	**MCP19035-AAABE/MF**	High Speed Synchronous Buck Controller

NOTES:

7.0 PACKAGING INFORMATION

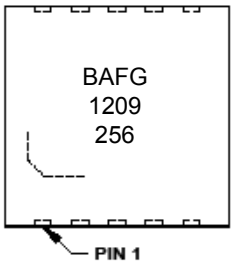
7.1 Package Marking Information

10-Lead DFN (3x3x0.9 mm)



Part Number	Code
MCP19035-AAAAE/MF	BAFG
MCP19035T-AAAAE/MF	BAFG
MCP19035-AAABE/MF	BAFP
MCP19035T-AAABE/MF	BAFP
MCP19035-BAAAE/MF	BAFH
MCP19035T-BAAAE/MF	BAFH
MCP19035-BAABE/MF	BAFQ
MCP19035T-BAABE/MF	BAFQ

Example:

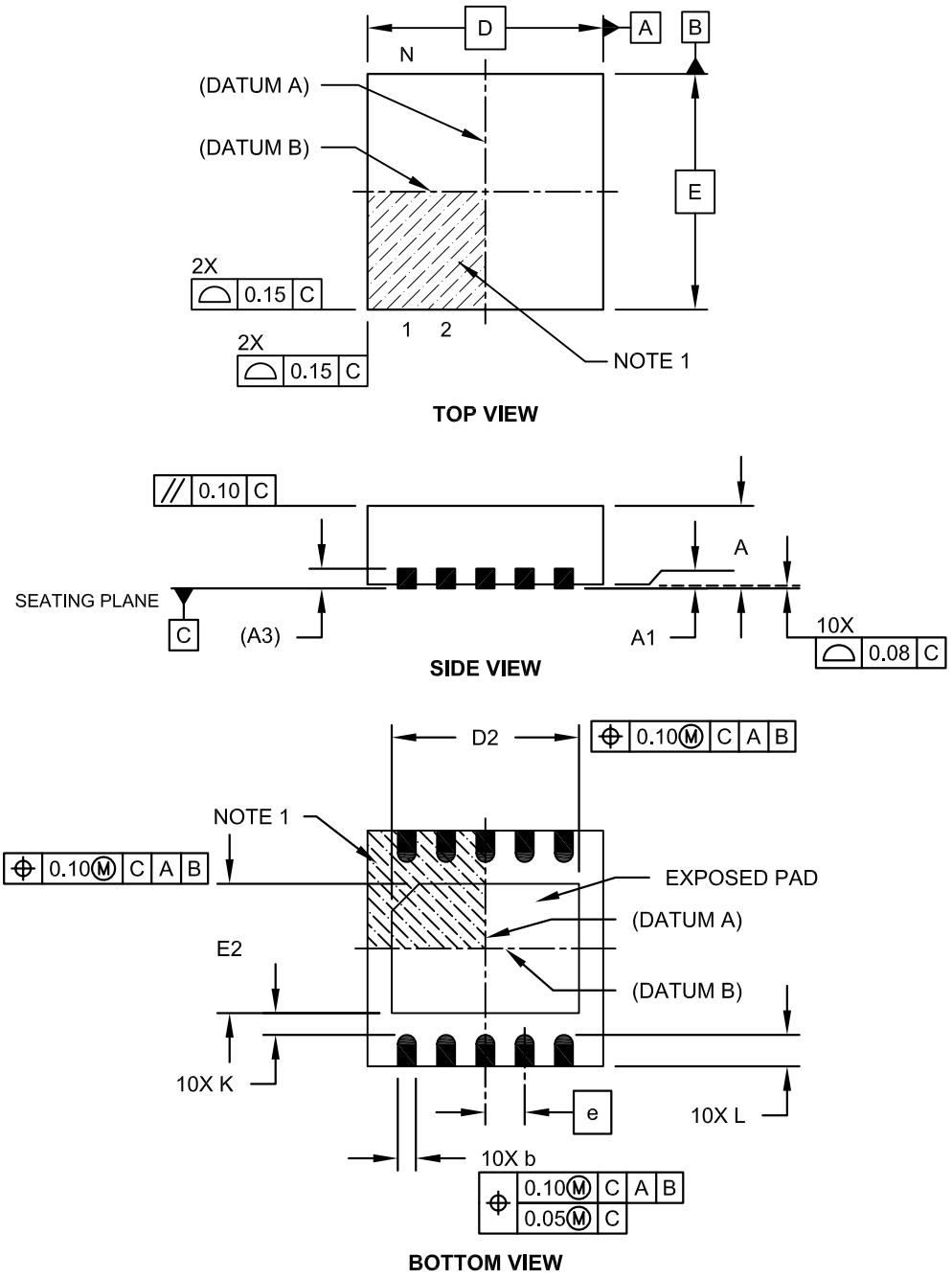


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

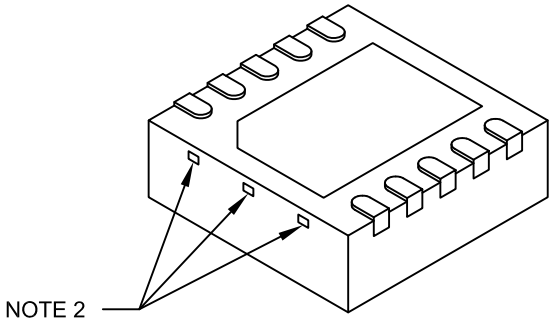
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-063C Sheet 1 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.15	2.35	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.40	1.50	1.75
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

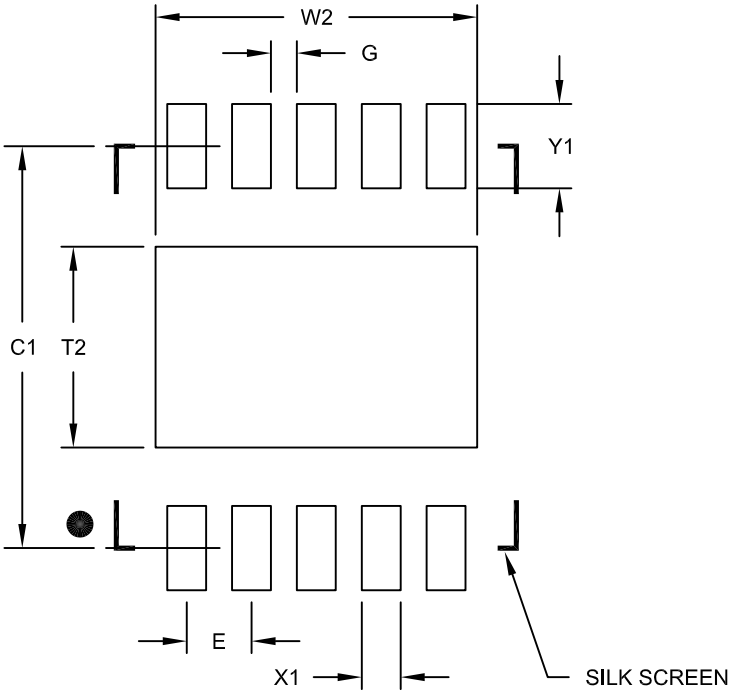
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			2.48
Optional Center Pad Length	T2			1.55
Contact Pad Spacing	C1		3.10	
Contact Pad Width (X10)	X1			0.30
Contact Pad Length (X10)	Y1			0.65
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B

APPENDIX A: REVISION HISTORY

Revision B (March 2013)

The following is the list of modifications:

1. Added the 600 kHz option Switching Frequency parameter and related information throughout the document.
2. Updated the DC Electrical Characteristics table to reflect the 600 kHz option for the Switching Frequency parameter.
3. Updated Figure 2-1, Figure 2-3, and Figure 2-10.
4. Updated **Section 4.4 "Internal Oscillator"**.
5. Updated the Switching Frequency value in Equation 4-1.
6. Updated **Section 4.11 "Soft Start"**.
7. Updated Figure 4-3.
8. Added a note to **Section 4.12 "Pre-Bias Load Start-up"**.
9. Updated **Section 5.2.1 "Switching Frequency and the Maximum Conversion Ratio"**.
10. Updated **Section 7.1 "Package Marking Information"** with the 600 kHz Switching Frequency option markings.
11. Updated the Product Identification System page with the 600 kHz Switching Frequency option marking information.

Revision A (November 2012)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	X	X	X	X	/XX
Device	Switching Frequency	Reference Voltage	LDRV OC Threshold	Dead Time	Temperature Range	Package

Device:	MCP19035:	High-Speed Synchronous Buck Controller
	MCP19035T:	High-Speed Synchronous Buck Controller (Tape and Reel)
Switching Frequency:	A	=300 kHz
	B	=600 kHz
Reference Voltage:	A	=600 mV
LDRV OC Threshold:	A	=200 mV
Dead Time:	A	=20 ns
	B	=12 ns
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	MF	= Plastic Dual Flat, No Lead Package - 3x3x0.9 mm, 10-Lead

Examples:

a) MCP19035-AAAAE/MF: 300 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 20 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

b) MCP19035T-AAAAE/MF: Tape and Reel, 300 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 20 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

c) MCP19035-AAABE/MF: 300 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 12 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

d) MCP19035T-AAABE/MF: Tape and Reel, 300 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 12 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

e) MCP19035-BAAAE/MF: 600 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 20 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

f) MCP19035T-BAAAE/MF: Tape and Reel, 600 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 20 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

g) MCP19035-BAABE/MF: 600 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 12 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

h) MCP19035T-BAABE/MF: Tape and Reel, 600 kHz Switching Freq., 600 mV V_{REF}, 200 mV LDRV OC Threshold, 12 ns Dead Time, Extended Temperature, 10LD 3x3 DFN Package

NOTES:

Note the following details of the code protection feature on Microchip devices:

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- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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