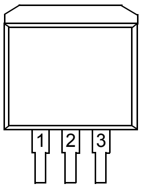
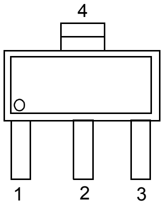
Package Types

MCP1790

DDPAK-3



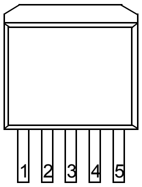
SOT-223-3



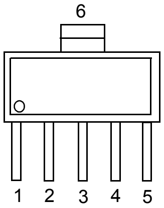
Pin	
1	V_{IN}
2	GND (TAB)
3	V_{OUT}
4	GND (TAB)

MCP1791

DDPAK-5

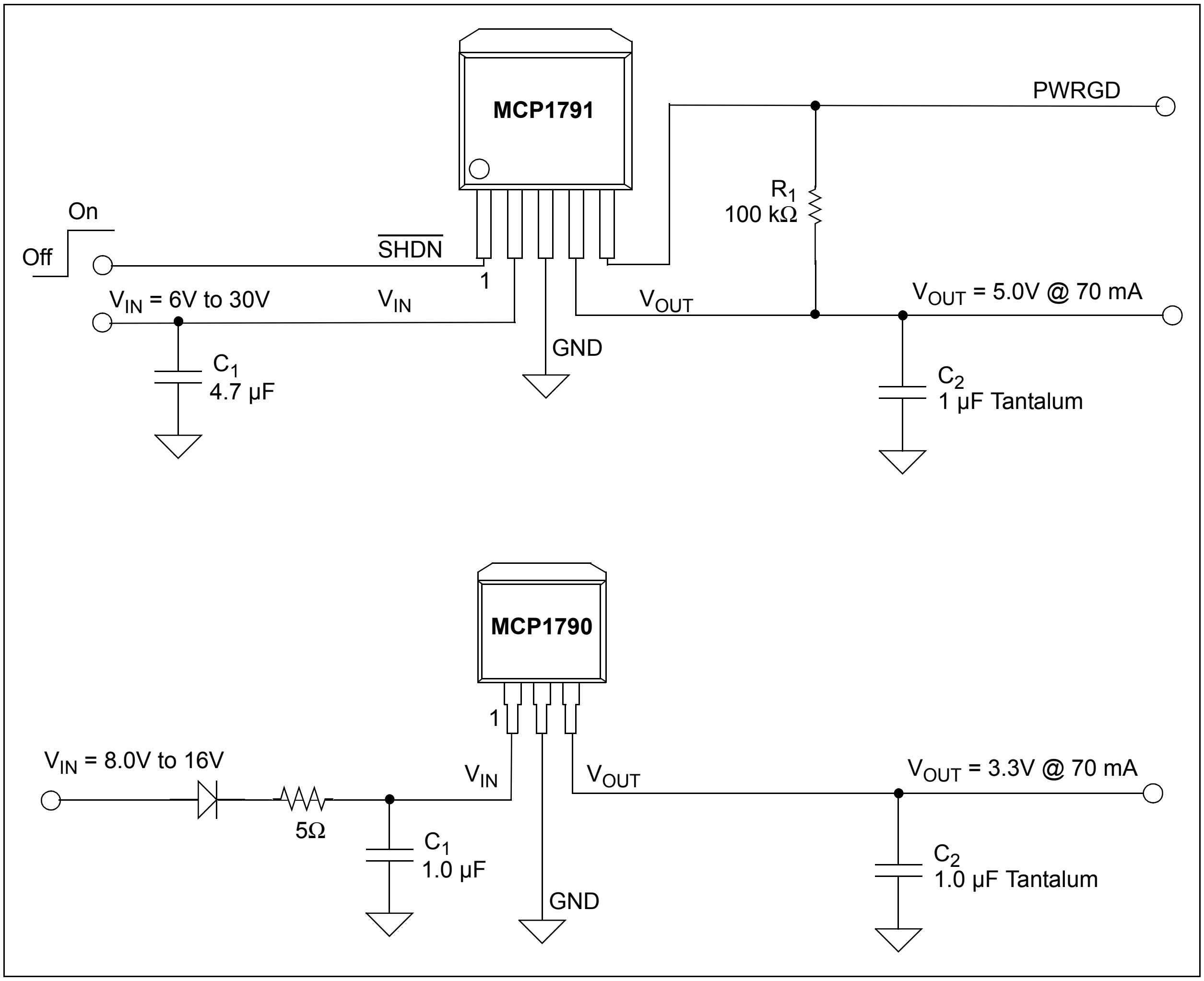


SOT-223-5



Pin	
1	$\overline{SHDN}$
2	V_{IN}
3	GND (TAB)
4	V_{OUT}
5	PWRGD
6	GND (TAB)

TYPICAL APPLICATION



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage, V_{IN}	+48.0V
V_{IN}, PWRGD, $\overline{SHDN}$	(GND-0.3V) to (V_{IN}+0.3V)
V_{OUT}	(GND-0.3V) to (+5.5V)
Internal Power Dissipation	Internally-Limited **(Note 4)**
Output Short Circuit Current	Continuous
Storage temperature	-55°C to +150°C
Maximum Junction Temperature	165°C **(Note 7)**
Operating Junction Temperature	-40°C to +125°C
ESD protection on all pins	≥ 6 kV HBM and $\geq$ 400V MM

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

AC/DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **(Note 1)**, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF (X7R Ceramic), C_{IN} = 4.7 µF (X7R Ceramic), T_A = +25°C, $\overline{SHDN}$ > 2.4V.
Boldface type applies for junction temperatures, T_J **(Note 5)** of **-40°C to +125°C.**

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Input Operating Voltage	V_{IN}	**6.0**	—	**30.0**	V	+48V_{DC} Load Dump Peak < 500 ms
Input Quiescent Current	I_q	—	70	**130**	µA	I_L = 0 mA
Input Quiescent Current for $\overline{SHDN}$ Mode	$I_{\overline{SHDN}}$	—	10	**25**	µA	$\overline{SHDN}$ = GND
Ground Current	IGND	—	110	**210**	µA	I_L = 70 mA
Maximum Output Current	I_{OUT}	**70**	—	—	mA	
Line Regulation	$\Delta V_{OUT}/(V_{OUT} X \Delta V_{IN})$	—	±0.0002	**±0.05**	%/V	6.0V < V_{IN} < 30V
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	**-0.45**	±0.2	**0.45**	%	I_{OUT} = 1 mA to 70 mA **(Note 3)**
Output Peak Short Circuit Current	I_{OUT_SC}	—	V_R/10	—	A	$R_{LOAD} < 0.1\Omega$, Peak Current
Output Voltage Regulation	V_{OUT}	**V_R-2.5%**	V_R	**V_R+2.5%**	V	—
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	65	—	ppm/°C	**Note 9**
Input Voltage to Turn On Output	V_{ON}	—	5.5	**6.0**	V	Rising V_{IN}

Note 1: The minimum V_{IN}, $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

4: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.

5: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(\mathbf{MAX})}$.

7: Sustained junction temperatures above 165°C can impact the device reliability.

8: The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125 °C. If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.

9: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW}) * 10\text{^}6/(V_R * \Delta Temperature)$, $V_{OUT\text{-}HIGH}$ = highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ = lowest voltage measured over the temperature range.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **(Note 1)**, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF (X7R Ceramic), C_{IN} = 4.7 µF (X7R Ceramic), T_A = +25°C, SHDN > 2.4V.
Boldface type applies for junction temperatures, T_J **(Note 5)** of **-40°C to +125°C.**

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Short Circuit Foldback Voltage Corner	$V_{FOLDBACK}$	—	4.2	—	V	V_R = 5.0V Falling V_{OUT}, $R_{LOAD} < 0.1\Omega$
		—	3.0	—	V	V_R = 3.3V Falling V_{OUT}, $R_{LOAD} < 0.1\Omega$
		—	2.7	—	V	V_R = 3.0V Falling V_{OUT}, $R_{LOAD} < 0.1\Omega$
Short Circuit Foldback Current		—	105	—	mA	V_{OUT} ~= 0V, $R_{LOAD} < 0.1\Omega$, V_R = 5.0V **(Note 2)**
		—	99	—	mA	V_R = 3.3V **(Note 2)**
		—	99	—	mA	V_R = 3.0V **(Note 2)**
Startup Voltage Overshoot	V_{OVER}	—	0.10	—	% V_{OUT}	V_{IN} = 0V to 6.0V
Dropout Voltage	$V_{DROPOUT}$	—	700	**1300**	mV	I_{OUT} = 70 mA, **(Note 6)**
Dropout Current I_{OUT} = 0 mA	I_{DO}	—	130	—	µA	V_R = 5.0V, V_{IN} = 4.500V
		—	75	—	µA	V_R = 3.3V, V_{IN} = 4.500V
		—	75	—	µA	V_R = 3.0V, V_{IN} = 4.500V
Shutdown Input						
Logic High Input	$V_{SHDN\text{-}HIGH}$	**2.4**	—	$V_{IN(MAX)}$	V	—
Logic Low Input	$V_{SHDN\text{-}LOW}$	0	—	**0.8**	V	—
Shutdown Input Leakage Current	$\overline{SHDN}_{ILK}$	— —	0.100 3.0	**0.500** **5.0**	µA	$\overline{SHDN}$ = GND $\overline{SHDN}$ = 6V
Power Good Characteristics						
PWRGD Input Voltage Operating Range	V_{PWRGD_VIN}	**2.8**	—	—	V	—
PWRGD Threshold Voltage (Referenced to V_{OUT})	V_{PWRGD_TH}	**88**	90	**92**	$\%V_{OUT}$	Falling Edge of V_{OUT}
PWRGD Threshold Hysteresis	V_{PWRGD_HYS}	**1.0**	2.0	**3.0**	$\%V_{OUT}$	Rising Edge of V_{OUT}
PWRGD Output Voltage LOW	V_{PWRGD_L}	—	0.2	**0.4**	V	$I_{PWRGD\ SINK}$ = 5.0 mA, V_{OUT} = 0V
PWRGD Output Sink Current	I_{PWRGD_L}	5.0	—	—	mA	V_{PWRGD} <= 0.4V
PWRGD Leakage	I_{PWRGD_LK}	—	1.0	—	nA	$V_{PWRGD} = V_{IN}$ = 6.0V
PWRGD Time Delay	T_{PG}	—	30	—	µs	Rising Edge

Note 1: The minimum V_{IN}, $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

4: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.

5: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(\mathbf{MAX})}$.

7: Sustained junction temperatures above 165°C can impact the device reliability.

8: The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125 °C. If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.

9: $TCV_{OUT} = (V_{OUT\text{-}HIGH} - V_{OUT\text{-}LOW})$ *10^6/(V_R * ΔTemperature), $V_{OUT\text{-}HIGH}$ = highest voltage measured over the temperature range. $V_{OUT\text{-}LOW}$ = lowest voltage measured over the temperature range.

AC/DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_{OUT(MAX)} + V_{DROPOUT(MAX)}$, **(Note 1)**, I_{OUT} = 1 mA, C_{OUT} = 4.7 µF (X7R Ceramic), C_{IN} = 4.7 µF (X7R Ceramic), T_A = +25°C, SHDN > 2.4V.
Boldface type applies for junction temperatures, T_J **(Note 5)** of **-40°C to +125°C.**

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Detect Threshold to PWRGD Active Time Delay	$TV_{DET-PWRGD}$	—	235	—	µs	$V_{OUT} = V_{PWRGD\_TH}$ + 100 mV to V_{PWRGD_TH} - 100 mV
AC Performance						
Output Delay from $\overline{SHDN}$	T_{OR}	—	200	—	µs	$\overline{SHDN}$ = GND to V_{IN}, V_{OUT} = GND to 95% V_R, C_{OUT} = 1.0 µF
PWRGD Delay from $\overline{SHDN}$	T_{SHDN_PG}	—	400	—	ns	$\overline{SHDN}$ = V_{IN} to GND, C_{OUT} = 1.0 µF
Output Noise	e_N	—	1.2	—	(µV/√Hz)	I_{OUT} = 50 mA, f = 1 kHz
Power Supply Ripple Rejection Ratio	PSRR				dB	V_{IN} = 7.0V, C_{IN} = 0 µF, I_{OUT} = 10 mA, V_{INAC} = 400 mVpp
		—	90	—		f = 100 Hz
		—	75	—		f = 1 kHz, V_R = 5.0V
		—	80	—		f = 1 kHz, V_R = < 5.0V
Thermal Shutdown Temperature	T_{SD}	—	157	—	°C	Rising Temperature
Thermal Shutdown Hysteresis	ΔT_{SD}	—	20	—	°C	Falling Temperature
Short Circuit Recovery Time	t_{THERM}	—	0	—	ms	**(Note 8)**

Note 1: The minimum V_{IN}, $V_{IN(MIN)}$ must meet two conditions: $V_{IN} \geq 6.0V$ and $V_{IN} \geq V_{OUT(MAX)} + V_{DROPOUT(MAX)}$.

2: V_R is the nominal regulator output voltage.

3: Load regulation is measured at a constant junction temperature using low duty cycle pulse testing. Load regulation is tested over a load range from 1 mA to the maximum specified output current.

4: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air. (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum 165°C rating. Sustained junction temperatures above 165°C can impact the device reliability.

5: The junction temperature is approximated by soaking the device under test at an ambient temperature equal to the desired Junction temperature. The test time is small enough such that the rise in the Junction temperature over the ambient temperature is not significant.

6: Dropout voltage is defined as the input-to-output voltage differential at which the output voltage drops 2% below its nominal value that was measured with an input voltage of $V_{IN} = V_R + V_{DROPOUT(\mathbf{MAX})}$.

7: Sustained junction temperatures above 165°C can impact the device reliability.

8: The Short Circuit Recovery Time test is done by placing the device into a short circuit condition and then removing the short circuit condition before the device die temperature reaches 125 °C. If the device goes into thermal shutdown, then the Short Circuit Recovery Time will depend upon the thermal dissipation properties of the package and circuit board.

9: $TCV_{OUT} = (V_{OUT-HIGH} - V_{OUT-LOW})$ *10^6/(V_R * ΔTemperature), $V_{OUT-HIGH}$ = highest voltage measured over the temperature range. $V_{OUT-LOW}$ = lowest voltage measured over the temperature range.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_J	-40	—	+125	°C	—
Operating Temperature Range	T_J	-40	—	+125	°C	—
Storage Temperature Range	T_A	-55	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3LD DDPAK	θ_{JA} θ_{JC}	—	31.4 3	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 3LD SOT-223	θ_{JA} θ_{JC}	—	62 15	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 5LD DDPAK	θ_{JA} θ_{JC}	—	31.4 3	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board
Thermal Resistance, 5LD SOT-223	θ_{JA} θ_{JC}	—	62 15	—	°C/W	EIA/JEDEC JESD51-751-7 4 Layer Board

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, C_{OUT} = 4.7 uF Ceramic (X7R), C_{IN} = 10.0 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = 6.0V, R_{PWRGD_PULLUP} = 10 kΩ To V_{OUT}, $V_{\overline{SHDN}} = V_{IN}$, and device is MCP1790.

Note: Junction Temperature (TJ) is approximated by soaking the device under test to an ambient temperature equal to the desired junction temperature. The test time is small enough such that the rise in Junction Temperature over the Ambient temperature is not significant.

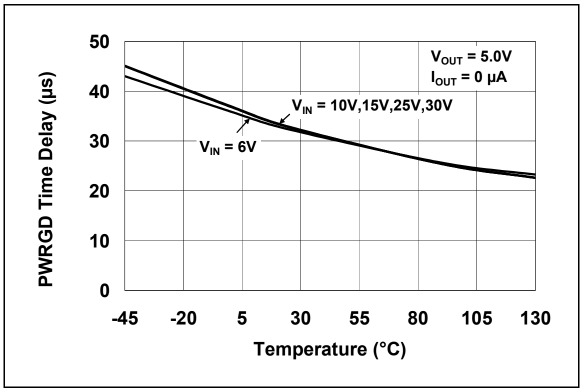


FIGURE 2-1: Power Good Time Delay vs. Temperature (MCP1791).

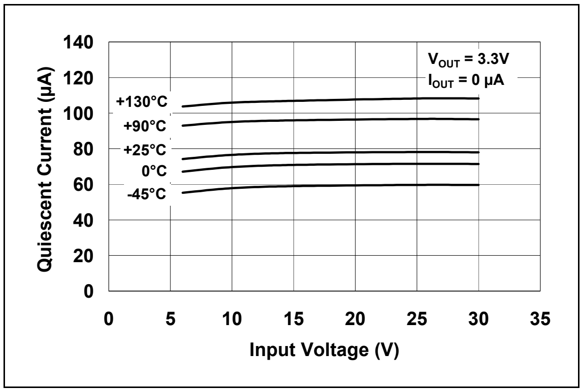


FIGURE 2-2: Quiescent Current vs. Input Voltage.

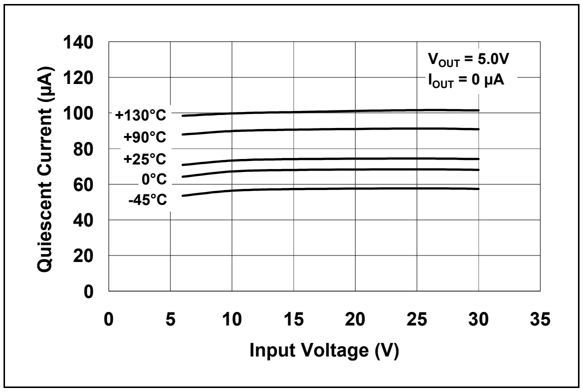


FIGURE 2-3: Quiescent Current vs. Input Voltage.

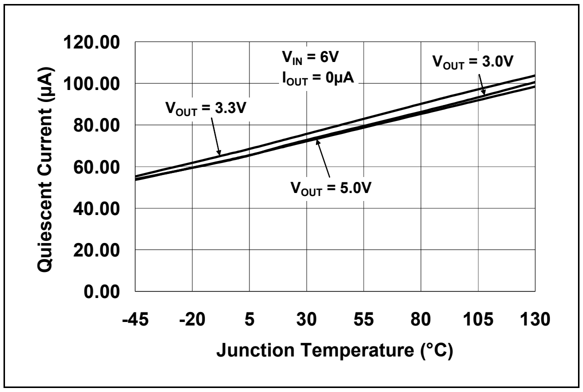


FIGURE 2-4: Quiescent Current vs. Junction Temperature.

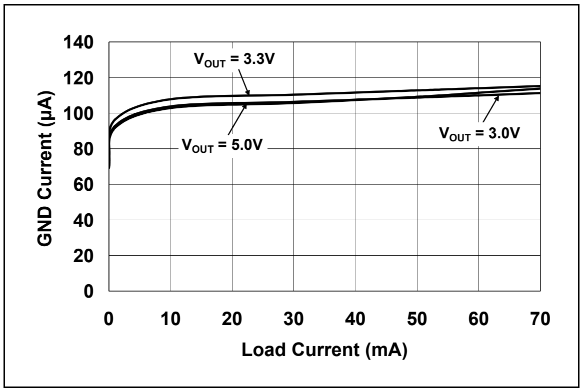


FIGURE 2-5: Ground Current vs. Load Current.

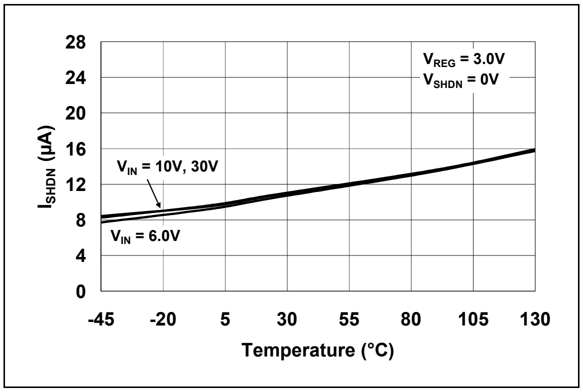


FIGURE 2-6: $I_{\overline{SHDN}}$ vs Temperature.

Note: Unless otherwise indicated, C_{OUT} = 4.7 uF Ceramic (X7R), C_{IN} = 10.0 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = 6.0V, R_{PWRGD_PULLUP} = 10 kΩ To V_{OUT}, $\overline{V_{SHDN}}$ = V_{IN}, and device is MCP1790.

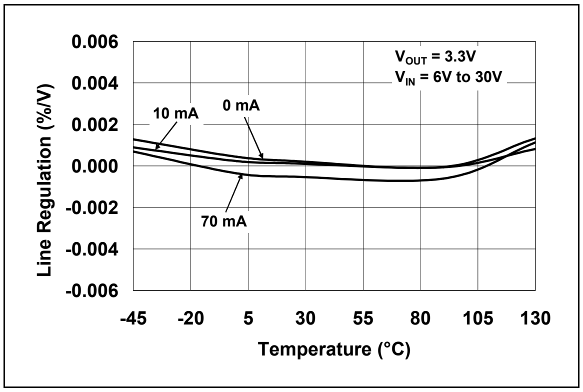


FIGURE 2-7: *Line Regulation vs. Temperature.*

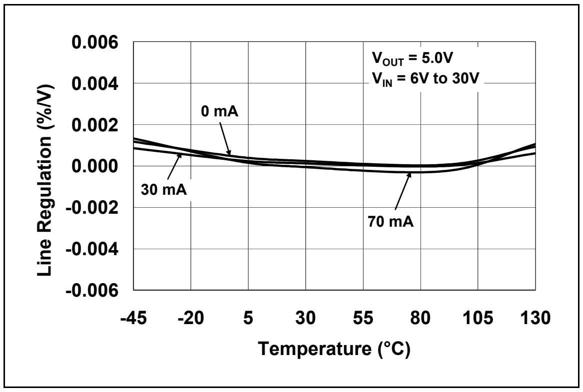


FIGURE 2-8: *Line Regulation vs. Temperature.*

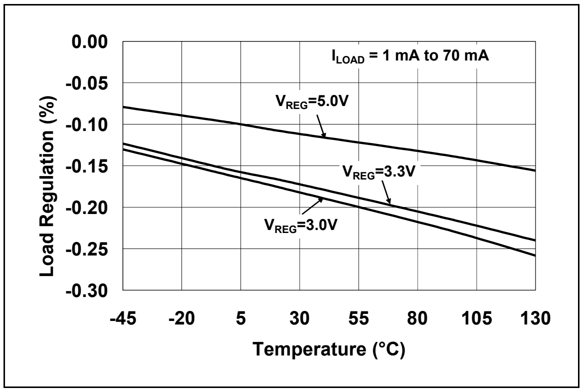


FIGURE 2-9: *Load Regulation vs. Temperature.*

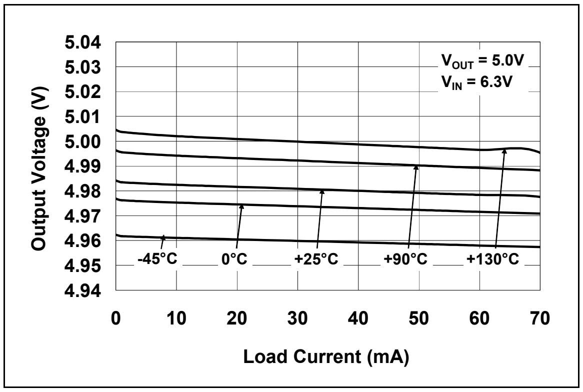


FIGURE 2-10: *Output Voltage vs. Load Current.*

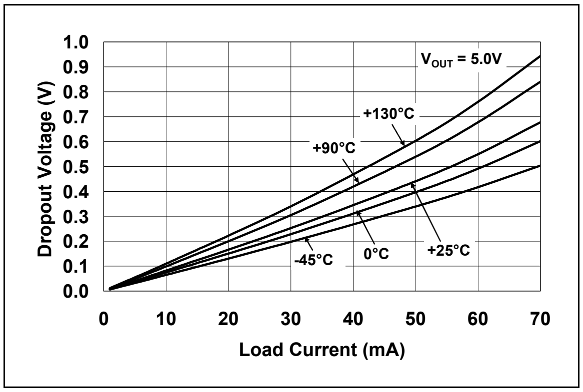


FIGURE 2-11: *Dropout Voltage vs. Load Current.*

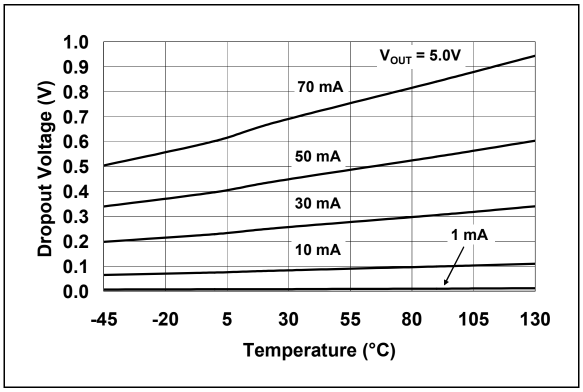


FIGURE 2-12: *Dropout Voltage vs. Temperature.*

Note: Unless otherwise indicated, C_{OUT} = 4.7 uF Ceramic (X7R), C_{IN} = 10.0 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = 6.0V, R_{PWRGD_PULLUP} = 10 kΩ To V_{OUT}, $\overline{V_{SHDN}}$ = V_{IN}, and device is MCP1790.

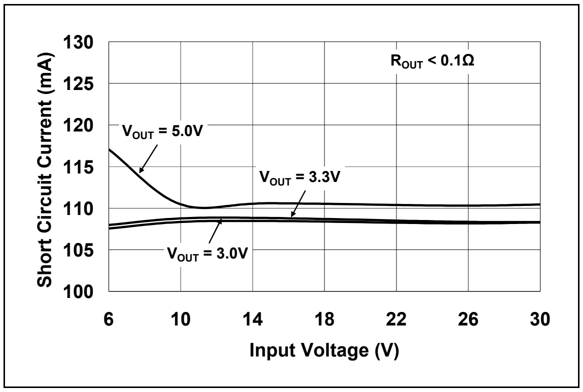


FIGURE 2-13: *Short Circuit Current vs Input Voltage.*

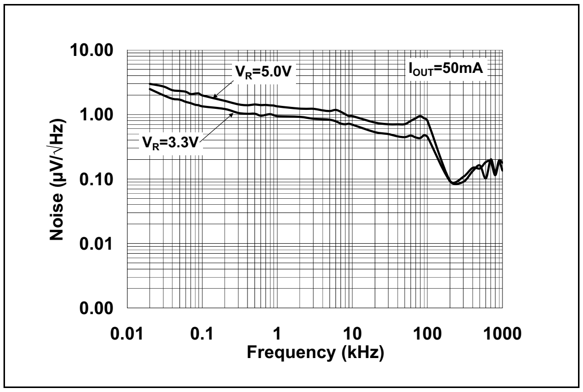


FIGURE 2-14: *Output Noise Voltage Density vs. Frequency.*

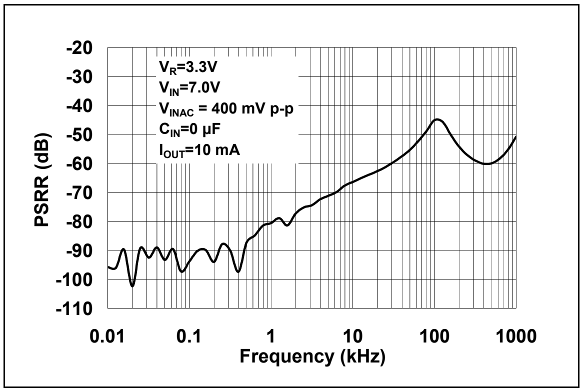


FIGURE 2-15: *Power Supply Ripple Rejection vs. Frequency.*

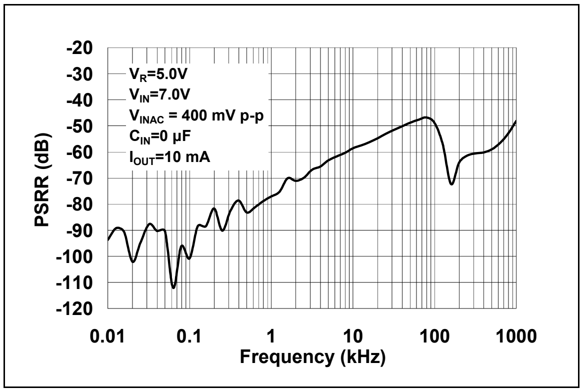


FIGURE 2-16: *Power Supply Ripple Rejection vs. Frequency.*

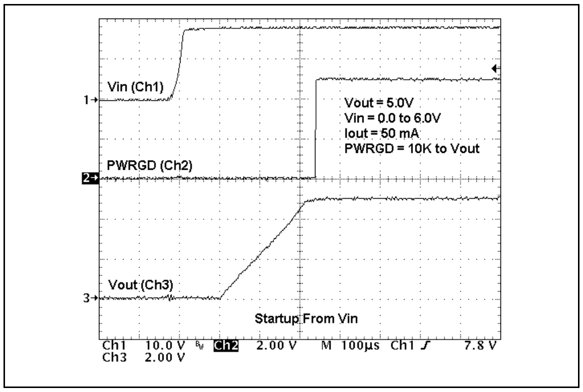


FIGURE 2-17: *Startup from V_{IN} (MCP1791).*

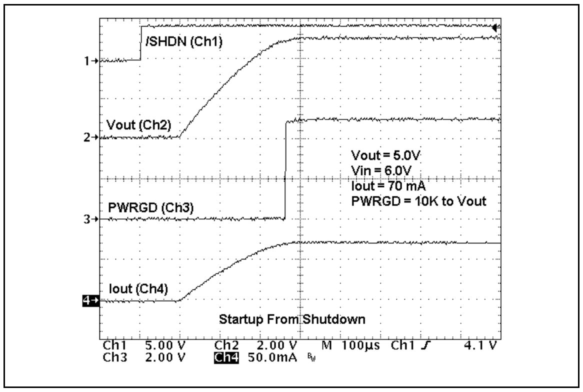


FIGURE 2-18: *Startup from Shutdown (MCP1791).*

Note: Unless otherwise indicated, C_{OUT} = 4.7 uF Ceramic (X7R), C_{IN} = 10.0 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = 6.0V, R_{PWRGD_PULLUP} = 10 kΩ To V_{OUT}, $\overline{V_{SHDN}}$ = V_{IN}, and device is MCP1790.

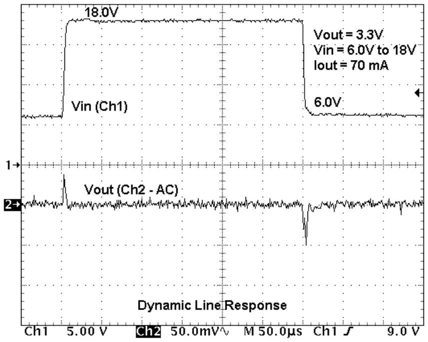


FIGURE 2-19: Dynamic Line Response.

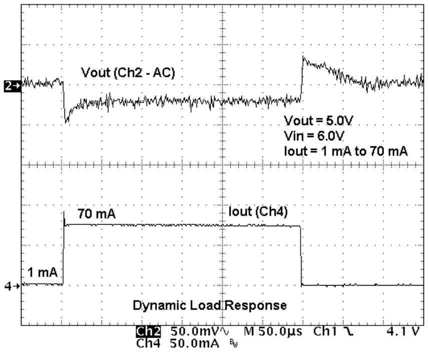


FIGURE 2-22: Dynamic Load Response.

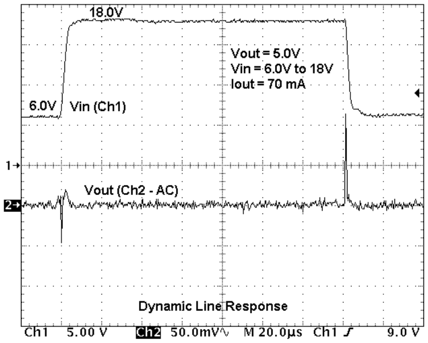


FIGURE 2-20: Dynamic Line Response.

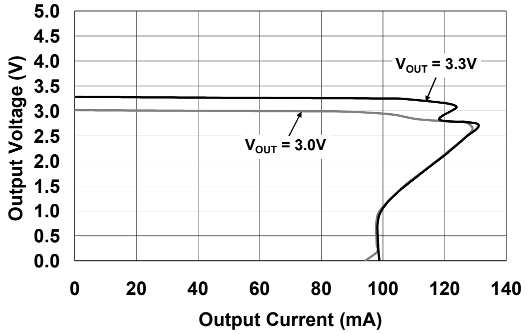


FIGURE 2-23: Short Circuit Response.

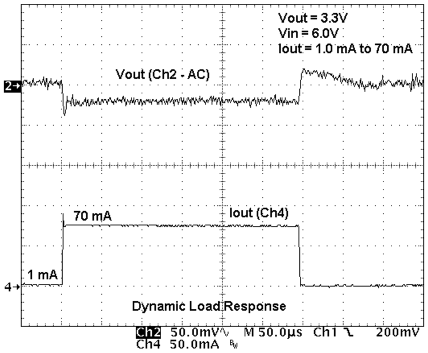


FIGURE 2-21: Dynamic Load Response.

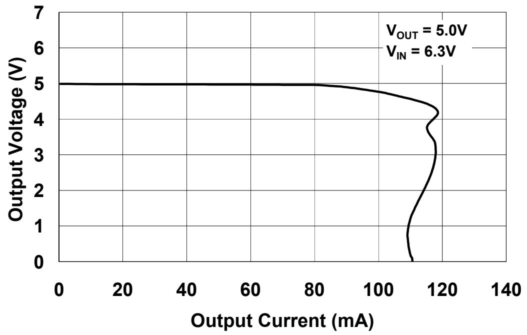


FIGURE 2-24: Short Circuit Response.

Note: Unless otherwise indicated, C_{OUT} = 4.7 uF Ceramic (X7R), C_{IN} = 10.0 µF Ceramic (X7R), I_{OUT} = 1 mA, Temperature = +25°C, V_{IN} = 6.0V, R_{PWRGD_PULLUP} = 10 kΩ To V_{OUT}, $\overline{V_{SHDN}}$ = V_{IN}, and device is MCP1790.

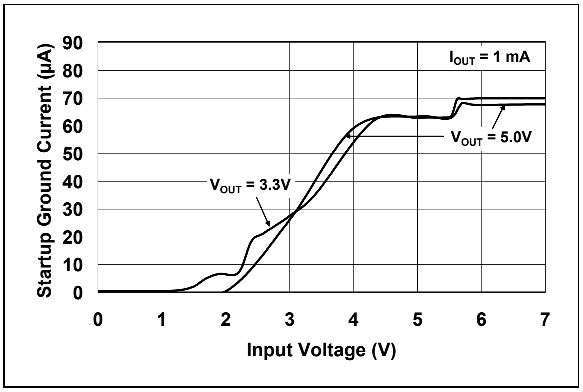


FIGURE 2-25: *Startup Ground Current.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1 and Table 3-2.

TABLE 3-1: MCP1790 PIN FUNCTION TABLE

Pin No. SOT-223-3	Pin No. DDPAK-3	Symbol	Function
1	1	V_{IN}	Unregulated Supply Voltage
2,Tab	2,Tab	GND	Ground Terminal
3	3	V_{OUT}	Regulated Output Voltage

TABLE 3-2: MCP1791 PIN FUNCTION TABLE

Pin No. SOT-223-5	Pin No. DDPAK-5	Symbol	Function
1	1	$\overline{SHDN}$	Shutdown Input
2	2	V_{IN}	Unregulated Supply Voltage
3	3	GND	Ground Terminal
4	4	V_{OUT}	Regulated Output Voltage
5	5	PWRGD	Power Good Open-Drain Output
Tab	Tab	—	Connected to Ground
—	—	N/C	No connection

3.1 Input Voltage Supply (V_{IN})

Connect the unregulated or regulated input voltage source to V_{IN}. If the input voltage source is located several inches away from the regulator or the input source is a battery, it is recommended that an input capacitor is used. A typical input capacitance value of 1 µF to 10 µF should be sufficient for most applications. The type of capacitor used can be ceramic, tantalum or aluminum electrolytic. The low ESR characteristics of the ceramic will yield better noise and PSRR performance at high-frequency.

3.2 Ground (GND)

Tie GND to the negative side of the output and the negative side of the input capacitor. Only the regulator bias current flows out of this pin; there is no high current. The regulator output regulation is referenced to this pin. Minimize voltage drops between this pin and the negative side of the load.

3.3 Regulated Output Voltage (V_{OUT})

The V_{IN} pin is the regulated output voltage of the regulator. A minimum output capacitance of 1.0 µF tantalum, 1.0 µF electrolytic, or 4.7 µF ceramic is required for stability. The MCP1790 is stable with ceramic, tantalum, and electrolytic capacitors. See **Section 4.7 "Output Capacitor"** for output capacitor selection guidance.

3.4 Shutdown ($\overline{SHDN}$)

The $\overline{SHDN}$ pin is an active-low input signal that turns the regulator output voltage on and off. When the $\overline{SHDN}$ input is at a logic-high level, the regulator output voltage is enabled. When the $\overline{SHDN}$ input is pulled to a logic-low level, the regulator output voltage is disabled. When the $\overline{SHDN}$ input is pulled low, the PWRGD output signal also goes low and the regulator enters a low quiescent current shutdown state where the typical quiescent current is 10 µA. The $\overline{SHDN}$ pin is bonded to V_{IN} in the 3-pin versions of the regulator. See Table 4-1.

3.5 Power Good Output (PWRGD)

The PWRGD pin is an open-drain output signal that is used to indicate when the regulator output voltage is within 90% (typically) of its nominal regulation value. The PWRGD threshold has a typical hysteresis value of 2%. The typical PWRGD delay time due to V_{OUT} rising above 90% +3% (maximum hysteresis) is 30 µs. The typical PWRGD delay time due to V_{OUT} falling below 90% is 235 µs. These delay times are internally fixed.

3.6 Exposed Pad (EP)

The DDPAK package has an exposed tab on the package. A heat sink may be mounted to the tab to aid in the removal of heat from the package during operation.

The exposed tab or pad of all of the available packages is at the ground potential of the regulator.

4.0 DEVICE OVERVIEW

The MCP1790/MCP1791 are high input voltage regulators capable of providing up to 70 mA of current at output voltages up to 5.0V. The devices have an input voltage operating range from 6.0V to 30V, 48V absolute max. The MCP1790 devices are 3-pin devices consisting of V_{IN}, V_{OUT} and GND. The MCP1791 devices have 5 or more pins which add Shutdown and Power-Good functions to the MCP1790 device.

4.1 Startup

In the start phase, the device must see at least 6.0V to initiate operation during power up. In the Power-down mode, the V_{IN} monitor will be turned off.

4.2 Thermal Shutdown

The regulator has a thermal shutdown. If the thermal protection circuit detects an over temperature condition, typically 157°C junction temperature, the regulator will shut down. The device will recover from the thermal shutdown when the junction temperature drops to 137°C (typical).

4.3 Regulator Output Voltage

The MCP1790/MCP1791 regulators are available in fixed output voltage configurations. The standard output voltages are 3.0V, 3.3V, and 5.0V.

4.4 External Protection

4.4.1 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

The regulator is capable of withstanding a 48V (43.5V ±10) load dump transient for a duration of 500 ms and a repetition rate of 30 seconds (ES-XW7T-1A278-AC, Ford Motor Company, Test Pulse G Loaded).

While not necessary, good design practice dictates adding an external transient suppressor, between VBB and ground, with a low value resistor in series with the battery supply and the V_{IN} pin, to limit currents and voltages due to electrical transients. Because of the regulator startup current, the resistor value should be less than (V_{BAT} -6V) / 200 mA. For a 12V battery voltage, the resistor value should be less than 30 ohms.

4.4.2 REVERSE BATTERY PROTECTION

An external reverse battery blocking diode may be used to provide polarity protection.

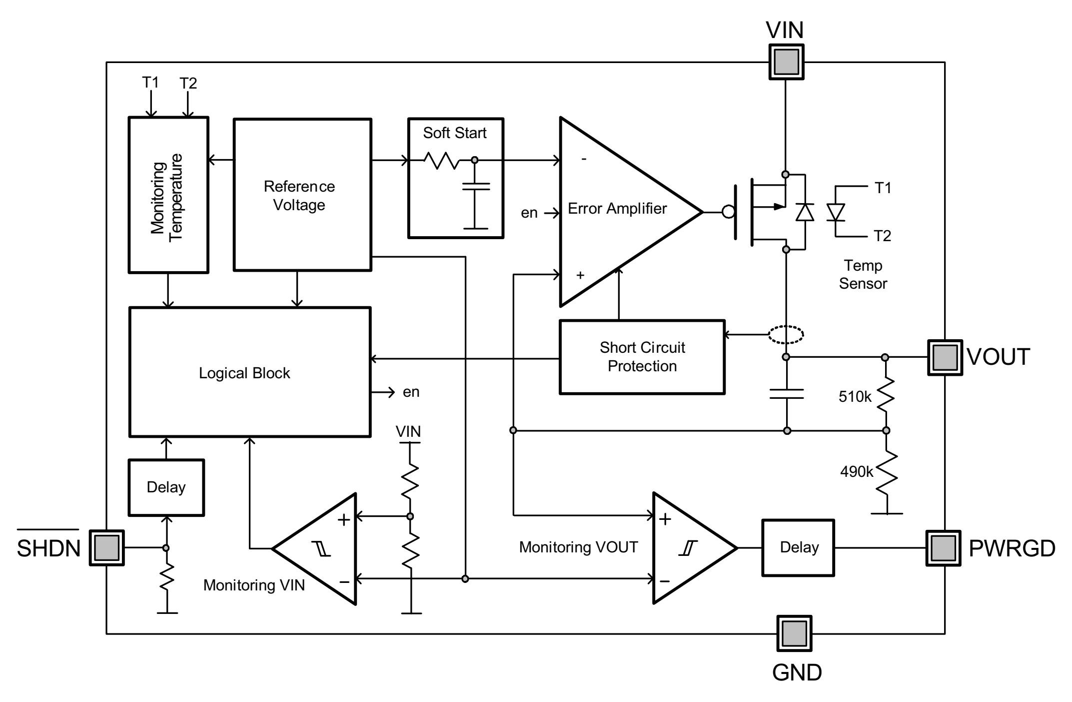


FIGURE 4-1: *MCP1790/MCP1791 Block Diagram.*

4.5 Shutdown ($\overline{\text{SHDN}}$)

The MCP1791 has a Shutdown ($\overline{\text{SHDN}}$) input signal that enables or disables the regulator output voltage. When the $\overline{\text{SHDN}}$ input signal is greater than 2.40V, the regulator output voltage is enabled. Note that the regulator output may still be disabled by the undervoltage lockout incorporated within the V_{IN} circuitry.

The value of the $\overline{\text{SHDN}}$ signal to put the regulator into Shutdown mode is ≤0.8V. The $\overline{\text{SHDN}}$ pin is pulled low by an internal resistor. If the $\overline{\text{SHDN}}$ pin is left floating, the internal pull-down resistor will put the regulator into shutdown mode.

When the $\overline{\text{SHDN}}$ input signal is pulled to a logic-low, the PWRGD output signal will also go low and the regulator will enter a low quiescent current state where the typical quiescent current is 10 µA. There is a short time delay (approximately 400 ns) when the $\overline{\text{SHDN}}$ input signal transitions from high-to-low to prevent signal noise from disabling the regulator. The $\overline{\text{SHDN}}$ pin will ignore low-going pulses that are up to 400 ns in pulse width. If the $\overline{\text{SHDN}}$ input is pulled low for more than 400 ns, the regulator will enter Shutdown mode. This small bit of filtering helps to reject any system noise spikes on the $\overline{\text{SHDN}}$ input signal.

On the rising edge of the $\overline{\text{SHDN}}$ input, the shutdown circuitry will have a 100 µs delay before allowing the regulator output to turn on. This delay helps to reject any false turn-on signals or noise on the $\overline{\text{SHDN}}$ input signal. After the 100 µs delay, the regulator will start charging the output capacitor as the regulator output voltage rises from 0V to its final regulated value. The charging current will be limited by the short circuit current value of the device. If the $\overline{\text{SHDN}}$ input signal is pulled low during the 100 µs delay period, the timer will be reset and the delay time will start over again on the next rising edge of the $\overline{\text{SHDN}}$ input. The total time from the $\overline{\text{SHDN}}$ input going high (turn-on) to the regulator output being in regulation shall typically be 200 µs (100 µs + 100 µs) for a C_{LOAD} = 1.0 µF.

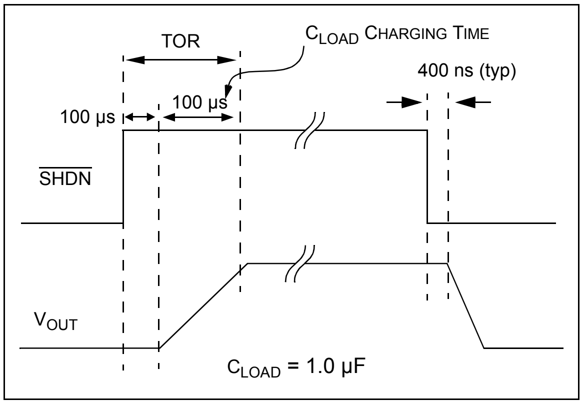


FIGURE 4-2: Shutdown Input Timing Diagram.

4.6 Low Voltage Shutdown

The MCP1790/MCP1791 incorporates a Low Voltage Shutdown circuit that turns off the output of the regulator whenever the input voltage, V_{IN}, is below the specified turn off voltage, V_{OFF}. When the input voltage (V_B) drops below the differential needed to provide stable regulation, the output voltage (V_{REG}) shall track the input down to approximately +4.00V. The regulator will turn off the output at this point.

The output will turn on when V_{IN} rises above the V_{ON} value specified in the data sheet. This feature is independent of the Shutdown input signal ($\overline{\text{SHDN}}$) that is provided for external regulator control. If the $\overline{\text{SHDN}}$ input signal is active (LOW), then the output of the regulator shall be disabled regardless of input voltage.

TABLE 4-1: SHUTDOWN LOGIC

V_{IN}	$\overline{\text{SHDN}}$	V_{OUT}
< V_{OFF}	L	OFF
< V_{OFF}	H	OFF
> V_{ON}	L	OFF
> V_{ON}	H	ON

4.7 Output Capacitor

The MCP1790/MCP1791 requires a minimum output capacitance of 1 µF tantalum or electrolytic capacitance. The minimum value for ceramic capacitors is 4.7 µF. The regulator is stable for all three types of capacitors from 4.7 µF to 1000 µF (see Figure 4-3). The MCP1790/MCP1791 regulator may be used with a 1 µF ceramic output capacitor if a 0.300Ω resistor is placed in series with the capacitor. The low ESR and corresponding pole of the ceramic capacitor causes the instability below 4.7 µF.

The Equivalent Series Resistance (ESR) of the output capacitor must be no greater than 3 ohms. The output capacitor should be located as close to the regulator output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are recommended because of their size, cost and environmental robustness qualities.

4.8 Output Current and Current Limiting

The MCP1790/MCP1791 devices are tested and ensured to supply a minimum of 70 mA of output current.

The MCP1790/MCP1791 also incorporate an output current limit foldback. When the regulator is in an overcurrent condition, V_{OUT} will decrease with increasing load. When V_{OUT} falls below 30% (typical) of V_R, the output current will start to fold back. The output current will fold back to less than 100 mA (typical) when V_{OUT} is near 0 volts.

The 5.0V regulator has an overload current limiting of approximately 120 mA. If V_{REG} is lower than 3.5V, I_{OUT} will start to fold back and decrease along with V_{REG} until IOUT is less than 105 mA and V_{REG} is near 0 volts.

The 3.3V regulator has an overload current limiting of approximately 130 mA. If V_{REG} is lower than 2.5V, I_{OUT} will start to fold back and decrease along with V_{REG} until IOUT is less than 99 mA and V_{REG} is near 0 volts.

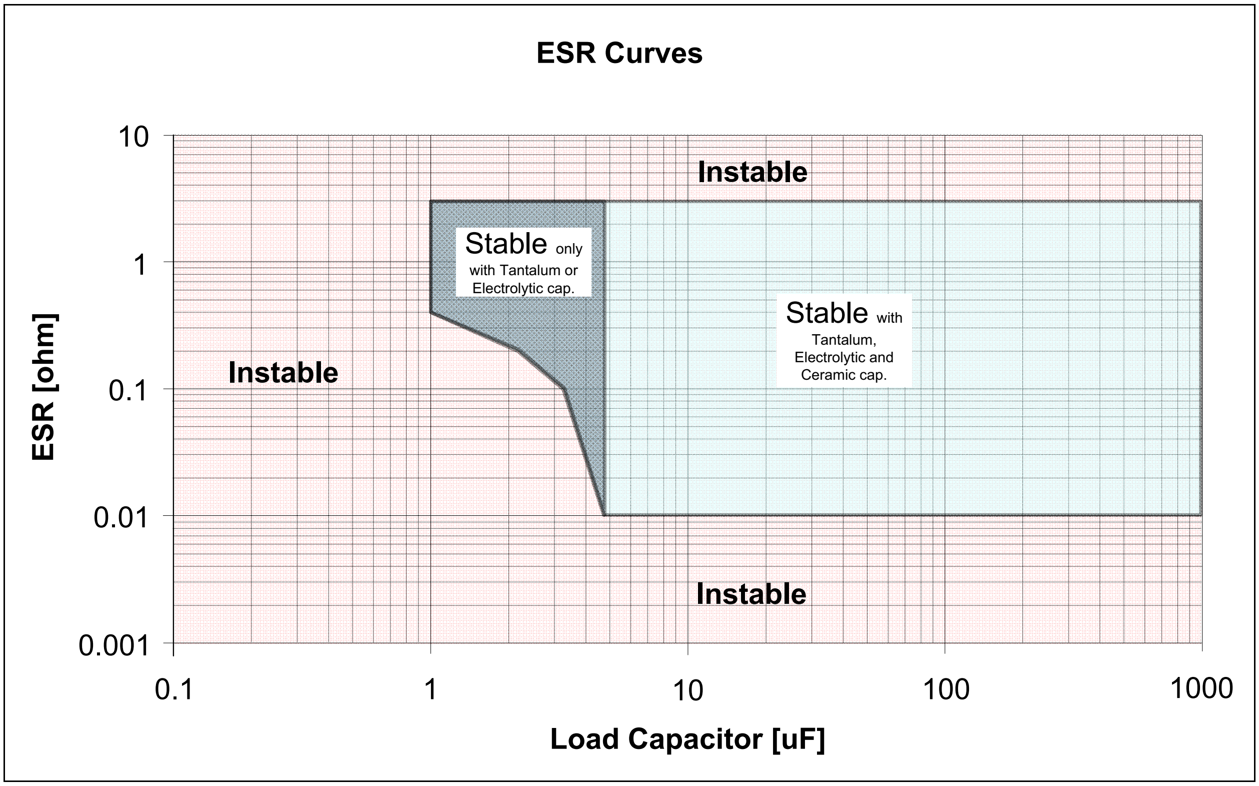


FIGURE 4-3: *ESR Curves for Load Capacitor Selection.*

4.9 Power Good Output (PWRGD)

The MCP1791 has an open-drain Power Good (PWRGD) output signal capable of sinking a minimum of 5.0 mA of current while maintaining a PWRGD output voltage of 0.4V or less.

As the output voltage of the LDO rises, the PWRGD output will be held low until the output voltage has exceeded the power good threshold (V_{PWRGD_TH}) level by an amount equal to the power good hysteresis value ((V_{PWRGD_HYS}), typically 2% of V_R. Once this threshold has been exceeded, the power good output signal will be pulled high by an external pull-up resistor, indicating that the output voltage is stable and within regulation limits.

If the output voltage of the LDO falls below the power good threshold (V_{PWRGD_TH}) level, the power good output will transition low. The power good circuitry has a 235 µs delay when detecting a falling output voltage, which helps to increase noise immunity of the power good output and avoid false triggering of the power good output during fast output transients. See Figure 4-4 for power good timing characteristics.

When the LDO is put into Shutdown mode using the $\overline{SHDN}$ input, the power good output is pulled low within 400 ns typical, indicating that the output voltage will be out of regulation. The timing diagram for the power good output when using the shutdown input is shown in Figure 4-5.

The PWRGD output may be pulled up to either V_{IN} or V_{OUT}. When pulled to V_{OUT}, the PWRGD output will sink very little current during shutdown. When PWRGD is pulled up to V_{IN} , the PWRGD output will sink current during shutdown. That is because V_{OUT} is 0 during shutdown while V_{IN} is still active. When the PWRGD output is pulled to V_{IN} , the PWRGD output signal will track V_{IN} at startup until the threshold of the PWRGD circuitry has been reached and the PWRGD circuitry pulls the signal back low. Therefore, when pulling PWRGD to V_{IN} instead of V_{OUT}, the designer must be aware of the PWRGD signal going high while the input voltage is rising at startup. Pulling PWRGD to V_{OUT} removes the startup pulse.

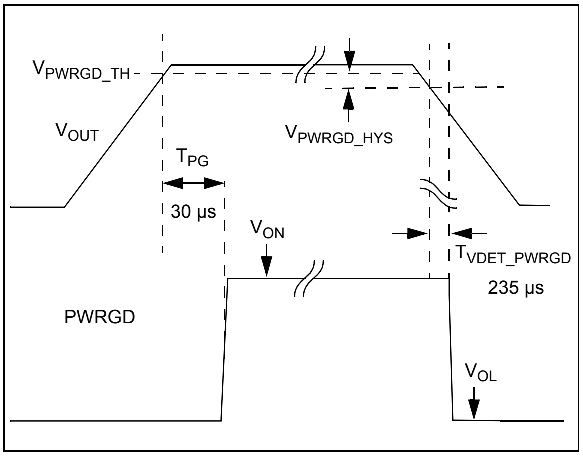


FIGURE 4-4: *Power Good Timing.*

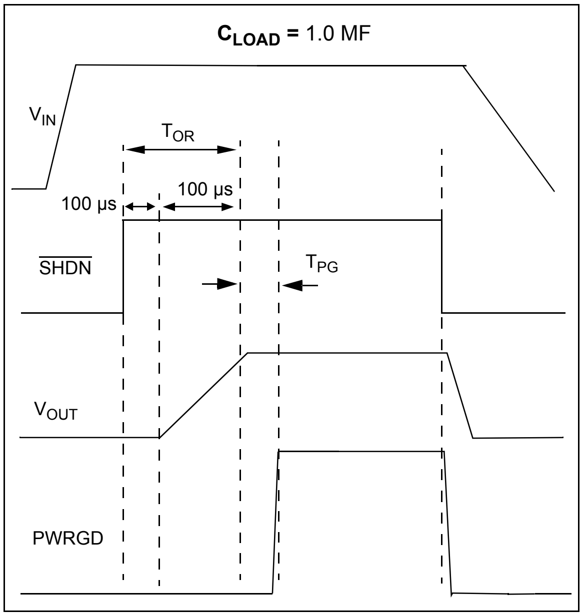


FIGURE 4-5: *Power Good Timing from Shutdown.*

5.0 APPLICATION CIRCUITS/ ISSUES

5.1 Typical Application

The MCP1790/MCP1791 is most commonly used as a voltage regulator. It is a high voltage input capability and thermal protection make it ideal for automotive and 24V industrial applications.

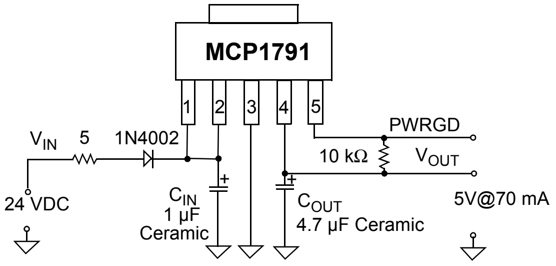


FIGURE 5-1: *Typical Application.*

5.1.1 APPLICATION INPUT CONDITIONS

Package Type = SOT-223-5
Input Voltage Range = 8V to 24V
V_{IN} maximum = 24V
V_{OUT} typical = 5.0V
I_{OUT} = 70 mA maximum

5.2 Power Calculations

5.2.1 POWER DISSIPATION

The internal power dissipation of the MCP1790/MCP1791 is a function of input voltage, output voltage and output current. The power dissipation, as a result of the quiescent current draw, is so low, it is insignificant (70.0 µA x V_{IN}). The following equation can be used to calculate the internal power dissipation of the LDO.

EQUATION 5-1:

$$P_{LDO} = (V_{IN(MAX))} - V_{OUT(MIN)}) \times I_{OUT(MAX))}$$

P_{LDO} = LDO Pass device internal power dissipation
$V_{IN(MAX)}$ = Maximum input voltage
$V_{OUT(MIN)}$ = LDO minimum output voltage

The maximum continuous operating junction temperature specified for the MCP1790/MCP1791 is +125°C. To estimate the internal junction temperature of the MCP1790/MCP1791, the total internal power dissipation is multiplied by the thermal resistance from junction to ambient ($R\theta_{JA}$). The thermal resistance from junction to ambient for the SOT-223-5 package is estimated at 62°C/W.

EQUATION 5-2:

$$T_{J(MAX)} = P_{TOTAL} \times R\theta_{JA} + T_{AMAX}$$

$T_{J(MAX)}$ = Maximum continuous junction temperature
P_{TOTAL} = Total device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction to ambient
T_{AMAX} = Maximum ambient temperature

The maximum power dissipation capability for a package can be calculated given the junction-to-ambient thermal resistance and the maximum ambient temperature for the application. The following equation can be used to determine the package maximum internal power dissipation.

EQUATION 5-3:

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_{A(MAX)})}{R\theta_{JA}}$$

$P_{D(MAX)}$ = Maximum device power dissipation
$T_{J(MAX)}$ = Maximum continuous junction temperature
$T_{A(MAX)}$ = Maximum ambient temperature
$R\theta_{JA}$ = Thermal resistance from junction to ambient

EQUATION 5-4:

$$T_{J(RISE)} = P_{TOTAL} \times R\theta_{JA}$$

$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
P_{TOTAL} = Total device power dissipation
$R\theta_{JA}$ = Thermal resistance from junction-to-ambient

EQUATION 5-5:

$$T_J = T_{J(RISE)} + T_A$$

T_J = Junction Temperature
$T_{J(RISE)}$ = Rise in device junction temperature over the ambient temperature
T_A = Ambient temperature

5.3 Power Dissipation Example

Internal power dissipation, junction temperature rise, junction temperature and maximum power dissipation are calculated in the following example. The power dissipation, as a result of ground current, is small enough to be neglected.

5.3.1 POWER DISSIPATION EXAMPLE

Package:

Package Type = SOT-223-5

Input Voltage:

V_{IN} = 8V to 24V

LDO Output Voltages and Currents:

V_{OUT} = 5.0V

I_{OUT} = 50 mA

Maximum Ambient Temperature:

$T_{A(MAX)}$ = +40°C

Internal Power Dissipation:

Internal Power dissipation is the product of the LDO output current times the voltage across the LDO (V_{IN} to V_{OUT}).

$P_{LDO(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \times I_{OUT(MAX)}$

P_{LDO} = (24V - (0.98 x 5.0V)) x 50 mA

P_{LDO} = 955 milli-Watts

5.3.1.1 Device Junction Temperature Rise

The internal junction temperature rise is a function of internal power dissipation and the thermal resistance from junction to ambient for the application. The thermal resistance from junction to ambient ($R\theta_{JA}$) is derived from an EIA/JEDEC standard for measuring thermal resistance for small surface mount packages. The EIA/JEDEC specification is JESD51-7, “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages”. The standard describes the test method and board specifications for measuring the thermal resistance from junction to ambient. The actual thermal resistance for a particular application can vary depending on many factors, such as copper area and thickness. Refer to AN792, “A Method to Determine How Much Power a SOT23 Can Dissipate in an Application”, (DS00792), for more information regarding this subject.

$T_{J(RISE)} = P_{TOTAL} \times Rq_{JA}$

T_{JRISE} = 955 milli-Watts x 62°C/Watt

T_{JRISE} = 59.2°C

5.3.1.2 Junction Temperature Estimate

To estimate the internal junction temperature, the calculated temperature rise is added to the ambient or offset temperature. For this example, the worst-case junction temperature is estimated below.

$T_J = T_{JRISE} + T_{A(MAX)}$

T_J = 99.2°C

5.3.1.3 Maximum Package Power Dissipation at +40°C Ambient Temperature

SOT-223-5 (62°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 40°C) / 62°C/W

$P_{D(MAX)}$ = 1.371 Watts

DDPAK-5 (32°C/Watt = $R\theta_{JA}$)

$P_{D(MAX)}$ = (125°C - 40°C) / 32°C/W

$P_{D(MAX)}$ = 2.656 Watts

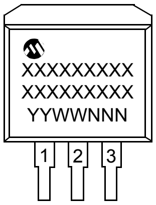
5.4 Pulsed Load Applications

For some applications, there are pulsed load current events that may exceed the specified 70 mA maximum specification of the MCP1790/MCP1791. The internal current foldback feature of the MCP1790/MCP1791 will prevent high peak load demands from causing non-recoverable damage. The Current Foldback feature of the device will limit the output voltage and output current during pulsed applications. As the current rises above the foldback current threshold, the output voltage will decrease.

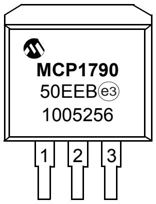
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

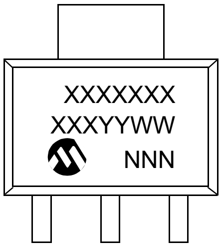
3-Lead DDPAK (MCP1790)



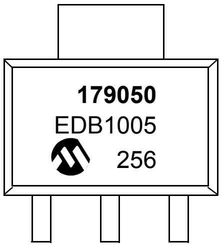
Example:



3-Lead SOT-223 (MCP1790)



Example:

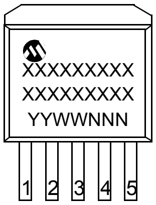


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

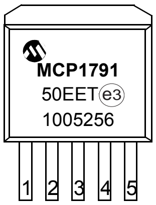
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

6.1 Package Marking Information (Continued)

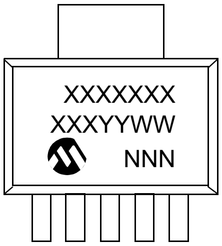
5-Lead DDPAK (Fixed) (MCP1791)



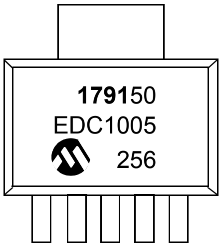
Example:



5-Lead SOT-223 (MCP1791)



Example:

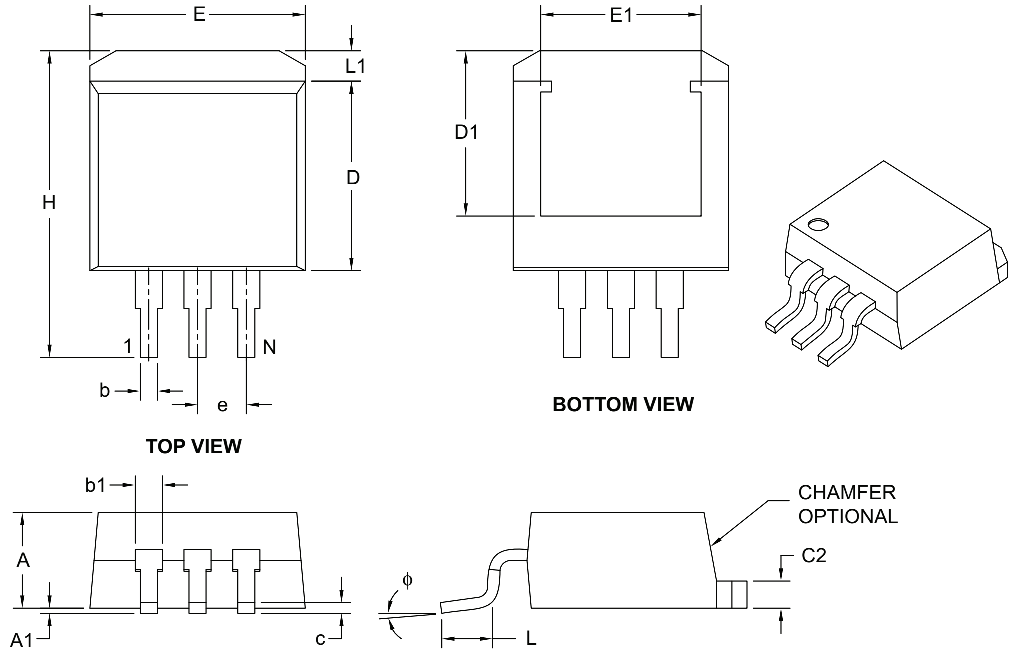


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

3-Lead Plastic (EB) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	3		
Pitch	e	.100 BSC		
Overall Height	A	.160	–	.190
Standoff §	A1	.000	–	.010
Overall Width	E	.380	–	.420
Exposed Pad Width	E1	.245	–	–
Molded Package Length	D	.330	–	.380
Overall Length	H	.549	–	.625
Exposed Pad Length	D1	.270	–	–
Lead Thickness	c	.014	–	.029
Pad Thickness	C2	.045	–	.065
Lower Lead Width	b	.020	–	.039
Upper Lead Width	b1	.045	–	.070
Foot Length	L	.068	–	.110
Pad Length	L1	–	–	.067
Foot Angle	ϕ	0°	–	8°

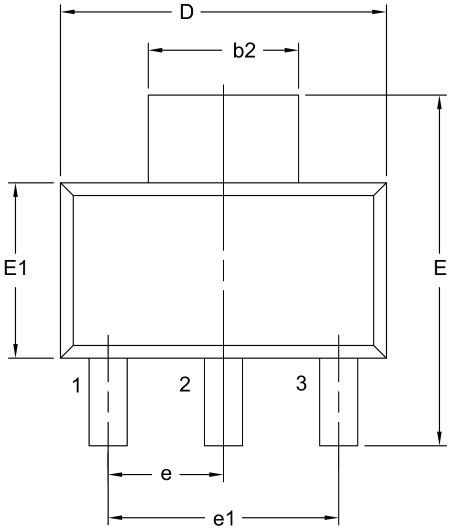
Notes:

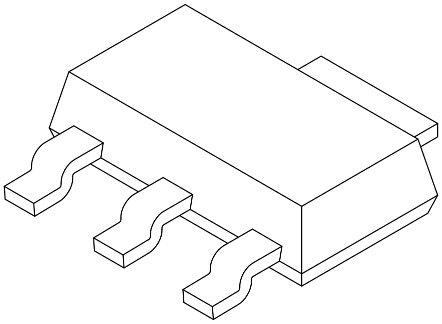
1. § Significant Characteristic.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

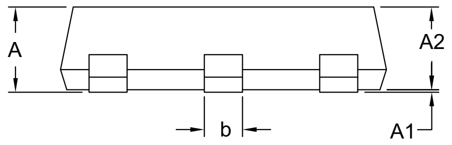
Microchip Technology Drawing C04-011B

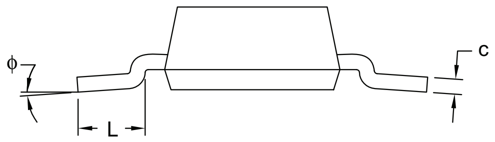
3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	3		
Lead Pitch	e	2.30 BSC		
Outside Lead Pitch	e1	4.60 BSC		
Overall Height	A	–	–	1.80
Standoff	A1	0.02	–	0.10
Molded Package Height	A2	1.50	1.60	1.70
Overall Width	E	6.70	7.00	7.30
Molded Package Width	E1	3.30	3.50	3.70
Overall Length	D	6.30	6.50	6.70
Lead Thickness	c	0.23	0.30	0.35
Lead Width	b	0.60	0.76	0.84
Tab Lead Width	b2	2.90	3.00	3.10
Foot Length	L	0.75	–	–
Lead Angle	ϕ	0°	–	10°

Notes:

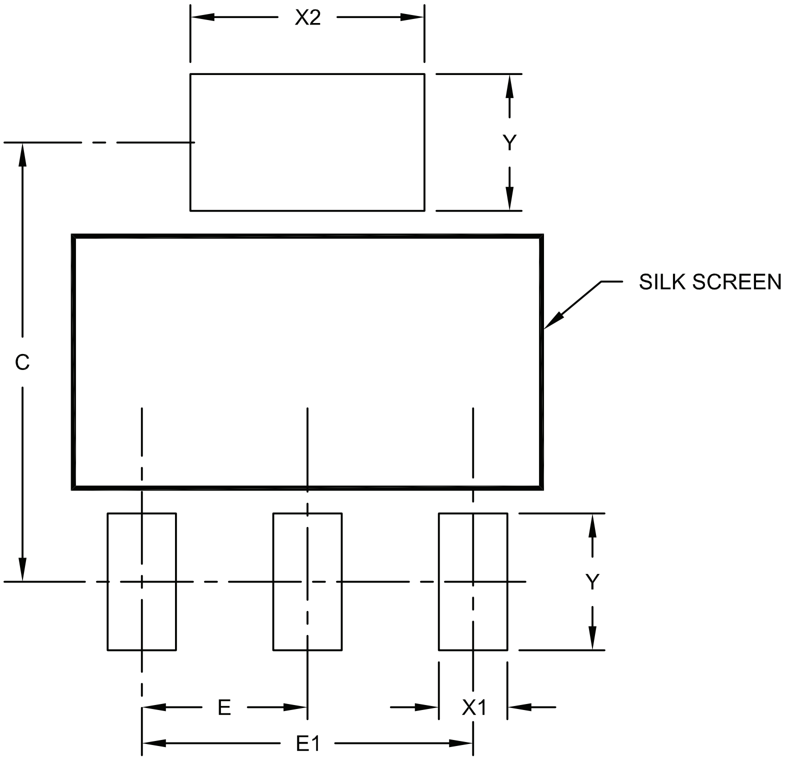
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-032B

3-Lead Plastic Small Outline Transistor (DB) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		2.30 BSC	
Overall Pitch	E1		4.60 BSC	
Contact Pad Spacing	C		6.10	
Contact Pad Width	X1			0.95
Contact Pad Width	X2			3.25
Contact Pad Length	Y			1.90

Notes:

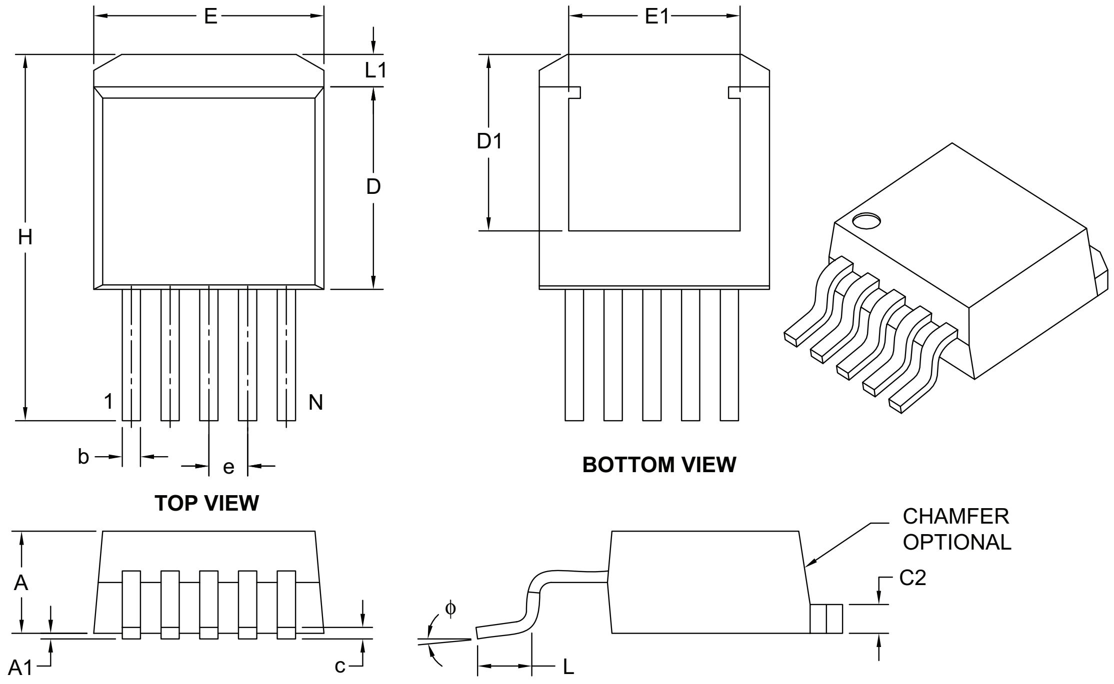
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2032A

5-Lead Plastic (ET) [DDPAK]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	INCHES	
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	.067 BSC		
Overall Height	A	.160	–	.190
Standoff §	A1	.000	–	.010
Overall Width	E	.380	–	.420
Exposed Pad Width	E1	.245	–	–
Molded Package Length	D	.330	–	.380
Overall Length	H	.549	–	.625
Exposed Pad Length	D1	.270	–	–
Lead Thickness	c	.014	–	.029
Pad Thickness	C2	.045	–	.065
Lead Width	b	.020	–	.039
Foot Length	L	.068	–	.110
Pad Length	L1	–	–	.067
Foot Angle	ϕ	0°	–	8°

Notes:

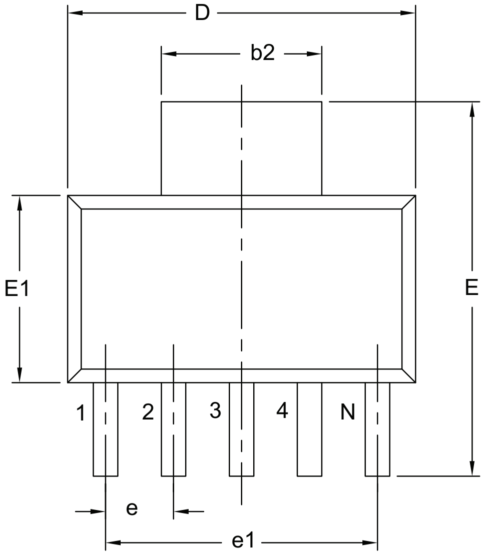
1. § Significant Characteristic.
2. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

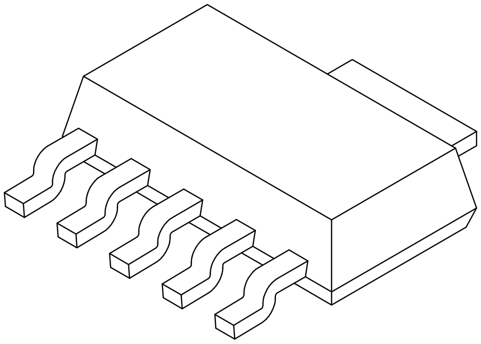
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

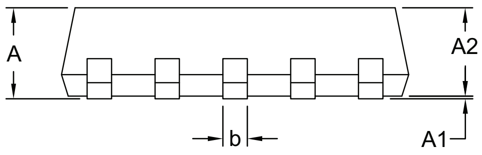
Microchip Technology Drawing C04-012B

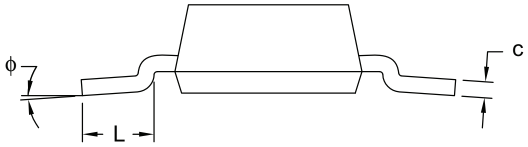
5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		5	
Lead Pitch	e		1.27 BSC	
Outside Lead Pitch	e1		5.08 BSC	
Overall Height	A	–	–	1.80
Standoff	A1	0.02	0.06	0.10
Molded Package Height	A2	1.55	1.60	1.65
Overall Width	E	6.86	7.00	7.26
Molded Package Width	E1	3.45	3.50	3.55
Overall Length	D	6.45	6.50	6.55
Lead Thickness	c	0.24	0.28	0.32
Lead Width	b	0.41	0.457	0.51
Tab Lead Width	b2	2.95	3.00	3.05
Foot Length	L	0.91	–	1.14
Lead Angle	φ	0°	4°	8°

Notes:

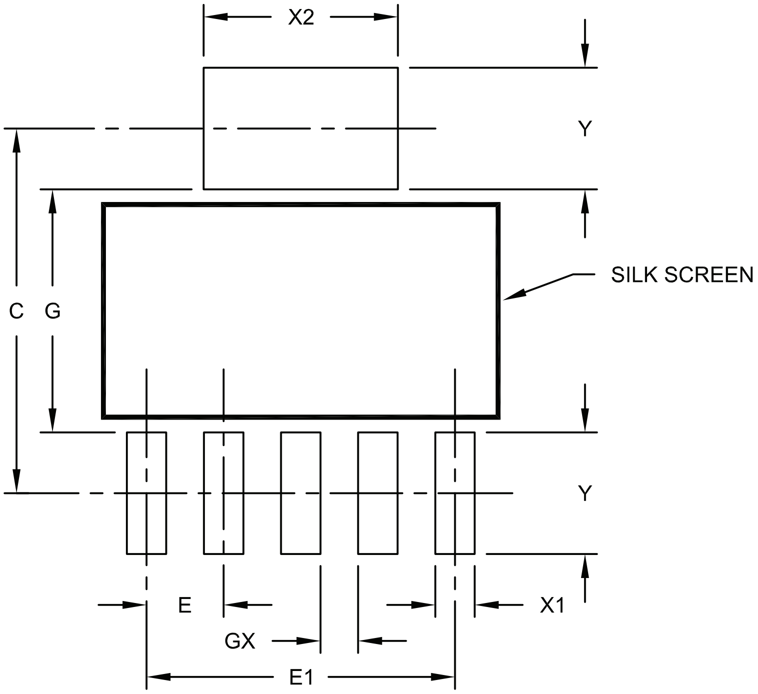
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-137B

5-Lead Plastic Small Outline Transistor (DC) [SOT-223]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Pad Pitch	E		1.27 BSC	
Overall Pad Pitch	E1		5.08 BSC	
Pad Spacing	C		6.00	
Pad Width	X1			0.65
Pad Width	X2			3.20
Pad Length	Y			2.00
Distance Between Pads	G	4.00		
Distance Between Pads	GX	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2137A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (September 2010)

The following is the list of modifications:

- Updated the Features section.
- Removed conditions for the Output Voltage Regulation parameter in the AC/DC Characteristics table.
- Updated the symbol used for the Storage Temperature Range parameter in the TEMPERATURE SPECIFICATIONS table.

Revision A (March 2008)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	X	X	X/	XX
Device	**Output Voltage**	**Feature Code**	**Tolerance**	**Temp.**	**Package**

Device:
MCP1790: 70 mA High Voltage Regulator
MCP1790T: 70 mA High Voltage Regulator Tape and Reel
MCP1791: 70 mA High Voltage Regulator
MCP1791T: 70 mA High Voltage Regulator Tape and Reel

Output Voltage *:
30 = 3.0V “Standard”
33 = 3.3V “Standard”
50 = 5.0V “Standard”

*Contact factory for other output voltage options

Extra Feature Code: 0 = Fixed

Tolerance: 2 = 2.5% (Standard)

Temperature: E = -40° C to +125° C

Package Type:
EB = Plastic, DDPAK, 3-lead
ET = Plastic, DDPAK, 5-lead
DB = Plastic Transistor Outline, SOT-223, 3-lead
DC = Plastic Transistor Outline, SOT-223, 5-lead

Examples:

a) MCP1790-3002E/EB: 3.0V LDO Regulator, 3LD DDPAK
b) MCP1790-3302E/EB: 3.3V LDO Regulator, 3LD DDPAK
c) MCP1790-5002E/EB: 5.0V LDO Regulator, 3LD DDPAK
d) MCP1790-3002E/DB: 3.0V LDO Regulator, 3LD SOT-223
e) MCP1790-3302E/DB: 3.3V LDO Regulator, 3LD SOT-223
f) MCP1790-5002E/DB: 5.0V LDO Regulator, 3LD SOT-223

a) MCP1791-3002E/ET: 3.0V LDO Regulator 5LD DDPAK
b) MCP1791-3302E/ET 3.3V LDO Regulator 5LD DDPAK
c) MCP1791-5002E/ET: 5.0V LDO Regulator 5LD DDPAK
d) MCP1791-3002E/DC 3.0V LDO Regulator 5LD SOT-223
e) MCP1791-3302E/DC 3.3V LDO Regulator 5LD SOT-223
f) MCP1791-5002E/DC 5.0V LDO Regulator 5LD SOT-223

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Trademarks

The Microchip name and logo, the Microchip logo, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, PIC^{32} logo, rfPIC and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, HI-TECH C, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, HI-TIDE, In-Circuit Serial Programming, ICSP, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, Omniscient Code Generation, PICC, PICC-18, PICDEM, PICDEM.net, PICkit, PICtail, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, UniWinDriver, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2010, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

ISBN: 978-1-60932-511-4

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Downloaded from Arrow.com.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/04/10