

MC74VHC74

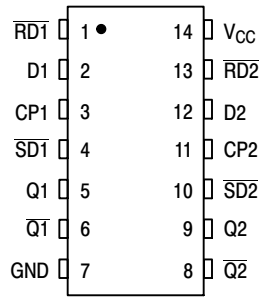


Figure 2. PIN ASSIGNMENT

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V _{in}	DC Input Voltage	– 0.5 to + 7.0	V
V _{out}	DC Output Voltage	– 0.5 to V _{CC} + 0.5	V
I _{IK}	Input Diode Current	–20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	–65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	–55	+ 125	°C
t _r , t _f	Input Rise and Fall Time V _{CC} = 3.3V ±0.3V V _{CC} = 5.0V ±0.5V	0 0	100 20	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V _{CC} V	T _A = 25°C			T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7			1.50 V _{CC} × 0.7		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 to 5.5			0.50 V _{CC} × 0.3		0.50 V _{CC} × 0.3	V
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OH} = - 50μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V _{in} = V _{IH} or V _{IL} I _{OH} = - 4mA I _{OH} = - 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{OL} = 50μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V _{in} = V _{IH} or V _{IL} I _{OL} = 4mA I _{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I _{in}	Maximum Input Leakage Current	V _{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{in} = V _{CC} or GND	5.5			2.0		20.0	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

Symbol	Parameter	Test Conditions	T _A = 25°C			T _A = -55°C to +125°C		Unit
			Min	Typ	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, CP to Q or \bar{Q}	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		6.7 9.2	11.9 15.4	1.0 1.0	14.0 17.5	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.6 6.1	7.3 9.3	1.0 1.0	8.5 10.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, SD or RD to Q or \bar{Q}	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF		7.6 10.1	12.3 15.8	1.0 1.0	14.5 18.0	ns
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF		4.8 6.3	7.7 9.7	1.0 1.0	9.0 11.0	
f _{max}	Maximum Clock Frequency (50% Duty Cycle)	V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF	80 50	125 75		70 45		MHz
		V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF	130 90	170 115		110 75		
C _{in}	Maximum Input Capacitance			4	10		10	pF

C _{PD}	Power Dissipation Capacitance (Note 1)	Typical @ 25°C, V _{CC} = 5.0V	pF
		25	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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TIMING REQUIREMENTS (Input $t_r = t_f = 3.0\text{ns}$)

Symbol	Parameter	V_{CC} V	Guaranteed Limit		Unit
			$T_A = 25^\circ\text{C}$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
t_w	Minimum Pulse Width, CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_w	Minimum Pulse Width, \overline{RD} or \overline{SD}	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_{su}	Minimum Setup Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	6.0 5.0	7.0 5.0	ns
t_h	Minimum Hold Time, D to CP	3.3 ± 0.3 5.0 ± 0.5	0.5 0.5	0.5 0.5	ns
t_{rec}	Minimum Recovery Time, \overline{SD} or \overline{RD} to CP	3.3 ± 0.3 5.0 ± 0.5	5.0 3.0	5.0 3.0	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74VHC74DR2	SOIC-14	2500 Tape & Reel
MC74VHC74DR2G	SOIC-14 (Pb-Free)	2500 Tape & Reel
MC74VHC74DT	TSSOP-14	96 Units / Rail
MC74VHC74DTG	TSSOP-14	96 Units / Rail
MC74VHC74DTR2	TSSOP-14	2500 Tape & Reel
MC74VHC74DTR2G	TSSOP-14	2500 Tape & Reel
MC74VHC74MEL	SOEIAJ-14	2000 Tape & Reel
MC74VHC74MELG	SOEIAJ-14 (Pb-Free)	2000 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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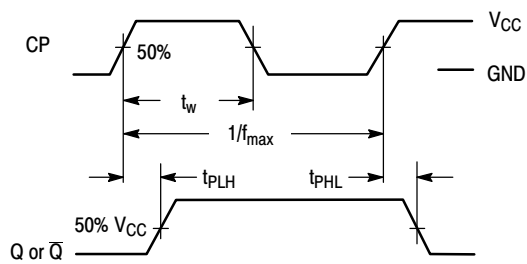


Figure 3.

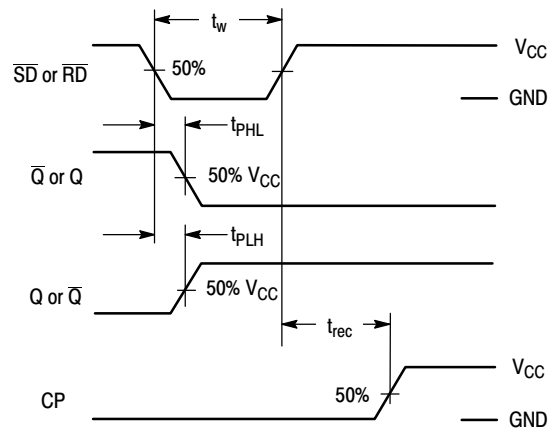


Figure 4.

Switching Waveforms

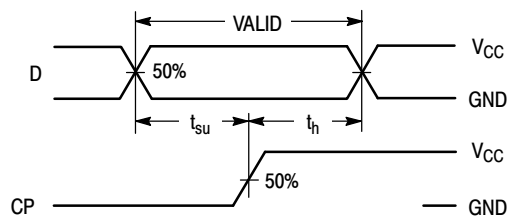
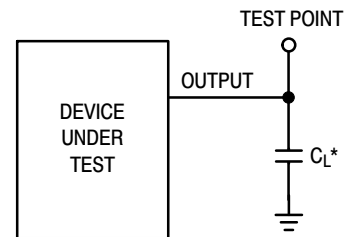


Figure 5.



*Includes all probe and jig capacitance

Figure 6.

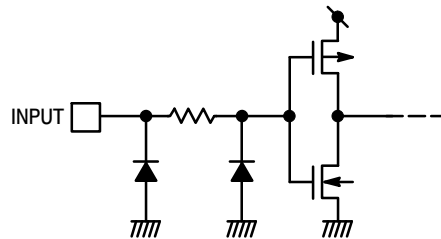
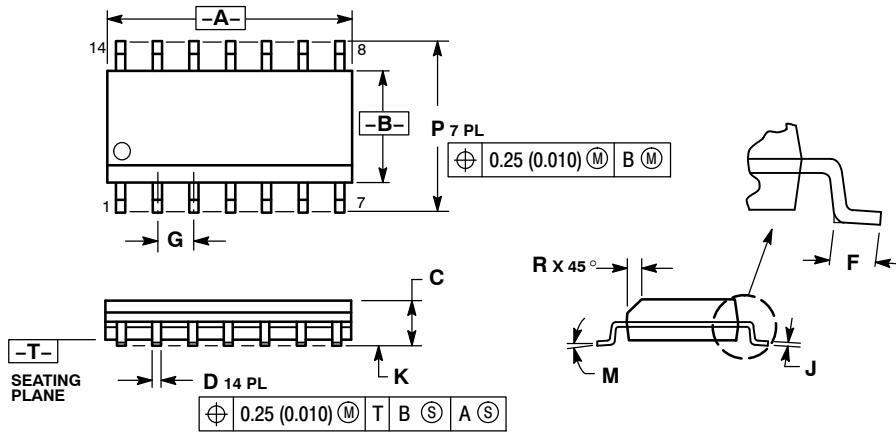


Figure 7. Input Equivalent Circuit

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PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE J

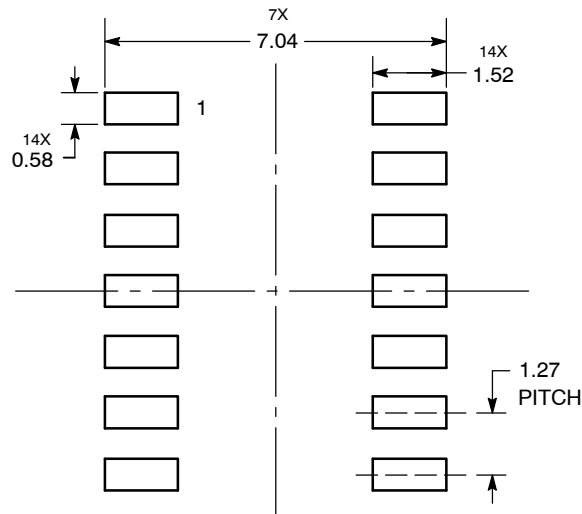


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



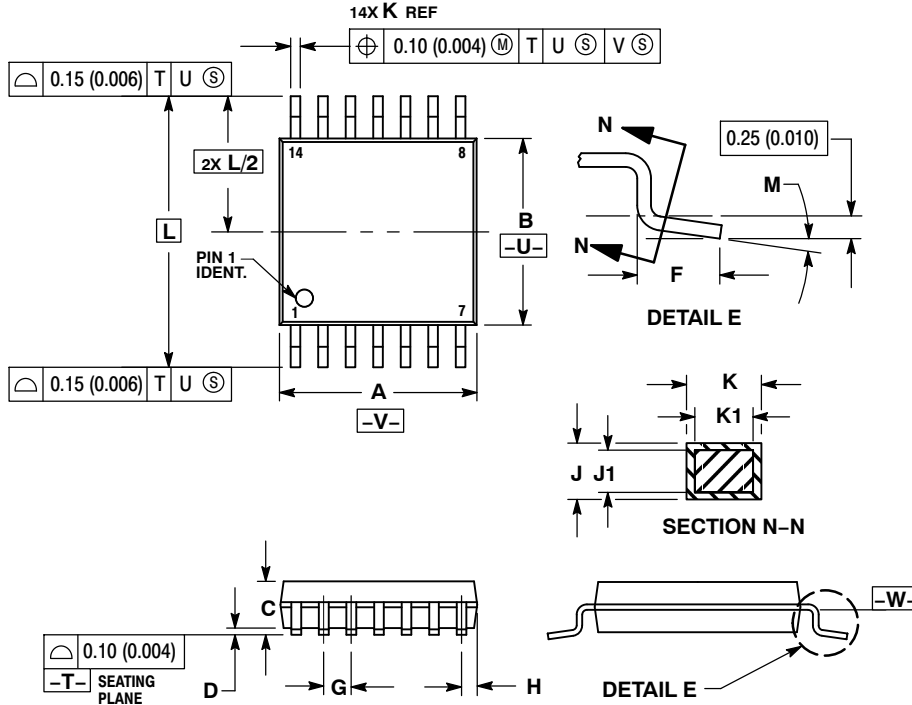
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

TSSOP-14
DT SUFFIX
CASE 948G-01
ISSUE B

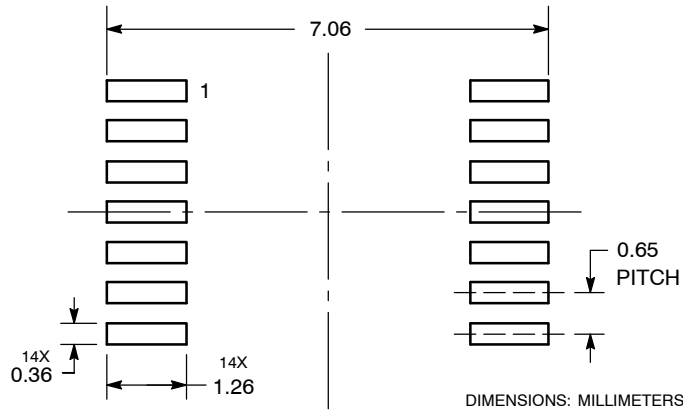


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

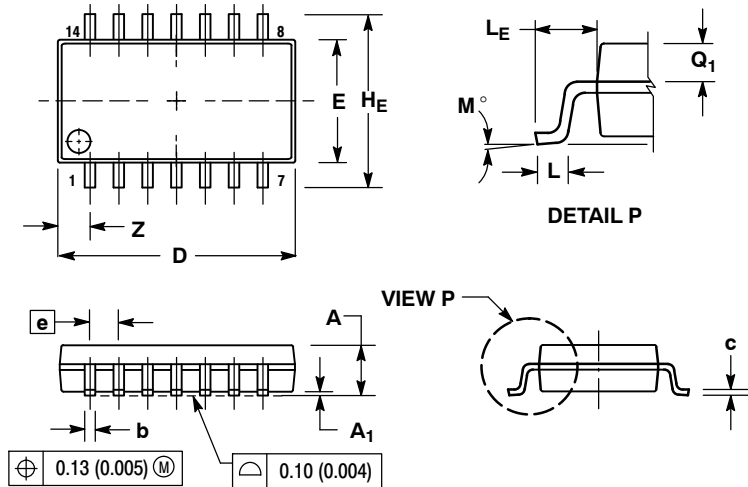
SOLDERING FOOTPRINT



MC74VHC74

PACKAGE DIMENSIONS


SOEIAJ-14
CASE 965-01
ISSUE B



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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