+3V Voltage Monitoring, Low-Cost µP Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
  V_{CC} ....-0.3V to +6V
  All Other Inputs (Note 1)..........................-0.3V to (V_{CC} + 0.3V)
Input Current
  V_{CC} 20mA
  GND 20mA
Output Current (all outputs) 20mA
Continuous Power Dissipation (T_A = +70°C)
  8-Pin CERDIP (derate 8mW/°C above +70°C).............640mW
  8-Pin PDIP (derate 9.1mW/°C above +70°C)............727.3mW
  8-Pin SO (derate 5.9mW/°C above +70°C)................470.6mW
  8-Pin µMAX (derate 4.5mW/°C above +70°C).............362mW
Operating Temperature Range
  MAX70_C ....0°C to +70°C
  MAX70_E ....-40°C to +85°C
  MAX70_M ....-55°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: The input-voltage limits on PFI, WDI, and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX70_P/R, MAX706AP/AR: V_{CC} = 2.7V to 5.5V; MAX70_S, MAX706AS: V_{CC} = 3.0V to 5.5V; MAX70_T, MAX706AT: V_{CC} = 3.15V to 5.5V; T_J = T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{CC}		MAX70_C	1.0		5.5	V
			MAX70_E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	V_{CC} < 3.6V	MAX706_C		90	200	µA
			MAX706_E/M		90	300	
			MAX708_C		50	200	
			MAX708_E/M		50	300	
		V_{CC} < 5.5V	MAX706_C		135	350	
			MAX706_E/M		135	500	
			MAX708_C		65	350	
			MAX708_E/M		65	500	
Reset Threshold (Note 3) (V_{CC} Falling)	V_{RST}	MAX70_P/R, MAX706AP/AR		2.55	2.63	2.70	V
		MAX70_S, MAX706AS		2.85	2.93	3.00	
		MAX70_T, MAX706AT		3.00	3.08	3.15	
Reset Threshold Hysteresis (Note 3)	V_{HYS}				20		mV
Reset Pulse Width (Note 3)	t_{RST}	MAX70_P/R, MAX706AP/AR V_{CC} = 3.0V		140	200	280	ms
		MAX70_S, MAX706AS, V_{CC} = 3.3V		140	200	280	
		V_{CC} = 5V			200		
RESET OUTPUT							
Output-Voltage High (MAX70_R/S/T) (MAX706AR/AS/AT)	V_{OH}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)}$ < V_{CC} < 3.6V	I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	$I_{RSOURCE}$ = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 3.2mA			0.4	
	V_{OL}	MAX70_C V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX70_E/M: V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

(MAX70_P/R, MAX706AP/AR: V_{CC} = 2.7V to 5.5V; MAX70_S, MAX706AS: V_{CC} = 3.0V to 5.5V; MAX70_T, MAX706AT: V_{CC} = 3.15V to 5.5V; T_J = T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_J = T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output-Voltage High (MAX706P) (MAX706AP)	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SOURCE} = 215µA	V_{CC} – 0.6			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SINK} = 1.2mA			0.3	
	V_{OH}	4.5 < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 3.2mA			0.4	
Output-Voltage High (MAX708_)	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SINK} = 500µA			0.3	
	V_{OH}	4.5V < V_{CC} < 5.5V	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	4.5V < V_{CC} < 5.5V	I_{SINK} = 1.2mA			0.4	
WATCHDOG INPUT							
Watchdog Timeout Period	t_{WD}	MAX706P/R, MAX706AP/AR, V_{CC} = 3.0V		1.00	1.6	2.25	s
		MAX706S/T, MAX706AS/AT, V_{CC} = 3.3V		1.00	1.6	2.25	
WDI Pulse Width (MAX706_, MAX706A_)	t_{WP}	V_{IL} = 0.4V	$V_{RST(MAX)} < V_{CC}$ < 3.6V	100			ns
		V_{IH} = 0.8V x V_{CC}	4.5V < V_{CC} < 5.5V	50			
Watchdog Input Threshold (MAX706_, MAX706A_)	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$				0.6	V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$		0.7 x V_{CC}			
	V_{IL}	V_{CC} = 5.0V				0.8	
	V_{IH}	V_{CC} = 5.0V		3.5			
WDI Input Current		WDI = 0V or V_{CC}	MAX706_	-1.0	+0.02	+1.0	µA
			MAX706A_	-5		+5	

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ELECTRICAL CHARACTERISTICS (continued)

(MAX70_P/R, MAX706AP/AR: V_{CC} = 2.7V to 5.5V; MAX70_S, MAX706AS: V_{CC} = 3.0V to 5.5V; MAX70_T, MAX706AT: V_{CC} = 3.15V to 5.5V; $T_J = T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at $T_J = T_A$ = +25°C.) (Note 2)

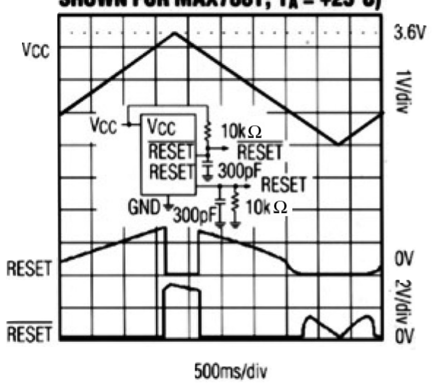
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
WATCHDOG OUTPUT							
$\overline{WDO}$ Output Voltage (MAX706_, MAX706A_)	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SINK} = 500µA			0.3	
	V_{OH}	$4.5V < V_{CC} < 5.5V$	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	$4.5V < V_{CC} < 5.5V$	I_{SINK} = 1.2mA			0.4	
MANUAL RESET INPUT							
$\overline{MR}$ Pullup Current		$\overline{MR}$ = 0	$V_{RST(MAX)} < V_{CC} < 3.6V$	25	70	250	µA
			$4.5V < V_{CC} < 5.5V$	100	250	600	
$\overline{MR}$ Pulse Width	t_{MR}	$V_{RST(MAX)} < V_{CC} < 3.6V$		500			ns
		$4.5V < V_{CC} < 5.5V$		150			
$\overline{MR}$ Input Threshold	V_{IL}	$V_{RST(MAX)} < V_{CC} < 3.6V$				0.6	V
	V_{IH}	$V_{RST(MAX)} < V_{CC} < 3.6V$		0.7 x V_{CC}			
	V_{IL}	$4.5V < V_{CC} < 5.5V$				0.8	
	V_{IH}	$4.5V < V_{CC} < 5.5V$		2.0			
$\overline{MR}$ to Reset Output Delay	t_{MD}	$V_{RST(MAX)} < V_{CC} < 3.6V$				750	ns
		$4.5V < V_{CC} < 5.5V$				250	
POWER-FAILURE COMPARATOR							
PFI Input Threshold		(MAX70_P/R, MAX706AP/AR) PFI falling V_{CC} = 3.0V		1.2	1.25	1.3	V
		(MAX70_S/T, MAX706AS/AT) PFI falling, V_{CC} = 3.3V		1.2	1.25	1.3	
PFI Input Current				-25	+0.01	+25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SOURCE} = 500µA	0.8 x V_{CC}			V
	V_{OL}	$V_{RST(MAX)} < V_{CC} < 3.6V$	I_{SINK} = 1.2mA			0.3	
	V_{OH}	$4.5V < V_{CC} < 5.5V$	I_{SOURCE} = 800µA	V_{CC} - 1.5			
	V_{OL}	$4.5V < V_{CC} < 5.5V$	I_{SINK} = 3.2mA			0.4	

Note 2: All devices 100% production tested at T_A = +85°C. Limits over temperature are guaranteed by design.
Note 3: Applies to both $\overline{RESET}$ in the MAX70_R/S/T and MAX706AR/AS/AT, and RESET in the MAX706P/MAX706AP.

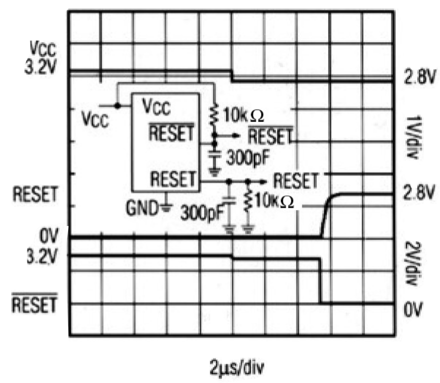
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

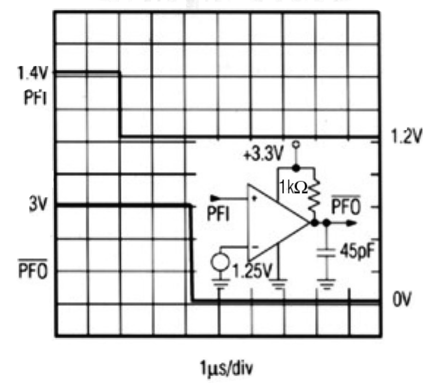
RESET, $\overline{RESET}$ OUTPUT VOLTAGES vs. SUPPLY VOLTAGE (RESET OUTPUTS AND RESET THRESHOLDS SHOWN FOR MAX708T, T_A = +25°C)



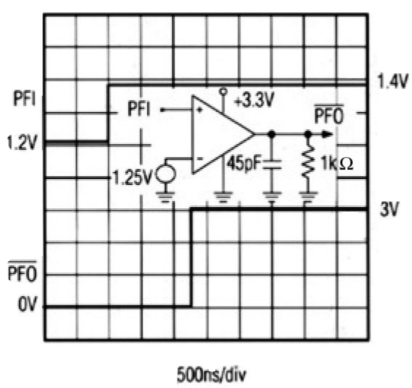
RESET, $\overline{RESET}$ RESPONSE TIMES



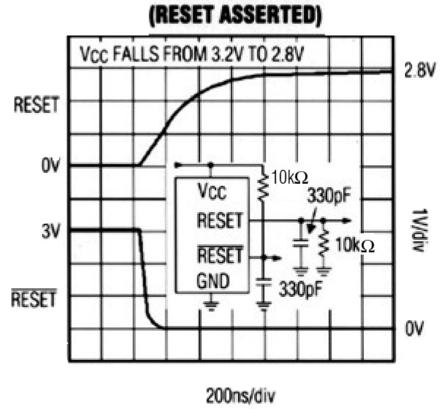
POWER-FAIL COMPARATOR ASSERTION RESPONSE TIME



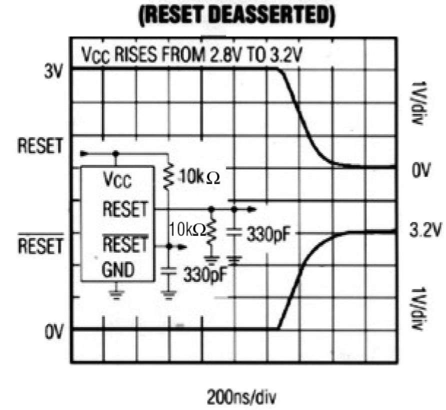
POWER-FAIL COMPARATOR DEASSERTION RESPONSE TIME



RESET, $\overline{RESET}$ RISE AND FALL TIMES (RESET ASSERTED)



RESET, $\overline{RESET}$ RISE AND FALL TIMES (RESET DEASSERTED)



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Pin Description

MAX706P MAX706AP		MAX706R/S/T, MAX706AR/AS/AT		MAX708R/S/T		NAME	FUNCTION
SO/DIP	µMAX	SO/DIP	µMAX	SO/DIP	µMAX		
1	3	1	3	1	3	$\overline{MR}$	Active-Low, Manual-Reset Input. Pull $\overline{MR}$ below 0.6V to trigger a reset pulse. $\overline{MR}$ is TTL/CMOS compatible when V_{CC} = 5V and can be shorted to GND with a switch. $\overline{MR}$ is internally connected to a 70µA source current. Connect to V_{CC} or leave unconnected.
2	4	2	4	2	4	V_{CC}	Supply Voltage Input
3	5	3	5	3	5	GND	Ground
4	6	4	6	4	6	PFI	Adjustable Power-Fail Comparator Input. Connect PFI to a resistive divider to set the desired PFI threshold. When PFI is less than 1.25V, $\overline{PFO}$ goes low and sinks current; otherwise, $\overline{PFO}$ remains high. Connect PFI to GND if not used.
5	7	5	7	5	7	$\overline{PFO}$	Active-Low, Power-Fail Comparator Output. $\overline{PFO}$ asserts when PFI is below the internal 1.25V threshold. $\overline{PFO}$ deasserts when PFI is above the internal 1.25V threshold. Leave $\overline{PFO}$ unconnected if not used.
6	8	6	8	—	—	WDI	Watchdog Input. A falling or rising transition must occur at WDI within 1.6s to prevent $\overline{WDO}$ from asserting (see Figure 4). The internal watchdog timer is reset to zero when reset is asserted or when transition occurs at WDI. The watchdog function for the MAX706P/R/S/T can not be disabled. The watchdog timer for the MAX706AP/AR/AS/AT disables when WDI input is left open or connected to a tri-state output in its high-impedance state with a leakage current of less than 600nA.
7	1	—	—	8	2	RESET	Active-High Reset Output. RESET remains high when V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains low for 200ms after the reset conditions end (Figure 3).
8	2	8	2	—	—	$\overline{WDO}$	Active-Low Watchdog Output. $\overline{WDO}$ goes low when a transition does not occur at WDI within 1.6s and remains low until a transition occurs at WDI (indicating the watchdog interrupt has been serviced). $\overline{WDO}$ also goes low when V_{CC} falls below the reset threshold; however, unlike the reset output signal, $\overline{WDO}$ goes high as soon as V_{CC} rises above the reset threshold.
—	—	7	1	7	1	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ remains low when V_{CC} is below the reset threshold or $\overline{MR}$ is held low. It remains low for 200ms after the reset conditions end (Figure 3).
—	—	—	—	6	8	N.C.	No Connection. Not internally connected.

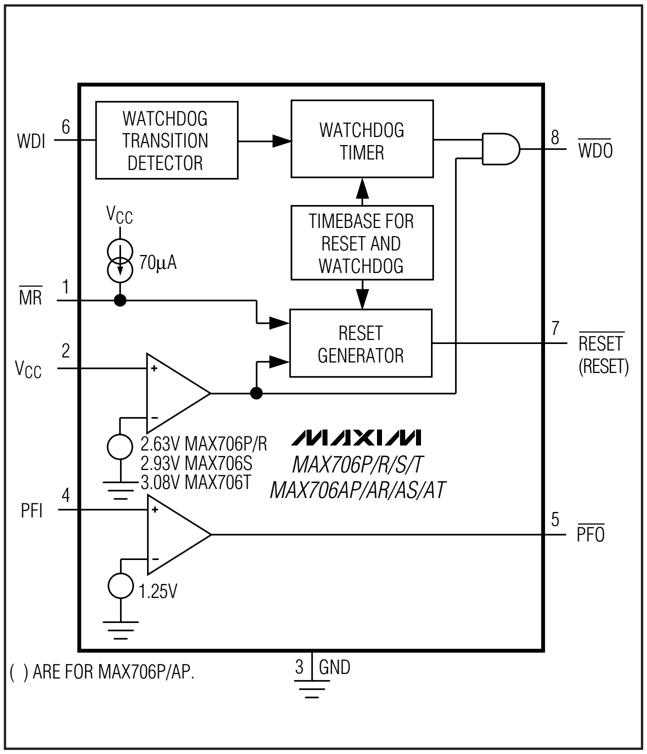

Figure 1. MAX706_ Functional Diagram

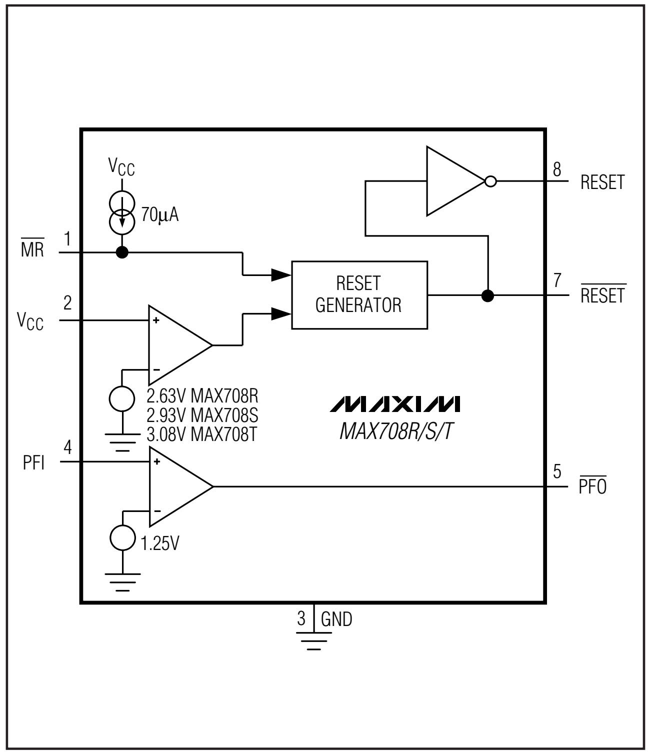

Figure 2. MAX708_ Functional Diagram

RESET and $\overline{\text{RESET}}$ Outputs

A microprocessor's (µP's) reset input starts in a known state. When the µP is in an unknown state, it should be held in reset. The MAX706P/R/S/T and the MAX706AP/AR/AS/AT assert reset when V_{CC} is low, preventing code execution errors during power-up, power-down, or brownout conditions.

On power-up once V_{CC} reaches 1V, $\overline{\text{RESET}}$ is guaranteed to be logic-low and RESET is guaranteed to be logic-high. As V_{CC} rises, $\overline{\text{RESET}}$ and RESET remain asserted. Once V_{CC} exceeds the reset threshold, the internal timer causes $\overline{\text{RESET}}$ and RESET to be deasserted after a time equal to the reset pulse width, which is typically 200ms (Figure 3).

If a power-fail or brownout condition occurs (i.e., V_{CC} drops below the reset threshold), $\overline{\text{RESET}}$ and RESET are asserted. As long as V_{CC} remains below the reset threshold, the internal timer is continually reset, causing the $\overline{\text{RESET}}$ and RESET outputs to remain asserted. Thus, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-down once V_{CC} drops below the reset threshold, $\overline{\text{RESET}}$ and RESET are guaranteed to be asserted for $V_{CC} \geq 1V$.

The MAX706P/MAX706AP provide a RESET signal, and the MAX706R/S/T and MAX706AR/AS/AT provide a $\overline{\text{RESET}}$ signal. The MAX708R/S/T provide both RESET and $\overline{\text{RESET}}$.

Watchdog Timer

The MAX706P/R/S/T and the MAX706AP/AR/AS/AT watchdog circuit monitor the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6s, the watchdog output ($\overline{\text{WDO}}$) goes low (Figure 4). If the reset signal is asserted, the watchdog timer will be reset to zero and disabled. As soon as reset is released, the timer starts counting. WDI can detect pulses as narrow as 100ns with a 2.7V supply and 50ns with a 4.5V supply. The watchdog timer for the MAX706P/R/S/T cannot be disabled. The watchdog timer for the MAX706AP/AR/AS/AT operates similarly to the MAX706P/R/S/T. However, the watchdog timer for the MAX706AP/AR/AS/AT disables when the WDI input is left open or connected to a tri-state output in its high-impedance state and with a leakage current of less than 600nA. The watchdog timer can be disabled anytime, provided $\overline{\text{WDO}}$ is not asserted.

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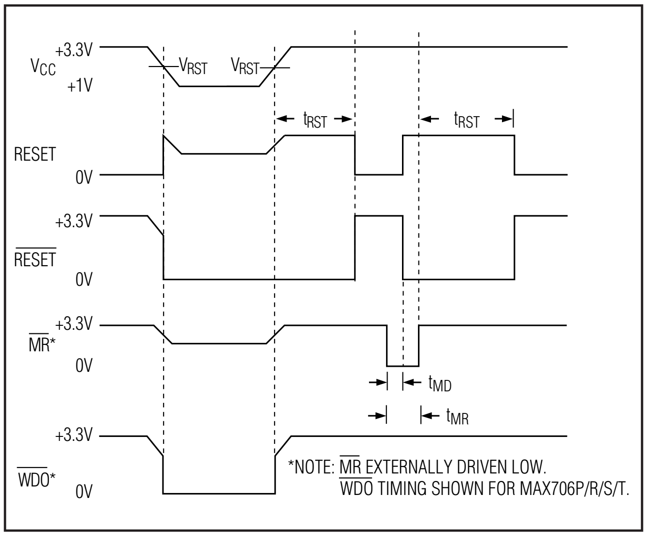


Figure 3. RESET, $\overline{RESET}$, $\overline{MR}$, and $\overline{WDO}$ Timing

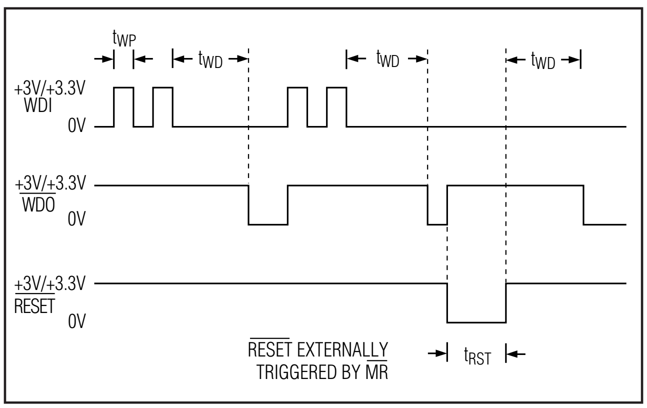
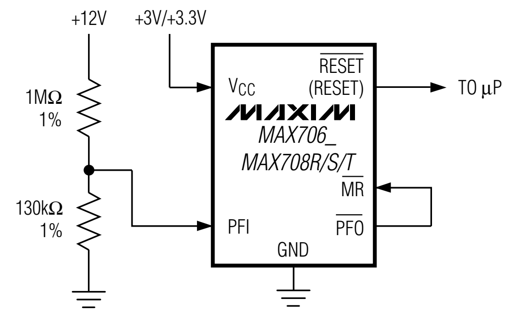


Figure 4. MAX706AP/AR/AS/AT Watchdog Timing

$\overline{WDO}$ can be connected to the nonmaskable interrupt (NMI) input of a µP. When V_{CC} drops below the reset threshold, $\overline{WDO}$ immediately goes low, even if the watchdog timer has not timed out (Figure 3). Normally, this would trigger an NMI, but since reset is asserted simultaneously, the NMI is overridden. The $\overline{WDO}$ should not be connected to $\overline{RESET}$ directly. Instead, connect $\overline{WDO}$ to $\overline{MR}$ to generate a reset pulse when it times out.

Manual Reset

The manual reset ($\overline{MR}$) input allows $\overline{RESET}$ and RESET to be activated by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ can be driven by an external logic line since it is TTL/CMOS compatible. The minimum $\overline{MR}$ input pulse width is 500ns when V_{CC} = +3V and 150ns when V_{CC} = +5V. Leave $\overline{MR}$ unconnected or connect to V_{CC} when not used.



PARAMETER	MIN	TYP	MAX	UNIT
+12V RESET THRESHOLD AT +25°C	10.24	10.87	11.50	V

( ) ARE FOR MAX706P/AP

Figure 5. Monitoring Both +3V/+3.3V and +12V

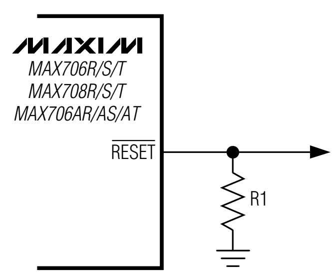


Figure 6. $\overline{RESET}$ Valid to GND Circuit

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference. The power-fail comparator has 10mV of hysteresis, which prevents repeated triggering of the power-fail output ($\overline{PFO}$).

To build an early-warning power-failure circuit, use the power-fail comparator input (PFI) to monitor the unregulated DC supply voltage (see the *Typical Operating Circuits*). Connect the PFI to a resistive-divider network such that the voltage at PFI falls below 1.25V just before the regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

Regulated and unregulated voltages can be monitored by simply adjusting the PFI resistive-divider network values to the appropriate ratio. In addition, the reset signal can be asserted at voltages other that V_{CC} reset threshold, as shown in Figure 5. Connect $\overline{PFO}$ to $\overline{MR}$ to initiate a reset pulse when the 12V supply drops below a user-specified threshold (11V in this example) or when V_{CC} falls below the reset threshold.

Operation with +3V and +5V Supplies

The MAX706P/R/S/T, the MAX706AP/AR/AS/AT, and the MAX708R/S/T provide voltage monitoring at the reset threshold (2.63V to 3.08V) when powered from either +3V or +5V. These devices are ideal in portable-instrument applications where power can be supplied from either a +3V battery or an AC-DC wall adapter that generates +5V (a +5V supply allows a µP or a microcontroller to run faster than a +3V supply). With a +3V supply, these ICs consume less power, but output drive capability is reduced, the $\overline{MR}$ to $\overline{RESET}$ delay time increases, and the $\overline{MR}$ minimum pulse width increases. The *Electrical Characteristics* table provides specifications for operation with both +3V and +5V supplies.

Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V

When V_{CC} falls below 1V, the MAX706R/S/T, MAX706AR/AS/AT, and MAX708R/S/T $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. High-impedance, CMOS logic inputs can drift to undetermined voltages if left as open circuit. If a pulldown resistor is added to the $\overline{RESET}$ pin , as shown in Figure 6, any stray charge or leakage current will flow to ground, holding $\overline{RESET}$ low. Resistor value R is not critical, but it should not load $\overline{RESET}$ and should be small enough to pull $\overline{RESET}$ and the input it is driving to ground. 100kΩ is suggested for R1.

Applications Information

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of the $\overline{PFO}$ when V_{IN} is near the power-fail comparator trip point. Figure 7 shows how to add hysteresis to the power-fail comparator. Select the ratio of R1 and R2 such that PFI

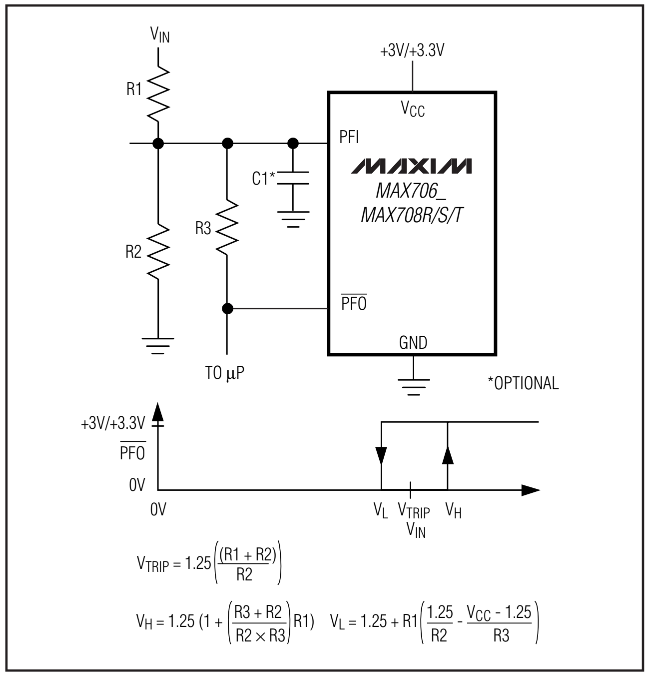


Figure 7. Adding Hysteresis to the Power-Fail Comparator

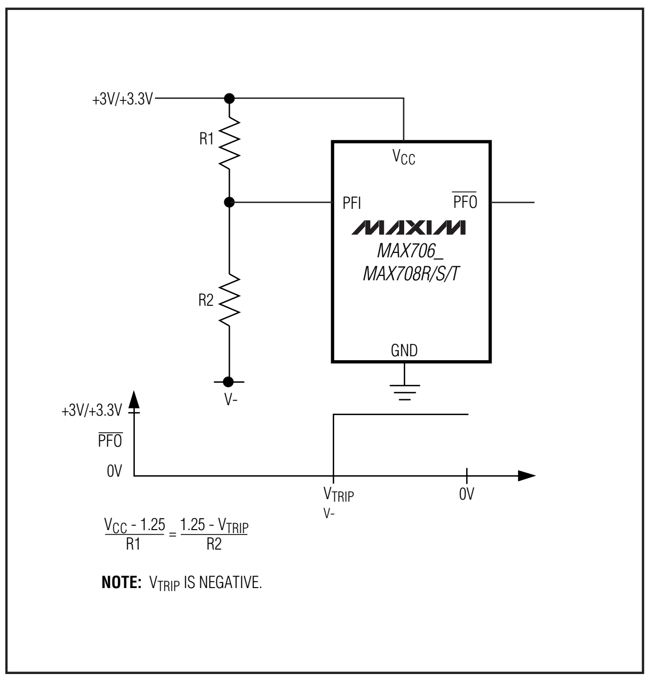


Figure 8. Monitoring a Negative Voltage

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sees 1.25V when V_{IN} falls to the desired trip point (V_{TRIP}). Resistor R3 adds hysteresis. R3 will typically be an order of magnitude greater than R1 and R2. The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point significantly. R3 should be larger than 10kΩ to prevent it from loading down the $\overline{PFO}$ pin. Capacitor C1 adds noise rejection.

Monitoring a Negative Voltage

The power-fail comparator can be used to monitor a negative supply voltage using the circuit of Figure 8. When the negative supply is valid, $\overline{PFO}$ is low. When the negative supply voltage drops, $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} voltage, and resistors R1 and R2.

Bypassing V_{CC}

For noisy systems, bypass V_{CC} with a 0.1µF capacitor to GND.

Ordering Information (continued)

PART†	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX706PEUA	-40°C to +85°C	8 µMAX	U8-1
MAX706PMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX706RCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX706RCSA	0°C to +70°C	8 SO	S8-2
MAX706RCUA	0°C to +70°C	8 µMAX	U8-1
MAX706REPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706RESA	-40°C to +85°C	8 SO	S8-2
MAX706REUA	-40°C to +85°C	8 µMAX	U8-1
MAX706RMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX706SCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX706SCSA	0°C to +70°C	8 SO	S8-2
MAX706SCUA	0°C to +70°C	8 µMAX	U8-1
MAX706SEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706SESA	-40°C to +85°C	8 SO	S8-2
MAX706SEUA	-40°C to +85°C	8 µMAX	U8-1
MAX706SMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX706TCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX706TCSA	0°C to +70°C	8 SO	S8-2
MAX706TCUA	0°C to +70°C	8 µMAX	U8-1
MAX706TEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706TESA	-40°C to +85°C	8 SO	S8-2
MAX706TEUA	-40°C to +85°C	8 µMAX	U8-1
MAX706TMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX706APEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706APESA	-40°C to +85°C	8 SO	S8-2
MAX706APEUA	-40°C to +85°C	8 µMAX	U8-1
MAX706AREPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706ARESA	-40°C to +85°C	8 SO	S8-2
MAX706AREUA	-40°C to +85°C	8µMAX	U8-1
MAX706ASEPA	-40°C to +85°C	8 Plastic Dip	P8-1

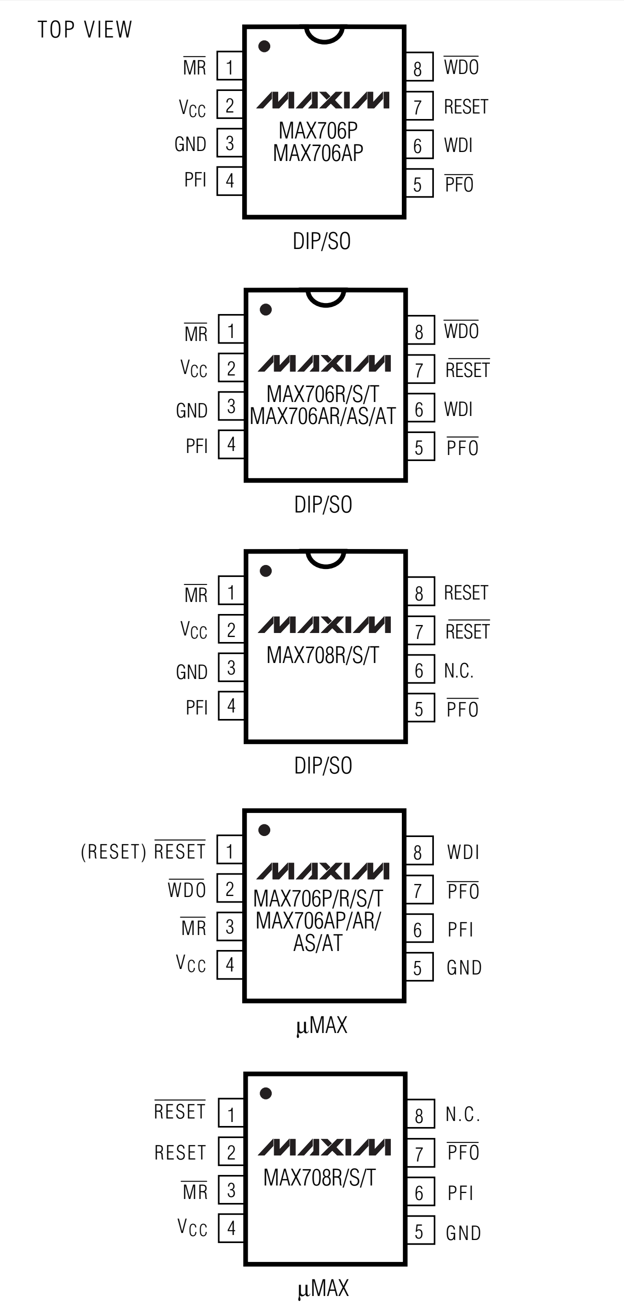
PART†	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX706ASESA	-40°C to +85°C	8 SO	S8-2
MAX706ASEUA	-40°C to +85°C	8 µMAX	U8-1
MAX706ATEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX706ATESA	-40°C to +85°C	8 SO	S8-2
MAX706ATEUA	-40°C to +85°C	8 µMAX	U8-1
MAX708RCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX708RCSA	0°C to +70°C	8 SO	S8-2
MAX708RCUA	0°C to +70°C	8 µMAX	U8-1
MAX708REPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX708RESA	-40°C to +85°C	8 SO	S8-2
MAX708REUA	-40°C to +85°C	8 µMAX	U8-1
MAX708RMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX708SCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX708SCSA	0°C to +70°C	8 SO	S8-2
MAX708SCUA	0°C to +70°C	8 µMAX	U8-1
MAX708SEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX708SESA	-40°C to +85°C	8 SO	S8-2
MAX708SEUA	-40°C to +85°C	8 µMAX	U8-1
MAX708SMJA	-55°C to +125°C	8 CERDIP*	J8-2
MAX708TCPA	0°C to +70°C	8 Plastic Dip	P8-1
MAX708TCSA	0°C to +70°C	8 SO	S8-2
MAX708TCUA	0°C to +70°C	8 µMAX	U8-1
MAX708TEPA	-40°C to +85°C	8 Plastic Dip	P8-1
MAX708TESA	-40°C to +85°C	8 SO	S8-2
MAX708TEUA	-40°C to +85°C	8 µMAX	U8-1
MAX708TMJA	-55°C to +125°C	8 CERDIP*	J8-2

†SO, µMAX, and PDIP packages are available in lead-free.
**Contact factory for availability and processing to MIL-STD-883.*

Chip Information

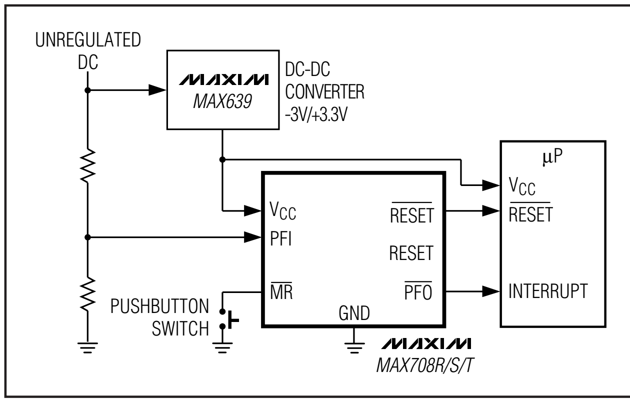
PROCESS: CMOS

Pin Configurations



( ) ARE FOR MAX706P/AP ONLY.

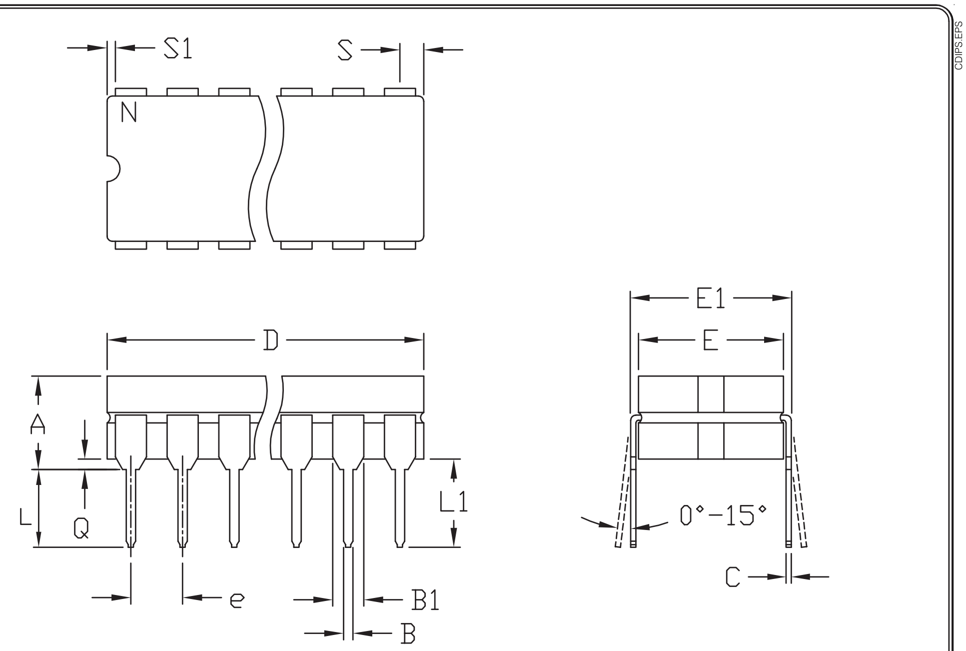
Typical Operating Circuits (continued)



+3V Voltage Monitoring, Low-Cost µP Supervisory Circuits

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

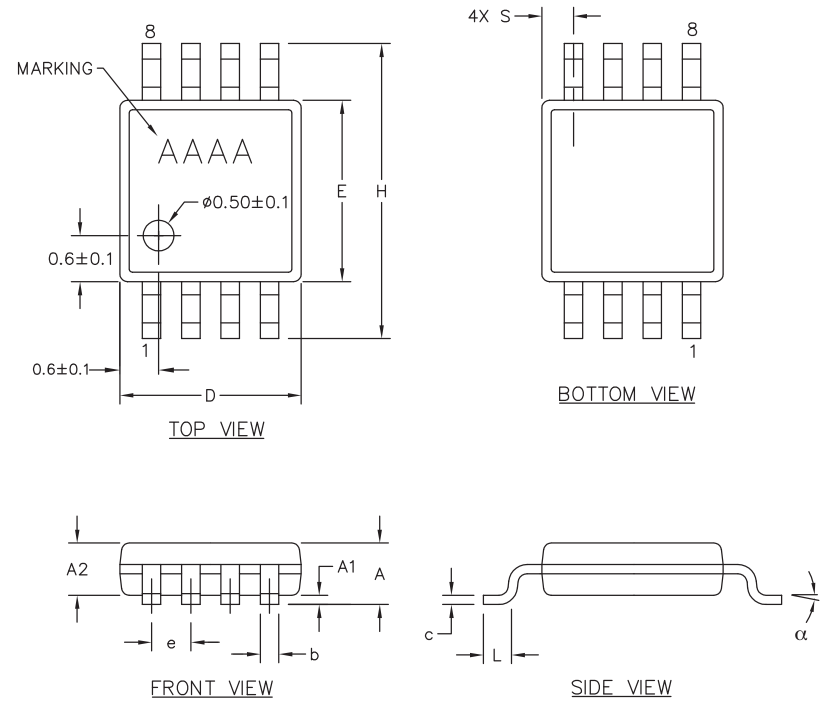
TITLE: PACKAGE FAMILY OUTLINE: CDIP .300"

1/1

DOCUMENT CONTROL NUMBER: 21-0045 REV: A

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8–1; U8–3; U8CN–1

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

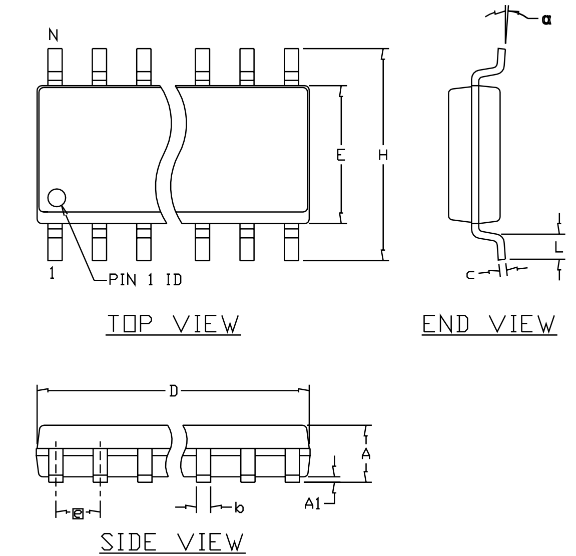
TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0036	L	1/1

+3V Voltage Monitoring, Low-Cost µP Supervisory Circuits

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
A	.053	.069	1.35	1.75
A1	.004	.010	0.10	0.25
b	.014	.019	0.35	0.49
c	.007	.010	0.19	0.25
E	.150	.157	3.80	4.00
e	.050 BSC		1.27 BSC	
H	.228	.244	5.80	6.20
L	.016	.050	0.40	1.27
α	0°	8°	0°	8°

VARIATION A				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.189	.197	4.80	5.00
N	8			
MS012	AA			
PKG. CODE	S8-2, S8-4, S8-5, S8-6F, S8-7F, S8-8F, S8-10F, S8-11F, S8-16F			

VARIATION B				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.337	.344	8.55	8.75
N	14			
MS012	AB			
PKG. CODE	S14-1, S14-4, S14-5, S14-6; S14M-4, S14M-5, S14M-6, S14M-7			

VARIATION C				
SYMBOL	INCHES		MM	
	MIN.	MAX.	MIN.	MAX.
D	.386	.394	9.80	10.00
N	16			
MS012	AC			
PKG. CODE	S16-1, S16-3, S16-5, S16-6, S16-8, S16-7F, S16-9F, S16-10F; S16M-3, S16M-6			

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.
2. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.15 MM (.006") PER SIDE.
4. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
5. MEETS JEDEC MS012
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

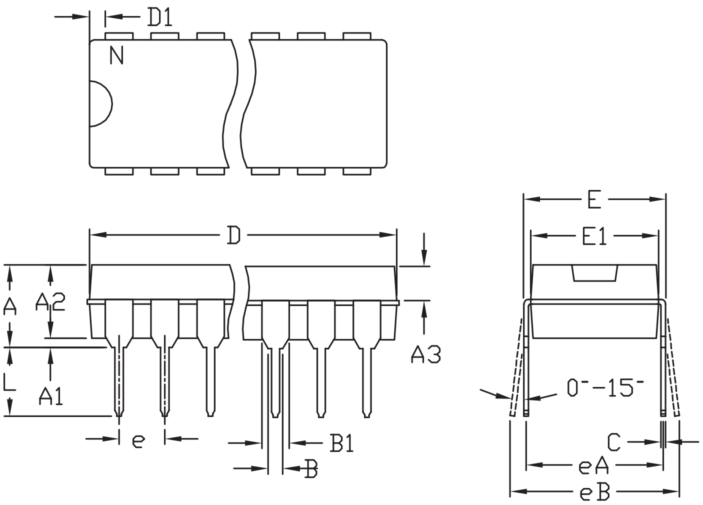
TITLE: PACKAGE OUTLINE, 8L, 14L, 16L SOIC .150 INCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	C	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR. SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0043 REV: D

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