Absolute Maximum Ratings

(All voltages referenced to GND)

V_{CC} .....-0.3V to +6V
Open-Drain $\overline{RESET}$, $\overline{MROUT}$.....-0.3V to +6V
$\overline{MR}$, Push-Pull $\overline{RESET}$, $\overline{MROUT}$ .....-0.3V to (V_{CC} + 0.3V)
$\overline{MR}$, RSTIN .....-0.3V to +6V
Input Current, All Pins .....±20mA
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 8.7mW/°C above +70°C) 696mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free.....+260°C
Containing Lead .....+240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 1.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}			1.0		5.5	V
V_{CC} Supply Current	I_{CC}	V_{CC} = 5.5V, no load			7	20	µA
		V_{CC} = 3.6V, no load			6	16	
V_{CC} Reset Threshold	V_{TH}	46		4.50	4.63	4.75	V
		44		4.25	4.38	4.50	
		31		3.00	3.08	3.15	
		29		2.85	2.93	3.00	
		26		2.55	2.63	2.70	
		23		2.25	2.32	2.38	
		22		2.12	2.19	2.25	
		17		1.62	1.67	1.71	
		16		1.52	1.58	1.62	
Reset Threshold Tempco					60		ppm/°C
Reset Threshold Hysteresis					2 × V_{TH}		mV
RSTIN Threshold	$V_{TH-RSTIN}$	T_A = 0°C to +85°C		0.615	0.630	0.645	V
		T_A = -40°C to +85°C		0.610		0.650	
RSTIN Threshold Hysteresis	V_{HYST}				2.5		mV
RSTIN Input Current	I_{RSTIN}			-25		+25	nA
RSTIN to Reset Output Delay		V_{RSTIN} falling at 1mV/µs			15		µs
Reset Timeout Period	t_{RP}			140	210	280	ms
V_{CC} to $\overline{RESET}$ Output Delay	t_{RD}	V_{CC} falling at 1mV/µs			20		µs
$\overline{MR}$ Minimum Setup Period (Pulse Width)	t_{MR}	$\overline{MR}$ to $\overline{RESET}$	K	6.72	10.08	13.44	s
			L	4.48	6.72	8.16	
			S	2.24	3.36	4.48	
			T	1.12	1.68	2.24	
$\overline{MR}$ Minimum Input Pulse		$\overline{RESET}$ asserted, MAX6455/MAX6456		2.24	3.36	4.48	s
$\overline{MR}$ Glitch Rejection					100		ns
$\overline{MR}$ to MROUT Delay					200		ns
Manual Reset Timeout Period	t_{MRP}			140	210	280	ms

Electrical Characteristics (continued)

(V_{CC} = 1.0V to 5.5V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

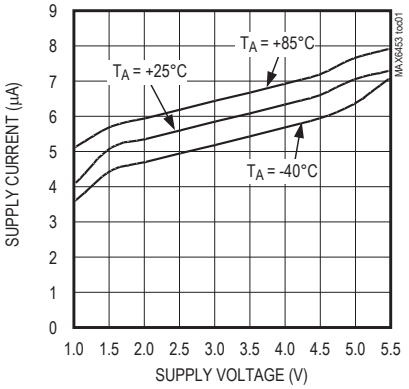
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{MR}$ to V_{CC} Pullup Impedance			25	50	75	kΩ
$\overline{RESET}$, $\overline{MROUT}$ Output Low (Open Drain or Push-Pull)	V_{OL}	V_{CC} ≥ 1.00V, I_{SINK} = 50µA, outputs asserted			0.3	V
		V_{CC} ≥ 1.20V, I_{SINK} = 100µA, outputs asserted			0.3	
		V_{CC} ≥ 2.55V, I_{SINK} = 1.2mA, outputs asserted			0.3	
		V_{CC} ≥ 4.25V, I_{SINK} = 3.2mA, outputs asserted			0.4	
$\overline{RESET}$, $\overline{MROUT}$ Output High (Push-Pull)	V_{OH}	V_{CC} ≥ 1.80V, I_{SOURCE} = 200µA, outputs deasserted	0.8 × V_{CC}			V
		V_{CC} ≥ 3.15V, I_{SOURCE} = 500µA, outputs deasserted	0.8 × V_{CC}			
		V_{CC} ≥ 4.75V, I_{SOURCE} = 800µA, outputs deasserted	0.8 × V_{CC}			
$\overline{RESET}$, $\overline{MROUT}$ Output Open-Drain Leakage Current	I_{LKG}	Outputs deasserted			1	µA
$\overline{MR}$ Input Low Voltage	V_{IL}				0.3 × V_{CC}	V
$\overline{MR}$ Input High Voltage	V_{IH}		0.7 × V_{CC}			V

Note 1: Devices production tested at T_A = 25°C. Overtemperature limits are guaranteed by design.

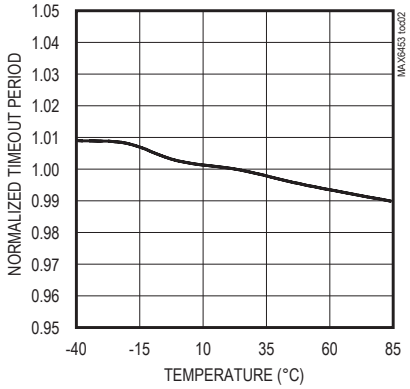
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

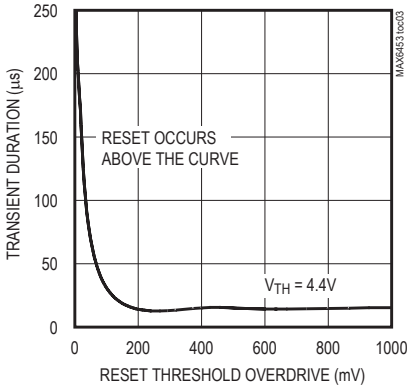
SUPPLY CURRENT vs. SUPPLY VOLTAGE



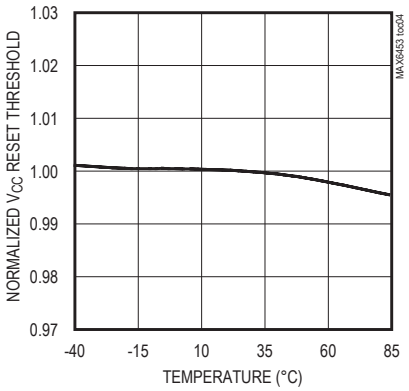
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



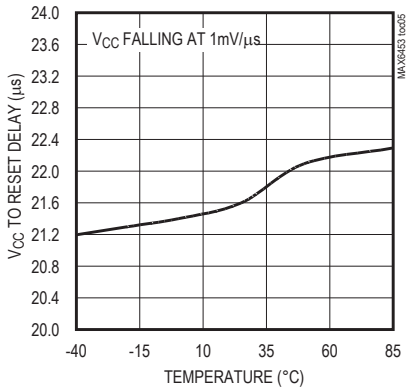
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



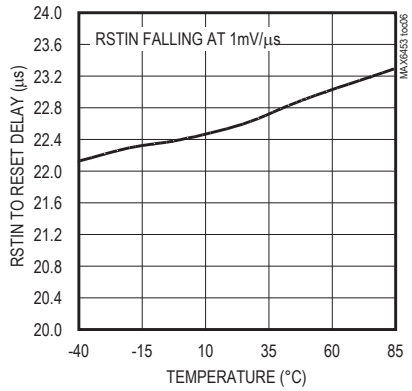
NORMALIZED V_{CC} RESET THRESHOLD vs. TEMPERATURE



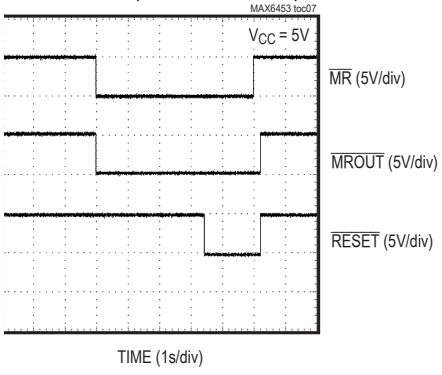
V_{CC} TO RESET DELAY vs. TEMPERATURE



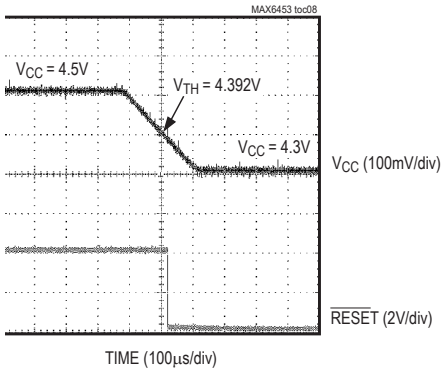
RSTIN TO RESET DELAY vs. TEMPERATURE (RSTIN FALLING)



MANUAL RESET TO $\overline{\text{MROUT}}$ AND $\overline{\text{RESET}}$ DELAY (MAX6455/MAX6456)



V_{CC} TO $\overline{\text{RESET}}$ DELAY



Pin Description

PIN		NAME	FUNCTION
MAX6453 MAX6454	MAX6455 MAX6456		
1	—	$\overline{RESET}$	Active-Low Push-Pull or Open-Drain Output. $\overline{RESET}$ changes from high to low when V_{CC} or RSTIN drops below its selected reset threshold. $\overline{RESET}$ remains low for the 140ms (min) reset timeout period after all monitored power-supply inputs exceed their selected reset thresholds. $\overline{MR}$ does not affect $\overline{RESET}$ output. For open-drain outputs, connect to an external pullup resistor.
—	1		Active-Low Push-Pull or Open-Drain Output. $\overline{RESET}$ changes from high to low when V_{CC} or RSTIN drops below its selected reset threshold. $\overline{RESET}$ remains low for the 140ms (min) reset timeout period after all monitored power-supply inputs exceed their selected reset thresholds. $\overline{RESET}$ changes from high to low after $\overline{MR}$ input is held low for the extended (typ) setup timeout period and deasserts 140ms (min) after $\overline{MR}$ deasserts. For open-drain outputs, connect to an external pullup resistor.
2	2	GND	Ground
3	3	$\overline{MROUT}$	Manual Reset Push-Pull or Open-Drain Output. $\overline{MROUT}$ asserts immediately after $\overline{MR}$ is pulled low. $\overline{MROUT}$ remains low for 140ms (min) after $\overline{MR}$ is deasserted. For open-drain outputs, connect to an external pullup resistor.
4	4	V_{CC}	V_{CC} Voltage Input. Power supply and input for the primary microprocessor voltage reset monitor.
5	5	RSTIN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RSTIN to the center point of an external resistor divider to set the threshold of the externally monitored voltage.
6	—	$\overline{MR}$	Manual Reset Input. Internal 50kΩ pullup to V_{CC}. Pull $\overline{MR}$ low to immediately assert $\overline{MROUT}$. $\overline{MR}$ does not affect $\overline{RESET}$ output.
—	6		Manual Reset Input. Internal 50kΩ pullup to V_{CC}. Pull $\overline{MR}$ low to immediately assert $\overline{MROUT}$. $\overline{RESET}$ changes from high to low after $\overline{MR}$ input is held low for the extended (typ) setup timeout period.

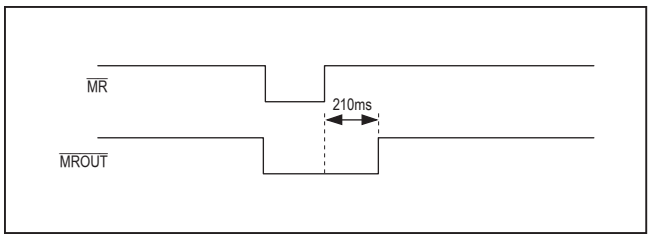


Figure 1. MAX6453/MAX6454 Timing Diagram

Detailed Description

Reset Output

The reset output is typically connected to the reset input of a microprocessor (µP). A µP's reset input starts or restarts the µP in a known state. The MAX6453–MAX6456 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down and brownout conditions (see the *Typical Operating Circuit*).

$\overline{RESET}$ changes from high to low whenever the monitored voltage (RSTIN or V_{CC}) drops below the reset threshold voltages. When VRSTIN and V_{CC} exceed their respective reset threshold voltages, $\overline{RESET}$ remains low for the reset timeout period, and then goes high. $\overline{RESET}$ changes from high to low after $\overline{MR}$ input is held low for the extended (typ) setup timeout period and deasserts 140ms (min) after $\overline{MR}$ deasserts.

$\overline{RESET}$ is guaranteed to be in the proper output logic state for V_{CC} inputs ≥ 1V. For applications requiring valid reset logic when V_{CC} is less than 1V, see the *Ensuring a Valid $\overline{RESET}$ Output Down to V_{CC} = 0V* section.

Manual Reset

The MAX6453/MAX6454 contain a manual reset output ($\overline{MROUT}$) that asserts low immediately after driving $\overline{MR}$ low and remains low for the reset timeout period after $\overline{MR}$ goes high (Figure 1). The pushbutton manual reset has no effect on the $\overline{RESET}$ output. $\overline{MROUT}$ output can be used to drive an NMI (nonmaskable interrupt) on the processor to save valuable data.

The MAX6455/MAX6456's $\overline{MROUT}$ is asserted immediately upon driving $\overline{MR}$ low. Driving $\overline{MR}$ low for longer than the extended (typ) setup timeout period asserts $\overline{RESET}$. When $\overline{MR}$ is deasserted, $\overline{MROUT}$ and $\overline{RESET}$ remain asserted low for the reset timeout period after $\overline{MR}$ goes high (Figure 2).

Adjustable Input Voltage (RSTIN)

The MAX6453–MAX6456 monitor the voltage on RSTIN using an adjustable reset threshold set with an external resistor voltage divider (Figure 3). Use the following formula to calculate the externally monitored voltage (V_{MON-TH}):

$$V_{MON-TH} = V_{TH-RSTIN} \times (R1 + R2)/R2$$

where V_{MON_TH} is the desired reset threshold voltage and $V_{TH-RSTIN}$ is the reset input threshold (0.63V). Resistors R1 and R2 can have very high values to minimize current consumption due to low leakage currents. Set R2 to some conveniently high value (250kΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2\ 5\ (V_{MON\_TH/VTH} - 1)\Omega$$

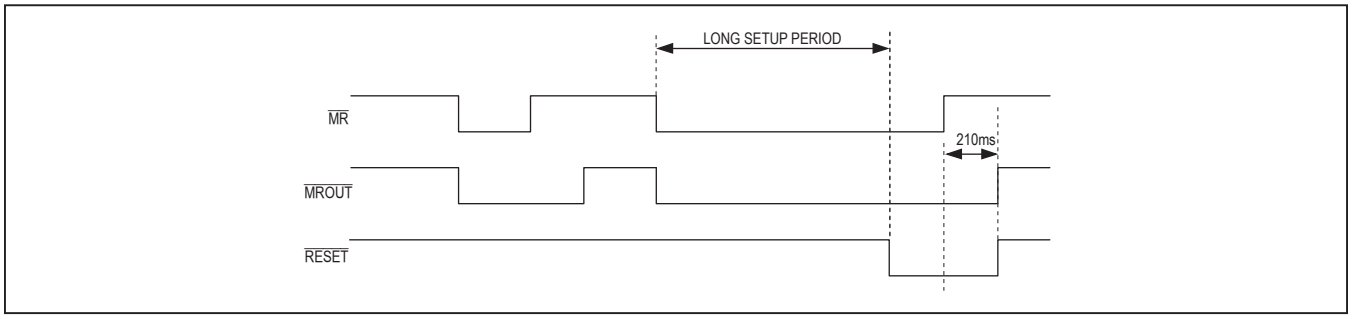


Figure 2. MAX6455/MAX6456 Timing Diagram

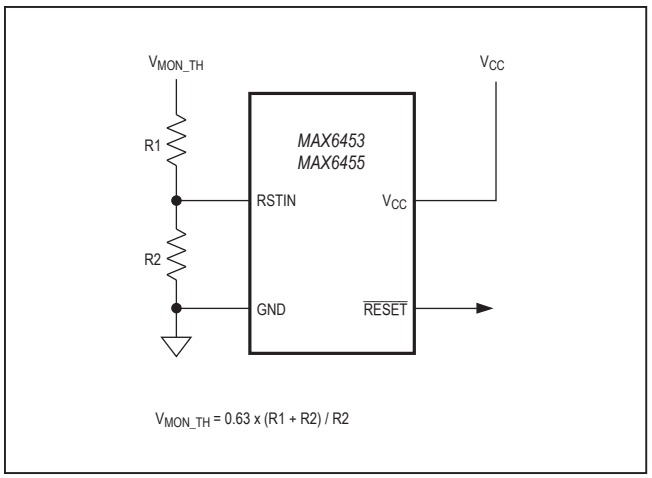


Figure 3. Calculating The Monitored Threshold Voltages

Applications Information

Interrupt Before Reset

To minimize data loss and speed system recovery/test, many applications interrupt the processor or reset only portions of the system before a processor hard reset is asserted. The extended setup time of the MAX6455/MAX6456 $\overline{MR}$ input allows the same pushbutton (Figure 4) to control both the interrupt and hard reset functions. If the pushbutton is closed for less than the extended setup timeout period, the processor is only interrupted ($\overline{MROUT}$). If the system still does not respond properly, the pushbutton can be closed for the full extended setup timeout period to hard reset the processor ($\overline{RESET}$). If desired, connect a LED to the $\overline{RESET}$ output to turn off (or on) to signify when the pushbutton is closed long enough for a hard reset (the same LED can be used as the front panel power-on display).

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{RESET}$ output can be used to interface to a μP with other logic levels. As shown in Figure 5, the open-drain output can be connected to voltages from 0 to 6V.

Generally, the pullup resistor connected to the $\overline{RESET}$ connects to the supply voltage being monitored at the IC's V_{CC} pin. However, some systems might use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 5). Keep in mind that as the supervisor's V_{CC} decreases toward 1V, so does the IC's ability to sink current at $\overline{RESET}$ ($\overline{RESET}$ is pulled high as V_{CC} decays toward 0). The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

Ensuring a Valid $\overline{RESET}$ Down to V_{CC} = 0V (Push-Pull $\overline{RESET}$)

When V_{CC} falls below 1V, $\overline{RESET}$ current-sinking capabilities decline drastically. The high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problem in most applications, because most μPs and other circuitry do not operate with V_{CC} below 1V.

In applications where $\overline{RESET}$ must be valid down to 0V, add a pulldown resistor between $\overline{RESET}$ and GND for the push/pull outputs. The resistor sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 6). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. The external pulldown cannot be used with the open-drain reset outputs.

Transient Immunity

In addition to issuing a reset to the μP during power-up, power-down and brownout conditions, these supervisors are relatively immune to short duration falling transients (glitches). The graph Maximum Transient Duration vs. Reset Threshold Overdrive in the *Typical Operating Characteristics* section shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a negative going pulse applied to V_{CC}, starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient increases (V_{CC} goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20μs or less does not cause a reset pulse to be issued.

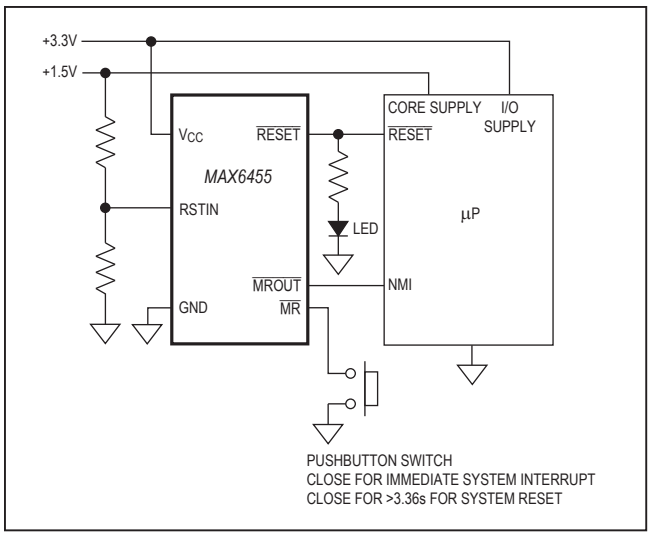


Figure 4. Interrupt Before Reset Application Circuit

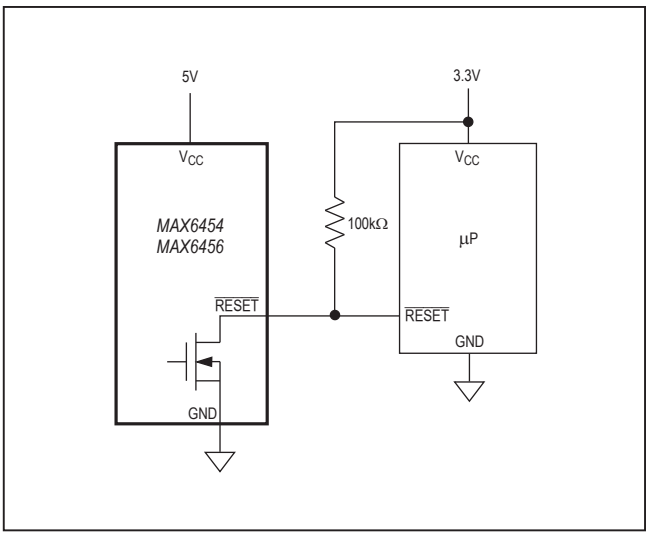


Figure 5. Interfacing to Other Voltage Levels

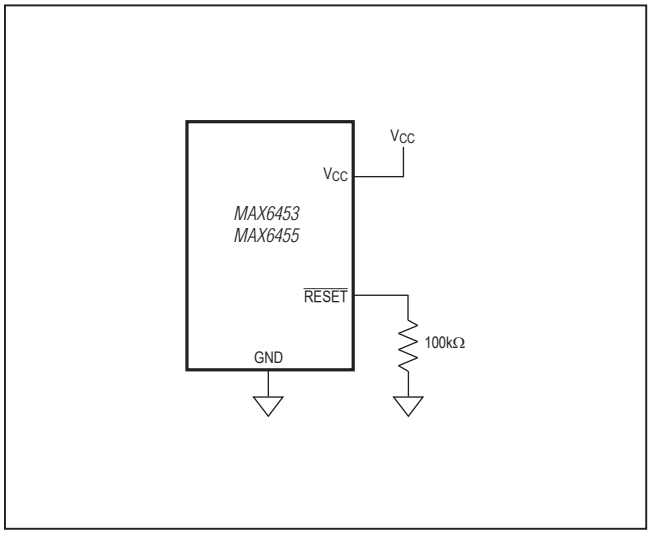


Figure 6. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0

Functional Diagram

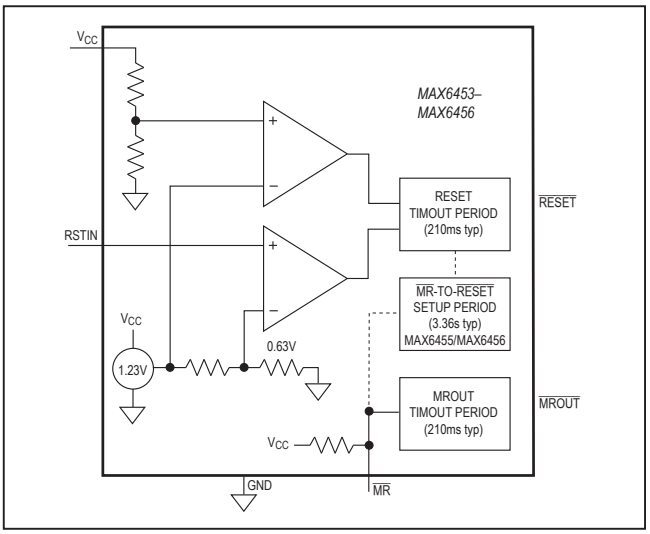


Table 1. Reset Voltage Threshold

PART NO. SUFFIX (_ _)	V_{CC} NOMINAL VOLTAGE THRESHOLD (V)
46	4.625
44	4.375
31	3.075
29	2.925
26	2.625
23	2.313
22	2.188
17	1.665
16	1.575

Table 2. Manual Reset Setup Period

PART NO. SUFFIX (_)	MANUAL RESET PERIOD (s)
K	10.08
L	6.72
S	3.36
T	1.68

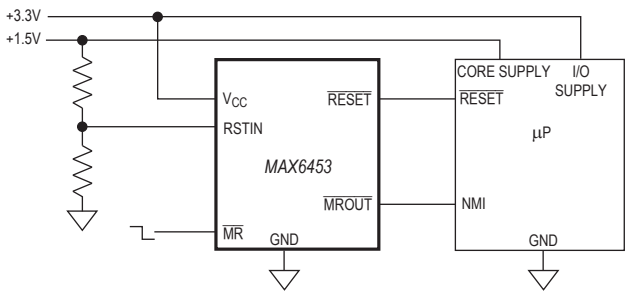
Table 3. Standard Versions Table

PART	TOP MARK	PART	TOP MARK
MAX6453UT16S	ABOG	**MAX6455**UT16S	ABOL
MAX6453UT23S	ABOH	MAX6455UT23S	ABOM
MAX6453UT26S	ABOI	MAX6455UT26S	ABON
MAX6453UT29S	ABOJ	MAX6455UT29S	ABOO
MAX6453UT46S	ABOK	MAX6455UT46S	ABER
MAX6454UT16S	ABOP	**MAX6456**UT16S	ABES
MAX6454UT23S	ABEQ	MAX6456UT23S	ABOT
MAX6454UT26S	ABOQ	MAX6456UT26S	ABOU
MAX6454UT29S	ABOR	MAX6456UT29S	ABOV
MAX6454UT46S	ABOS	MAX6456UT46S	ABOW

Selector Guide

PART	$\overline{MR}$ TO $\overline{RESET}$ DELAY	$\overline{MR}$ ASSERTION	$\overline{MROUT}$ AND $\overline{RESET}$ PUSH-PULL OUTPUT	$\overline{MROUT}$ AND $\overline{RESET}$ OPEN-DRAIN OUTPUT
MAX6453	—	$\overline{MROUT}$	✔	—
MAX6454	—	$\overline{MROUT}$	—	✔
MAX6455	✔	$\overline{MROUT}$ and $\overline{RESET}$	✔	—
MAX6456	✔	$\overline{MROUT}$ and $\overline{RESET}$	—	✔

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
6 SOT23	U6-1	21-0058	90-0175

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/02	Initial release	—
3	6/10	Revised the *General Description, Features, Applications, Ordering Information, Absolute Maximum Ratings, Electrical Characteristics, Pin Description,* the *Reset Output, Manual Reset,* and *Interrupt Before Reset* sections, and Tables 2 and 3 to add extended setup time specifications.	1, 2, 5, 6, 7, 9
4	5/14	No /V OPNs; removed automotive reference from *Applications* section	1