High-Current, 25Ω, SPDT, CMOS Analog Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +44V
V- to GND .....-44V to +0.3V
V+ to V- .....-0.3V to +44V
All Other Pins to GND (Note 1) ..... (V- - 0.3V) to (V+ + 0.3V)
Continuous Current COM, NO, NC (MAX4660).....±150mA
Continuous Current COM, NO, NC (MAX4659).....±75mA
Continuous Current IN .....±30mA
Peak Current COM, NO, NC
MAX4660 (pulsed at 1ms, 10% duty cycle) .....±200mA
MAX4659 (pulsed at 1ms, 10% duty cycle) .....±150mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin µMAX-EP (derate 10.3mW/°C above +70°C)
MAX4660 .....825mW
8-Pin µMAX (derate 4.50mW/°C above +70°C)
MAX4659 .....362mW
8-Pin SO-EP (derate 18.9mW/°C above +70°C)
MAX4660 .....1509mW
8-Pin SO (derate 5.88mW/°C above +70°C)
MAX4659 .....471mW
Operating Temperature Ranges
MAX4659/MAX4660 .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Signals on NO, NC, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}			V-		V+	V
On-Resistance	R_{ON}	I_{COM} = 50mA; V_{NO} or V_{NC} = ±10V	+25°C		18	25	Ω
			T_{MIN} to T_{MAX}			30	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{COM} = 50mA; V_{NO} or V_{NC} = ±10V	+25°C		0.4	1.2	Ω
			T_{MIN} to T_{MAX}			1.5	
On-Resistance Flatness (Note 3)	$R_{FLAT (ON)}$	I_{COM} = 50mA; V_{NO} or V_{NC} = -5V, 0, +5V	+25°C		0.5	1.5	Ω
			T_{MIN} to T_{MAX}			2	
NO or NC Off-Leakage Current (Note 4)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V_{COM} = -14.5V, +14.5V; V_{NO} or V_{NC} = +14.5V, -14.5V	+25°C	-1	0.01	1	nA
			T_{MIN} to T_{MAX}	-10		10	
COM On-Leakage Current (Note 4)	$I_{COM(ON)}$	V_{COM} = +14.5V, -14.5V; V_{NO} or V_{NC} = +14.5V, -14.5V, or floating	+25°C	-2	0.02	2	nA
			T_{MIN} to T_{MAX}	-20		20	
DYNAMIC CHARACTERISTICS							
Transition Time	t_{TRANS}	V_{NO} or V_{NC} = 10V; R_L = 300Ω, C_L = 35pF; Figure 3	+25°C		85	150	ns
			T_{MIN} to T_{MAX}			200	
Break-Before-Make Delay	t_{BBM}	V_{NO} or V_{NC} = 10V; R_L = 300Ω, C_L = 35pF, Figure 3	+25°C	10	20		ns
			T_{MIN} to T_{MAX}	5			

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF, Figure 4	+25°C		1.5		pC
-3dB Bandwidth	BW		+25°C		225		MHz
Off-Isolation (Note 5)	V_{ISO}	f = 1MHz, R_L = 50Ω, Figure 5	+25°C		-70		dB
Total Harmonic Distortion	THD	f = 20Hz to 20kHz, $V_{N\_}$ = 5Vp-p, R_L = 600Ω	+25°C		0.005		%
Crosstalk	V_{CROSS}	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	+25°C		-76		dB
NO or NC Off-Capacitance	$C_{NO(OFF)}$, $C_{NC(OFF)}$	f = 1MHz, Figure 7	+25°C		6		pF
COM On-Capacitance	$C_{COM(ON)}$	f = 1MHz, Figure 8	+25°C		25		pF
DIGITAL I/O							
Input Logic High	V_{IH}		T_{MIN} to T_{MAX}	2.4			V
Input Logic Low	V_{IL}		T_{MIN} to T_{MAX}			0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0.8V or 2.4V	T_{MIN} to T_{MAX}	-1		1	µA
POWER SUPPLY							
Power-Supply Range			T_{MIN} to T_{MAX}	±4.5		±20	V
Positive Supply Current	I+	V_{IN} = 0 or 5V, $V_{N\_}$ = 3V, I_{SWITCH} = 100mA, MAX4660; I_{SWITCH} = 50mA, MAX4659	+25°C		135	200	µA
			T_{MIN} to T_{MAX}			300	
Negative Supply Current	I-	V_{IN} = 0 or 5V, $V_{N\_}$ = 3V, I_{SWITCH} = 100mA, MAX4660; I_{SWITCH} = 50mA, MAX4659	+25°C		30	50	µA
			T_{MIN} to T_{MAX}			75	
Ground Current	I_{GND}	V_{IN} = 0 or 5V, $V_{N\_}$ = 3V, I_{SWITCH} = 100mA, MAX4660; I_{SWITCH} = 50mA, MAX4659	+25°C		100	175	µA
			T_{MIN} to T_{MAX}			225	

High-Current, 25Ω, SPDT, CMOS Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0, V_{IH} = 2.4V, V_{IL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 2, 6)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{IN}		T_{MIN} to T_{MAX}	0		V+	V
On-Resistance	R_{ON}	I_{COM} = 25mA; V_{NO} or V_{NC} = +10V	+25°C		38	50	Ω
			T_{MIN} to T_{MAX}			60	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{COM} = 25mA; V_{NO} or V_{NC} = ±10V	+25°C		0.4	2	Ω
			T_{MIN} to T_{MAX}			2.5	
On-Resistance Flatness (Note 3)	$R_{FLAT (ON)}$	I_{COM} = 25mA; V_{NO} or V_{NC} = +2V, +6V, +10V	+25°C		4	7	Ω
			T_{MIN} to T_{MAX}			9	
DYNAMIC CHARACTERISTICS							
Transition Time	t_{TRANS}	V_{NO} or V_{NC} = 10V; R_L = 300Ω; C_L = 35pF, Figure 2	+25°C		120	200	ns
			T_{MIN} to T_{MAX}			250	
Break-Before-Make Delay	t_{BBM}	V_{NO} or V_{NC} = 10V; R_L = 300 Ω; C_L = 35pF, Figure 2	+25°C	20	50		ns
			T_{MIN} to T_{MAX}	10			
Charge Injection	Q	V_{GEN} = 0, R_{GEN} = 0, C_L = 1nF, Figure 4	+25°C		1		pC
POWER SUPPLY							
Power-Supply Range	V+			+9		+40	V
Positive Supply Current	I+	V_{IN} = 0 or 12V, $V_{N\_}$ = 3V; I_{SWITCH} = 50mA, MAX4660; I_{SWITCH} = 25mA, MAX4659	+25°C		50	100	µA
			T_{MIN} to T_{MAX}			125	
		V_{IN} = 5V, $V_{N\_}$ = 3V; I_{SWITCH} = 50mA, MAX4660; I_{SWITCH} = 25mA, MAX4659	+25°C		70	125	
			T_{MIN} to T_{MAX}			150	

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.

Note 4: Leakage parameters are 100% tested at maximum-rated hot temperature and guaranteed by correlation at T_A = +25°C.

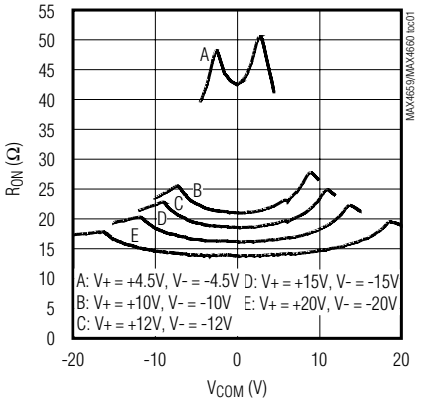
Note 5: Off-isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.

Note 6: -40°C specifications are guaranteed by design.

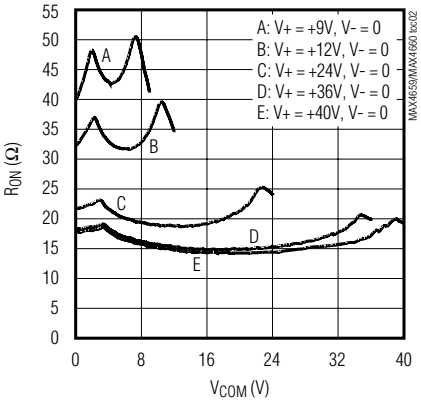
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

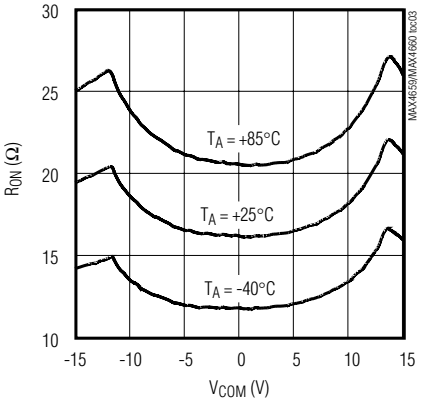
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



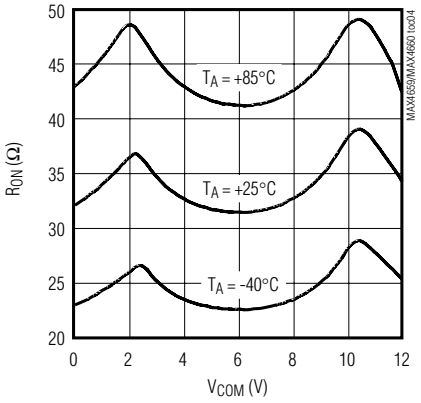
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



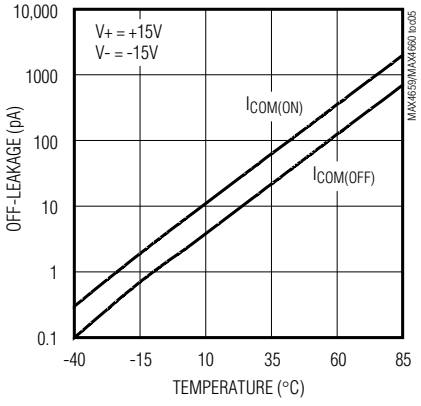
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



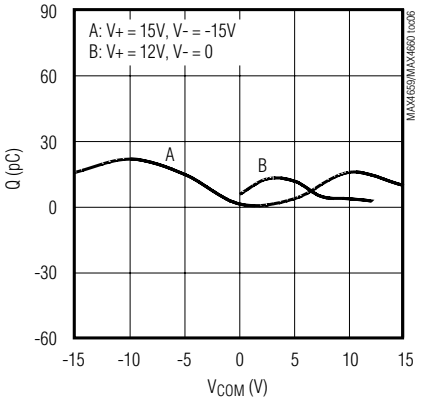
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



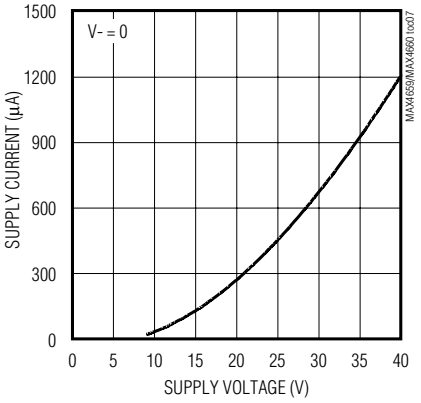
LEAKAGE CURRENT vs. TEMPERATURE



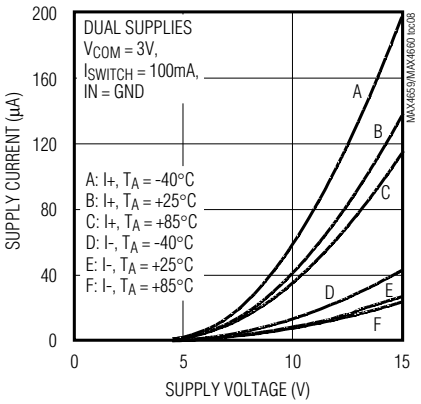
CHARGE INJECTION vs. V_{COM}



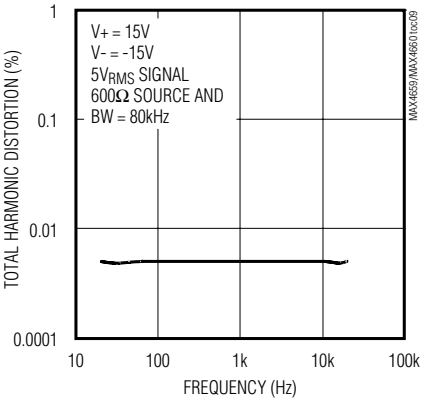
SUPPLY CURRENT vs. SUPPLY VOLTAGE (SINGLE SUPPLY)



SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



TOTAL HARMONIC DISTORTION vs. FREQUENCY

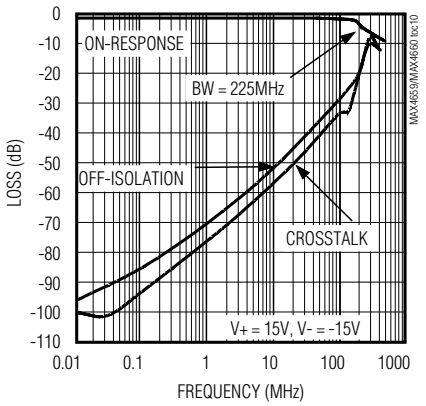


High-Current, 25Ω, SPDT, CMOS Analog Switches

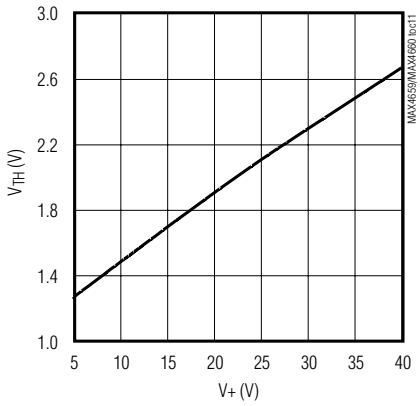
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

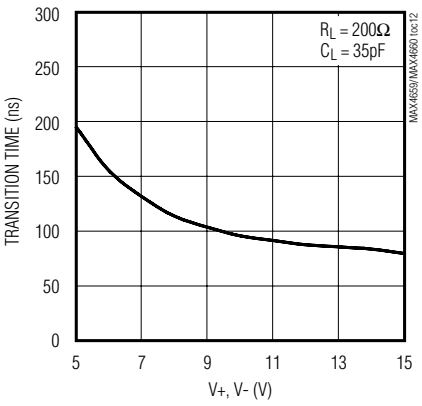
FREQUENCY RESPONSE



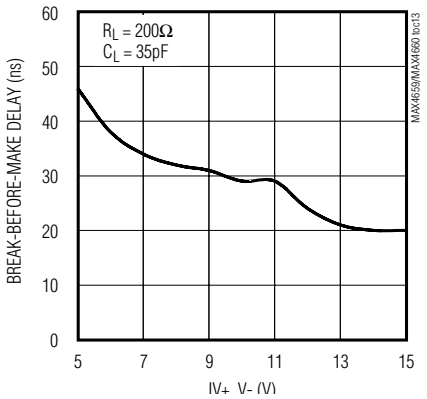
LOGIC LEVEL THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



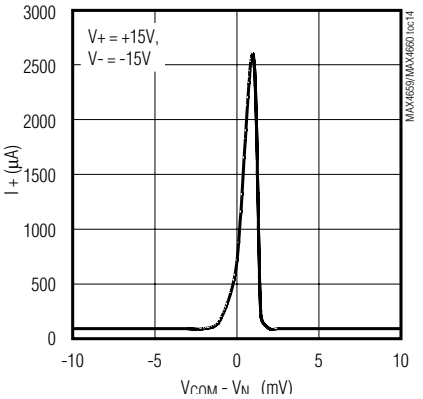
TRANSISTION TIME vs. SUPPLY VOLTAGE



BREAK-BEFORE-MAKE DELAY vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. VOLTAGE ACROSS SWITCH



Pin Description

PIN	NAME	FUNCTION
1	COM	Analog Switch Common
2	NC	Normally Closed Switch Terminal. NC is connected to COM when IN is low.
3	GND	Ground
4	V+	Positive Supply Voltage Input
5	N.C.	No Connection
6	IN	Digital Control Input
7	V-	Negative Supply Voltage Input
8	NO	Normally Open Switch Terminal. NO is connected to COM when IN is high.
—	EP	Exposed Paddle. Connect EP to V+ or leave unconnected.

Detailed Description

The MAX4659/MAX4660 are single, single-pole/double-throw (SPDT) CMOS analog switches. The CMOS switch construction provides rail-to-rail signal handling while consuming very little power. The switch is controlled by a TTL/CMOS level compatible digital input. The MAX4659/MAX4660 have a normally open switch and a normally closed switch.

These devices can be operated with either single power supplies or dual power supplies. Operation at up to ±20V supplies allows users a wide switching dynamic range. Additionally, asymmetrical operation is possible to tailor performance to a particular application.

These switches have been specifically designed to handle high switch currents, up to 200mA peak current and 150mA continuous currents. In order to do this, a new technique is used to drive the body of the output N-channel device. (Note: The basic switch between the input, NC/NO terminal and the output common terminal consists of an N-channel MOSFET and a P-channel MOSFET in parallel.) The standard method limits operation to approximately a 600mV drop across the switch. More than 600mV causes an increase in Id_{ON} leakage current (due to the turn-on of on-chip parasitic diodes), and an increase in V+ supply current. With this new sensing method, there is no limitation to the voltage drop across the switch. Current and voltage are limited only by the power dissipation rating of the package and the absolute maximum ratings of the switch.

When the analog input voltage drop is approximately 7mV there is an increase in power supply current from 90µA to 2mA (typ) within a 1mV to 7mV range, caused by the new sensing/driving circuitry.

Applications Information

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the devices. First, connect GND, followed by V+, V-, and the remaining pins. If power-supply sequencing is not possible, add two small-signal diodes (D1, D2) in series with supply pins (Figure 1). Adding diodes reduces the analog signal range to one diode drop below V+ and one diode drop above V-, but does not affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 44V. The protection diode for the negative supply is not required when V- is connected to GND.

Off-Isolation at High Frequencies

In 50Ω systems, the high-frequency on-response of these parts extends from DC to above 100MHz, with a typical loss of -2dB. When the switch is turned off, however, it behaves like a capacitor and off-isolation decreases with increasing frequency. This effect is more pronounced with higher source and load impedances. Above 5MHz, circuit board layout becomes critical. The graphs shown in the *Typical Operating Characteristics* were taken using a 50Ω source and load connected with BNC connectors.

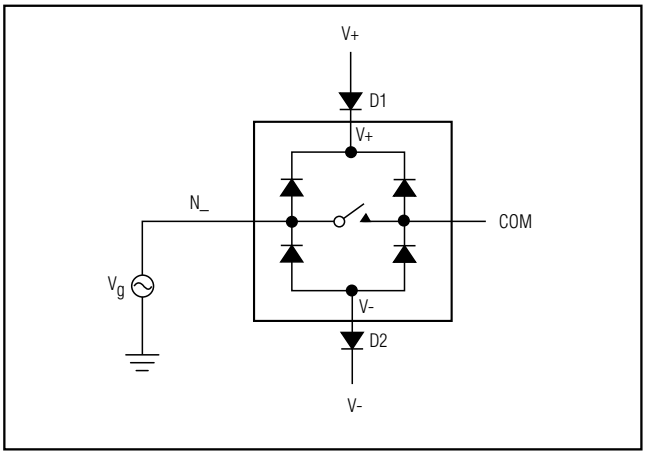


Figure 1. Overvoltage Protection Using Blocking Diodes

High-Current, 25Ω, SPDT, CMOS Analog Switches

Test Circuits/Timing Diagrams

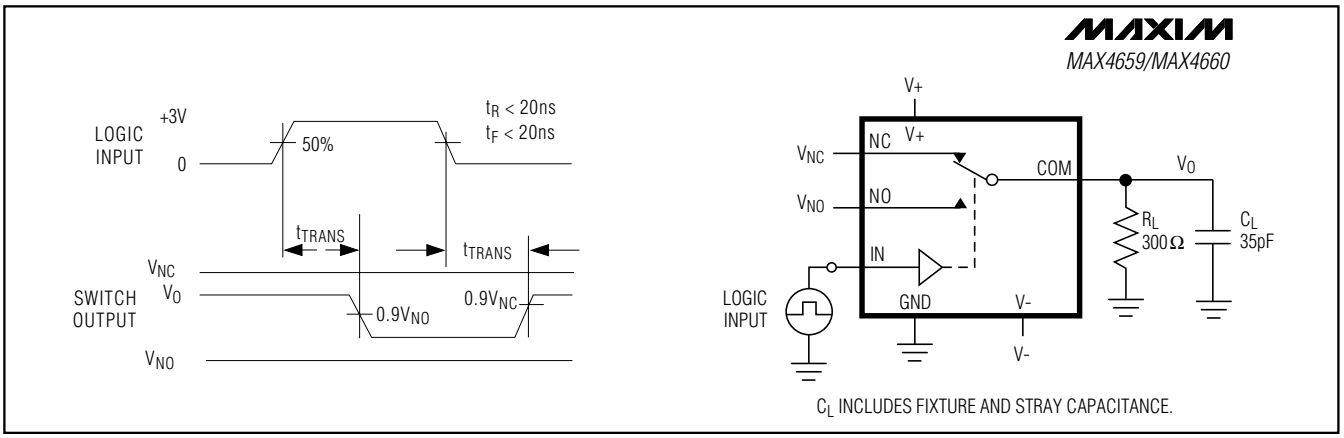


Figure 2. Functional Diagram

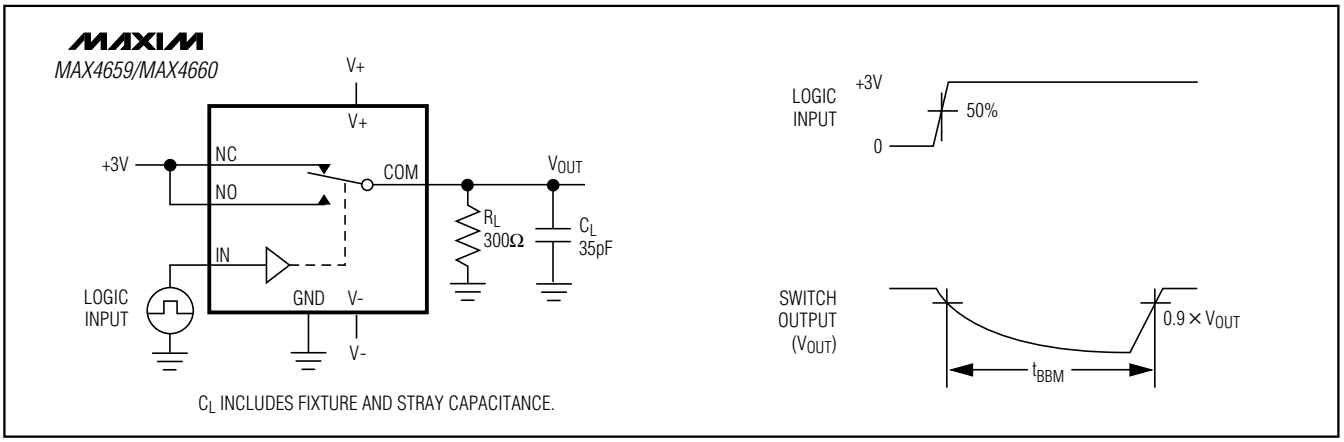


Figure 3. Break-Before-Make Time

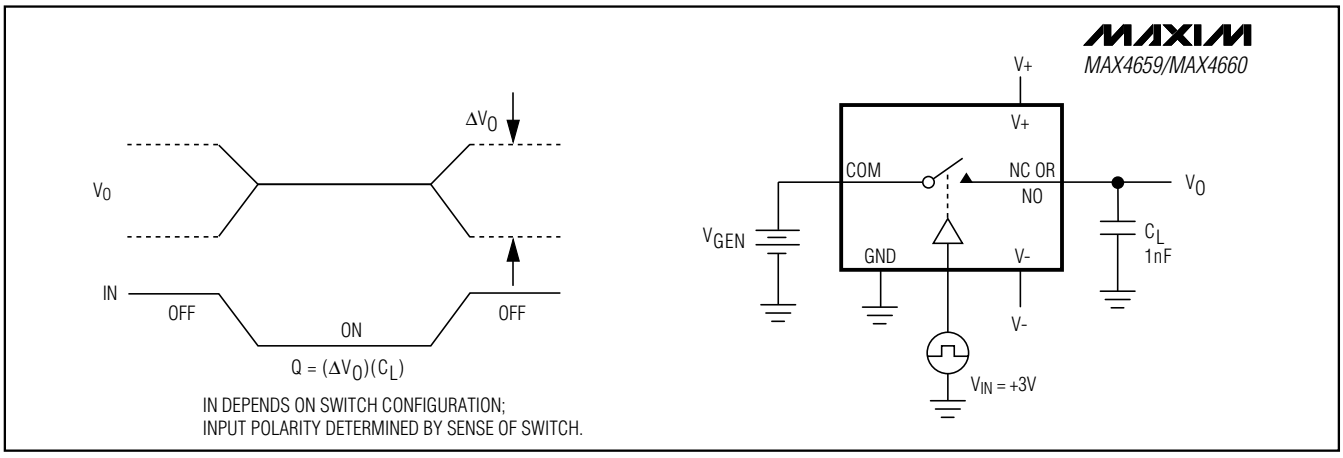


Figure 4. Charge Injection

Test Circuits/Timing Diagrams (continued)

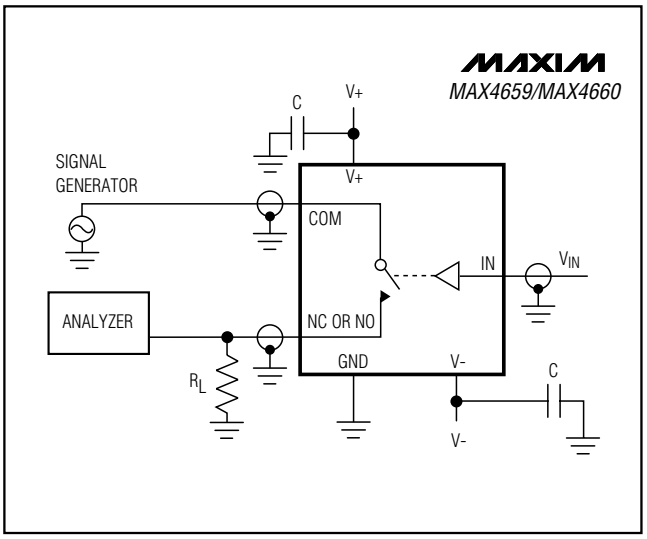


Figure 5. Off-Isolation

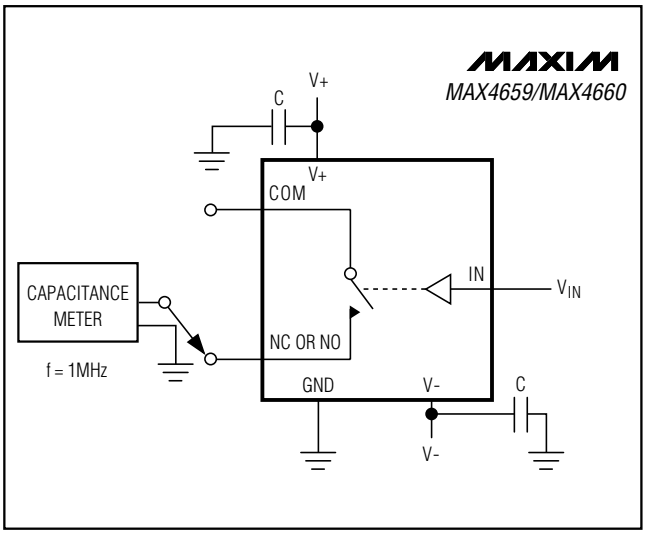


Figure 7. Channel Off-Capacitance

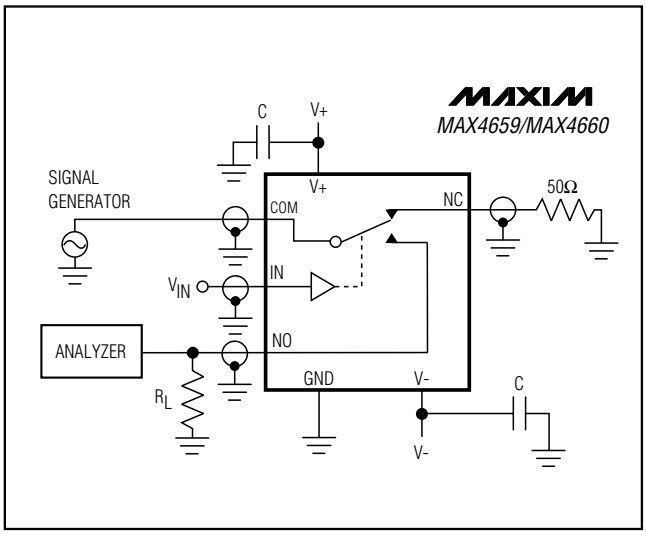


Figure 6. Crosstalk

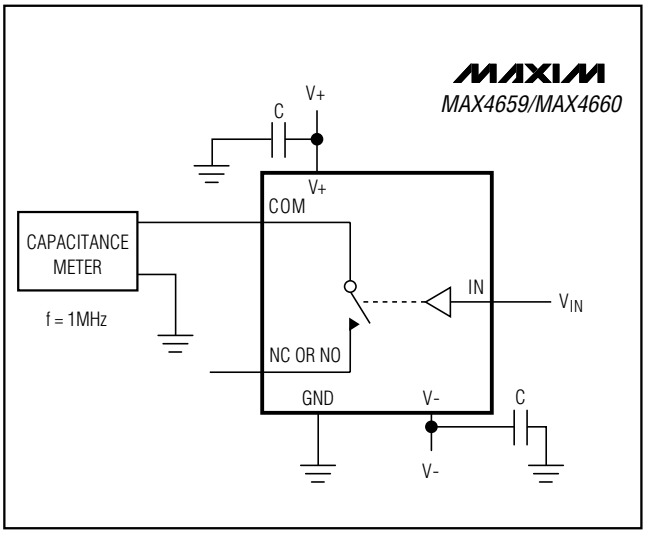


Figure 8. Channel On-Capacitance

Chip Information

TRANSISTOR COUNT: 45

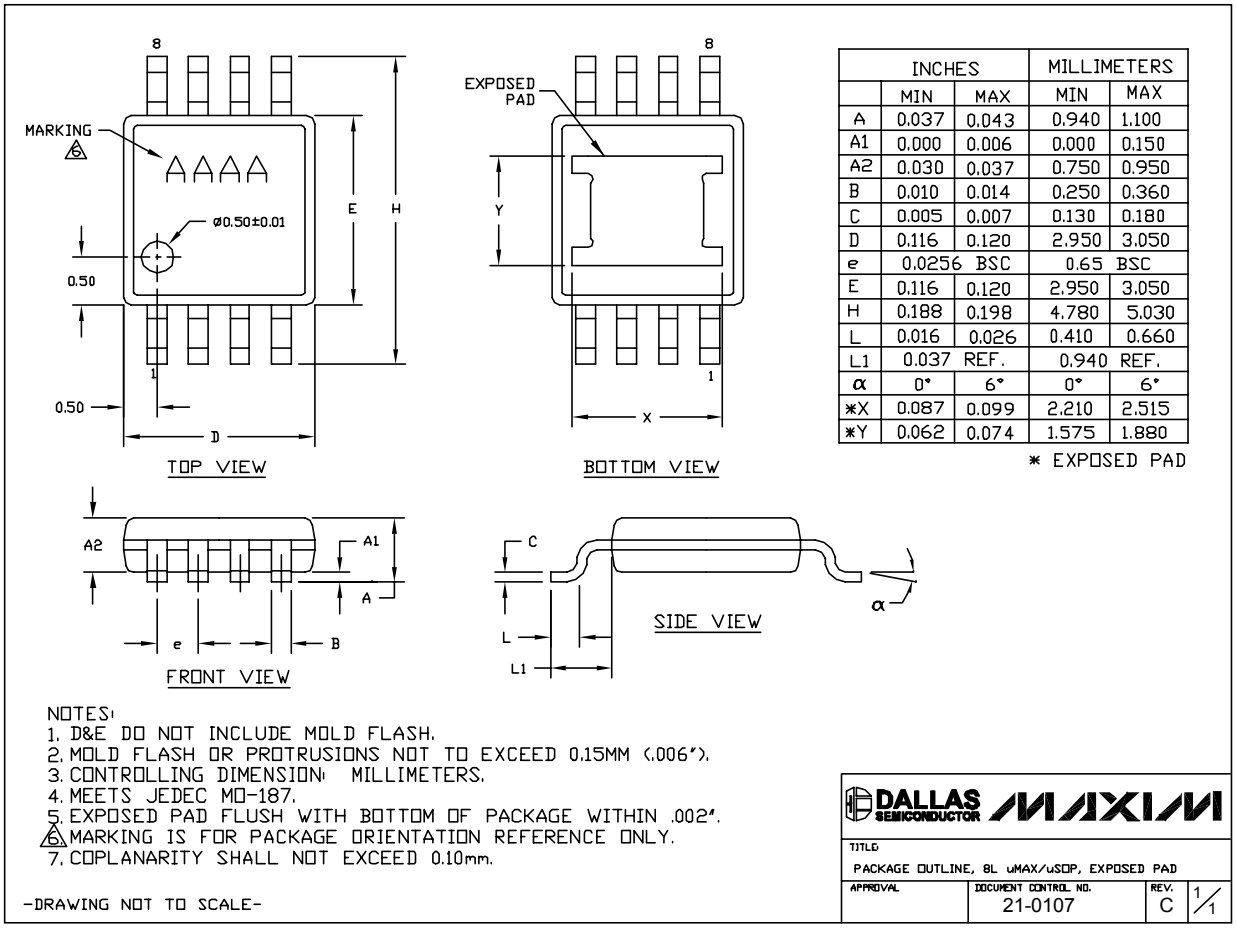
PROCESS: CMOS

High-Current, 25Ω, SPDT, CMOS Analog Switches

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

8L, µMAX, EXP PAD.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.037	0.043	0.940	1.100
A1	0.000	0.006	0.000	0.150
A2	0.030	0.037	0.750	0.950
B	0.010	0.014	0.250	0.360
C	0.005	0.007	0.130	0.180
D	0.116	0.120	2.950	3.050
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.950	3.050
H	0.188	0.198	4.780	5.030
L	0.016	0.026	0.410	0.660
L1	0.037 REF.		0.940 REF.	
α	0°	6°	0°	6°
*X	0.087	0.099	2.210	2.515
*Y	0.062	0.074	1.575	1.880

* EXPOSED PAD

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187.
5. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. COPLANARITY SHALL NOT EXCEED 0.10mm.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 8L uMAX/uSOP, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0107	C	1/1

Package Information (continued)

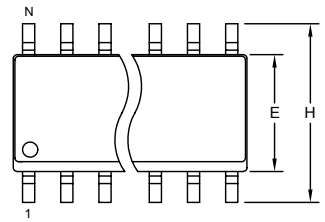
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

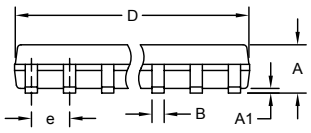
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

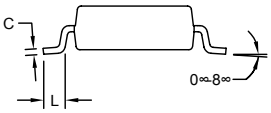
	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

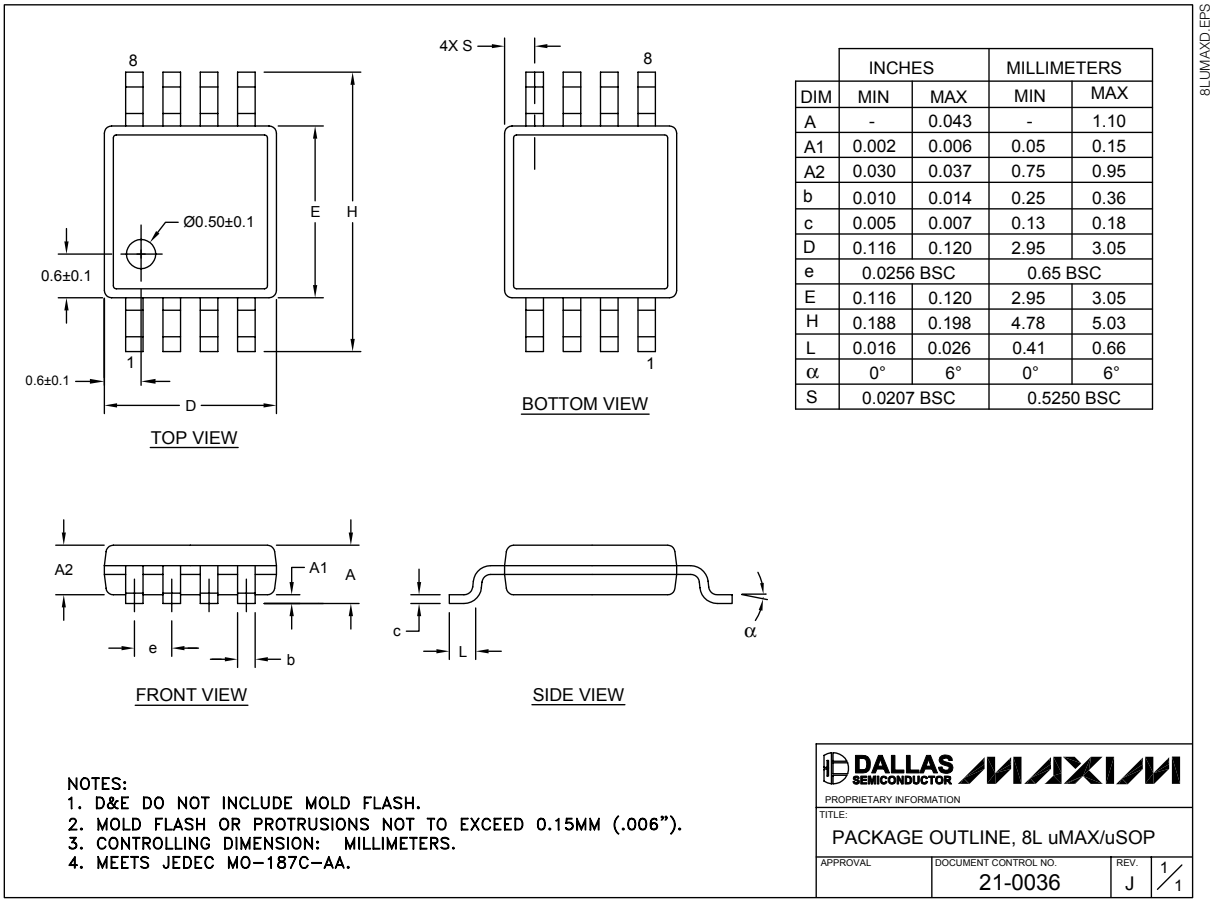
TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

High-Current, 25Ω, SPDT, CMOS Analog Switches

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256 BSC		0.65 BSC	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

Revision History

Pages changed at Rev 1: 1, 6, 12

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