4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN0–AIN3, A0, REF to GND .....-0.3V to (V_{DD} + 0.3V)
SDA, SCL, $\overline{INT}$ to GND .....-0.3V to +6V
Maximum Current Into Any Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 8.6mW/°C above +70°C) 689.7mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 2.7V to 3.6V (MAX1361), V_{DD} = 4.5V to 5.5V (MAX1362), V_{REF} = 2.048V (MAX1361), V_{REF} = 4.096V (MAX1362), C_{REF} = 0.1µF, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (f_{SAMPLE} = 94.4ksps) (Note 1)						
Resolution			10			Bits
Relative Accuracy	INL	(Note 2)			±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error					±1	LSB
Offset-Error Temperature Coefficient		Relative to FSR		0.3		ppm/°C
Gain Error		(Note 3)			±1	LSB
Gain Temperature Coefficient		Relative to FSR		0.3		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB
DYNAMIC PERFORMANCE ($f_{IN(SINE-WAVE)}$ = 10kHz, $V_{IN(P-P)}$ = V_{REF}, f_{SAMPLE} = 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			60		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Full-Power Bandwidth		SINAD > 57dB		3.0		MHz
Full-Linear Bandwidth		-3dB point		5.0		MHz
CONVERSION RATE						
Conversion Time (Note 4)	t_{CONV}	Internal clock			6.8	µs
		External clock	10.6			
Throughput Rate (Note 5)	f_{SAMPLE}	Internal clock, SCAN[1:0] = 01		53		ksps
		External clock			94.4	
		Monitor mode, SCAN[1:0] = 10			150	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1361), V_{DD} = 4.5V to 5.5V (MAX1362), V_{REF} = 2.048V (MAX1361), V_{REF} = 4.096V (MAX1362), C_{REF} = 0.1µF, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time				800			ns
Internal Clock Frequency					2.8		MHz
Aperture Delay (Note 6)	t_{AD}	External clock, fast mode			60		ns
		External clock, high-speed mode			30		
ANALOG INPUT (AIN0–AIN3)							
Input Voltage Range, Single-Ended and Differential (Note 7)		Unipolar		0		V_{REF}	V
		Bipolar		$-V_{REF}/2$		$+V_{REF}/2$	
Input Multiplexer Leakage Current		ON/OFF leakage current, $V_{AIN\_}$ = 0V or V_{DD}			±0.01	±1	µA
Input Capacitance	C_{IN}				22		pF
INTERNAL REFERENCE (Note 8)							
Reference Voltage	V_{REF}	T_A = +25°C	MAX1361	2.027	2.048	2.068	V
			MAX1362	4.055	4.096	4.137	
Reference-Voltage Temperature Coefficient	TCV_{REF}				25		ppm/°C
REF Short-Circuit Current						2	mA
REF Source Impedance					1.5		kΩ
EXTERNAL REFERENCE							
REF Input Voltage Range	V_{REF}	(Note 9)		1		V_{DD}	V
REF Input Current	I_{REF}	f_{SAMPLE} = 94.4ksps				40	µA
DIGITAL INPUTS/OUTPUTS (SCL, SDA, A_0)							
Input High Voltage	V_{IH}			0.7 x V_{DD}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD}	V
Input Hysteresis	V_{HYST}	SCL, SDA		0.1 x V_{DD}			V
		Ao			0.1 x V_{DD}		
Input Current	I_{IN}					±10	µA
Input Capacitance	C_{IN}				15		pF
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
$\overline{INT}$ OUTPUT							
Output Low Voltage		I_{SINK} = 3mA				0.4	V
$\overline{INT}$ Leakage Current		No faults detected				±10	µA
Output Capacitance					15		pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX1361		2.7		3.6	V
		MAX1362		4.5		5.5	

4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1361), V_{DD} = 4.5V to 5.5V (MAX1362), V_{REF} = 2.048V (MAX1361), V_{REF} = 4.096V (MAX1362), C_{REF} = 0.1µF, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	MAX1361	f_{SAMPLE} = 150ksps, monitor mode (Note 10)	Internal reference		660	1600	µA
				External reference		436	1350	
			f_{SAMPLE} = 94.4ksps, external clock	Internal reference		900	1150	
				External reference		670	900	
			f_{SAMPLE} = 40ksps, internal clock	Internal reference		530		
				External reference		230		
			f_{SAMPLE} = 10ksps, internal clock	Internal reference		380		
				External reference		60		
			f_{SAMPLE} = 1ksps, internal clock	Internal reference		330		
				External reference		6		
		MAX1362	f_{SAMPLE} = 150ksps, monitor mode (Note10)	Internal reference		666	1600	
				External reference		436	1350	
			f_{SAMPLE} = 94.4ksps, external clock	Internal reference		900	1150	
				External reference		670	900	
			f_{SAMPLE} = 40ksps, internal clock	Internal reference		530		
				External reference		230		
			f_{SAMPLE} = 10ksps, internal clock	Internal reference		380		
				External reference		60		
			f_{SAMPLE} = 1ksps, internal clock	Internal reference		330		
				External reference		6		
Shutdown Current		Internal reference on				330		µA
		Internal reference off				0.5	10	
Power-Supply Rejection Ratio	PSRR	Full-scale input (Note 11)				±0.01	±0.5	LSB/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1361), V_{DD} = 4.5V to 5.5V (MAX1362), V_{REF} = 2.048V (MAX1361), V_{REF} = 4.096V (MAX1362), C_{REF} = 0.1µF, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS FOR FAST MODE (Figures 1a, 2)						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP (P) and a START (S) Condition	t_{BUF}		1.3			µs
Hold Time for START (S) Condition	$t_{HD, STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$		0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	0		300	ns
Fall Time of SDA Transmitting	t_F	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	0		300	ns
Setup Time for STOP (P) Condition	$t_{SU, STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed					50	ns
TIMING CHARACTERISTICS FOR HIGH-SPEED MODE (C_B = 400pF, Figures 1a, 2) (Note 12)						
Serial-Clock Frequency	f_{SCLH}	(Note 13)			1.7	MHz
Hold Time, Repeated START Condition (Sr)	$t_{HD, STA}$		160			ns
Low Period of the SCL Clock	t_{LOW}	(Note 13)	320			ns
High Period of the SCL Clock	t_{HIGH}		120			ns
Setup Time for a Repeated START Condition (Sr)	$t_{SU, STA}$		160			ns
Data Hold Time	$t_{HD, DAT}$	(Note 14)	0		150	ns
Data Setup Time	$t_{SU, DAT}$		10			ns
Rise Time of SCL Signal	t_{RCL}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		80	ns
Rise Time of SCL Signal After Acknowledge Bit	t_{RCL1}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		160	ns
Fall Time of SCL Signal	t_{FCL}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		80	ns
Rise Time of SDA Signal	t_{RDA}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		160	ns
Fall Time of SDA Signal	t_{FDA}	Measured from $0.3V_{DD}$ to $0.7V_{DD}$	20		160	ns
Setup Time for STOP (P) Condition	$t_{SU, STO}$		160			ns
Capacitive Load for Each Bus	C_B				400	pF
Pulse Width of Spike Suppressed			0		10	ns

4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 2.7V to 3.6V (MAX1361), V_{DD} = 4.5V to 5.5V (MAX1362), V_{REF} = 2.048V (MAX1361), V_{REF} = 4.096V (MAX1362), C_{REF} = 0.1µF, f_{SCL} = 1.7MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Note 1: Devices configured for unipolar single-ended inputs.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the gain and offset have been calibrated.

Note 3: Offset nulled.

Note 4: Conversion time is defined as the number of clock cycles needed for conversion multiplied by the clock period. Conversion time does not include acquisition time. SCL is the conversion clock in the external clock mode.

Note 5: The throughput rate of the I^2C bus is limited to 94.4ksps. The MAX1361/MAX1362 can perform conversions up to 150ksps in monitor mode when not reading back results on the I^2C bus.

Note 6: A filter on the SDA and SCL inputs suppresses noise spikes and delays the sampling instant.

Note 7: The absolute input voltage range for the analog inputs (AIN0–AIN3) is from GND to V_{DD}.

Note 8: When the internal reference is configured to be available at AIN3/REF (SEL[2:1] = 11), decouple AIN3/REF to GND with a 0.01µF capacitor.

Note 9: ADC performance is limited by the converter's noise floor, typically 300µV_{P-P}.

Note 10: Maximum conversion throughput in internal clock mode when the data is not clocked out.

Note 11: For the MAX1361, PSRR is measured as

$$\frac{\left[\left[V_{FS}(3.6V) - V_{FS}(2.7V)\right] \times \frac{2^N - 1}{V_{REF}}\right]}{(3.6V - 2.7V)}$$

and for the MAX1362, PSRR is measured as

$$\frac{\left[\left[V_{FS}(5.5V) - V_{FS}(4.5V)\right] \times \frac{2^N - 1}{V_{REF}}\right]}{(5.5V - 4.5V)}$$

Note 12: C_B = total capacitance of one bus line in pF.

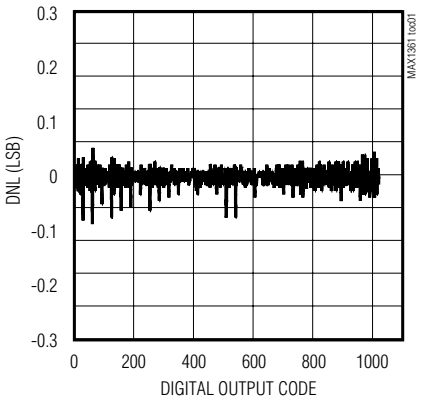
Note 13: f_{SCLH} must meet the minimum clock low time plus the rise/fall times.

Note 14: A master device must provide a data hold time for SDA (referred to V_{IL} of SCL) to bridge the undefined region of SCL's falling edge.

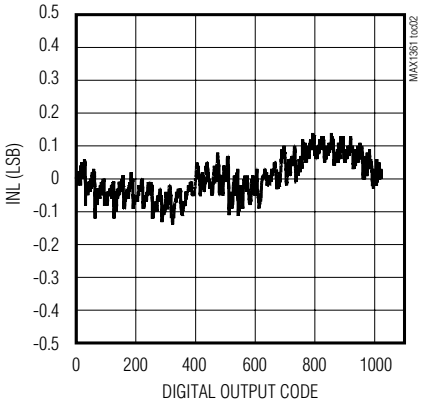
Typical Operating Characteristics

(V_{DD} = 3.3V (MAX1361), V_{DD} = 5V (MAX1362), f_{SCL} = 1.7MHz, external clock, f_{SAMPLE} = 94.4ksps, single-ended, unipolar, T_A = +25°C, unless otherwise noted.)

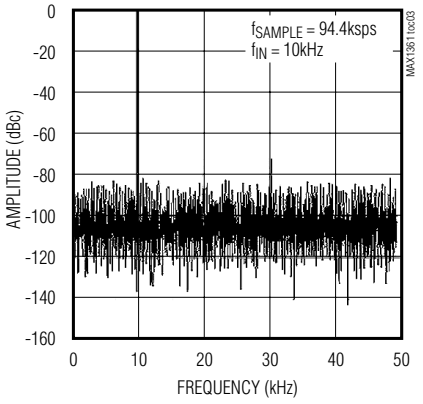
DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



INTEGRAL NONLINEARITY vs. DIGITAL CODE



FFT PLOT

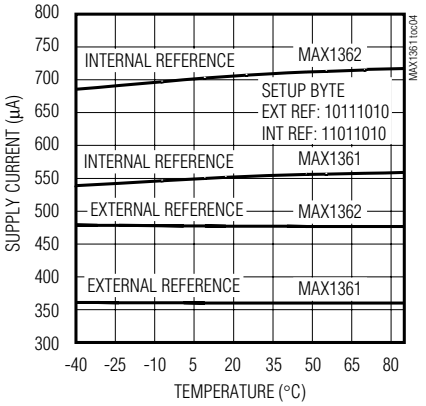


4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

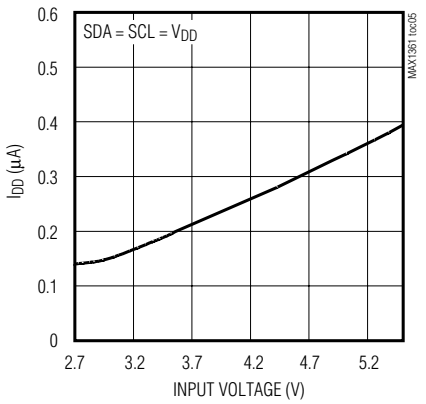
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V (MAX1361), V_{DD} = 5V (MAX1362), f_{SCL} = 1.7MHz, external clock, f_{SAMPLE} = 94.4ksps, single-ended, unipolar, T_A = +25°C, unless otherwise noted.)

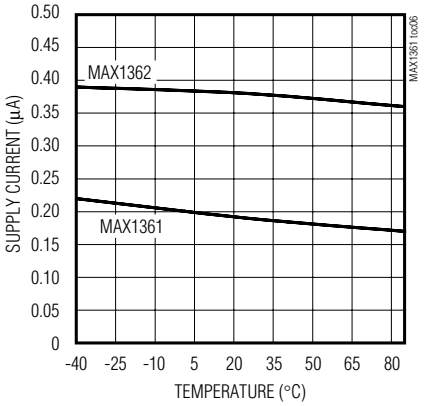
SUPPLY CURRENT vs. TEMPERATURE



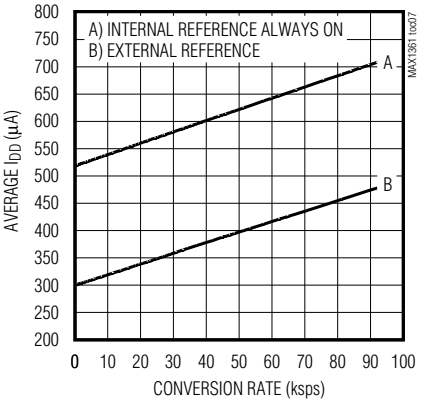
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



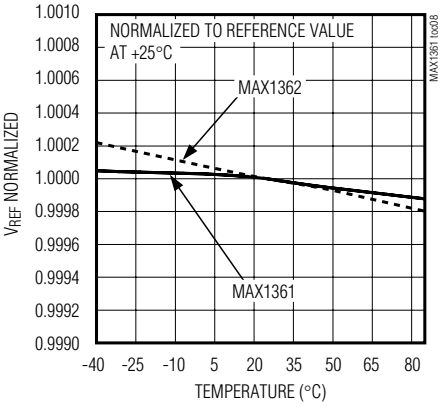
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



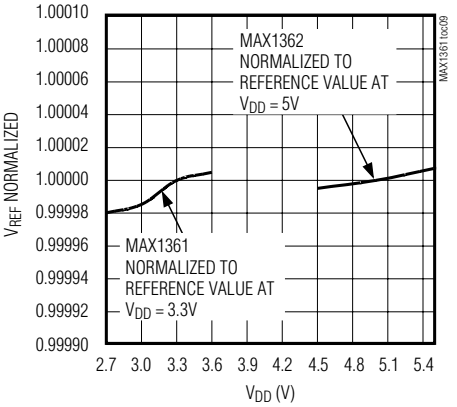
AVERAGE SUPPLY CURRENT vs. CONVERSION RATE (EXTERNAL CLOCK)



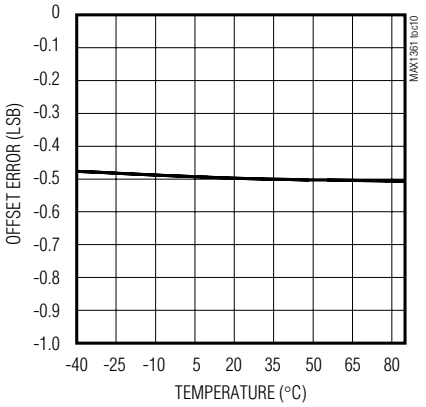
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



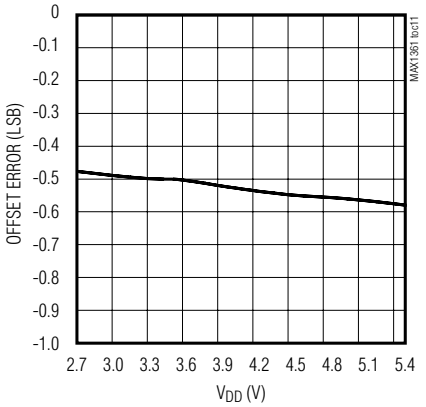
NORMALIZED REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



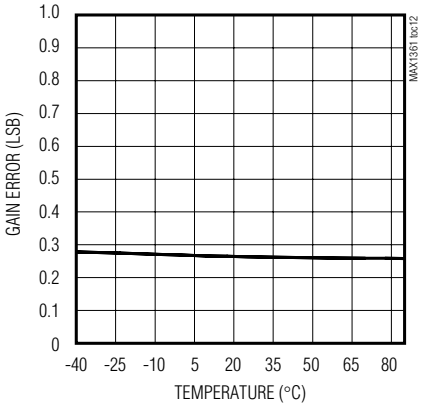
OFFSET ERROR vs. TEMPERATURE



OFFSET ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE

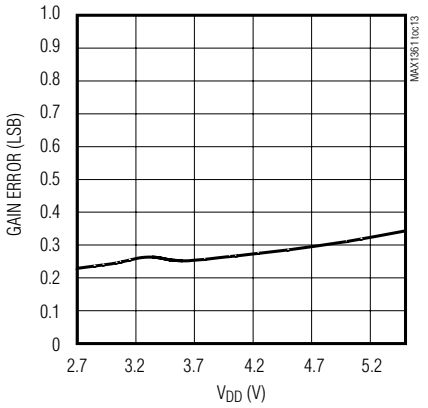


4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

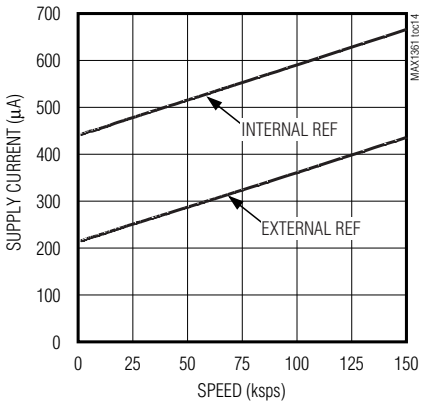
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V (MAX1361), V_{DD} = 5V (MAX1362), f_{SCL} = 1.7MHz, external clock, f_{SAMPLE} = 94.4ksps, single-ended, unipolar, T_A = +25°C, unless otherwise noted.)

GAIN ERROR vs. SUPPLY VOLTAGE



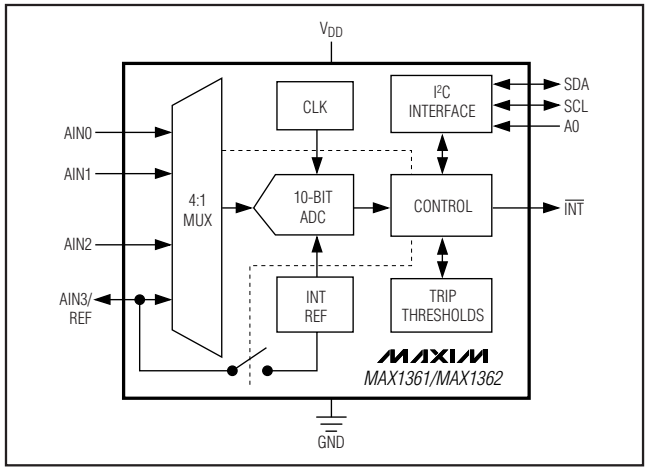
MONITOR-MODE SUPPLY CURRENT vs. SPEED



Pin Description

PIN	NAME	FUNCTION
1	AIN0	Analog Input
2	AIN1	Analog Input
3	AIN2	Analog Input
4	AIN3/V_{REF}	Analog Input or Reference Input or Output. See Table 3.
5	A0	I^2C Address Select Input. Connect to V_{DD} or GND. See Table 1.
6	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output
7	SCL	I^2C Clock Input
8	SDA	I^2C Data Input/Output
9	GND	Ground
10	V_{DD}	Positive Supply Voltage. Bypass V_{DD} to GND with a 0.1µF capacitor.

Functional Diagram



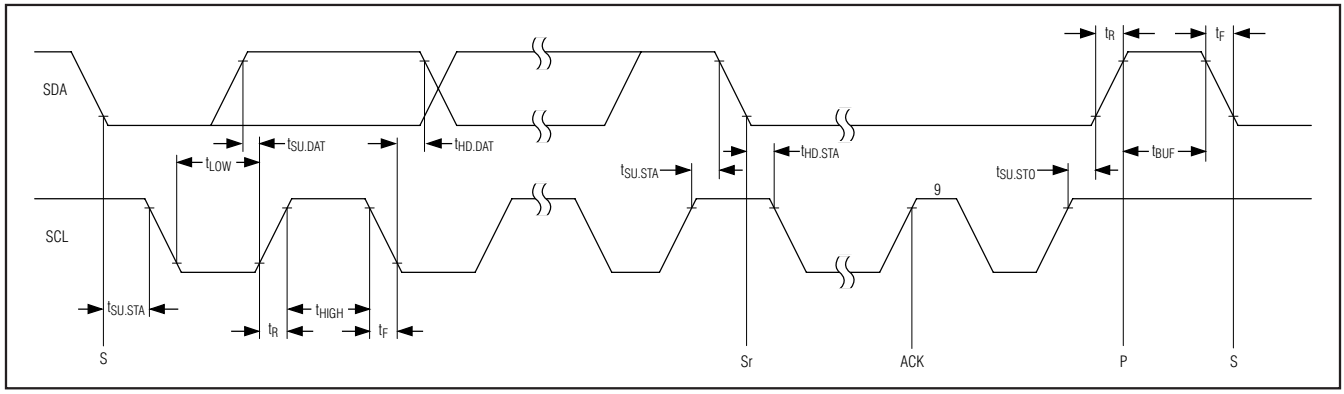


Figure 1a. F/S-Mode 2-Wire Serial-Interface Timing

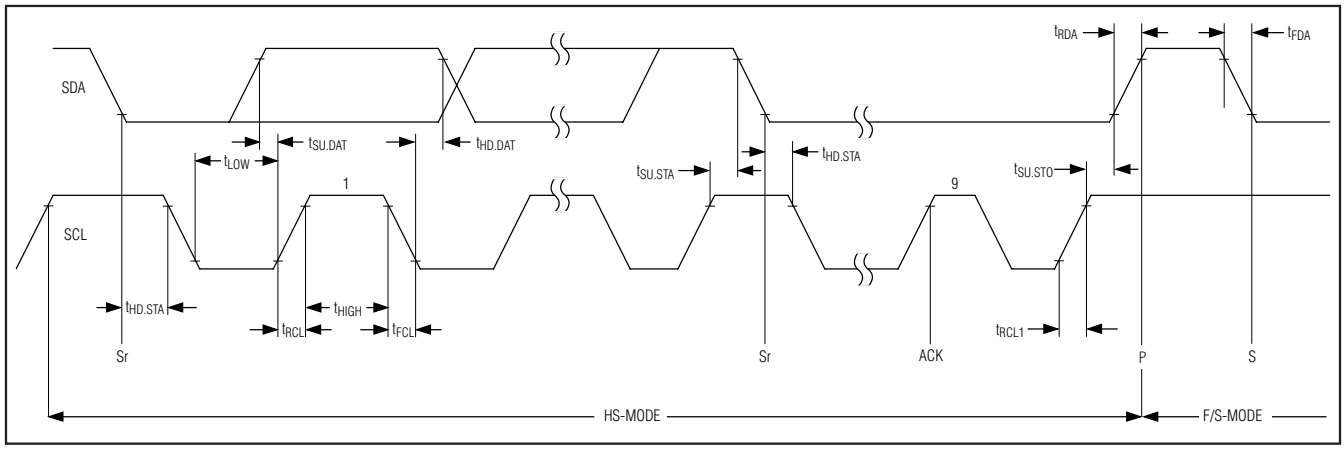


Figure 1b. HS-Mode 2-Wire Serial-Interface Timing

Detailed Description

The MAX1361/MAX1362 4-channel ADCs use successive-approximation conversion techniques and fully differential input track/hold (T/H) circuitry to capture and convert analog signals to a serial 10-bit digital output. The MAX1361/MAX1362 feature a monitor mode with programmable trip thresholds and window comparator. The monitor function asserts an interrupt when any channel violates the programmed upper or lower thresholds. SMBus alert response allows the host microcontroller (µC) to quickly identify which device caused the interrupt. A programmable delay between monitoring intervals lowers power consumption at lower monitor rates.

The MAX1361/MAX1362 integrate an internal voltage reference and clock. The software configures the analog inputs for unipolar/bipolar and single-ended/fully differential operation. Integrated first-in/first-out (FIFO) allows conversion of all channels, or eight conversions on a selected channel to reduce interface overhead. An I^2C-compatible serial interface complies with standard, fast, and high-speed (1.7MHz) modes.

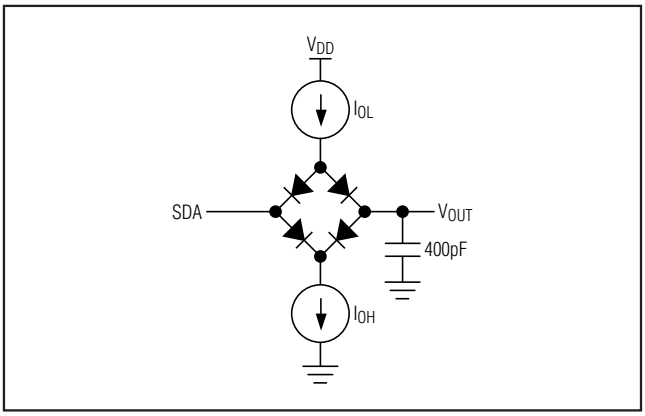


Figure 2. Load Circuits

4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

Power Supply

The MAX1361 (2.7V to 3.6V) and MAX1362 (4.5V to 5.5V) operate from a single supply and consume 670µA (typ) at sampling rates up to 94.4ksps and 436µA in monitor mode at 150ksps. The MAX1361 features a 2.048V internal reference and the MAX1362 features a 4.096V internal reference. All devices can be configured for use with an external reference from 1V to V_{DD}. Bypass V_{DD} to GND using a 0.1µF or greater ceramic capacitor for best performance.

Analog Input and Track/Hold

The MAX1361/MAX1362 analog-input architecture contains an analog-input multiplexer (MUX), fully differential T/H, comparator, and a fully differential switched capacitive digital-to-analog converter (DAC). Figure 3 shows the equivalent input circuit for the MAX1361/MAX1362.

In single-ended mode, the analog-input MUX connects $C_{T/H}$ between the analog input selected by CS[3:0] and GND (see the *Configuration/Setup Bytes (Write Cycle)* section). In differential mode, the analog-input MUX connects $C_{T/H}$ to the plus and minus analog inputs selected by CS[3:0].

During the acquisition interval, the T/H switches are in the track position, and $C_{T/H}$ charges to the analog-input signal. At the end of the acquisition interval, the T/H switches move to the hold position, retaining the charge on $C_{T/H}$ as a stable sample of the input signal.

During the conversion, a switched capacitive DAC adjusts to restore the comparator input voltage to 0V within the limits of 10-bit resolution. This action requires 10 conversion clock cycles and is equivalent to transferring a charge of 11pF x (V_{IN+} - V_{IN-}) from $C_{T/H}$ to the binary-weighted capacitive DAC, forming a digital representation of the analog-input signal.

Use a low source impedance to ensure an accurate sample. A source impedance of up to 1.5kΩ does not significantly degrade sampling accuracy. For larger source impedances, connect a 100pF capacitor from the analog input to GND or buffer the input.

In internal clock mode, the T/H circuitry enters track mode on the eighth rising clock edge of the address byte (see the *Slave Address* section). The T/H circuitry enters hold mode on the falling clock edge of the acknowledge bit of the address byte (the ninth clock pulse). The conversions are then internally clocked, during which time the MAX1361/MAX1362 hold SCL low.

In external clock mode, the T/H circuitry enters track mode after a valid address on the rising edge of the clock during the read bit (R/$\overline{W}$ = 1, bit 8). Hold mode is entered on the rising edge of the second clock pulse during the shifting out of the 1st byte of the result. The next 10 clock cycles perform the conversions (see Figure 13).

The time required for the T/H circuitry to acquire an input signal is a function of the input sample capacitance. If the analog-input source impedance is high, the acquisition-time constant lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} \geq 7 \times (R_{SOURCE} + R_{IN}) \times C_{IN}$$

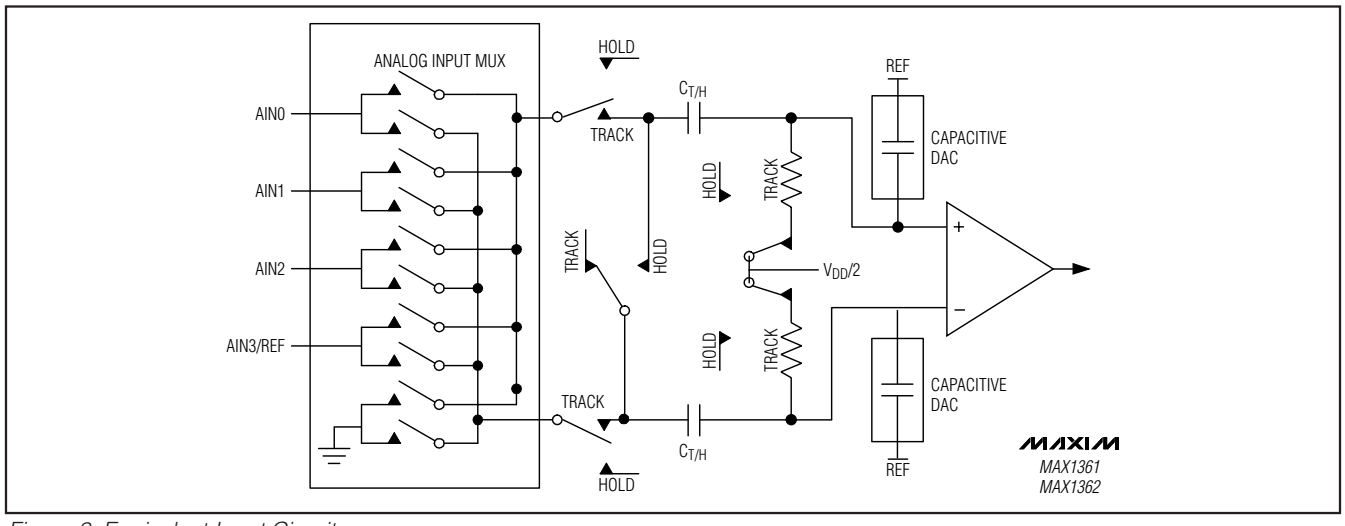


Figure 3. Equivalent Input Circuit

where R_{SOURCE} is the analog-input source impedance, R_{IN} = 2.5kΩ, and C_{IN} = 22pF. For internal clock mode, t_{ACQ} = 1.5/f_{SCL}, and for external clock mode t_{ACQ} = 2/f_{SCL}.

Analog-Input Bandwidth

The MAX1361/MAX1362 feature input-tracking circuitry with a 5MHz small-signal bandwidth. The 5MHz input bandwidth makes it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals from aliasing into the frequency band of interest, use anti-aliasing filtering.

Analog-Input Range and Protection

Internal protection diodes clamp the analog inputs to V_{DD} and GND. These diodes allow the analog inputs to swing from (V_{GND} - 0.3V) to (V_{DD} + 0.3V) without causing damage to the device. For accurate conversions the inputs must remain within 50mV below GND or above V_{DD}.

Single-Ended/Differential Input

The SE/$\overline{DIF}$ of the configuration byte configures the MAX1361/MAX1362 analog-input circuitry for single-ended or differential input. In single-ended mode (SE/$\overline{DIF}$ = 1), the digital conversion results are the difference between the analog input selected by CS[3:0] and GND. In differential mode (SE/$\overline{DIF}$ = 0), the digital conversion results are the difference between the plus and the minus analog inputs selected by CS[3:0] (see Tables 5 and 6).

Unipolar/Bipolar

Unipolar mode sets the differential input range from 0 to V_{REF}. A negative differential analog input in unipolar mode causes the digital output code to be zero. Selecting bipolar mode sets the differential input range to ±V_{REF}/2. The digital output code is binary in unipolar mode and two's complement in bipolar mode. (See the *Transfer Functions* section.)

In single-ended mode the MAX1361/MAX1362 always operate in unipolar mode. The analog inputs are internally referenced to GND with a full-scale input range from 0 to V_{REF} (Table 7).

Reference

SEL[1:0] of the setup byte controls the reference and the AIN3/REF configuration. When AIN3/REF is configured as a reference input or reference output (SEL0 = 1), differential conversions on AIN3/REF appear as if AIN3/REF is connected to GND. A single-ended conversion in scan mode on AIN3/REF is ignored by an internal limiter that sets the highest available channel at AIN2 (Table 2).

Internal Reference

The internal reference is 2.048V for the MAX1361 and 4.096V for the MAX1362. SEL0 of the setup byte controls whether AIN3/REF is used for an analog input or a reference (SEL0 = 0 selects AIN3/REF as AIN3, and SEL0 = 1 selects AIN3/REF as REF). Decouple AIN3/REF to GND with a 0.1µF capacitor and a 2kΩ resistor in series when AIN3/REF is configured as an internal reference output (SEL[1:0] = 11). See the *Typical Operating Circuit.* Once powered up, the reference remains on until reconfigured. Do not use the reference to supply current for external circuitry.

External Reference

The external reference ranges from 1V to V_{DD}. For maximum conversion accuracy, the reference must deliver 40µA and have an impedance of 500Ω or less. For noisy or high-output-impedance references, insert a 0.1µF bypass capacitor to GND as close to AIN3/REF as possible.

Clock Modes

The clock mode determines the conversion clock and the data acquisition and conversion time. The clock mode also affects the scan mode. The state of the setup byte's $\overline{INT}$/EXT clock bit determines the clock mode. At power-up, the MAX1361/MAX1362 default to internal clock mode ($\overline{INT}$/EXT clock = 0).

Internal Clock

See the *Configuration/Setup Bytes (Write Cycle)* section. In internal clock mode ($\overline{INT}$/EXT clock = 0), the MAX1361/MAX1362 use an internal oscillator for the conversion clock. The MAX1361/MAX1362 begin tracking the analog input after a valid address on the eighth rising edge of the clock. On the falling edge of the ninth clock, the analog signal is acquired and the conversion begins. While converting, the MAX1361/MAX1362 hold SCL low (clock stretching). After completing the conversion, the results are stored in internal memory. For scan-mode configurations with multiple conversions (see the *Scan Modes* section), all conversions happen in succession with each additional result stored in memory. Once all conversions are complete, the MAX1361/MAX1362 release SCL, allowing it to go high. The master can now clock the results out in the same order as the scan conversion.

The converted results are read back in a FIFO sequence. If AIN3/REF is configured as a reference input or output, AIN3/REF is excluded from multichannel scan. If reading continues past the final result stored in memory, the pointer wraps around and points to the first result. Only the current conversion results are read from memory. The MAX1361/MAX1362 must

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be addressed with a read command to obtain new conversion results.

External Clock

See the *Configuration/Setup Bytes (Write Cycle)* section. When configured for external clock mode ($\overline{INT}$/EXT = 1), the MAX1361/MAX1362 use SCL as the conversion clock. In external clock mode, the MAX1361/MAX1362 begin tracking the analog input on the eighth rising clock edge of a valid slave address byte. Two SCL clock cycles later, the analog signal is acquired and the conversion begins. Unlike internal clock mode, converted data is clocked out immediately in the format described in the *Reading a Conversion (Read Cycle)* section.

The device continuously converts input channels dictated by the scan mode until given a not acknowledge (NACK). There is no need to readdress the device with a read command to obtain new conversion results.

The conversion must complete in 1ms or droop on the T/H capacitor degrades conversion results. Use internal clock mode if the SCL clock period exceeds 60µs.

Use external clock mode for conversion rates from 40ksps to 94.4ksps. Use internal clock mode for conversions under 40ksps. Internal clock mode consumes less power. Monitor mode always uses internal clock mode regardless of conversion rate.

Applications Section

Power-On Reset

The configuration and setup registers default to a single-ended, unipolar, single-channel conversion on AIN0 using the internal clock with V_{DD} as the reference and AIN3/REF configured as an analog input. The memory contents are unknown at power-up (see the *Software Description* section).

I²C-Compatible 2-Wire Serial Interface

The MAX1361/MAX1362 use an I²C-compatible 2-wire interface consisting of a serial-data line (SDA) and serial-clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX1361/MAX1362 and the master at rates up to 1.7MHz. The master (typically a microcontroller) initiates data transfer on the bus and generates the SCL signal to permit data transfer. The MAX1361/MAX1362 behave as I²C slave devices that transfer and receive data.

SDA and SCL must be pulled high for proper I²C operation. This is typically done with pullup resistors (750Ω or greater). Series resistors (R_S) are optional (see the *Typical Operating Circuit* section). The resistors protect the input architecture of the MAX1361/MAX1362 from high voltage spikes on the bus lines and minimize crosstalk and undershoot of the bus signals.

One bit transfers during each SCL clock cycle. A minimum of nine clock cycles is required to transfer a byte in or out of the MAX1361/MAX1362 (8 bits and an ACK/NACK). The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *START and STOP Conditions* section). Both SDA and SCL remain high when the bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high (Figure 4). A repeated START condition (Sr) can be used in place of a STOP condition to leave the bus active and the mode unchanged (see the *HS I²C Mode* section).

Acknowledge and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX1361/MAX1362 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 5).

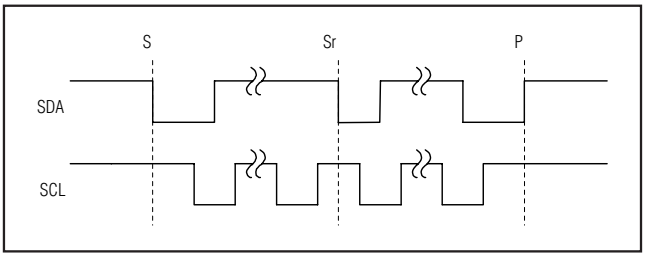

Figure 4. START and STOP Conditions

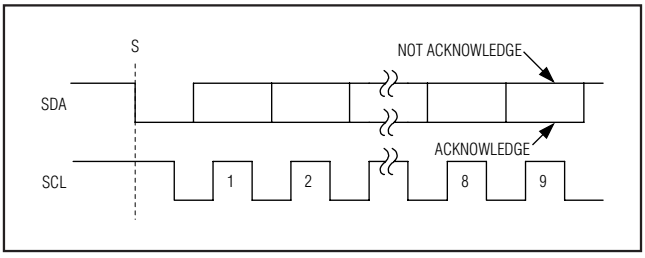

Figure 5. Acknowledge Bits

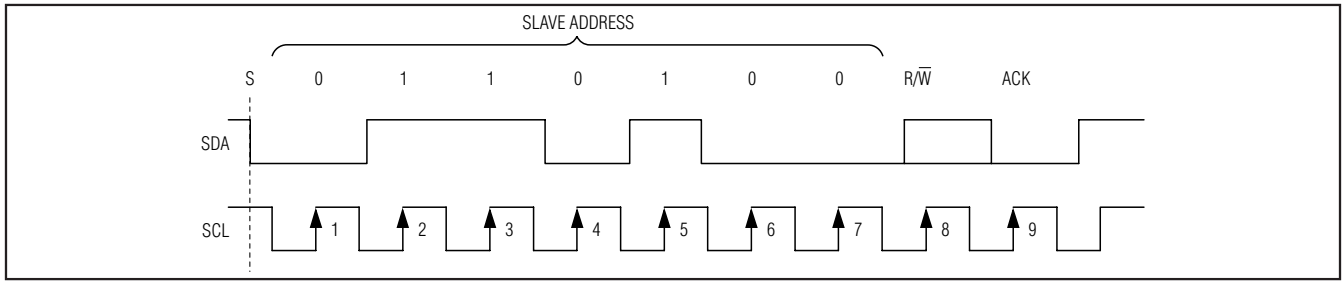

Figure 6. MAX1361/MAX1362 Slave Address Byte

Table 1. I²C Slave Selection Table

A0 STATE	SUFFIX	ADDRESS
Low	EUB	0110100
High	EUB	0110101
Low	MEUB	0110110
High	MEUB	0110111

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master reattempts communication at a later time.

Slave Address

The MAX1361/MAX1362 have a 7-bit I²C slave address. The slave address is selected using A0. The MAX1361/MAX1362 (EUB and MEUB) have 2 base address options, allowing up to 4 devices concurrently per I²C bus (see Table 1).

The MAX1361/MAX1362 continuously wait for a START condition followed by its slave address. When the device recognizes its slave address, it is ready to accept or send data depending on the R/$\overline{W}$ bit (Figure 6).

HS I²C Mode

At power-up, the MAX1361/MAX1362 bus timing is set for fast mode (F/S mode, up to 400kHz I²C clock), which limits the conversion rate to approximately 22ksps. Switch to high-speed mode (HS mode, up to 1.7MHz I²C clock) to achieve conversion rates up to 94.4ksps. The MAX1361/MAX1362 convert up to 150ksps in monitor mode, regardless of I²C mode. If conversion results are unread, I²C bandwidth limitations do not apply in monitor mode.

Select HS mode by addressing all devices on the bus with the HS-mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX1361/MAX1362 issue a NACK, allowing SDA to be pulled high for one clock cycle (Figure 7).

After the NACK, the MAX1361/MAX1362 operate in HS mode. Send a repeated START (Sr) followed by a slave address to initiate HS-mode communication. If the master generates a STOP condition the MAX1361/MAX1362 return to F/S mode. Use a repeated START condition (Sr) in place of a STOP condition to leave the bus active and the mode unchanged.

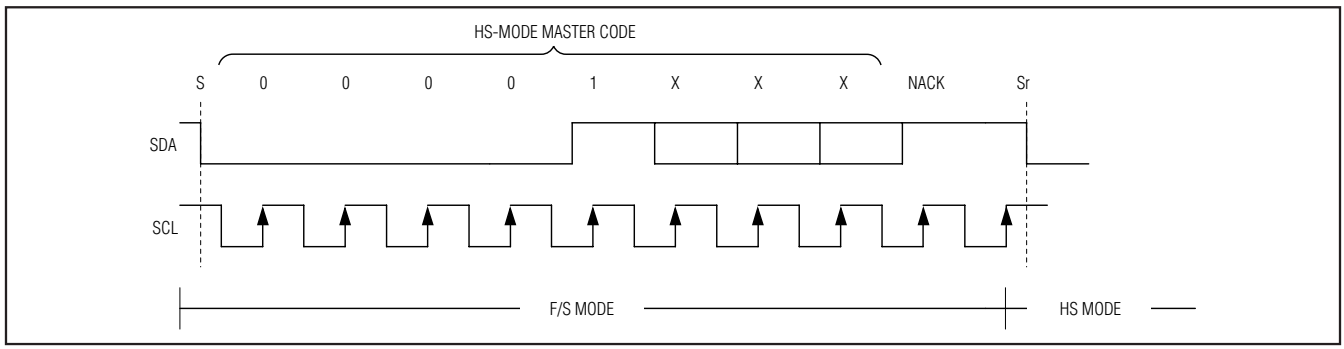

Figure 7. F/S-Mode to HS-Mode Transfer

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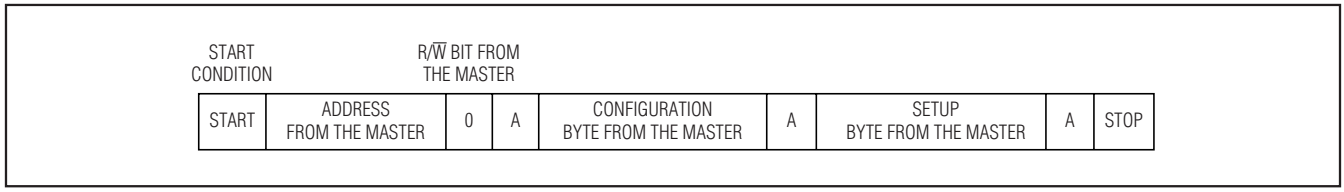

Figure 8. Example of Writing Setup and Control Bytes

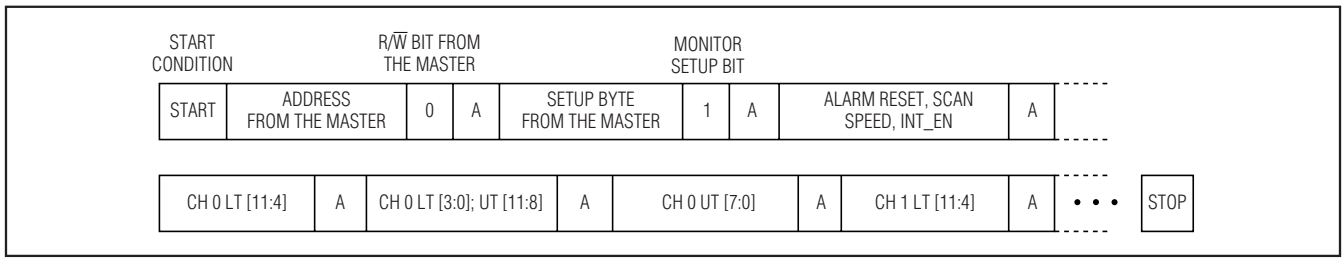

Figure 9. Example of Extended Setup-Byte Writing

Table 2. Configuration Byte Format*

BIT	NAME	DESCRIPTION
7(MSB)	CONFIG	The configuration byte always starts with 0.
6	SCAN1	SCAN1, SCAN0 = [0,0], scans from channel 0 to the upper channel chosen by CS1, CS0. SCAN1, SCAN0 = [0,1], converts a single channel chosen by CS1, CS0 eight times. SCAN1, SCAN0 = [1,0] monitor mode monitors from channel 0 to the upper channel chosen by CS1, CS0. SCAN1, SCAN0 = [1,1], single channel conversion for the channel is chosen by CS0, CS1.
5	SCAN0	
4	CS3	CS3, CS2 = [1,1] enables readback of monitor-mode setup data.
3	CS2	
2	CS1	Selects the upper limit of the channel range used for the conversion sequence in scan modes SCAN = [0,0] and monitor modes SCAN = [1,0]. Selects the conversion channel when SCAN = [0,1] or when SCAN = [1,1]. (Tables 5 and 6)
1	CS0	
0	SE/$\overline{DIF}$	1 = single-ended inputs. 0 = differential inputs. AIN0 and AIN1 form the first differential pair and AIN2 and AIN3 form the second differential pair. (See Tables 4 and 5.) Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referenced to GND. In differential mode, the voltage difference between two channels is measured. When single-ended mode is used, the MAX1361/MAX1362 perform unipolar conversions regardless of the $\overline{UNI}$/BIP bit in the setup byte. (Table 7)

**Power-on defaults: 0x01*

Software Description

Configuration/Setup Bytes (Write Cycle)

A write cycle begins with the bus master issuing a START condition followed by 7 address bits and a write bit (R/$\overline{W}$ = 0). If the address byte is successfully received, the MAX1361/MAX1362 (slave) issue an ACK. The master then writes to the slave. If the most significant bit (MSB) is 1, the slave recognizes the received byte as the setup byte (Table 4). If the MSB is 0, the slave recognizes that byte as the configuration byte (Table 2). Write to the configuration byte before writing to the setup byte (Figure 8). If enabling $\overline{RESET}$ in the setup byte, rewrite the configuration byte after writing the setup byte, since $\overline{RESET}$ clears the contents of the configuration byte back to the power-up state.

When the monitor-setup bit of the setup byte is set to 1, writing extends up to 13 bytes to clock in monitor-setup data. Terminate writing monitor-setup data at any time by issuing a STOP or repeated START condition. If the slave receives a byte successfully, it issues an ACK (Figure 9).

Note: When operating in HS mode, a STOP condition returns the bus into F/S mode (see the *HS I^2C Mode* section).

Automatic Shutdown

AutoShutdown occurs between conversions when the MAX1361/MAX1362 are idle. When operating in external clock mode, issue a STOP, NACK, or repeated START condition to place the devices in idle mode and benefit from automatic shutdown. A STOP condition is not necessary in internal clock mode for automatic shutdown because power-down occurs once all conversions are complete. Shutdown reduces supply current to less than 0.5µA (external reference mode, typ) and 300µA (internal reference mode, typ).

When idle, the MAX1361/MAX1362 continuously wait for a START condition followed by their slave address. Upon reading a valid address byte, the MAX1361/MAX1362 power up. The internal reference requires 10ms to wake up. Therefore, power up the internal reference 10ms prior to conversion or leave the reference continuously powered. Wake-up is transparent when using an external reference or V_{DD} as the reference.

Automatic shutdown results in dramatic power savings, particularly at slow conversion rates with internal clock. For example, using an external reference at a conversion rate of 10ksps, the average supply current for the MAX1361 is 60µA (typ) and drops to 6µA (typ) at 1ksps. At 0.1ksps, the average supply current is just 1µA. Table 3 shows AIN3/REF configuration and reference power-down state.

Scan Modes

SCAN1 and SCAN0 of the configuration byte set the scan-mode configuration. When configuring AIN3/REF for reference input or output (SEL0 = 1), AIN3/REF is excluded from a multichannel scan. The scanned results write to memory in the same order as the conversion. Start a conversion sequence by initiating a read with the desired scan mode. Read the results from memory in the order they were converted (see the *Reading a Conversion (Read Cycle)* section).

Selecting channel scan mode [0,0] starts converting from channel 0 up to the channel chosen by CS1, CS0.

Selecting channel scan mode [0,1] converts the channel selected by CS1, CS0 eight times and returns eight consecutive results.

Selecting monitor mode [1,0] initiates a continuous conversion scan sequence from channel 0 to the channel selected by CS1, CS0. See the *Monitor Mode* section for more details.

Selecting channel scan mode [1,1] performs a single conversion on the channel selected by CS1, CS0 and returns the result.

Table 3. Reference Voltage and AIN3/REF Format

SEL1	SEL0	INT REF POWERDOWN	REFERENCE VOLTAGE	AIN3/REF	INTERNAL REFERENCE STATE
0	0	X	V_{DD}	Analog input	Always off
0	1	X	External reference	Reference input	Always off
1	0	0	Internal reference	Analog input	Always off
1	0	1	Internal reference	Analog input	Always on
1	1	0	Internal reference	Reference output	Always off
1	1	1	Internal reference	Reference output	Always on

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Table 4. Setup-Byte Format*

BIT	NAME	DESCRIPTION
7 (MSB)	Setup	Setup byte always starts with 1.
6	REF/AIN SEL1	When [0,0], REF/AIN3 = AIN3, REF = V_{DD}. When [0,1], REF/AIN3 = REF, REF = external reference. When [1,0], REF/AIN3 = AIN3, REF = internal reference. When [1,1], REF/AIN3 = REF, REF = internal reference. (Table 3)
5	REF/AIN SEL0	
4	INT REF Power Down	1 = internal reference always powered up. 0 = internal reference always powered down. (Table 3)
3	$\overline{INT}$/EXT Clock	0 = internal clock. 1 = external clock (MAX1361/MAX1362 use the SCL clock for conversions).
2	$\overline{UNI}$/BIP	0 = unipolar. 1 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, analog signal in 0 to V_{REF} range can be converted. In differential bipolar mode, input signal can range from $-V_{REF}/2$ to $+V_{REF}/2$. When single-ended mode is chosen, the SE/$\overline{DIF}$ bit of configuration byte overrides $\overline{UNI}$/BIP, and conversions are performed in unipolar mode.
1	Reset	1 = no action. 0 = resets $\overline{INT}$ and configuration register. Setup register and channel trip thresholds are unaffected.
0	Monitor Setup	0 = no action. 1 = extends writing up to 13 bytes (104 bits) of alarm reset mask. Scans speed selection and alarm thresholds. See the *Configuring Monitor Mode* section.

**Power-on defaults: 0x82*

Table 5. Channel Selection in Single-Ended Mode (SE/$\overline{DIF}$ = 1)

CS1	CS0	CH0	CH1	CH2	CH3
0	0	+			
0	1		+		
1	0			+	
1	1				+

Table 6. Channel Selection in Differential Mode (SE/$\overline{DIF}$ = 0)

CS1	CS0	CH0	CH1	CH2	CH3
0	0	+	-		
0	1	-	+		
1	0			+	-
1	1			-	+

Table 7. SE/$\overline{DIF}$ and $\overline{UNI}$/BIP Table

SE/$\overline{DIF}$	$\overline{UNI}$/BIP	MODE
0	0	Differential inputs, unipolar
0	1	Differential inputs, bipolar
1	0	Single-ended inputs, unipolar
1	1	Single-ended inputs, unipolar

Reading a Conversion (Read Cycle)

Initiate a read cycle to start a conversion sequence and to obtain conversion results. See the *Scan Modes* section for details on the channel-scan sequence. Read cycles begin with the bus master issuing a START condition followed by 7 address bits and a read bit (R/$\overline{W}$ = 1). After successfully receiving the address byte, the MAX1361/MAX1362 (slave) issue an ACK. The master then reads from the slave. (See Figures 10–13.)

The result is transmitted in 2 bytes. The 1st byte consists of a leading 1 followed by a 2-bit binary channel address tag, a 12/$\overline{10}$ bit flag (0 for the MAX1361/MAX1362), 2 bits of 1s, the first 2 bits of the data result, and the expected ACK from the master. The 2nd byte

Table 8. Data Format

HIGH	CH1	CH0	12/$\overline{10}$	HIGH	HIGH	DATA (MSB)	D8		D7	D6	D5	D4	D3	D2	D1	D0	
1	0/1	0/1	0 = 10b 1 = 12b	1	1	0/1	0/1	ACK	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	ACK/ NACK

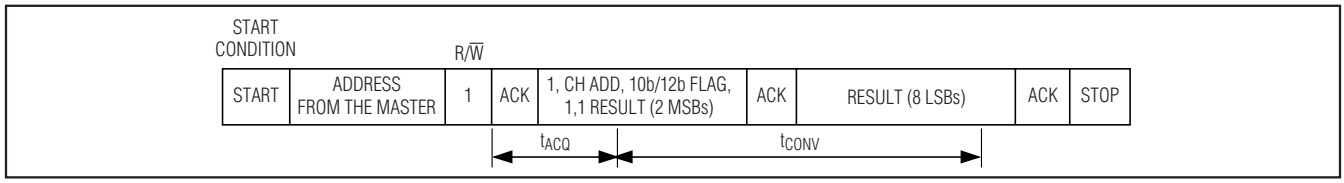

Figure 10. Example of Reading the Conversion Result—External Clock Mode

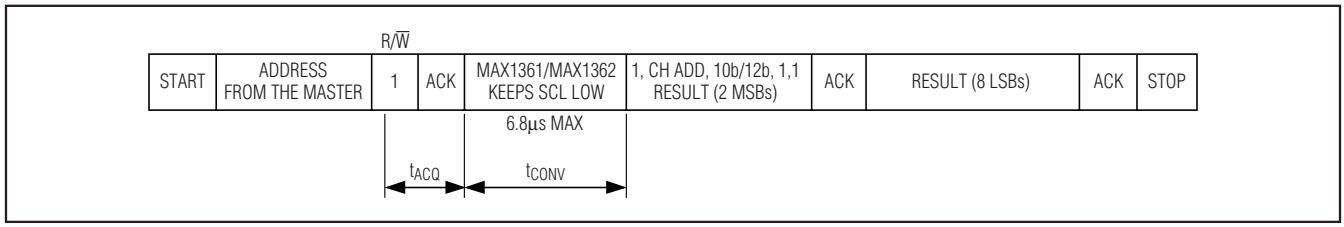

Figure 11. Example of a Single Conversion Using the Internal Clock, SCAN = 1,1

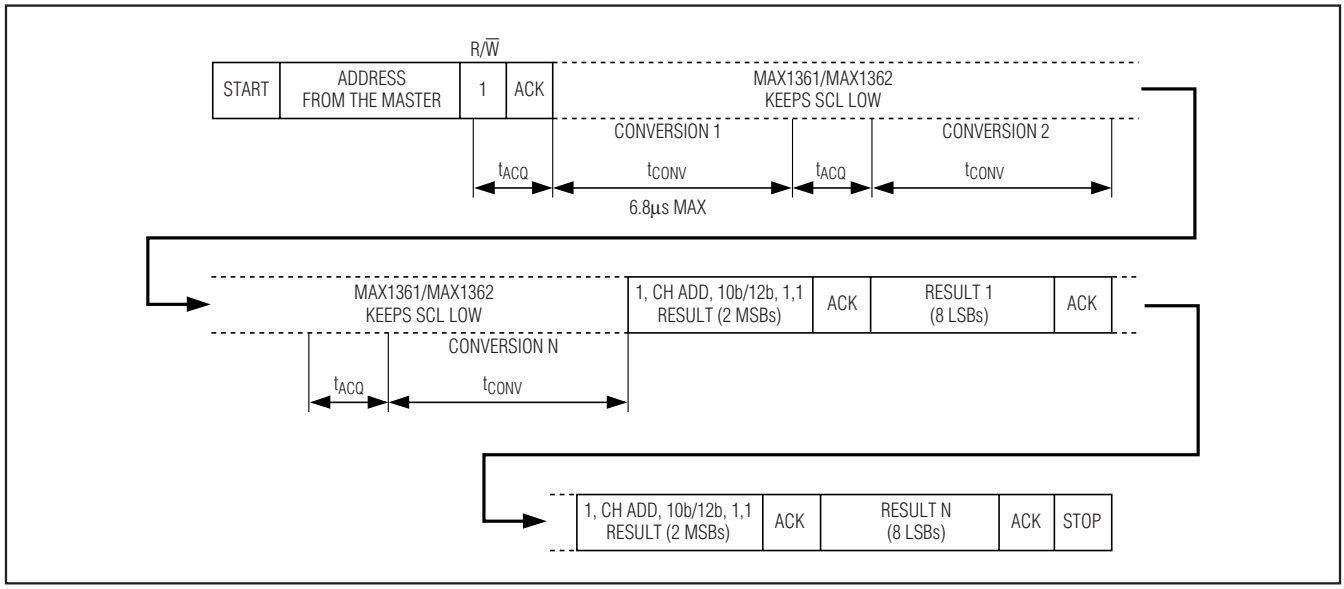

Figure 12. Example of Scan-Mode Conversions Using the Internal Clock, SCAN = 0,0 and 0,1

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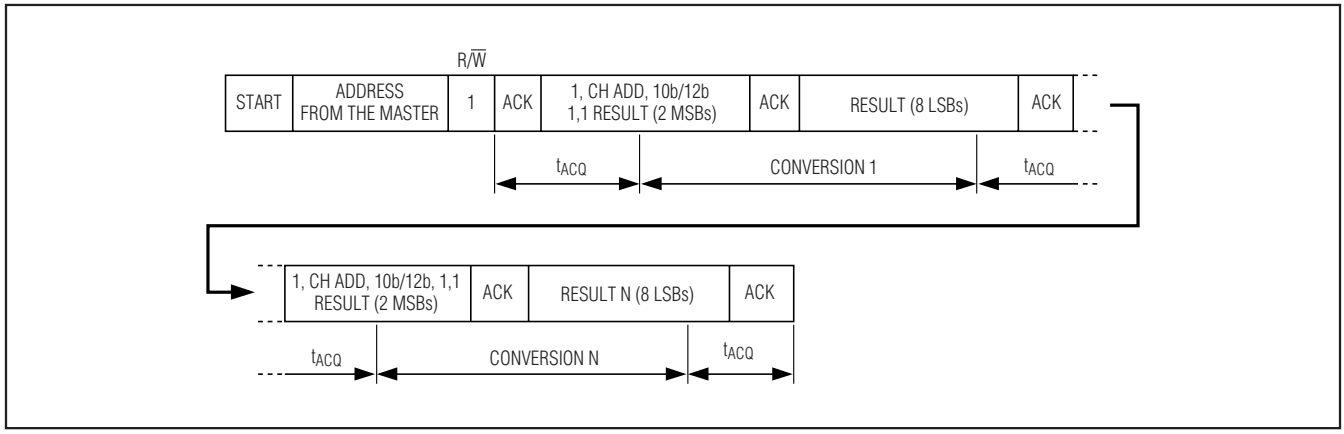

Figure 13. Example of Scan-Mode Conversions Using the External Clock, SCAN = 0,0 and 0,1

contains D7–D0. To read the next conversion result, issue an ACK. To stop reading, issue a NACK.

When the MAX1361/MAX1362 receive a NACK, they release SDA allowing the master to generate a STOP or a repeated START condition.

Monitor Mode

Monitor-Mode Overview

The MAX1361/MAX1362 automatically monitor up to four input channels. For systems with limited I^2C bandwidth, monitor mode allows the µC to set a window by programming lower and upper thresholds during initialization, and only intervening if the MAX1361/MAX1362 detect an alarm condition. This allows an interrupt-driven approach as an alternative to continuously polling the ADC with the µC. Monitor mode reduces processor overhead and conserves I^2C bandwidth.

The following shows an example of events in monitor mode:

1) Fault condition(s) detected, $\overline{INT}$ asserted.
2) Host µC services interrupt and send SMBus alert to identify the alarming device. The MAX1361/MAX1362 respond with the I^2C slave address, pending arbitration rules. (See the *SMBus Alert* section.)
3) The MAX1361/MAX1362 release the $\overline{INT}$.
4) Host-µC reads the alarm-status register, latched-fault register, and current-conversion results to determine the alarming channel(s) and course of action.
5) Host µC services alarm(s); adjusts system parameters as needed and/or adjust lower and upper thresholds.
6) Clears the alarm register. See the *Configuring Monitor Mode* section.
7) Monitor mode resumes.
8) If there is still an active fault, the device asserts $\overline{INT}$ again. See step 1.

Writing SCAN1 and SCAN0 bits = [1,0] in the configuration byte activates monitor mode. The MAX1361/MAX1362 scan from channels 0 up to the channel selected by [CS1:CS0] at a rate determined by the scan delay bits. The MAX1361/MAX1362 compare the conversion results with the lower and upper thresholds for each channel. When any conversion exceeds the threshold, the MAX1361/MAX1362 assert an interrupt by pulling $\overline{INT}$ low (if enabled). The MAX1361/MAX1362 set the corresponding flag bit in the alarm-status register and write conversion results to the latched-fault register to record the event causing the alarm condition.

$\overline{INT}$ active state is randomly delayed with respect to the conversion. Depending on the number of channels scanned and the position in the channel scan sequence, the maximum possible delay for asserting $\overline{INT}$ is five conversion periods (34µs typ, delay = 0,0,0).

Configuring Monitor Mode

To write monitoring setup data, set the monitor-setup bit (bit 0 in setup byte) to 1 to extend writing up to 104 bits (13 bytes) of monitoring setup data. The number of bits written to the MAX1361/MAX1362 depends on whether the part is in single-ended or differential mode and whether the upper channel limit is set by [CS1:CS0] (Table 9).

Terminate writing at any time by using a STOP or repeated START condition. Previous monitoring setup data not overwritten remains valid.

Table 9. Monitor-Mode Setup Data Format

Alarm reset, scan speed, INT_EN , (8 bits)	AIN0 thresholds (24 bits)	AIN1 thresholds (skip if differential mode, or CS1, CS0 < 1) (24 bits)	AIN2 thresholds (skip if CS1, CS0 < 2) (24 bits)	AIN3 thresholds (skip if differential mode, or CS1, CS0 < 3) (24 bits)

Table 10. Alarm Reset, Scan Speed Register, and INT_EN Data Format

RESET ALARM CH 0	RESET ALARM CH 1	RESET ALARM CH 2	RESET ALARM CH 3	DELAY 2	DELAY 1	DELAY 0	INT_EN
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Table 11. Delay Settings

DELAY 2	DELAY 1	DELAY 0	MONITOR-MODE CONVERSION RATE (ksps)
0	0	0	150.0*
0	0	1	75.0
0	1	0	37.5
0	1	1	18.8
1	0	0	9.4
1	0	1	4.7
1	1	0	2.3
1	1	1	1.2

**When using delay = [0,0,0] in internal reference mode and AIN3/REF configured as a REF output, the MAX1361/MAX1362 may exhibit a code-dependant gain error due to insufficient internal reference drive. Gain error caused by this phenomenon is typically less than 1%FSR (0.1µF C_{REF} in series with a 2kΩ resistor) and increases with a larger C_{REF}. Avoid this gain error by using an external reference, V_{DD}, as a reference or use an internal reference with AIN3/REF as an analog input (see Table 4). Alternatively, choose delay bits other than [0,0,0] to lower the conversion rate.*

A 1 written to the reset alarm CH_ clears the alarm, otherwise no action occurs (Table 10). Deassert $\overline{INT}$ by clearing all alarms or by initiating an SMBus alert during an alarm condition (see the *SMBus Alert* section)

The Delay 2, Delay 1, and Delay 0 bits set the speed of monitoring by changing the delay between conversions. Delay 2, 1, and 0 = 000 sets the maximum possible speed; 001 divides the maximum speed by approximately 2. Increasing delay values further divides the previous speed by two (Table 11).

INT_EN controls the open-drain INT output. Set INT_EN to 1 to enable the hardware interrupt. Set INT_EN to 0 to disable the hardware interrupt output. The $\overline{INT}$ output is high impedance when disabled or when there are no alarms. The master can also poll the alarm status register at any time to check the alarm status.

Repeat clocking channel threshold data up to the channel programmed by CS1 and CS0 (Table 12). For differential input mode, omit odd channels; the lower and upper threshold data applies to channel pairs. There is no need to clock in dummy data for odd (or even) channels (Table 6).

Table 12. Lower and Upper Threshold Data Format

BYTE	B7	B6	B5	B4	B3	B2	B1	B0	ACKNOWLEDGE
1	X	X	LT9 (MSB)	LT8	LT7	LT6	LT5	LT4	ACK
2	LT3	LT2	LT1	LT0 (LSB)	X	X	UT9 (MSB)	UT8	ACK
3	UT7	UT6	UT5	UT4	UT3	UT2	UT1	UT0 (LSB)	ACK

X = Don't care.
ACK = Acknowledge.

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Table 13. Readback-Mode Format

SCAN SPEED AND INT_EN								AIN0 THRESHOLDS	AIN1 THRESHOLDS (SKIP IF DIFFERENTIAL MODE OR CS1, CS0 < 1)	AIN2 THRESHOLDS (SKIP IF CS1, CS0 < 2)	AIN3 THRESHOLDS (SKIP IF DIFFERENTIAL MODE OR CS1, CS0 < 3)
1	1	1	1	D2	D1	D0	INT_EN	24 bits	24 bits	24 bits	24 bits

Table 14. Reading in Monitor-Mode Data Format

ALARM-STATUS REGISTER	LATCHED-FAULT REGISTER	CURRENT-CONVERSION RESULTS
8 bits	16, 32, 48, or 64 bits (depends on CSO, CS1, and SE/$\overline{DIF}$)	16, 32, 48, or 64 bits (depends on CSO, CS1, and SE/$\overline{DIF}$)

Table 15. Alarm-Status Register

CH0 UP	CH0 LOW	CH1 UP	CH1 LOW	CH2 UP	CH2 LOW	CH3 UP	CH3 LOW
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

0 = Not-alarm condition.
1 = Alarm condition.

Table 16. Latched-Fault and Current-Conversion Register

AIN0	AIN1	AIN2	AIN3
16-bit read	16-bit read	16-bit read	16-bit read

To disable alarming on a specific channel, set the lower threshold to 0x800 and the upper threshold to 0x7FF for bipolar mode, or set the lower threshold to 0x000 and the upper threshold to 0xFFF for unipolar mode.

Readback Mode

Select readback mode by setting CS3, CS2 to [1,1] in the configuration byte. Begin a read operation to start reading back monitor-setup data. Clock out delay bit settings, INT_EN bit, and the lower and upper thresholds programmed for each channel. Readback mode follows exactly the same format as writing to the monitor-setup data, with the exception of the first 4 alarm-reset bits, which are always 1 (Table 13).

Reading in Monitor Mode

Reading in monitor mode reads back the alarm-status register, latched-fault register, and current-conversion results as shown in Table 14.

The MAX1361/MAX1362 register pointer loops back to the beginning of the current-conversion result after reading the last conversion result. Stop reading at any time by asserting a STOP condition or NACK.

Note: The MAX1361/MAX1362 do not update the current-conversion results register while reading in monitor mode. Monitor mode resumes after a STOP condition or NACK.

Alarm-Status Register

The latched-fault register records a snapshot of the alarming channel at the instance that a fault condition is asserted. An alarm-status bit of 1 (Table 15) indicates a fault, and the data in the latched-fault register of the corresponding channel contains the conversion result that caused the alarm to trip. Resetting alarms does not clear the latched-fault register, thus the latched-fault register contains valid data only if an alarm status bit is high for the given channel.

The current-conversion register contains the most recent conversion results. If the user attempts to read past the last result of the current-conversion register, the MAX1361/MAX1362 wraps back to the beginning of the current-conversion result.

The latched-fault register and current-conversion register follow the data format detailed in Tables 8 and 16. Register length depends on the number of conversions in one monitoring sequence. For example, when channel pairs 0/1 and channels 2/3 are monitored differentially, there are only two conversion results to report. The latched-fault register is 2 x 16 bits long, after which two current-conversion results follow. Likewise, if CS0 and CS1 limit the upper bound of the channel scan range from CH0 to CH2 in single-ended mode, the latched-fault register clocks out 3 x 16 bits of data followed by the current-conversion results, also 3 x 16 bits.

Resetting Alarm

Reset alarms by writing to monitor-setup data. See the *Configuring Monitor Mode* section and Table 10.

SMBus Alert

The SMBus-alert feature provides a quick method to identify alarming devices on a shared interrupt. Upon receiving an interrupt signal, the host µC can broadcast a receive byte request to the alert-response slave address (0001100). Any slave device that generated an interrupt attempts to identify itself by putting its own address on the bus. The alert response can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply, and the device with the lower address wins as a consequence of the open-collector bus. The losing device does not generate an acknowledgement and continues to hold the alert line low until serviced. Successful reading of the alert response address deasserts $\overline{INT}$.

The MAX1361/MAX1362 resume monitoring after cleaning an alarm-status register. $\overline{INT}$ may immediately reassert if a fault is still present, or if the alarm register has not been thoroughly cleared.

Transfer Functions

Output data coding for the MAX1361/MAX1362 is binary in unipolar mode and two's complement in bipolar mode with 1 LSB = $V_{REF}/2^N$, where N is the number of bits. Code transitions occur halfway between successive-integer LSB values. Figures 14 and 15 show the transfer functions for unipolar and bipolar operations, respectively.

Layout, Grounding, and Bypassing

Only use PC boards. Wire-wrap configurations are not recommended since the layout should ensure proper separation of analog and digital traces. Do not run analog and digital lines parallel to each other, and do not layout digital signal paths underneath the ADC package. Use separate analog and digital PC board ground sections with only one star point (Figure 16).

High-frequency noise in the power supply (V_{DD}) could influence the proper operation of the ADC's fast comparator. Bypass V_{DD} to the star ground with a network of two parallel capacitors, 0.1µF and 4.7µF, located as close as possible to the MAX1361/MAX1362 power supply. Minimize capacitor lead length for best supply noise rejection. For extremely noisy supplies, add an attenuation resistor (5Ω) in series with the power supply.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The

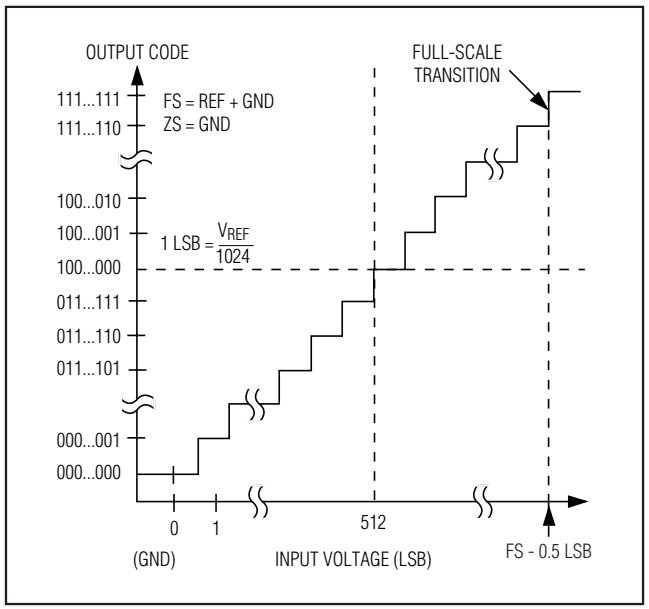

Figure 14. Unipolar Transfer Function

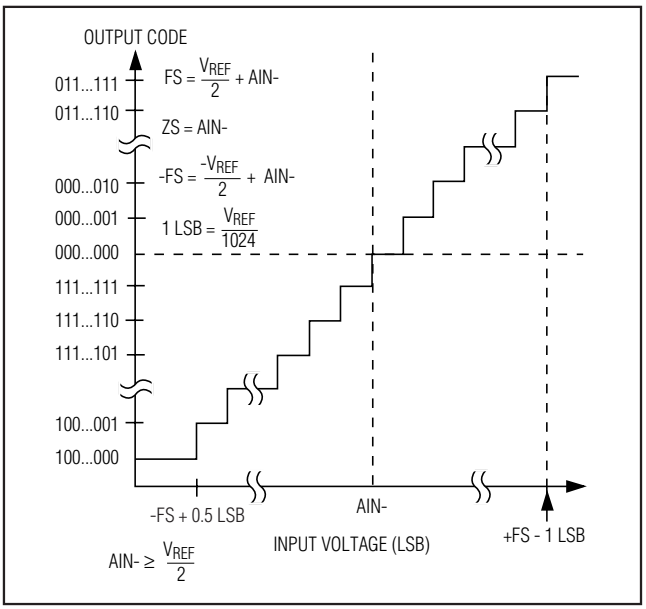

Figure 15. Bipolar Transfer Function

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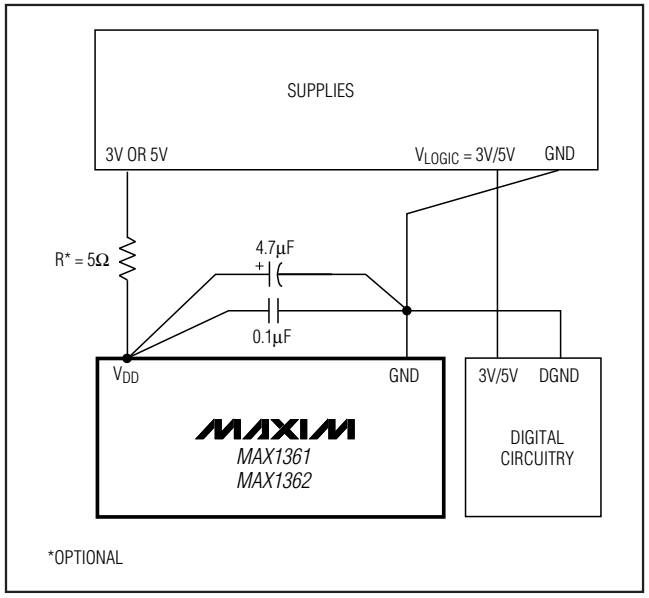


Figure 16. Power-Supply Grounding Connection

MAX1361/MAX1362's INL is measured using the end-point method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time between the falling edge of the sampling clock and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR\ (MAX)[dB] = 6.02dB \times N + 1.76dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD(dB) = 20 \times \log (SignalRMS/NoiseRMS)$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the ADC's full-scale range, calculate the ENOB as follows:

$$ENOB = (SINAD - 1.76)/6.02$$

$$SINAD(dB) = 20 \times \log \left[\frac{Signal_{RMS}}{Noise_{RMS} + THD_{RMS}} \right]$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\sqrt{\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2}{V_1}} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest distortion component.

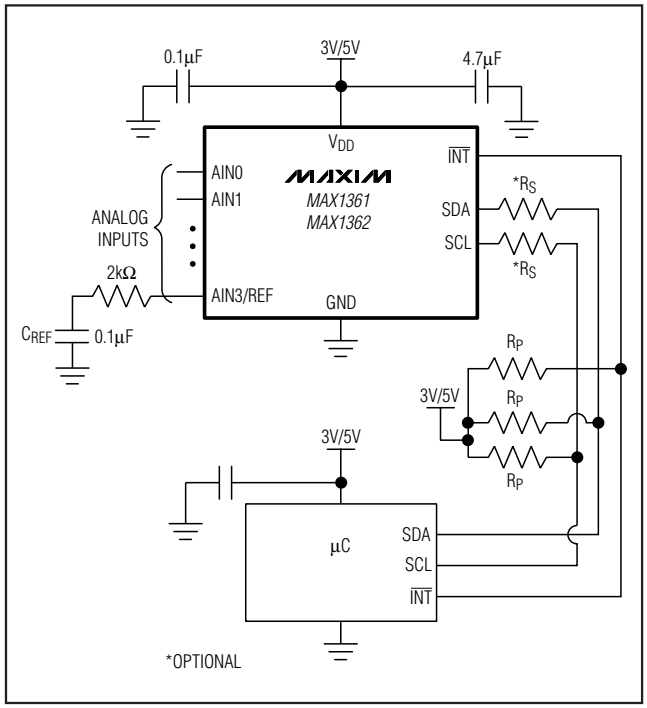
4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

Ordering Information/Selector Guide (continued)

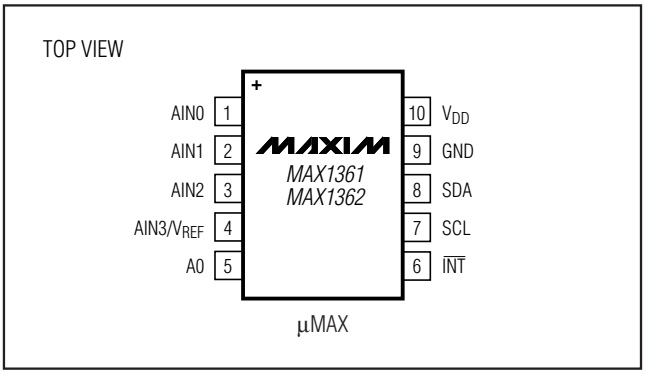
PART	TEMP RANGE	PIN-PACKAGE	I²C SLAVE ADDRESS	SUPPLY VOLTAGE (V)
MAX1362EUB+	-40°C to +85°C	10 µMAX	0110100/0110101	4.5 to 5.5
MAX1362MEUB+	-40°C to +85°C	10 µMAX	0110110/0110111	4.5 to 5.5

+Denotes a lead(Pb)-free/RoHS-compliant package.

Typical Operating Circuit



Pin Configuration



Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
10 µMAX	U10CN+1	21-0061	90-0330

4-Channel, 10-Bit, System Monitor with Programmable Trip Window and SMBus Alert Response

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	3/08	Removed L grade from data sheet	1, 13, 23
5	9/10	Changed the number of possible I^2C addresses to 4 (instead of 6) in the *Features* and *Slave Address* section	1, 13