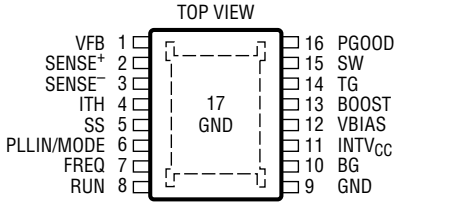
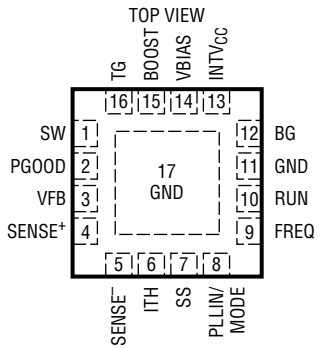
ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

VBIAS ..... –0.3V to 40V
BOOST ..... –0.3V to 71V
SW ..... –0.3V to 65V
RUN ..... –0.3V to 8V
Maximum Current Sourced into Pin from Source >8V 100µA
PGOOD, PLLIN/MODE ..... –0.3V to 6V
$INTV_{CC}$, (BOOST – SW) ..... –0.3V to 6V
$SENSE^+$, $SENSE^-$ ..... –0.3V to 40V
$SENSE^+ – SENSE^-$ ..... –0.3V to 0.3V
SS, ITH, FREQ, VFB ..... –0.3V to $INTV_{CC}$
Operating Junction Temperature Range (Notes 2, 3)
LTC3786E, LTC3786I ..... –40°C to 125°C
LTC3786H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Package Only ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC3786#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3786EMSE#PBF	LTC3786EMSE#TRPBF	3786	16-Lead Plastic MSOP	–40°C to 125°C
LTC3786IMSE#PBF	LTC3786IMSE#TRPBF	3786	16-Lead Plastic MSOP	–40°C to 125°C
LTC3786HMSE#PBF	LTC3786HMSE#TRPBF	3786	16-Lead Plastic MSOP	–40°C to 150°C
LTC3786EUD#PBF	LTC3786EUD#TRPBF	LFXW	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3786IUD#PBF	LTC3786IUD#TRPBF	LFXW	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 125°C
LTC3786HUD#PBF	LTC3786HUD#TRPBF	LFXW	16-Lead (3mm × 3mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
VBIAS	Chip Bias Voltage Operating Range			4.5		38	V
V_{FB}	Regulated Feedback Voltage	I_{TH} = 1.2V (Note 4)	●	1.188	1.200	1.212	V
I_{FB}	Feedback Current	(Note 4)			±5	±50	nA
$V_{REFLNREG}$	Reference Line Voltage Regulation	V_{BIAS} = 6V to 38V			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
g_m	Error Amplifier Transconductance	I_{TH} = 1.2V			2		mmho
I_Q	Input DC Supply Current Pulse-Skipping or Forced Continuous Mode Sleep Mode Shutdown	(Note 5) RUN = 5V; V_{FB} = 1.25V (No Load) RUN = 5V; V_{FB} = 1.25V (No Load) RUN = 0V			 0.8 55 8	 80 20	 mA µA µA
UVLO	$INTV_{CC}$ Undervoltage Lockout Thresholds	V_{INTVCC} Ramping Up V_{INTVCC} Ramping Down	● ●	 3.6	4.1 3.8	4.3 	V V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	●	1.18	1.28	1.38	V
V_{RUNHYS}	RUN Pin Hysteresis				100		mV
I_{RUNHYS}	RUN Pin Hysteresis Current	V_{RUN} > 1.28V			4.5		µA
I_{RUN}	RUN Pin Current	V_{RUN} < 1.28V			0.5		µA
I_{SS}	Soft-Start Charge Current	V_{SS} = 0V		7	10	13	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 1.1V	●	68	75	82	mV
$V_{SENSE(CM)}$	SENSE Pins Common Mode Range (BOOST Converter Input Supply Voltage V_{IN})			2.5		38	V
I_{SENSE^+}	$SENSE^+$ Pin Current	V_{FB} = 1.1V			200	300	µA
I_{SENSE^-}	$SENSE^-$ Pin Current	V_{FB} = 1.1V				±1	µA
$t_{r(TG)}$	Top Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
$t_{f(TG)}$	Top Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
$t_{r(BG)}$	Bottom Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
$t_{f(BG)}$	Bottom Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
$R_{UP(TG)}$	Top Gate Pull-Up Resistance				1.2		Ω
$R_{DN(TG)}$	Top Gate Pull-Down Resistance				1.2		Ω
$R_{UP(BG)}$	Bottom Gate Pull-Up Resistance				1.2		Ω
$R_{DN(BG)}$	Bottom Gate Pull-Down Resistance				1.2		Ω
$t_{D(TG/BG)}$	Top Gate Off to Bottom Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			80		ns
$t_{D(BG/TG)}$	Bottom Gate Off to Top Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			80		ns
DF_{MAXBG}	Maximum BG Duty Factor				96		%
$t_{ON(MIN)}$	Minimum BG On-Time	(Note 7)			110		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{BIAS} = 12V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
$V_{INTVCC(VIN)}$	Internal V_{CC} Voltage	6V < VBIAS < 38V		5.2	5.4	5.6	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
Oscillator and Phase-Locked Loop							
f_{PROG}	Programmable Frequency	R_{FREQ} = 25k R_{FREQ} = 60k R_{FREQ} = 100k		 335	105 400 760	 465	kHz kHz kHz
f_{LOW}	Lowest Fixed Frequency	V_{FREQ} = 0V		320	350	380	kHz
f_{HIGH}	Highest Fixed Frequency	V_{FREQ} = $INTV_{CC}$		485	535	585	kHz
f_{SYNC}	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis V_{FB} Ramping Positive Hysteresis		 –12 8 	 –10 2.5 10 2.5	 –8 12 	 % % % %
$t_{PGOOD(DELAY)}$	PGOOD Delay	PGOOD Going High to Low			25		µs
BOOST Charge Pump							
I_{BOOST}	BOOST Charge Pump Available Output Current	V_{SW} = 12V; V_{BOOST} – V_{SW} = 4.5V; FREQ = 0V, Forced Continuous or Pulse-Skipping Mode			85		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3786 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3786E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3786I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3786H is guaranteed over the –40°C to 150°C operating temperature range. High temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 68°C for the QFN package and θ_{JA} = 40°C for the MSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3786 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH} at the midpoint of the current limit range.

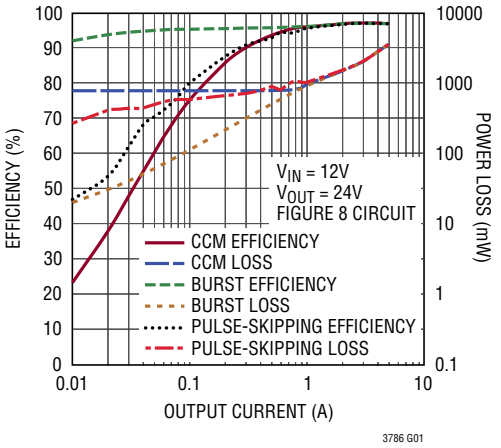
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

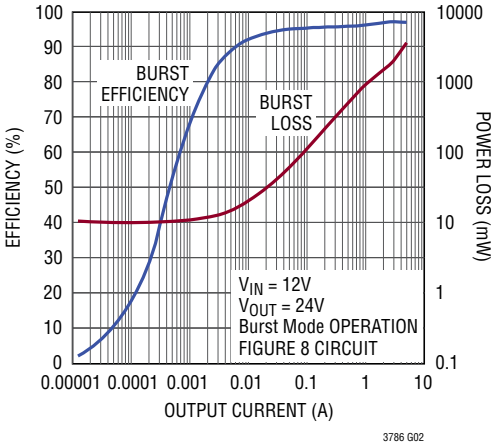
Note 7: see Minimum On-Time Considerations in the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

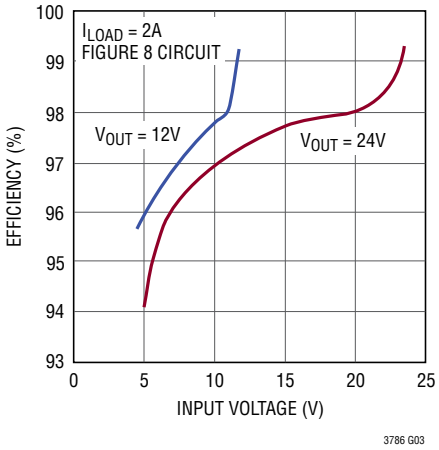
Efficiency and Power Loss vs Output Current



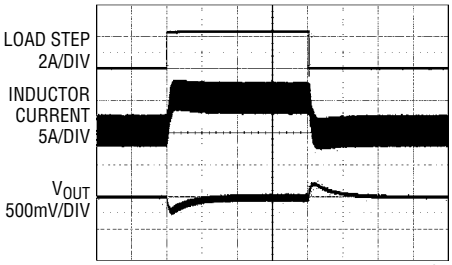
Efficiency and Power Loss vs Output Current



Efficiency vs Input Voltage

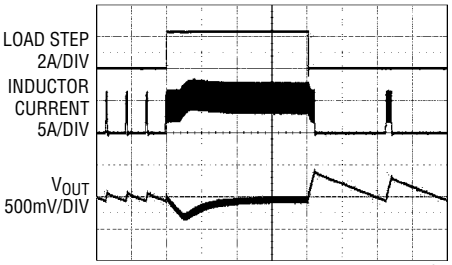


Load Step Forced Continuous Mode



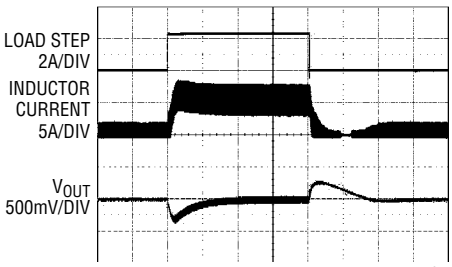
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Load Step Burst Mode Operation



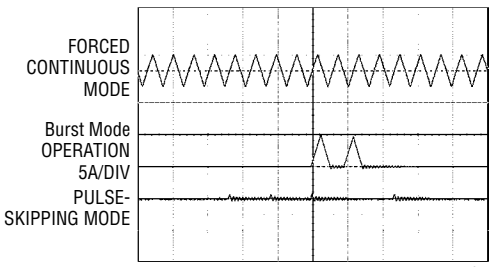
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Load Step Pulse-Skipping Mode



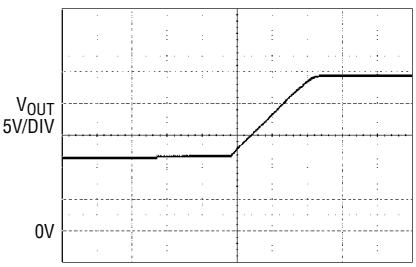
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Inductor Current at Light Load



VIN = 12V 5µs/DIV
VOUT = 24V
ILOAD = 200µA
FIGURE 8 CIRCUIT

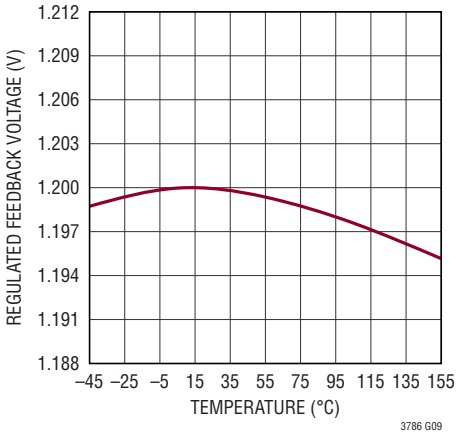
Soft Start-Up



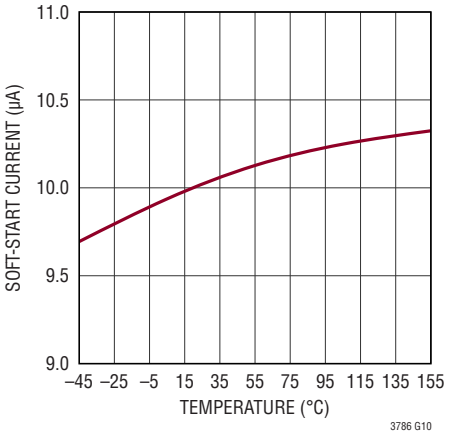
VIN = 12V 2ms/DIV
VOUT = 24V
FIGURE 8 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

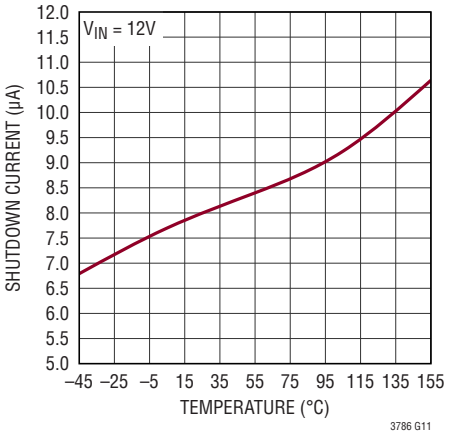
Regulated Feedback Voltage vs Temperature



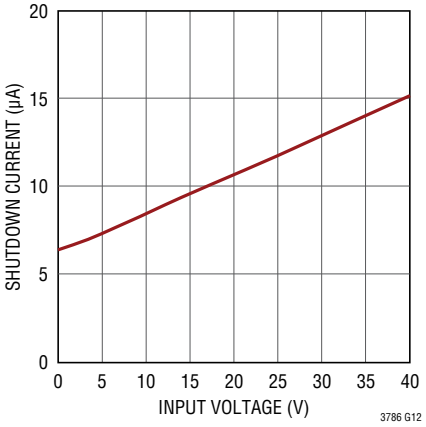
Soft-Start Pull-Up Current vs Temperature



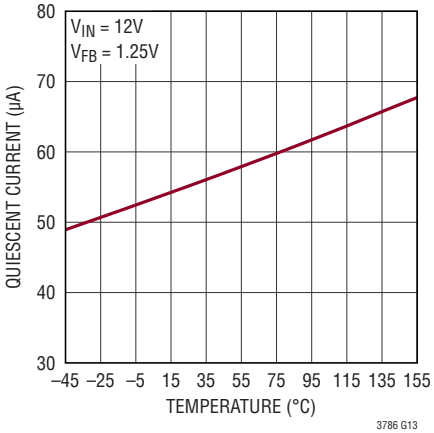
Shutdown Current vs Temperature



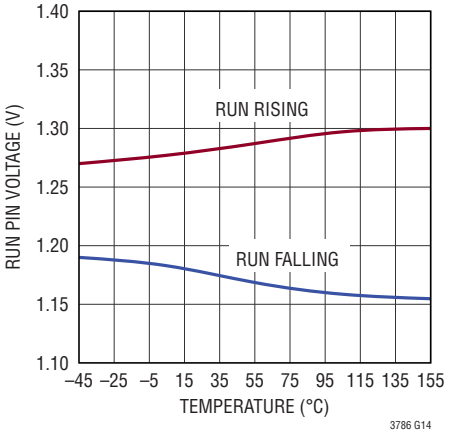
Shutdown Current vs Input Voltage



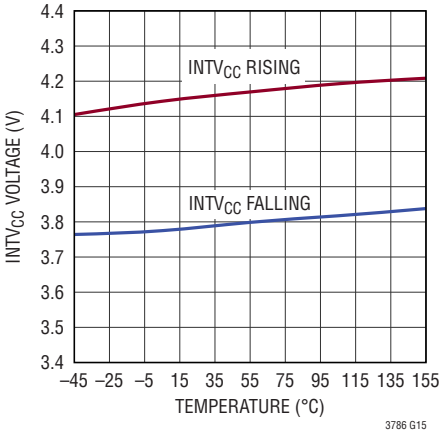
Quiescent Current vs Temperature



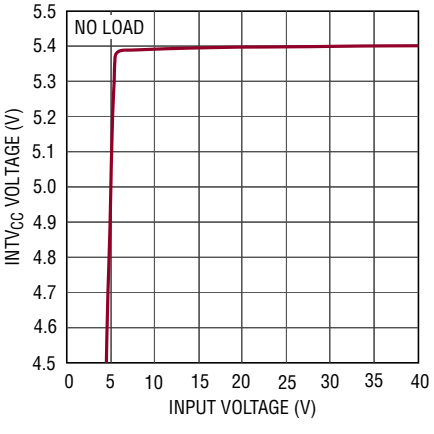
Shutdown (RUN) Threshold vs Temperature



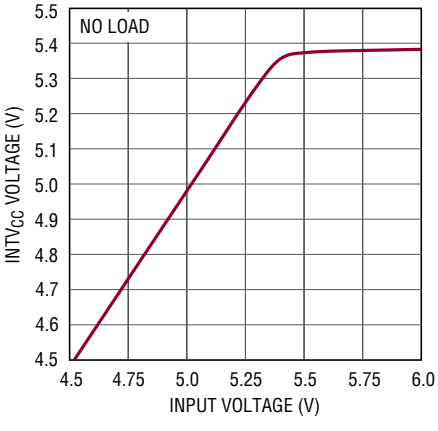
Undervoltage Lockout Threshold vs Temperature



INTVCC Line Regulation

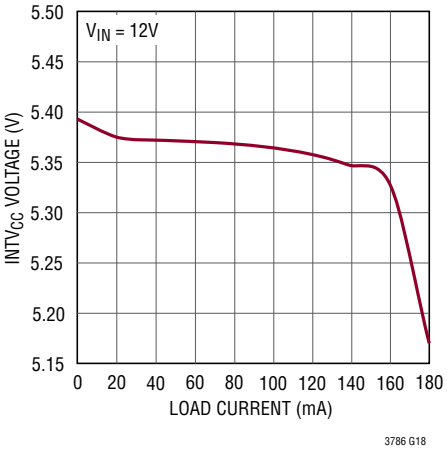


INTVCC Line Regulation

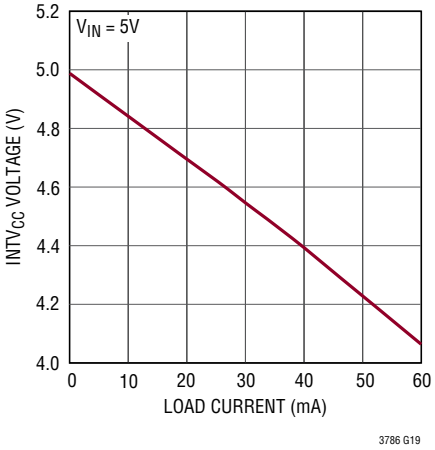


TYPICAL PERFORMANCE CHARACTERISTICS

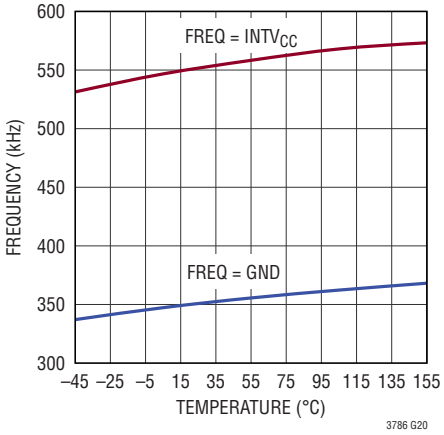
$INTV_{CC}$ vs Load Current



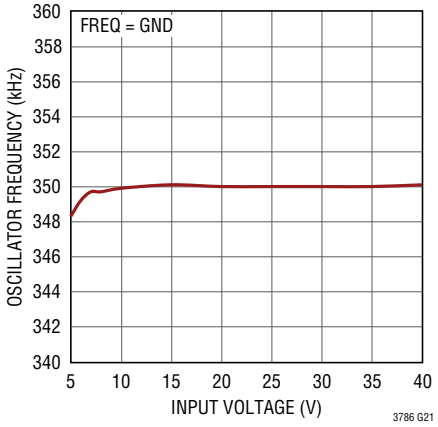
$INTV_{CC}$ vs Load Current



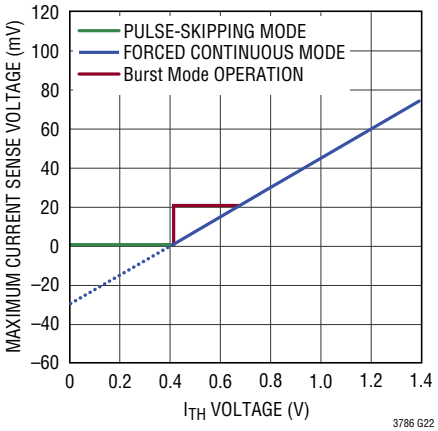
Oscillator Frequency vs Temperature



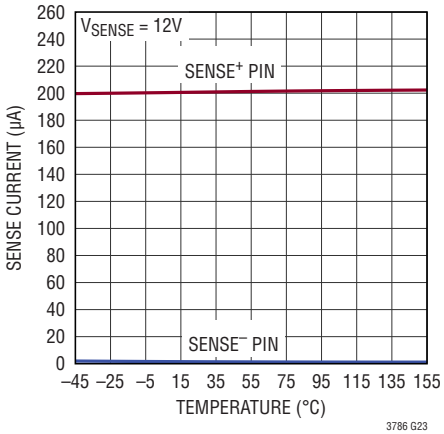
Oscillator Frequency vs Input Voltage



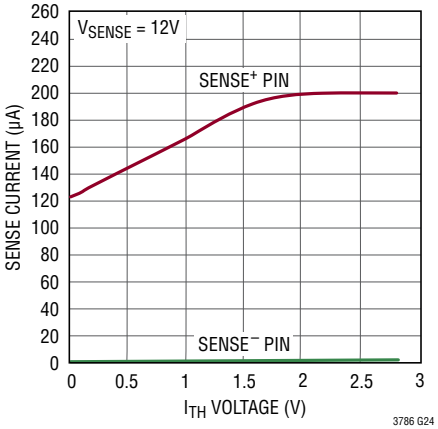
Maximum Current Sense Threshold vs I_{TH} Voltage



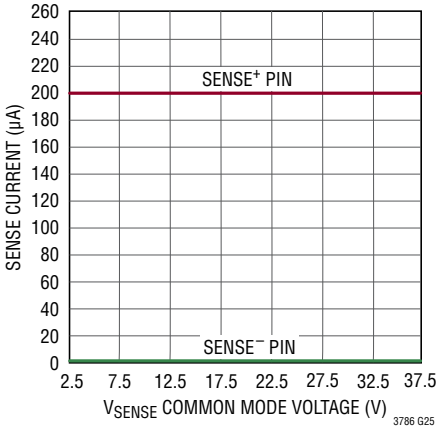
SENSE Pin Input Current vs Temperature



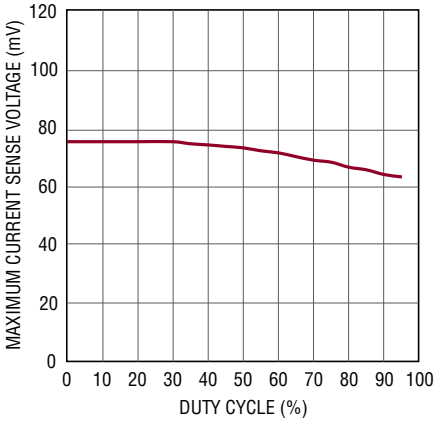
SENSE Pin Input Current vs I_{TH} Voltage



SENSE Pin Input Current vs V_{SENSE} Voltage

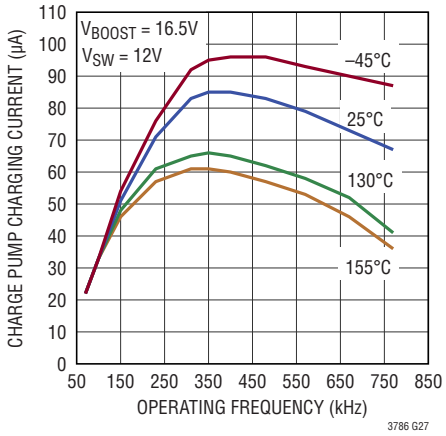


Maximum Current Sense Threshold vs Duty Cycle

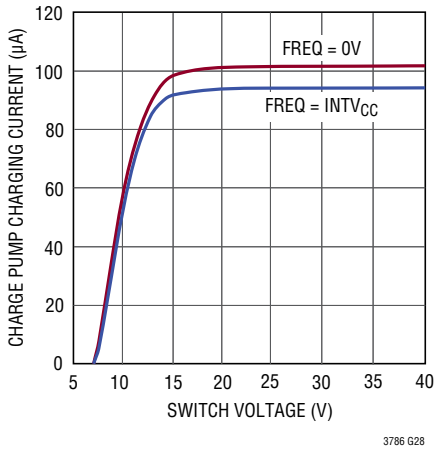


TYPICAL PERFORMANCE CHARACTERISTICS

Charge Pump Charging Current vs Operating Frequency



Charge Pump Charging Current vs Switch Voltage



PIN FUNCTIONS (MSOP/QFN)

VFB (Pin 1/Pin 3): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider connected across the output.

SENSE+ (Pin 2/Pin 4): Positive Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the positive terminal of a current sense resistor. The current sense resistor is normally placed at the input of the boost controller in series with the inductor. This pin also supplies power to the current comparator.

SENSE– (Pin 3/Pin 5): Negative Current Sense Comparator Input. The (–) input to the current comparator is normally connected to the negative terminal of a current sense resistor connected in series with the inductor. The common mode voltage range on the SENSE+ and SENSE– pins is 2.5V to 38V (40V abs max).

ITH (Pin 4/Pin 6): Current Control Threshold and Error Amplifier Compensation Point. The voltage on this pin sets the current trip threshold.

SS (Pin 5/Pin 7): Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during start-up.

PLLIN/MODE (Pin 6/Pin 8): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, it will force the controller into forced continuous mode of operation and the phase-locked loop will force the rising BG signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, this input determines how the LTC3786 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the PLLIN/MODE pin and $INTV_{CC}$.

PIN FUNCTIONS (MSOP/QFN)

FREQ (Pin 7/Pin 9): The Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed from 50kHz to 900kHz by connecting a resistor from the FREQ pin to GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

RUN (Pin 8/Pin 10): Run Control Input. Forcing this pin below 1.28V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC3786, reducing quiescent current to approximately 8µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. There is a 0.5µA pull-up current for this pin. Once the RUN pin raises above 1.28V, an additional 4.5µA pull-up current is added to the pin for programmable hysteresis.

GND (Pin 9, Exposed Pad Pin 17/ Pin 11, Exposed Pad Pin 17): Ground. Connects to the source of the bottom (main) N-channel MOSFET and the (–) terminal(s) of C_{IN} and C_{OUT}. All small-signal components and compensation components should also connect to this ground. The exposed pad must be soldered to the PCB for rated thermal performance.

BG (Pin 10/Pin 12): Bottom Gate. Connect to the gate of the main N-channel MOSFET.

$INTV_{CC}$ (Pin 11/Pin 13): Output of Internal 5.4V LDO. Power supply for control circuits and gate drivers. Decouple this pin to GND with a minimum 4.7µF low ESR ceramic capacitor.

VBIAS (Pin 12/Pin 14): Main Supply Pin. It is normally tied to the input supply V_{IN} or to the output of the boost converter. A bypass capacitor should be tied between this pin and the GND pin. The operating voltage range on this pin is 4.5V to 38V (40V abs max).

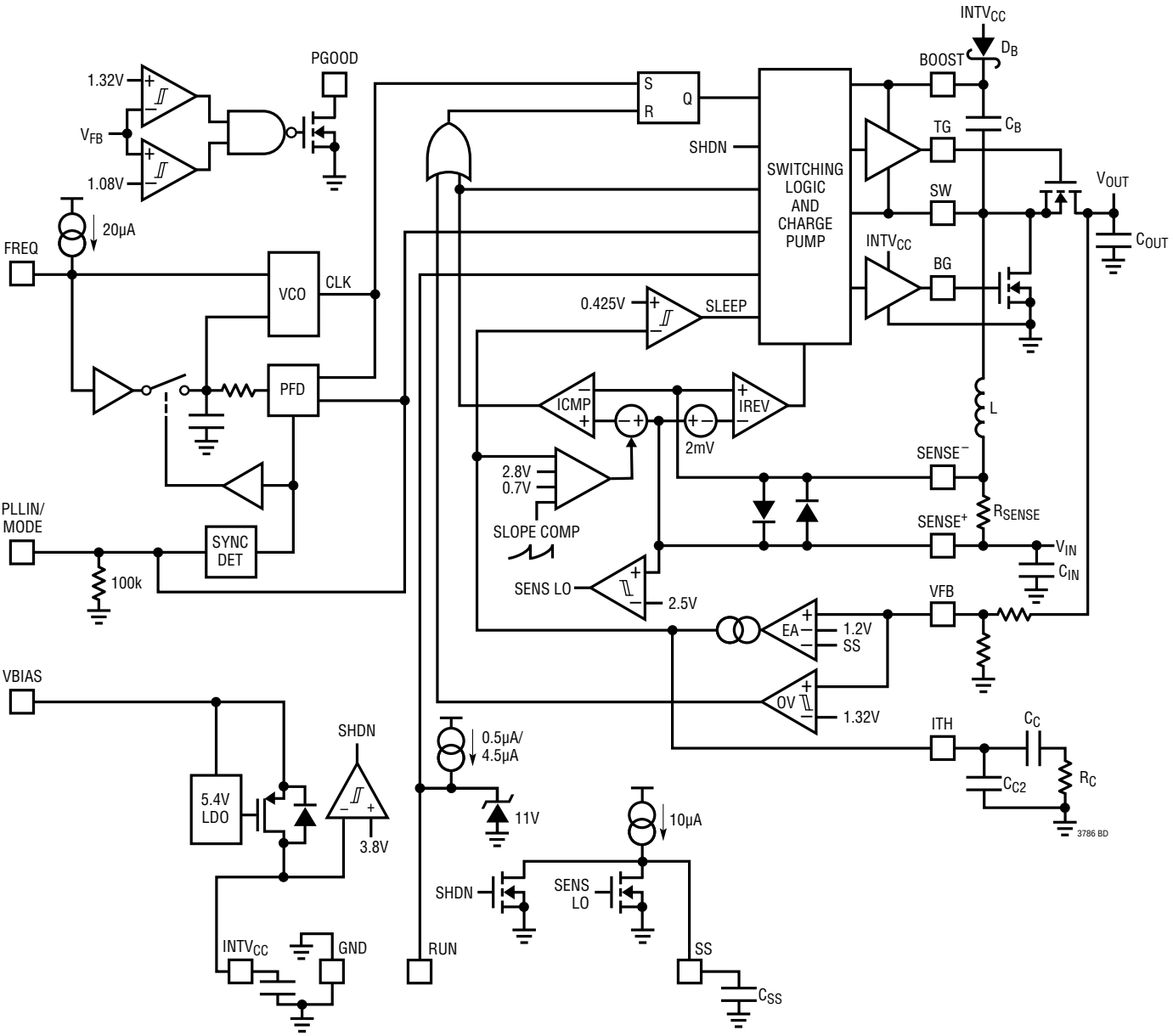
BOOST (Pin 13/Pin 15): Floating Power Supply for the Synchronous MOSFET. Bypass to SW with a capacitor and supply with a Schottky diode connected to $INTV_{CC}$.

TG (Pin 14/Pin 16): Top Gate. Connect to the gate of the synchronous NMOS.

SW (Pin 15/Pin 1): Switch Node. Connect to the source of the synchronous top MOSFET, the drain of the main bottom MOSFET, and the inductor.

PGOOD (Pin 16/Pin 2): Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is more than ±10 % away from the regulated output voltage. To avoid false trips the output voltage must be outside of the range for 25µs before this output is activated.

BLOCK DIAGRAM



OPERATION (Refer to the Block Diagram)

Main Control Loop

The LTC3786 uses a constant-frequency, current mode step-up control architecture. During normal operation, the external bottom MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the VFB pin, (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 1.200V reference voltage. In a boost converter, the required inductor current is determined by the load current, V_{IN} and V_{OUT}. When the load current increases, it causes a slight decrease in VFB relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current in each channel matches the new requirement based on the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IREV, or the beginning of the next clock cycle.

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. The VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to $INTV_{CC}$.

Shutdown and Start-Up (RUN and SS Pins)

The LTC3786 can be shut down using the RUN pin. Pulling this pin below 1.28V shuts down the main control loop. Pulling this pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3786 draws only 8µA of quiescent current. Note: Do not apply load while the chip is in shutdown. The output MOSFET will be turned off during shutdown and the output load may cause excessive power dissipation in the body diode.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), as long as the maximum current into the RUN pin does not exceed 100µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. Once running, a 4.5µA current is sourced from the RUN pin allowing the user to program hysteresis using the resistor values.

The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3786 regulates the VFB voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to GND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V, the output voltage rises smoothly to its final value.

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (PLLIN/MODE Pin)

The LTC3786 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground. To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to approximately 30% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the required current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.450V.

OPERATION (Refer to the Block Diagram)

In sleep mode, much of the internal circuitry is turned off and the LTC3786 draws only 55µA of quiescent current. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse-current comparator (IREV) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation.

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3786 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3786's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to GND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to GND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 5.

A phase-locked loop (PLL) is available on the LTC3786 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3786's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input to align the turn-on of the external bottom MOSFET to the rising edge of the synchronizing signal.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

OPERATION (Refer to the Block Diagram)

The typical capture range of the LTC3786's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling).

Operation When V_{IN} > Regulated V_{OUT}

When V_{IN} rises above the regulated V_{OUT} voltage, the boost controller can behave differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the loop keeps the top MOSFET on continuously once V_{IN} rises above V_{OUT}. The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage. (The amount of current the charge pump can deliver is characterized by two curves in the Typical Performance Characteristics section.)

In pulse-skipping mode, if V_{IN} is between 100% and 110% of the regulated V_{OUT} voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set to approximately 4% of the maximum ILIM current. If the controller is programmed to Burst Mode operation under this same V_{IN} window, then TG remains off regardless of the inductor current.

If V_{IN} rises above 110% of the regulated V_{OUT} voltage in any mode, the controller turns on TG regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the chip is asleep. With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. To prevent excessive power dissipation across the body diode of the top MOSFET in this situation, the chip can be switched over to forced continuous or pulse-skipping mode to enable the charge pump, or a Schottky diode can also be placed in parallel to the top MOSFET.

Power Good

The PGOOD pin is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.2V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the VFB pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max).

Operation at Low SENSE Pin Common Mode Voltage

The current comparator in the LTC3786 is powered directly from the $SENSE^+$ pin. This enables the common mode voltage of $SENSE^+$ and $SENSE^-$ pins to operate as low as 2.5V, which is below the $INTV_{CC}$ UVLO threshold. The figure on the first page shows a typical application when the controller's VBIAS is powered from V_{OUT} while V_{IN} supply can go as low as 2.5V. If the voltage on $SENSE^+$ drops below 2.5V, the SS pin will be held low. When the $SENSE^+$ voltage returns to the normal operating range, the SS pin will be released, initiating a new soft-start cycle.

BOOST Supply Refresh and Internal Charge Pump

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations to keep the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 100µs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET to be fully enhanced instead of waiting for the initial few cycles to charge the bootstrap capacitor, C_B. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 85µA.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3786 application circuit. LTC3786 can be configured to use either inductor DCR (DC resistance) sensing or a discrete sense resistor (R_{SENSE}) for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 2.5V to 38V. The current sense resistor is normally placed at the input of the boost controller in series with the inductor.

The SENSE+ pin also provides power to the current comparator. It draws ~200µA during normal operation. There is a small base current of less than 1µA that flows into the SENSE– pin. The high impedance SENSE– input to the current comparators allows accurate DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC3786, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

Sense Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ of 75mV. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, I_{MAX}, equal to the peak value

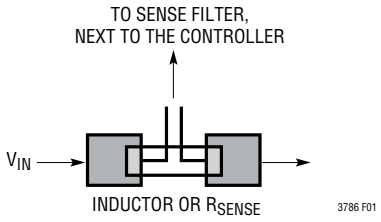
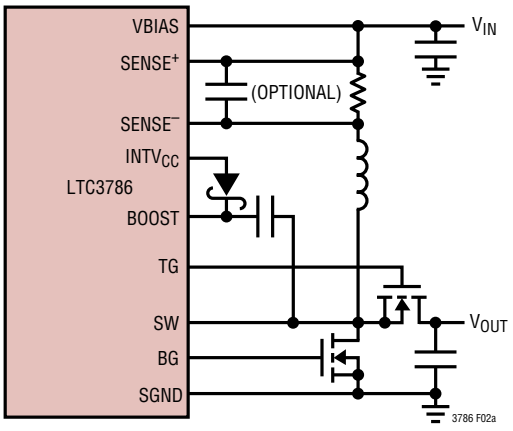
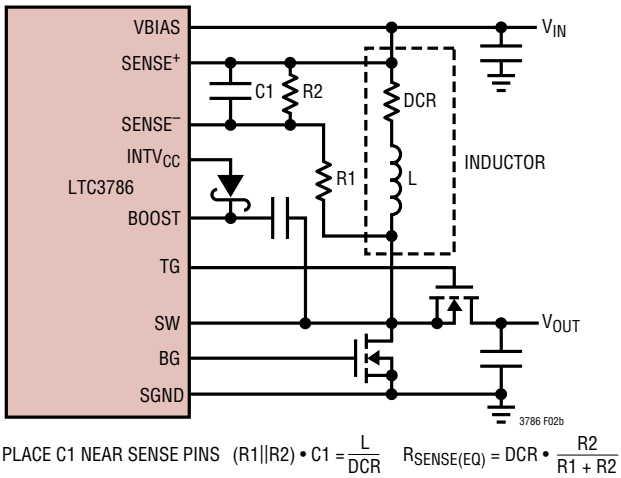


Figure 1. Sense Lines Placement with Inductor or Sense Resistor



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

APPLICATIONS INFORMATION

less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

When using the controller in low V_{IN} and very high voltage output applications, the maximum inductor current and correspondingly the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for boost regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current level depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3786 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturer's data sheets for detailed information.

Using the inductor ripple current value from the inductor value calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE– pin's ±1µA current.

The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D};\ R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at V_{IN} = 1/2 V_{OUT}:

$$P_{LOSS\_R1} = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

APPLICATIONS INFORMATION

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency, the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at $V_{IN} = 1/2\ V_{OUT}$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC3786: one N-channel MOSFET for the bottom (main) switch, and one N-channel MOSFET for the top (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.4V. Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturer's data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

If the maximum output current is $I_{OUT(MAX)}$ and each channel takes one-half of the total output current, the MOSFET power dissipations in each channel at maximum output current are given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V_{IN}^2} \bullet I_{OUT(MAX)}^2 \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{OUT}}{V_{IN}} \bullet I_{OUT(MAX)}^2 \bullet (1+\delta) \bullet R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ (approximately 1Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. The constant k, which

APPLICATIONS INFORMATION

accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low or during overvoltage when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The input capacitor, C_{IN}, voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of the C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage.

The steady ripple voltage due to charging and discharging the bulk capacitance in a single phase boost converter is given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet \left(V_{OUT} - V_{IN(MIN)}\right)}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (i.e., OS-CON and POSCAP).

Setting Output Voltage

The LTC3786 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 1.2V\left(1 + \frac{R_B}{R_A}\right)$$

Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also, keep the VFB node as small as possible to avoid noise pickup.

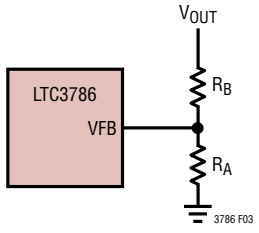


Figure 3. Setting Output Voltage

APPLICATIONS INFORMATION

Soft-Start (SS Pin)

The start-up of the V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC3786 regulates the VFB pin voltage to the voltage on the SS pin instead of 1.2V.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 4. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC3786 will regulate the V_{FB} pin (and hence, V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from V_{IN} to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

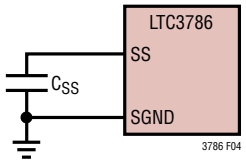


Figure 4. Using the SS Pin to Program Soft-Start

$INTV_{CC}$ Regulator

The LTC3786 features an internal P-channel low dropout linear regulator (LDO) that supplies power at the $INTV_{CC}$ pin from the VBIAS supply pin. $INTV_{CC}$ powers the gate drivers and much of the LTC3786's internal circuitry. The VBIAS LDO regulates $INTV_{CC}$ to 5.4V. It can supply at least 50mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3786 to be exceeded. The power dissipation for the IC is equal to VBIAS • I_{INTVCC}. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, at 70°C ambient temperature, the LTC3786 $INTV_{CC}$ current is limited to less than 20mA in the QFN package from a 40V supply:

$$T_J = 70°C + (20mA)(40V)(68°C/W) = 125°C$$

In an MSOP package, the $INTV_{CC}$ current is limited to less than 34mA from a 40V supply:

$$T_J = 70°C + (34mA)(40V)(40°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE = $INTV_{CC}$) at maximum VBIAS.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Block Diagram is charged though external diode, D_B, from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{OUT(MAX)}$.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. Pay close attention to the reverse leakage at high temperatures where it generally increases substantially.

The topside MOSFET driver includes an internal charge pump that delivers current to the bootstrap capacitor from the BOOST pin. This charge current maintains the bias voltage required to keep the top MOSFET on continuously during dropout/overvoltage conditions. The Schottky/silicon diode selected for the topside driver should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

A leaky diode D_B in the boost converter can not only prevent the top MOSFET from fully turning on but it can also completely discharge the bootstrap capacitor C_B and create a current path from the input voltage to the BOOST pin to $INTV_{CC}$. This can cause $INTV_{CC}$ to rise if the diode leakage exceeds the current consumption on $INTV_{CC}$. This is particularly a concern in Burst Mode operation where the load on $INTV_{CC}$ can be very small. The external Schottky or silicon diode should be carefully chosen such that $INTV_{CC}$ never gets charged up much higher than its normal regulation voltage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on-chip (such as an $INTV_{CC}$ short to ground), the overtemperature shutdown circuitry will shut down the LTC3786. When the junction temperature exceeds approximately 170°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO, causing the $INTV_{CC}$ supply to collapse and effectively shut down the entire LTC3786 chip. Once the junction temperature drops back to approximately 155°C, the $INTV_{CC}$ LDO turns back on. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Since the shutdown may occur at full load, beware that the load current won't result in high power dissipation in the body diodes of the top MOSFET. In this case, PGOOD output may be used to turn the system load off.

Phase-Locked Loop and Frequency Synchronization

The LTC3786 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). This allows the turn-on of the bottom MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The phase detector is an edge-sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, C_{LP}, holds the voltage at the VCO input.

Typically, the external clock (on PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Note that the LTC3786 can only be synchronized to an external clock whose frequency is within range of the LTC3786's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

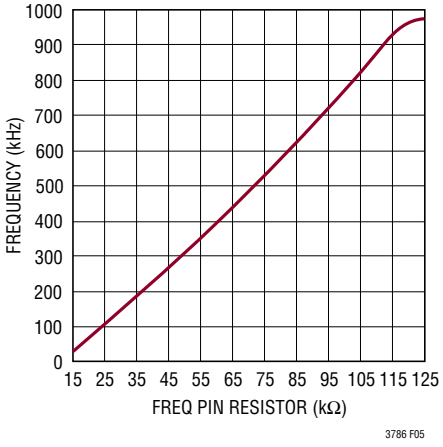


Figure 5. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

APPLICATIONS INFORMATION

Table 1 summarizes the different states in which the FREQ pin can be used.

Table 1

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3786 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit.

In forced continuous mode, if the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles but the output will continue to be regulated. More cycles will be skipped when V_{IN} increases. Once V_{IN} rises above V_{OUT}, the loop keeps the top MOSFET continuously on. The minimum on-time for the LTC3786 is approximately 110ns.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the greatest improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3786 circuits: 1) IC VBIAS current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Bottom MOSFET transition losses and 5) Body diode conduction losses.

1. The VBIAS current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. VBIAS current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

4. Transition losses apply only to the bottom MOSFET(s), and become significant only when operating at low input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\frac{V_{OUT}^3}{V_{IN}} I_{MAX} \bullet C_{RSS} \bullet f$$

5. Body diode conduction losses are more significant at higher switching frequency. During the dead time, the loss in the top MOSFETs is $I_{OUT} \bullet V_{DS}$, where V_{DS} is around 0.7V. At higher switching frequency, the dead time becomes a good percentage of switching cycle and causes the efficiency to drop.

Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} • ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Figure 8 circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PCB layout is complete and the particular output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate pulse generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V (max), V_{OUT} = 24V, $I_{OUT(MAX)}$ = 4A, $V_{SENSE(MAX)}$ = 75mV and f = 350kHz.

The inductance value is chosen first based on a 30% ripple current assumption. Tie the MODE/PLLIN pin to GND, generating 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

The largest ripple happens when V_{IN} = 1/2V_{OUT} = 12V, where the average maximum inductor is I_{MAX} = $I_{OUT(MAX)}$ • (V_{OUT}/V_{IN}) = 8A. A 6.8µH inductor will produce a 31% ripple current. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 9.25A.

APPLICATIONS INFORMATION

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{75mV}{9.25A} = 0.008\Omega$$

Choosing 1% resistors: R_A = 5k and R_B = 95.3k yields an output voltage of 24.072V.

The power dissipation on the topside MOSFET in each channel can be easily estimated. Choosing a Vishay Si7848BDP MOSFET results in: $R_{DS(ON)} = 0.012\Omega$, C_{MILLER} = 150pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{(24V - 12V)24V}{(12V)^2} \bullet (4A)^2$$
$$\bullet \left[1 + (0.005)(50°C - 25°C)\right] \bullet 0.008\Omega$$
$$+ (1.7)(24V)^3 \frac{4A}{12V}(150pF)(350kHz) = 0.7W$$

C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is:

$$I_{OUT(PEAK)} = I_{OUT(MAX)} \bullet \left(1 + \frac{RIPPLE\%}{2}\right)$$
$$= 4 \bullet \left(1 + \frac{31\%}{2}\right) = 4.62A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 23.1mV (assuming ESR dominate ripple).

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 6. Figure 7 illustrates the current waveforms present in the various branches the synchronous regulator operating in the continuous mode. Check the following in your layout:

1. Put the bottom N-channel MOSFET MBOT and the top N-channel MOSFET MTOP in one compact area with C_{OUT}.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the bottom N-channel MOSFET and the capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) source terminal of the bottom MOSFET.
3. Does the LTC3786 VFB pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground and placed close to the VFB pin. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pin? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially.
6. Keep the switching node (SW), top gate node (TG) and boost node (BOOST) away from sensitive small-signal nodes. All of these nodes have very large and fast moving signals and, therefore, should be kept on the output side of the LTC3786 and occupy a minimal PC trace area.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

APPLICATIONS INFORMATION

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold— typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pick-up at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

Reduce V_{IN} from its nominal level to verify operation with high duty cycle. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling.

An embarrassing problem, which can be missed in an otherwise properly working switching regulator results when the current sensing leads are hooked up backwards. The output voltage under this improper hook-up will still be maintained, but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

APPLICATIONS INFORMATION

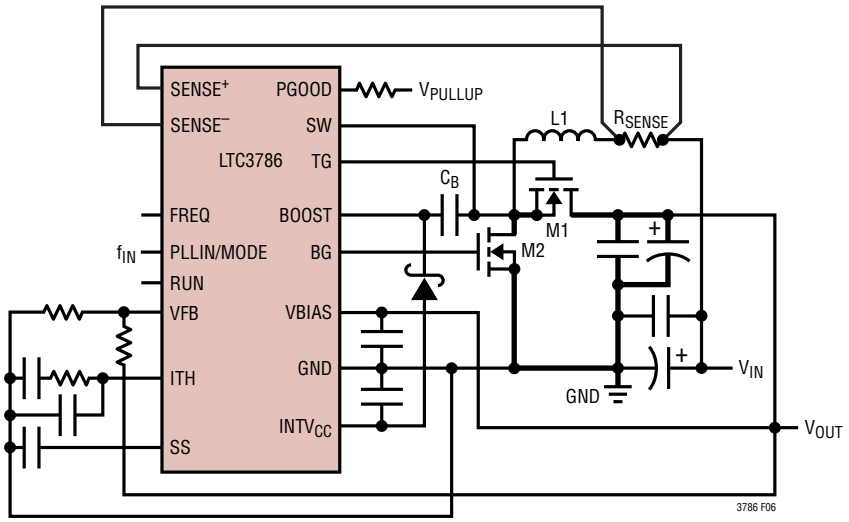


Figure 6. Recommended Printed Circuit Layout Diagram

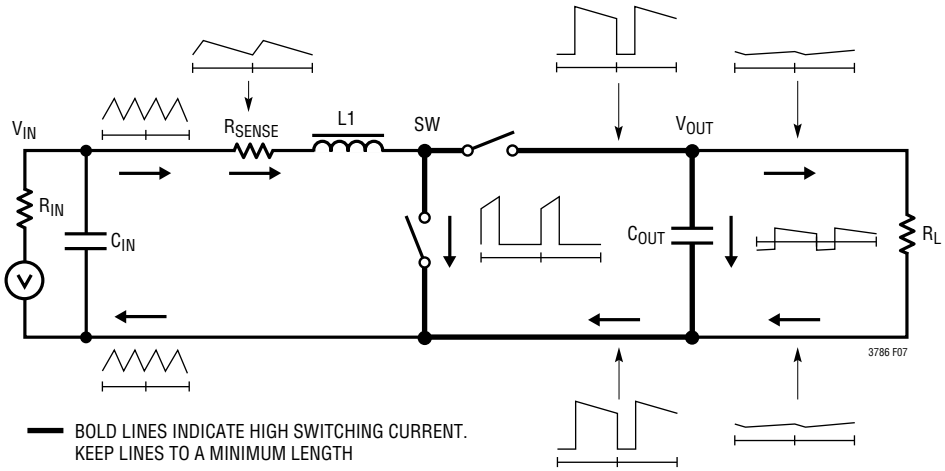
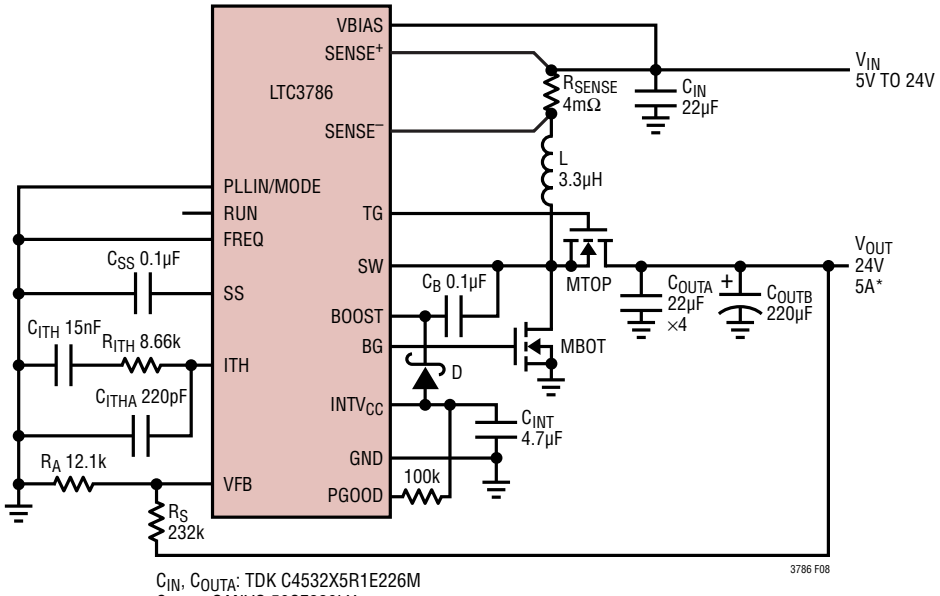


Figure 7. Branch Current Waveforms

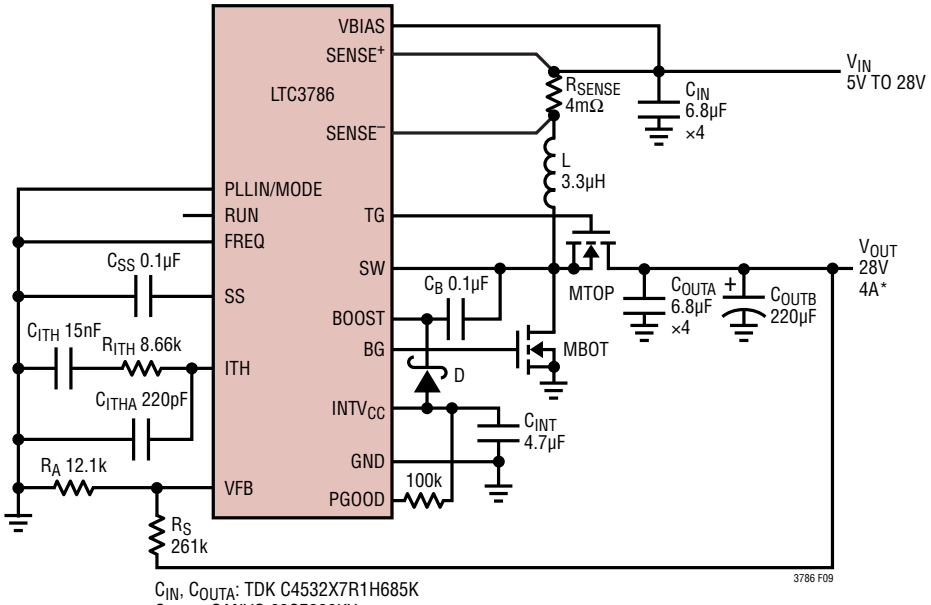
APPLICATIONS INFORMATION



C_{IN}, C_{OUTA}: TDK C4532X5R1E226M
C_{OUTB}: SANYO 50CE220LX
D: BAS140W
L: PULSE PA1494.362NL
MBOT, MTOP: RENESAS HAT2169H

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

Figure 8. High Efficiency 24V Boost Converter

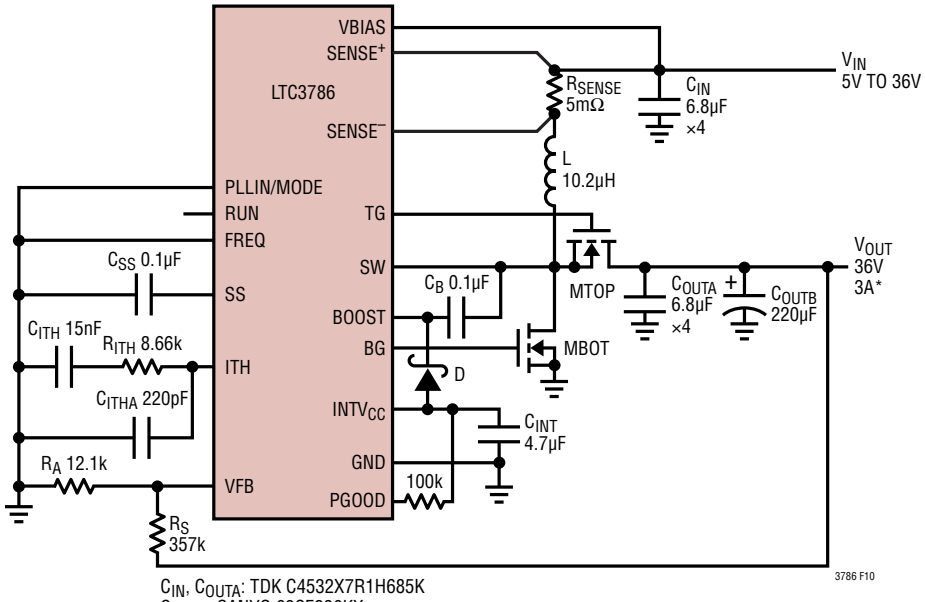


C_{IN}, C_{OUTA}: TDK C4532X7R1H685K
C_{OUTB}: SANYO 63CE220KX
D: BAS140W
L: PULSE PA1494.362NL
MBOT, MTOP: RENESAS HAT2169H

*WHEN V_{IN} < 8V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

Figure 9. High Efficiency 28V Boost Converter

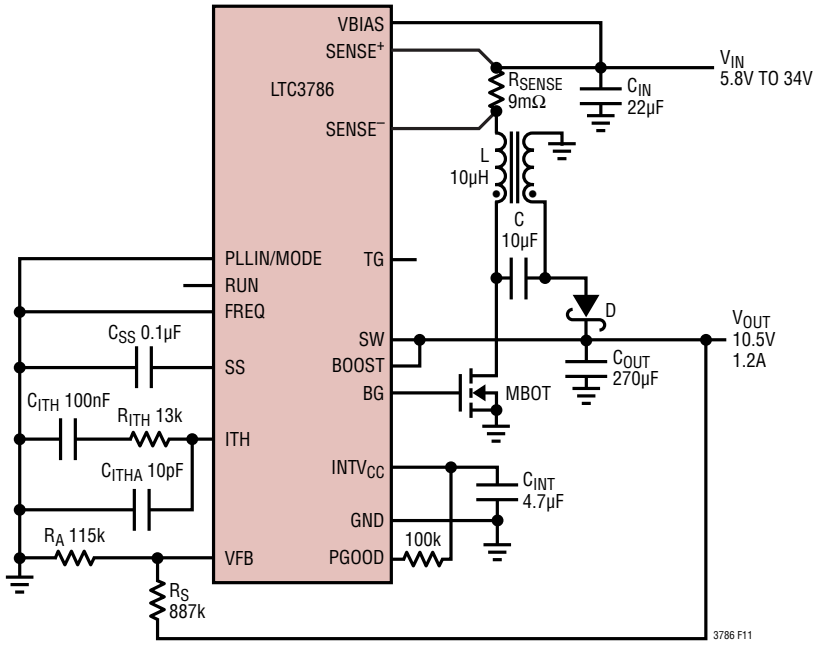
APPLICATIONS INFORMATION



C_{IN}, C_{OUTA}: TDK C4532X7R1H685K
C_{OUTB}: SANYO 63CE220KX
D: BAS170W
L: PULSE PA2050.103NL
MBOT, MTOP: RENESAS RJIC0652DPB

*WHEN V_{IN} < 9V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

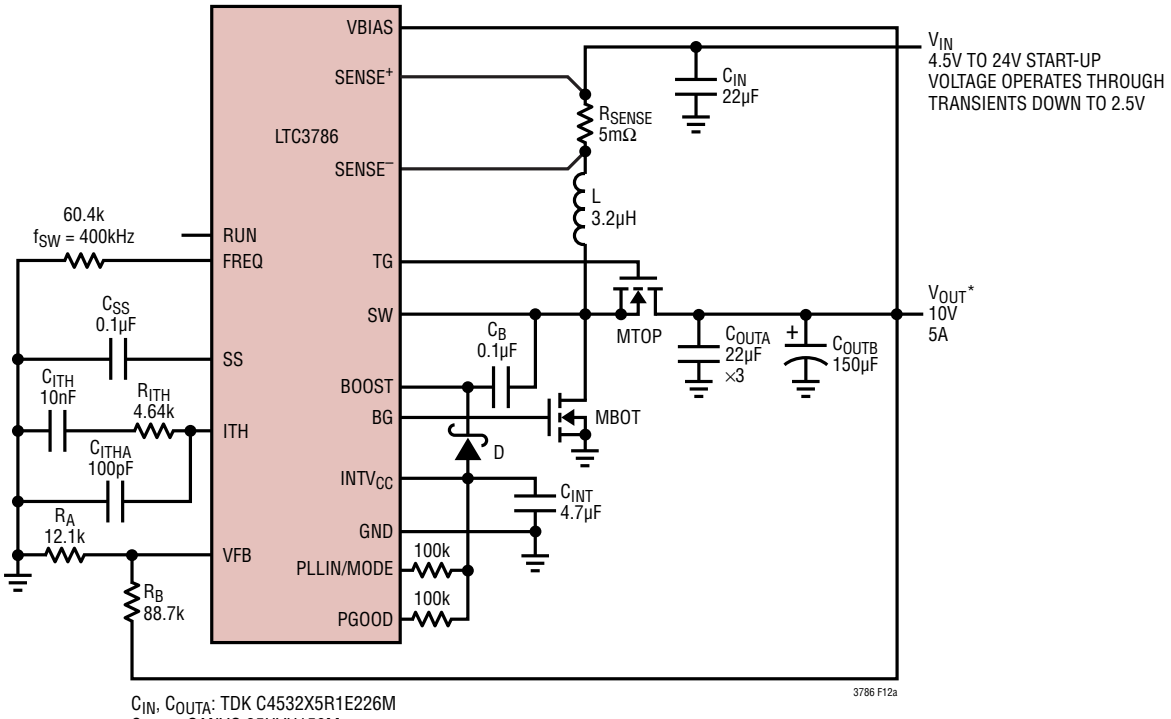
Figure 10. High Efficiency 36V Boost Converter



C_{IN}: SANYO 50CE220LX
C_{OUT}: SANYO SVPC270M
D: DIODES, INC. B360A-13-F
L: COOPER BUSSMANN DRQ125-100
MBOT: BSZ097NO4L

Figure 11. 10.5V Nonsynchronous SEPIC Converter

APPLICATIONS INFORMATION



CIN, COUTA: TDK C4532X5R1E226M
COUTB: SANYO 35HVH150M
L: SUMIDA CDEP106-3R2-88
MBOT, MTOP: RENESAS HAT2170
D: INFINEON BAS140W

*WHEN V_{IN} > 10V, V_{OUT} FOLLOWS V_{IN}.

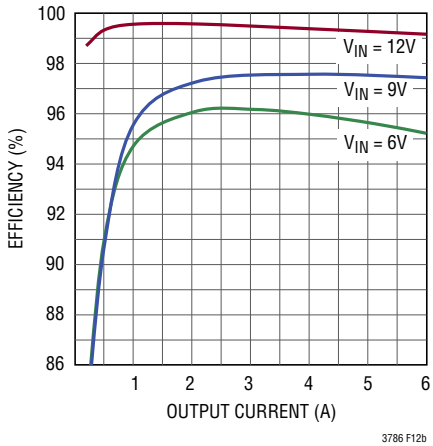
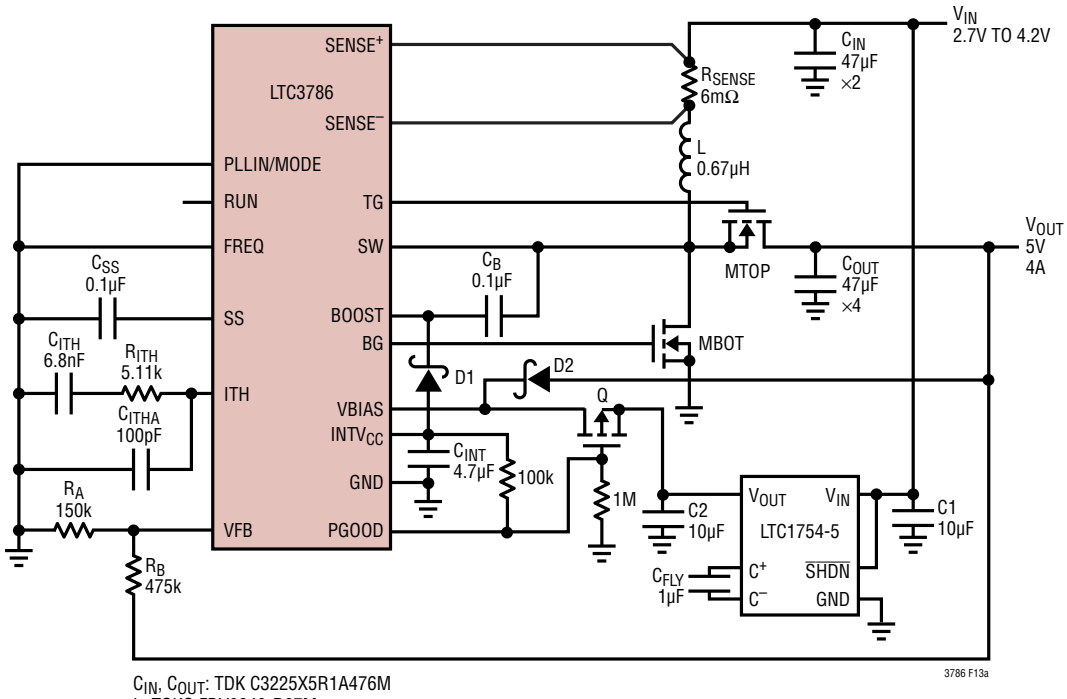


Figure 12. High Efficiency 10V Boost Converter

APPLICATIONS INFORMATION



CIN, COUT: TDK C3225X5R1A476M
L: TOKO FDV0840-R67M
MBOT, MTOP: INFINEON BSC046N02KS
Q: VISHAY SILICONIX Si1499DH
D1: INFINEON BAS140W
D2: NXP PMEG2005EJ
CFLY: MURATA GRM39X5R105K6.3AJ
C1, C2: MURATA GRM40X5R106K6.3AJ

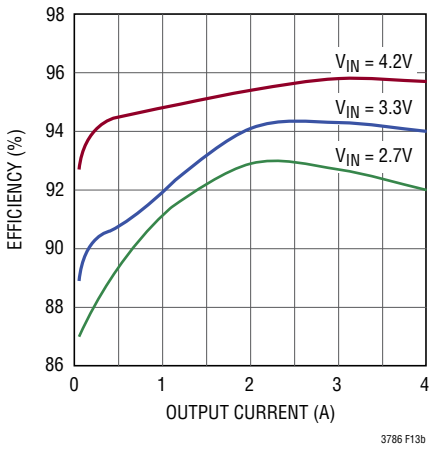
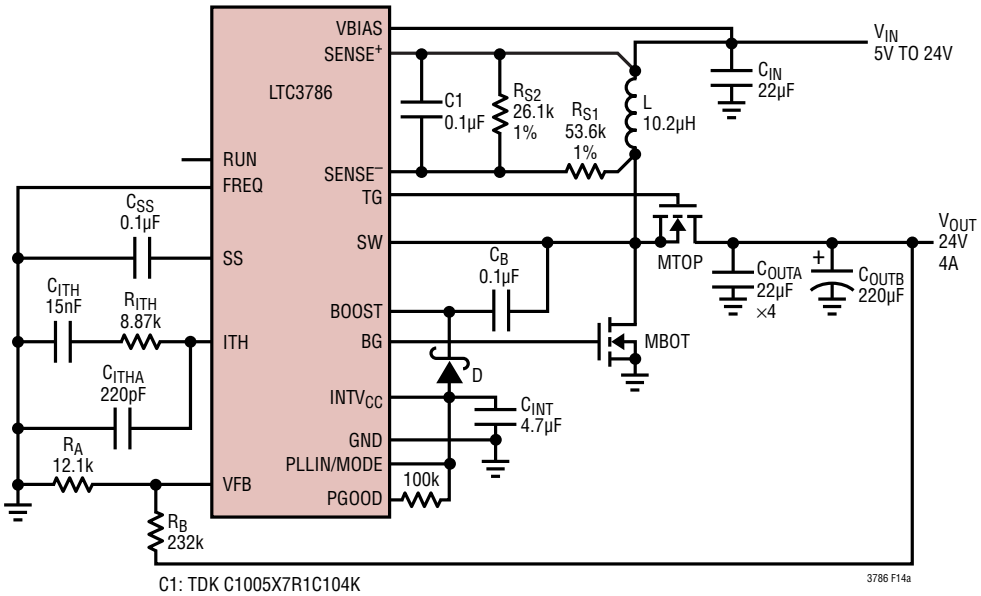


Figure 13. Low I_Q Lithium-Ion to 5V/4A Boost Converter

APPLICATIONS INFORMATION



C1: TDK C1005X7R1C104K
C_{IN}, C_{OUTA}: TDK C4532X5R1E226M
C_{OUTB}: SANYO, 50CE220AX
L: PULSE PA2050.103NL
MBOT, MTOP: RENESAS RJK0305
D: INFINEON BAS140W

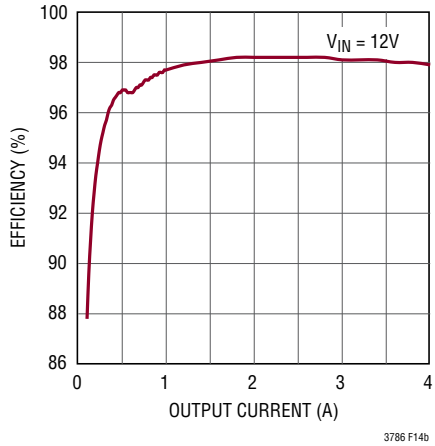
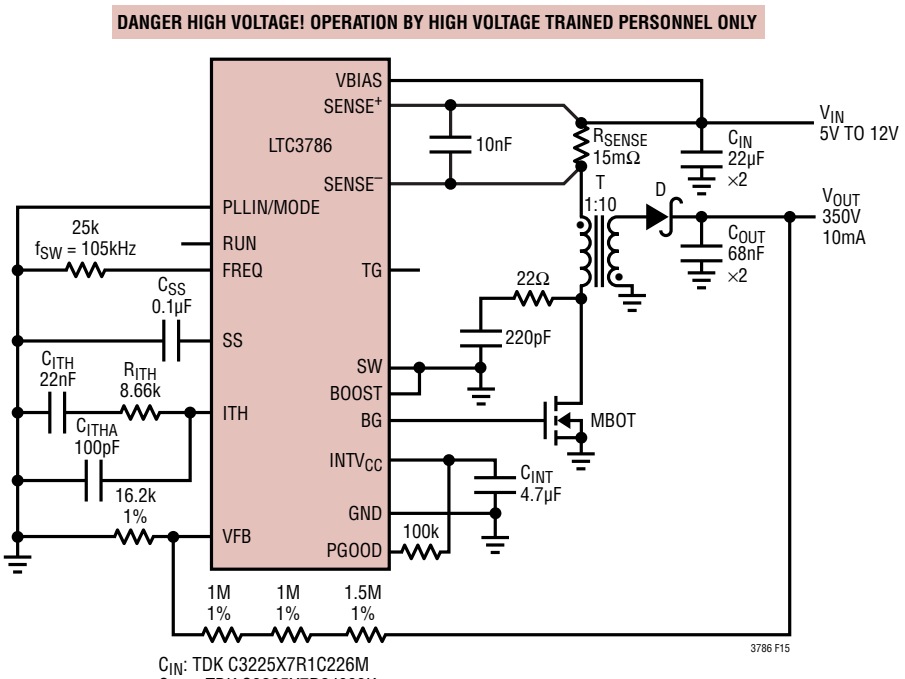


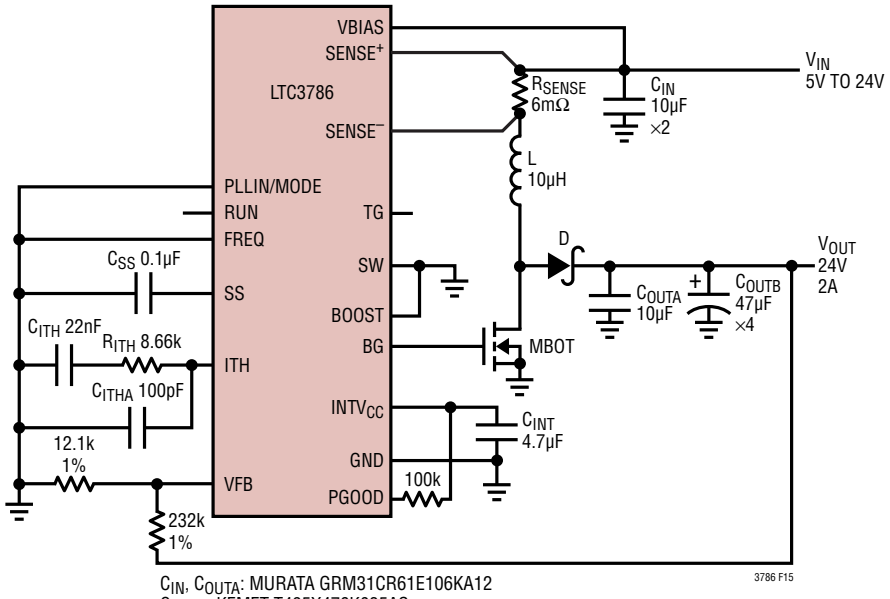
Figure 14. High Efficiency 24V Boost Converter with Inductor DCR Current Sensing

APPLICATIONS INFORMATION



C_{IN}: TDK C3225X7R1C226M
C_{OUT}: TDK C3225X7R2J683K
D: VISHAY SILICONIX GSD2004S DUAL DIODE CONNECTED IN SERIES
MBOT: VISHAY SILICONIX Si7850DP
T: TDK DCT15EFD-U44S003

Figure 15. Low I_Q High Voltage Flyback Power Supply



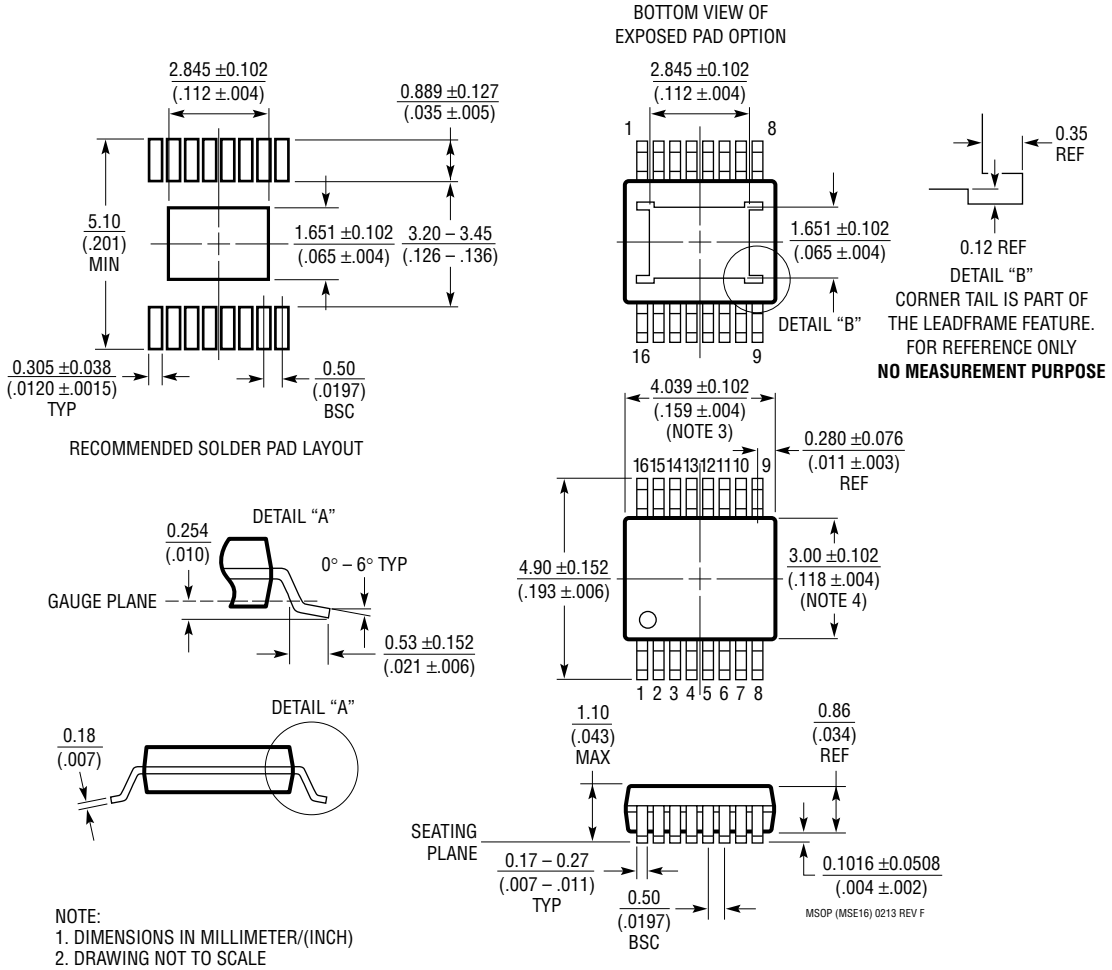
C_{IN}, C_{OUTA}: MURATA GRM31CR61E106KA12
C_{OUTB}: KEMET T495X476K035AS
D: ON SEMI MBRS340T3G
L: VISAY SILICONIX IHLP-5050FD-01 10µH
MBOT: VISHAY SILICONIX Si4840BDP

Figure 16. Low I_Q Nonsynchronous 24V/2A Boost Converter

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3786#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

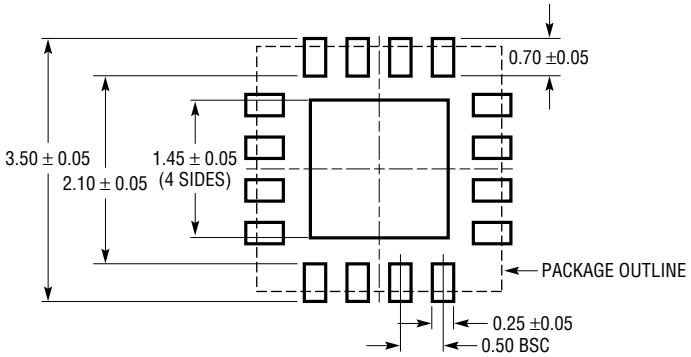


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

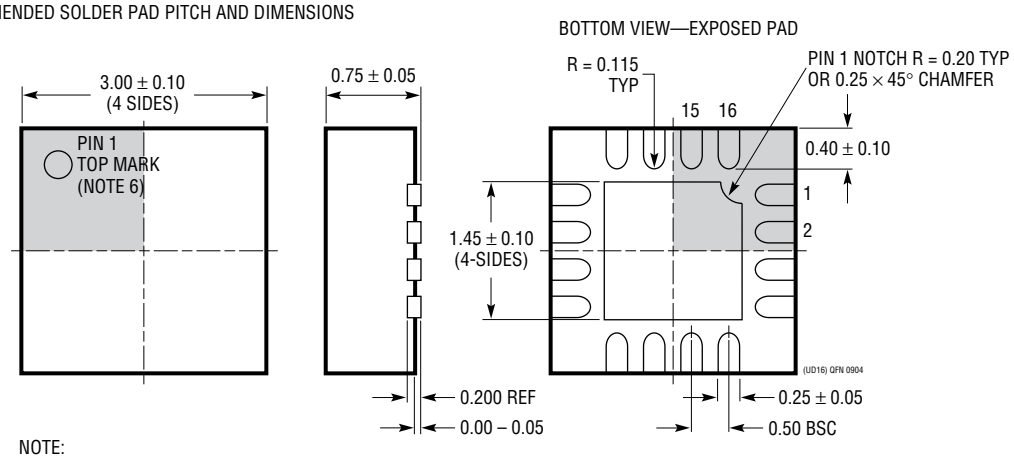
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3786#packaging for the most recent package drawings.

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



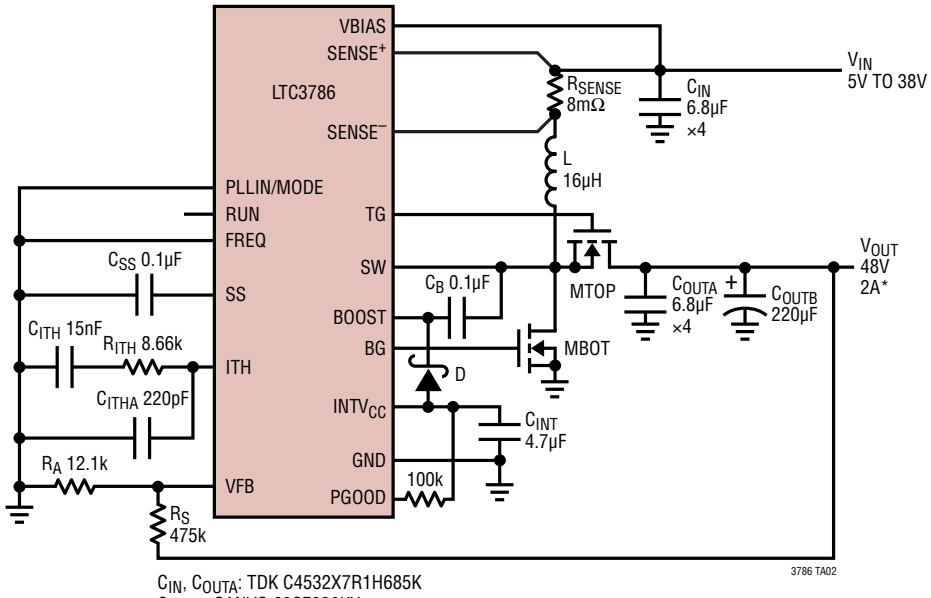
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	9/11	Updated the Topside MOSFET Driver Supply (C_B, D_B) section.	18
		Updated Figure 12.	27
B	9/16	Added H-Grade	2, 4
C	11/17	Clarified graphs G01 and G08	5
		Changed $INTV_{CC}$ to GND on G20	7
		Changed Pin 9 to Pin 8 for PLLIN/Mode pin function	8
		Changed from ($V_{OUT} \bullet V_{IN}$) to ($V_{OUT} - V_{IN}$)	15

TYPICAL APPLICATION

High Efficiency 48V Boost Converter



C_{IN}, C_{OUTA}: TDK C4532X7R1H685K
C_{OUTB}: SANYO 63CE220KX
D: BAS170W
L: PULSE PA2050.163NL
MBOT, MTOP: RENESAS RJK0652DPB

*WHEN V_{IN} < 13V, MAXIMUM LOAD CURRENT AVAILABLE IS REDUCED.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3788/LTC3788-1	Dual Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.5V after Start-up) ≤ V_{IN} ≤ 38V, V_{OUT} up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 5mm × 5mm QFN-32, SSOP-28
LTC3787	Single Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.5V after Start-up) ≤ V_{IN} ≤ 38V, V_{OUT} up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3769	60V Low I_Q Synchronous Boost Controller	4.5V (Down to 2.3V after Start-up) ≤ V_{IN} ≤ 60V, V_{OUT} up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 4mm QFN-24, TSSOP-20
LTC3784	60V Single Output, Low I_Q Multiphase Synchronous Boost Controller	4.5V (Down to 2.3V after Start-up) ≤ V_{IN} ≤ 60V, V_{OUT} up to 60V, 50kHz to 900kHz Fixed Operating Frequency, 4mm × 5mm QFN-28, SSOP-28
LTC3862/LTC3862-1	Single Output, Multiphase Current Mode Step-Up DC/DC Controller	4V ≤ V_{IN} ≤ 36V, 5V or 10V Gate Drive, 75kHz to 500kHz Fixed Operating Frequency, SSOP-24, TSSOP-24, 5mm × 5mm QFN-24
LT3757/LT3758	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V/100V, 100kHz to 1MHz Fixed Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LTC1871, LTC1871-1, LTC1871-7	Wide Input Range, No R_{SENSE} Low I_Q Boost, Flyback and SEPIC Controller	2.5V ≤ V_{IN} ≤ 36V, 50kHz to 1MHz Fixed Operating Frequency, MSOP-10
LTC3859AL	Low I_Q, Triple Output Buck/Buck/Boost Synchronous DC/DC Controller	All Outputs Remain in Regulation Through Cold Crank, 4.5V(Down to 2.5V after Start-up) ≤ V_{IN} ≤ 38V, $V_{OUT(BUCKS)}$ Up to 24V, $V_{OUT(BOOST)}$ Up to 60V, I_Q = 28µA
LTC3789	High Efficiency Synchronous 4-Switch Buck-Boost DC/DC Controller	4V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 38V, SSOP-28, 4mm × 5mm QFN-28, SSOP-28
LT8710	Synchronous SEPIC/Inverting/Boost Controller with Output Current Control	4V ≤ V_{IN} ≤ 80V, SSOP-28, TSSOP-20

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