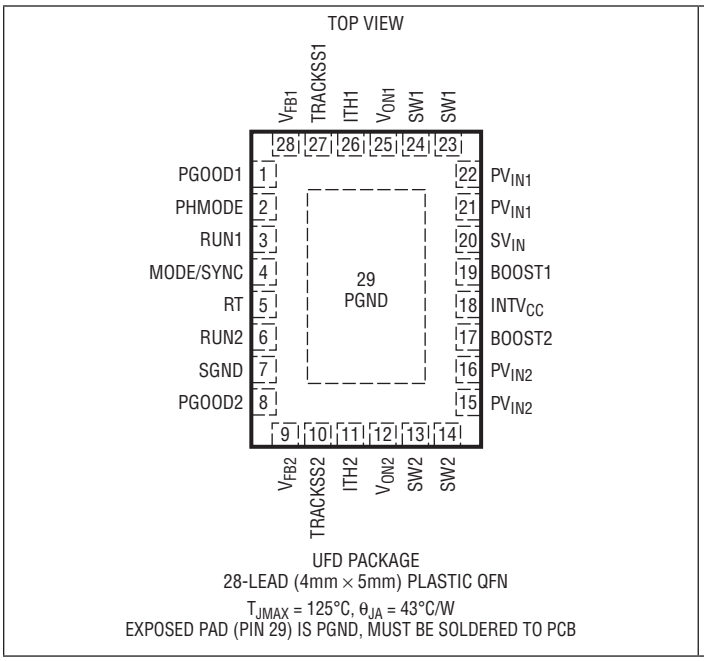
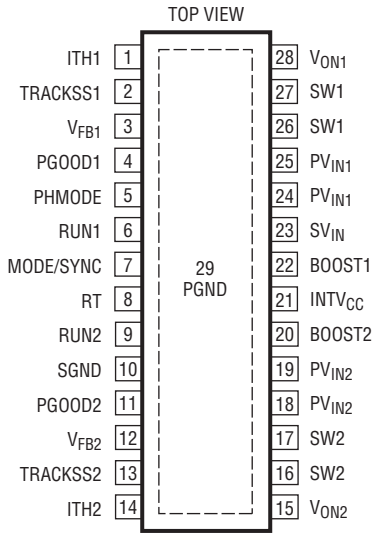
ABSOLUTE MAXIMUM RATINGS (Note 1)

PV_{IN1}, PV_{IN2}, SV_{IN} ..... –0.3V to 20V
PGOOD1, PGOOD2, V_{ON1}, V_{ON2} ..... –0.3V to 18V
BOOST1, BOOST2 ..... –0.3V to 23V
BOOST1-SW1, BOOST2-SW2 ..... –0.3V to 3.6V
$INTV_{CC}$, TRACKSS1, TRACKSS2 ..... –0.3V to 3.6V
ITH1, ITH2, RT, MODE/SYNC ..... –0.3V to $INTV_{CC}$ + 0.3V
V_{FB1}, V_{FB2}, PHMODE ..... –0.3V to $INTV_{CC}$ + 0.3V
RUN1 ..... –0.3V to SV_{IN} + 0.3V
RUN2 ..... –0.3V to 20V
Operating Junction Temperature Range
(Notes 3, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
28-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 29) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3633AEUFD-2#PBF	LTC3633AEUFD-2#TRPBF	633A2	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3633AIUFD-2#PBF	LTC3633AIUFD-2#TRPBF	633A2	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3633AEFE-2#PBF	LTC3633AEFE-2#TRPBF	LTC3633AFE-2	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3633AIFE-2#PBF	LTC3633AIFE-2#TRPBF	LTC3633AFE-2	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3633AEUFD-3#PBF	LTC3633AEUFD-3#TRPBF	633A3	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3633AIUFD-3#PBF	LTC3633AIUFD-3#TRPBF	633A3	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3633AEFE-3#PBF	LTC3633AEFE-3#TRPBF	LTC3633AFE-3	28-Lead Plastic TSSOP	–40°C to 125°C
LTC3633AIFE-3#PBF	LTC3633AIFE-3#TRPBF	LTC3633AFE-3	28-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). PV_{IN1} = PV_{IN2} = SV_{IN} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN}	Supply Range		●	3.6		20	V
	PV_{IN1} Supply Range PV_{IN2} Supply Range	 3.6V < SV_{IN} < 20V	● ●	1.5 1.5		20 20	V V
	Output Voltage Range (Note 4)	LTC3633A-2, V_{ON} = V_{OUT} LTC3633A-3, V_{ON} = V_{OUT}		0.6 1.5		6 12	V V
I_Q	Input DC Supply Current (PV_{IN1} + PV_{IN2} + SV_{IN}) Both Channels Active (Note 5) Sleep Current Shutdown	 MODE = 0V MODE = $INTV_{CC}$, V_{FB1}, V_{FB2} > 0.6 RUN1 = RUN2 = 0V			 1.3 500 13		 mA µA µA
V_{FB}	Feedback Reference Voltage		●	0.594	0.6	0.606	V
ΔV_{LINE_REG}	Reference Voltage Line Regulation	PV_{IN} = 3.6V to 20V			0.002		%/V
ΔV_{LOAD_REG}	Output Voltage Load Regulation	ITH = 0.8V to 1.6V			0.05		%
I_{FB}	Feedback Pin Input Current					±30	nA
$g_{m(EA)}$	Error Amplifier Transconductance	ITH = 1.2V			1.8		mS
t_{ON}	Minimum On Time	V_{ON} = 0.6V, PV_{IN} = 4V			20		ns
t_{OFF}	Minimum Off Time	PV_{IN} = 6V			45		ns
f_{OSC}	Oscillator Frequency	V_{RT} = $INTV_{CC}$ RT = 162k RT = 80.6k		1.4 1.7 3.4	2 2 4	2.6 2.3 4.6	MHz MHz MHz
I_{LIM}	Positive Valley Switch Current Limit			2.6	3.5	4.5	A
	Negative Inductor Valley Current Limit				–2		A
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance				130 65		mΩ mΩ
$I_{SW(LKG)}$	Switch Leakage Current	PV_{IN} = 20V, V_{RUN} = 0V			0.01	±1	µA
V_{VIN-OV}	V_{IN} Overvoltage Lockout Threshold	PV_{IN} Rising PV_{IN} Falling		 20.3	22.5 21.5	 22.5	V V
	$INTV_{CC}$ Voltage	3.6V < SV_{IN} < 20V, 0mA Load		3.1	3.3	3.5	V
	$INTV_{CC}$ Load Regulation	0mA to 50mA Load, SV_{IN} = 4V to 20V			1.3		%
	RUN Threshold Rising RUN Threshold Falling		● ●	1.18 0.98	1.22 1.01	1.26 1.04	V V
	RUN Leakage Current				0	±3	µA
	PGOOD Good-to-Bad Threshold	V_{FB} Rising V_{FB} Falling			8 –8	10 –10	% %
	PGOOD Bad-to-Good Threshold	V_{FB} Rising V_{FB} Falling		–3 3	–5 5		% %
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			20		Ω
t_{PGOOD}	Power Good Filter Time			20	40		µs
t_{SS}	Internal Soft-Start Time	10% to 90% Rise Time			400	700	µs
	V_{FB} During Tracking	TRACKSS = 0.3V		0.28	0.3	0.315	V
$I_{TRACKSS}$	TRACKSS Pull-Up Current				1.4		µA

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). PV_{IN1} = PV_{IN2} = SV_{IN} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PHMODE}	PHMODE Threshold Voltage	PHMODE V_{IH} PHMODE V_{IL}		1		 0.3	V V
$V_{MODE/SYNC}$	MODE/SYNC Threshold Voltage	MODE V_{IH} MODE V_{IL}		1		 0.4	V V
	SYNC Threshold Voltage	SYNC V_{IH}		0.95			V
I_{MODE}	MODE/SYNC Input Current	MODE = 0V MODE = $INTV_{CC}$			1.5 –1.5		µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3633A-2/LTC3633A-3 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3633AE-2/ LTC3633AE-3 is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3633AI-2/ LTC3633AI-3 is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Output voltages outside the specified range are not optimized for controlled on-time operation. Refer to the Applications Information section for further discussions related to the output voltage range.

Note 5: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

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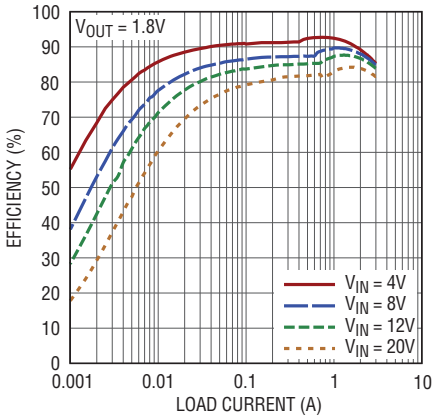
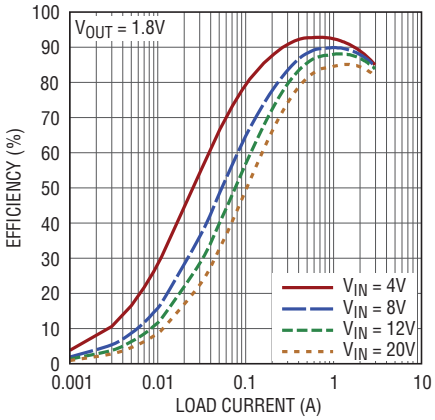
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, PV_{IN1} = PV_{IN2} = SV_{IN} = 12V, f_{SW} = 1MHz, L = 1µH unless otherwise noted.

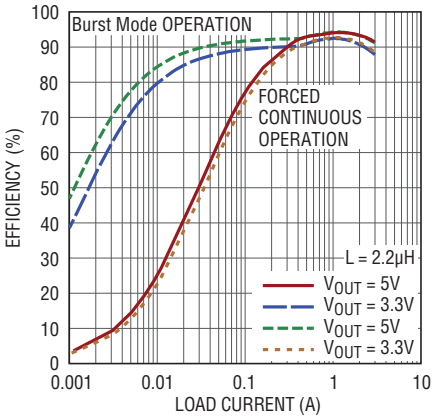
Efficiency vs Load Current Burst Mode Operation



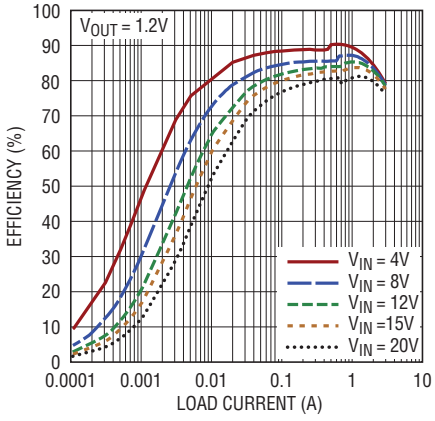
Efficiency vs Load Current Forced Continuous Mode Operation



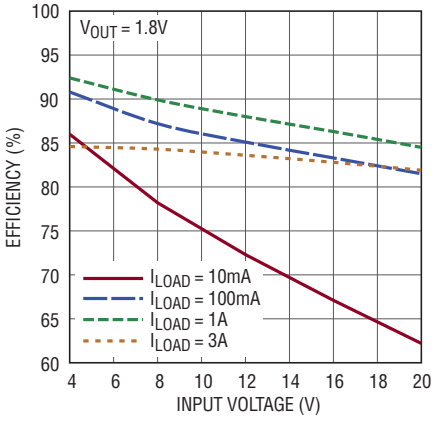
Efficiency vs Load Current



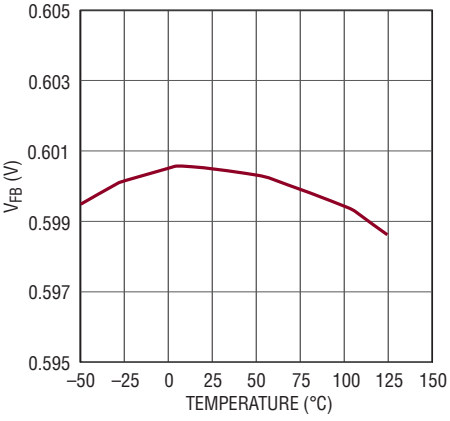
Efficiency vs Load Current Burst Mode Operation



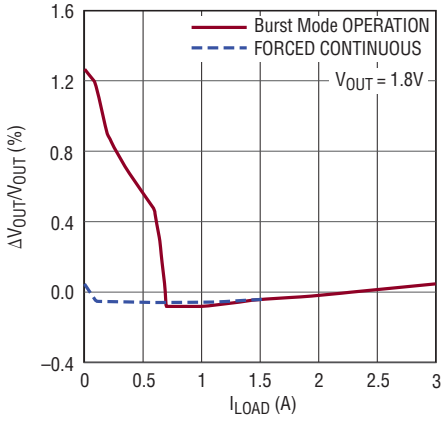
Efficiency vs Input Voltage Burst Mode Operation



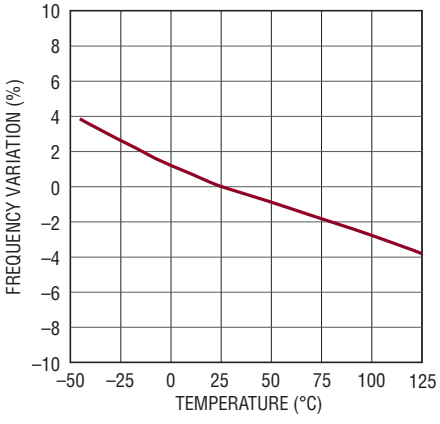
Reference Voltage vs Temperature



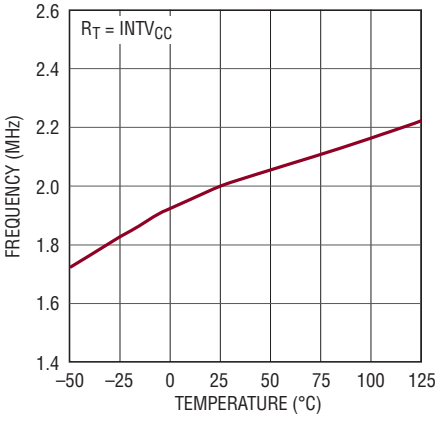
Load Regulation



Oscillator Frequency vs Temperature



Oscillator Internal Set Frequency vs Temperature



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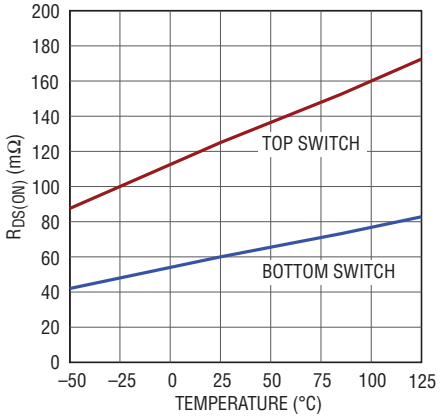
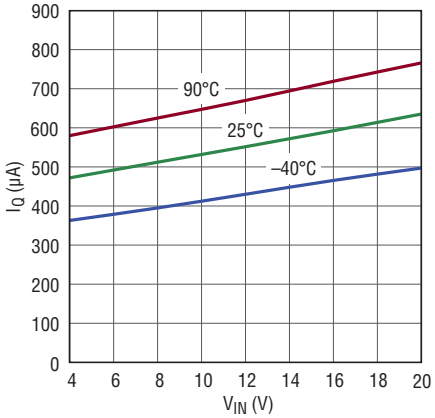
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, PV_{IN1} = PV_{IN2} = SV_{IN} = 12V, f_{SW} = 1MHz, L = 1µH unless otherwise noted.

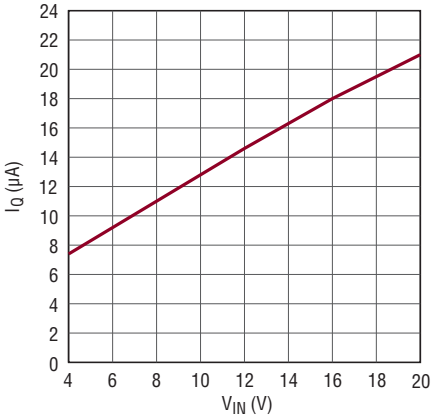
Internal MOSFET $R_{DS(ON)}$ vs Temperature



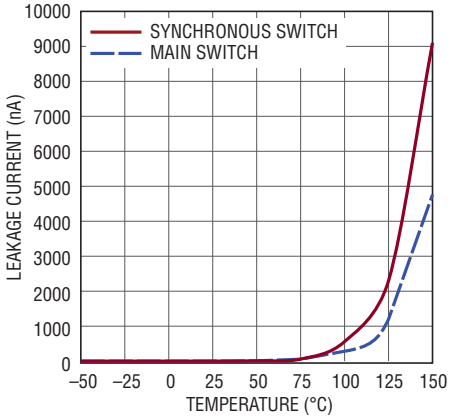
Quiescent Current vs V_{IN} Burst Mode Operation



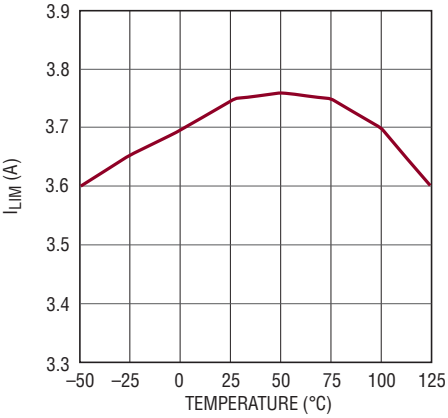
Shutdown Current vs V_{IN}



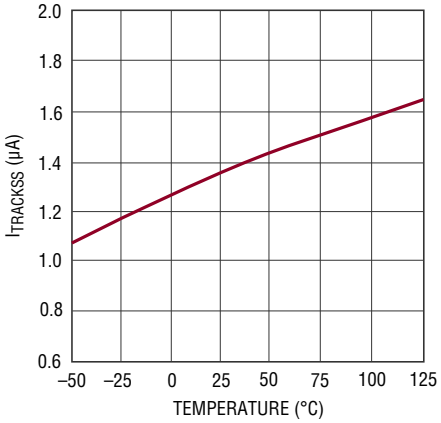
Switch Leakage vs Temperature



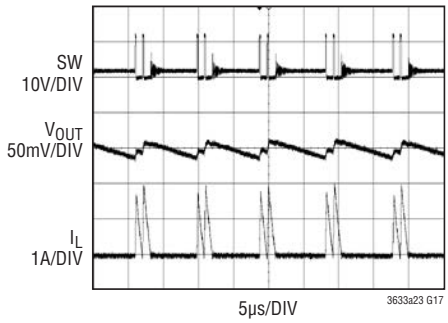
Valley Current Limit vs Temperature



TRACKSS Pull-Up Current vs Temperature

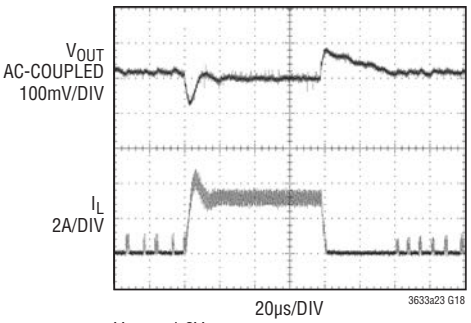


Burst Mode Operation



V_{OUT} = 1.8V
I_{LOAD} = 100mA

Load Step



V_{OUT} = 1.8V
I_{LOAD} = 100mA to 3A
C_{ITH} = 220pF
R_{ITH} = 13kΩ

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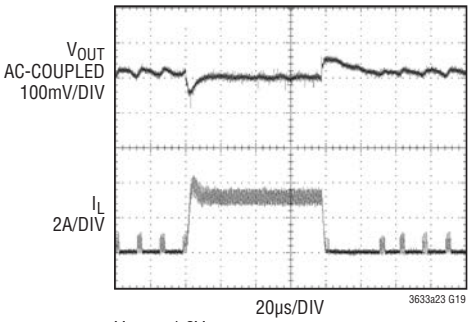
TYPICAL PERFORMANCE CHARACTERISTICS

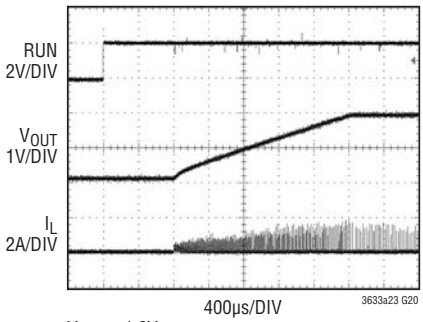
T_J = 25°C, PV_{IN1} = PV_{IN2} = SV_{IN} = 12V, f_{SW} = 1MHz, L = 1µH unless otherwise noted.

Load Step (Internal Compensation)



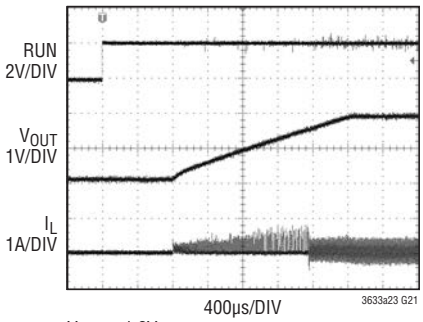
V_{OUT} = 1.8V
I_{LOAD} = 100mA to 3A
ITH = $INTV_{CC}$

Start-Up (Burst Mode Operation)



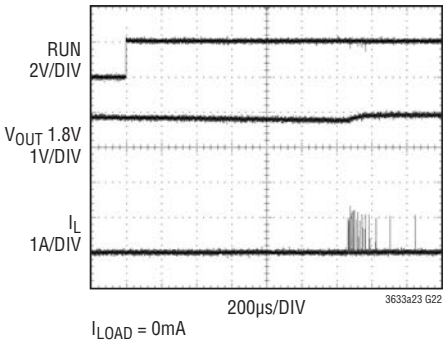
V_{OUT} = 1.8V
C_{SS} = 4.7nF
I_{LOAD} = 150mA

Start-Up (Forced Continuous Mode)



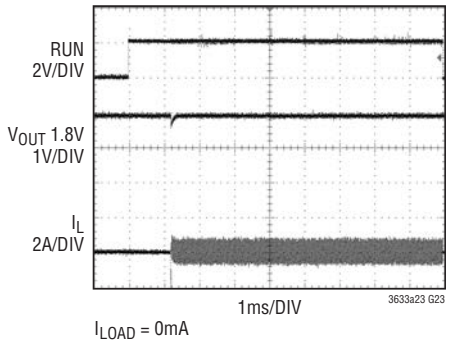
V_{OUT} = 1.8V
C_{SS} = 4.7nF
I_{LOAD} = 150mA

Start-Up into Prebiased Output (Burst Mode Operation)



I_{LOAD} = 0mA

Start-Up into Prebiased Output (Forced Continuous Mode)



I_{LOAD} = 0mA

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PIN FUNCTIONS (QFN/TSSOP)

PGOOD1 (Pin 1/Pin 4): Channel 1 Open-Drain Power Good Output Pin. PGOOD1 is pulled to ground when the voltage on the V_{FB1} pin is not within ±8% (typical) of the internal 0.6V reference. PGOOD1 becomes high impedance once the V_{FB1} pin returns to within ±5% (typical) of the internal reference.

PHMODE (Pin 2/Pin 5): Phase Select Input. Tie this pin to ground to force both channels to switch in phase. Tie this pin to $INTV_{CC}$ to force both channels to switch 180° out of phase. Do not float this pin.

RUN1 (Pin 3/Pin 6): Channel 1 Regulator Enable Pin. Enables channel 1 operation by tying RUN1 above 1.22V. Tying it below 1V places channel 1 into shutdown. Do not float this pin.

MODE/SYNC (Pin 4/Pin 7): Mode Select and External Synchronization Input. Tie this pin to ground to force continuous synchronous operation at all output loads. Floating this pin or tying it to $INTV_{CC}$ enables high efficiency Burst Mode operation at light loads. Drive this pin with a clock to synchronize the LTC3633A-2 switching. An internal phase-locked loop will force the bottom power NMOS's turn on signal to be synchronized with the rising edge of the CLKIN signal. When this pin is driven with a clock, forced continuous mode is automatically selected.

RT (Pin 5/Pin 8): Oscillator Frequency Program Pin. Connect an external resistor (between 80k to 640k) from this pin to SGND in order to program the frequency from 500kHz to 4MHz. When RT is tied to $INTV_{CC}$, the switching frequency will default to 2MHz.

RUN2 (Pin 6/Pin 9): Channel 2 Regulator Enable Pin. Enables channel 2 operation by tying RUN2 above 1.22V. Tying it below 1V places channel 2 into shutdown. Do not float this pin.

SGND (Pin 7/Pin 10): Signal Ground Pin. This pin should have a low noise connection to reference ground. The feedback resistor network, external compensation network, and RT resistor should be connected to this ground.

PGOOD2 (Pin 8/Pin 11): Channel 2 Open-Drain Power Good Output Pin. PGOOD2 is pulled to ground when the voltage on the V_{FB2} pin is not within ±8% (typical) of the internal 0.6V reference. PGOOD2 becomes high impedance once the V_{FB2} pin returns to within ±5% (typical) of the internal reference.

V_{FB2} (Pin 9/Pin 12): Channel 2 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.

TRACKSS2 (Pin 10/Pin 13): Output Tracking and Soft-Start Input Pin for Channel 2. Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The LTC3633A-2 will servo the FB pin to the TRACK voltage under this condition. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull up current from $INTV_{CC}$ allows a soft start function to be implemented by connecting a capacitor between this pin and SGND.

ITH2 (Pin 11/Pin 14): Channel 2 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

V_{ON2} (Pin 12/Pin 15): On-Time Voltage Input for Channel 2. This pin sets the voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT2} when V_{OUT2} is within the V_{ON2} sense range (0.6V – 6V for LTC3633A-2, 1.5V – 12V for LTC3633A-3). When V_{OUT2} is outside the V_{ON2} sense range, the switching frequency may deviate from the programmed frequency. The pin impedance is nominally 140kΩ.

SW2 (Pins 13, 14/Pins 16, 17): Channel 2 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PV_{IN}.

PV_{IN2} (Pins 15, 16/Pins 18, 19): Power Supply Input for Channel 2. Input voltage to the on chip power MOSFETs on channel 2. This input is capable of operating from a different supply voltage than PV_{IN1}.

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PIN FUNCTIONS (QFN/TSSOP)

BOOST2 (Pin 17/Pin 20): Boosted Floating Driver Supply for Channel 2. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to PV_{IN}+$INTV_{CC}$.

$INTV_{CC}$ (Pin 18/Pin 21): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. The internal regulator is disabled when both channel 1 and channel 2 are disabled with the RUN1/RUN2 inputs. Decouple this pin to power ground with a minimum of 1µF low ESR ceramic capacitor.

BOOST1 (Pin 19/Pin 22): Boosted Floating Driver Supply for Channel 1. The (+) terminal of the bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from a diode voltage drop below $INTV_{CC}$ up to PV_{IN} + $INTV_{CC}$.

SV_{IN} (Pin 20/Pin 23): Signal Input Supply. This pin powers the internal control circuitry. The internal LDO for $INTV_{CC}$ is powered from this pin.

PV_{IN1} (Pins 21, 22/Pins 24, 25): Power Supply Input for Channel 1. Input voltage to the on chip power MOSFETs on channel 1.

SW1 (Pins 23,24/Pins 26, 27): Channel 1 Switch Node Connection to External Inductor. Voltage swing of SW is from a diode voltage drop below ground to PV_{IN}.

V_{ON1} (Pin 25/Pin 28): On-Time Voltage Input for Channel 1. This pin sets the voltage trip point for the on-time comparator. Tying this pin to the regulated output voltage makes the on-time proportional to V_{OUT1} when V_{OUT1} is within the V_{ON1} sense range (0.6V – 6V for LTC3633A-2, 1.5V – 12V for LTC3633A-3). When V_{OUT} is outside the V_{ON} sense range, the switching frequency may deviate from the programmed frequency. The pin impedance is nominally 140kΩ.

ITH1 (Pin 26/Pin 1): Channel 1 Error Amplifier Output and Switching Regulator Compensation Pin. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

TRACKSS1 (Pin 27/Pin 2): Output Tracking and Soft-Start Input Pin for Channel 1. Forcing a voltage below 0.6V on this pin bypasses the internal reference input to the error amplifier. The LTC3633A-2 will servo the FB pin to the TRACK voltage. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA pull up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting a capacitor between this pin and SGND.

V_{FB1} (Pin 28/Pin 3): Channel 1 Output Feedback Voltage Pin. Input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to a resistor divider network to program the desired output voltage.

PGND (Exposed Pad Pin 29/Exposed Pad Pin 29): Power Ground Pin. The (–) terminal of the input bypass capacitor, C_{IN}, and the (–) terminal of the output capacitor, C_{OUT}, should be tied to this pin with a low impedance connection. This pin must be soldered to the PCB to provide low impedance electrical contact to power ground and good thermal contact to the PCB.

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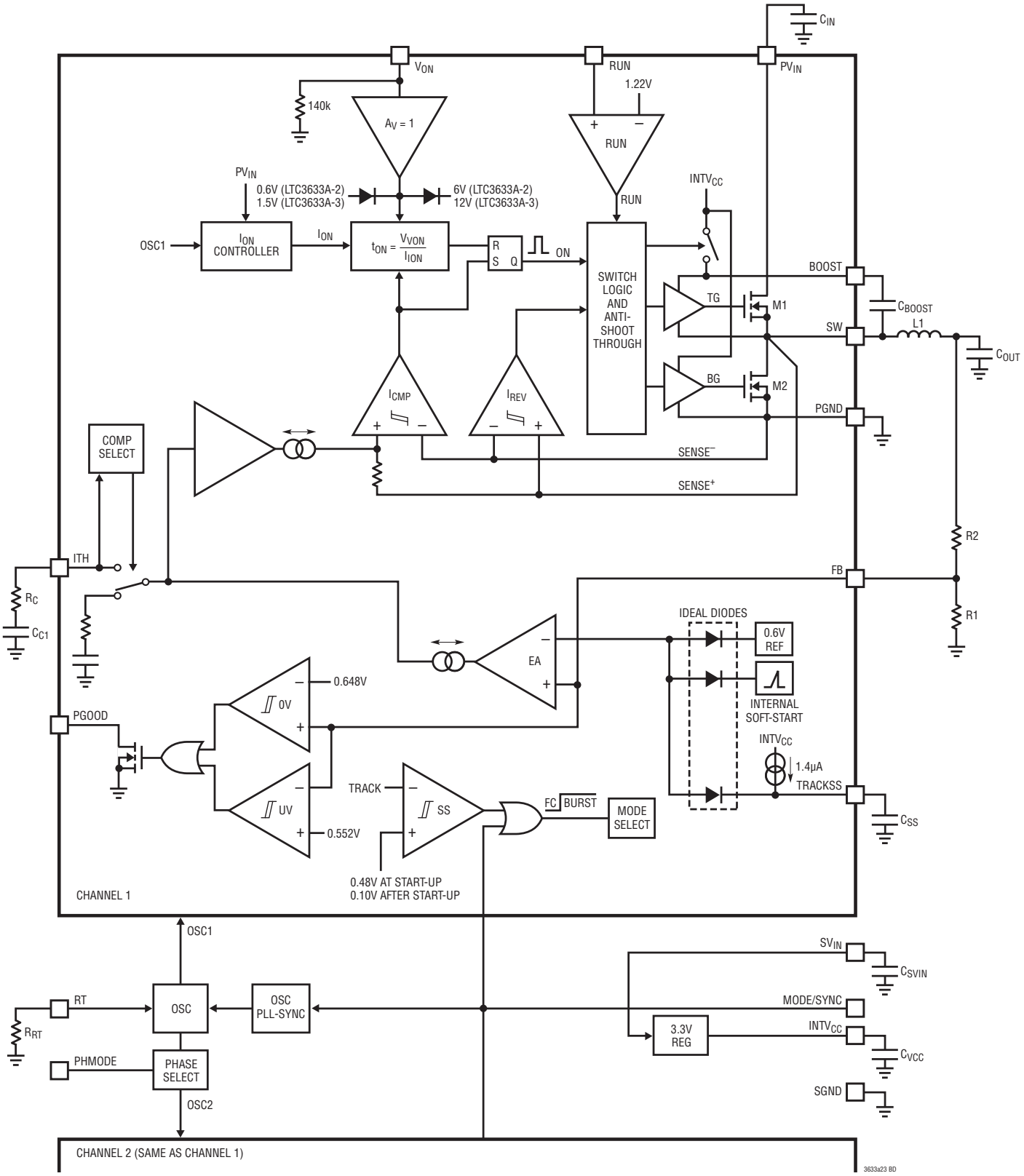
BLOCK DIAGRAM



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OPERATION

The LTC3633A-2 is a dual-channel, current mode monolithic step down regulator capable of providing 3A of output current from each channel. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a constant switching frequency. Each channel is enabled by raising the voltage on the RUN pin above 1.22V nominally.

The LTC3633A-2 has a V_{ON} sense range of 0.6V to 6V, while the LTC3633A-3 has a V_{ON} sense range of 1.5V to 12V. The following table highlights the difference between the parts in the 3633A family. Consult the LTC3633A/LTC3633A-1 data sheet for more details on specific characteristics of those products.

Table 1. LTC3633A Family Features

PART NUMBER	OUTPUT VOLTAGE SENSE RANGE	SV_{IN} INPUT	V2P5 OUTPUT	LTC3633 PIN COMPATIBLE
LTC3633A	0.6V TO 6V	NO	YES	YES
LTC3633A-1	1.5V TO 12V	NO	YES	YES
LTC3633A-2	0.6V TO 6V	YES	NO	NO
LTC3633A-3	1.5V TO 12V	YES	NO	NO

Main Control Loop

In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a fixed one-shot timer ("ON" signal in Block Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator I_{CMP} trips, thus restarting the one shot timer and initiating the next cycle. Inductor current is measured by sensing the voltage drop across the SW and PGND nodes of the bottom power MOSFET. The voltage on the ITH pin sets the comparator threshold corresponding to inductor valley current. The error amplifier EA adjusts this ITH voltage by comparing an internal 0.6V reference to the feedback signal V_{FB} derived from the output voltage. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference. The ITH voltage then rises until the average inductor current matches that of the load current.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-locked loop servos the switching regulator on-time to track the internal oscillator edge and force a constant switching frequency. A clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external source. The regulator defaults to forced continuous operation once the clock signal is applied.

At light load currents, the inductor current can drop to zero and become negative. In Burst Mode operation, a current reversal comparator (I_{REV}) detects the negative inductor current and shuts off the bottom power MOSFET, resulting in discontinuous operation and increased efficiency. Both power MOSFETs will remain off until the ITH voltage rises above the zero current level to initiate another cycle. During this time, the output capacitor supplies the load current and the part is placed into a low current sleep mode. Discontinuous mode operation is disabled by tying the MODE/SYNC pin to ground, which forces continuous synchronous operation regardless of output load current.

"Power Good" Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This condition is released once regulation within a ±5% window is achieved. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3633A-2 PGOOD falling edge includes a filter time of approximately 40µs.

PV_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient input voltage spikes, the LTC3633A-2 constantly monitors each PV_{IN} pin for an overvoltage condition. When PV_{IN} rises above 22.5V, the regulator suspends operation by shutting off both power MOSFETs on the corresponding channel. Once PV_{IN} drops below 21.5V, the regulator immediately resumes normal operation. The regulator executes its soft-start function when exiting an overvoltage condition.

Out-Of-Phase Operation

Tying the PHMODE pin high sets the SW2 falling edge to be 180° out of phase with the SW1 falling edge. There is a significant advantage to running both channels out of phase. When running the channels in phase, both top-side MOSFETs are on simultaneously, causing large current pulses to be drawn from the input capacitor and supply at the same time.

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OPERATION

When running the LTC3633A-2 channels out of phase, the large current pulses are interleaved, effectively reducing the amount of time the pulses overlap. Thus, the total RMS input current is decreased, which both relaxes the capacitance requirements for the input bypass capacitors and reduces the voltage noise on the supply line.

One potential disadvantage to this configuration occurs when one channel is operating at 50% duty cycle. In this situation, switching noise can potentially couple from one channel to the other, resulting in frequency jitter on one or both channels. This effect can be mitigated with a well designed board layout.

APPLICATIONS INFORMATION

A general LTC3633A-2 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and switching frequency. Component selection typically begins with the selection of the inductor L and resistor R_T. Once the inductor is chosen, the input capacitor, C_{IN}, and the output capacitor, C_{OUT}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, tracking/soft-start, input UVLO, and PGOOD.

Programming Switching Frequency

Selection of the switching frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

Connecting a resistor from the RT pin to SGND programs the switching frequency (f) between 500kHz and 4MHz according to the following formula:

$$R_{RT} = \frac{3.2E^{11}}{f}$$

where R_{RT} is in Ω and f is in Hz.

When RT is tied to $INTV_{CC}$, the switching frequency will default to approximately 2MHz, as set by an internal resistor. This internal resistor is more sensitive to process and temperature variations than an external resistor (see Typical Performance Characteristics) and is best used for applications where switching frequency accuracy is not critical.

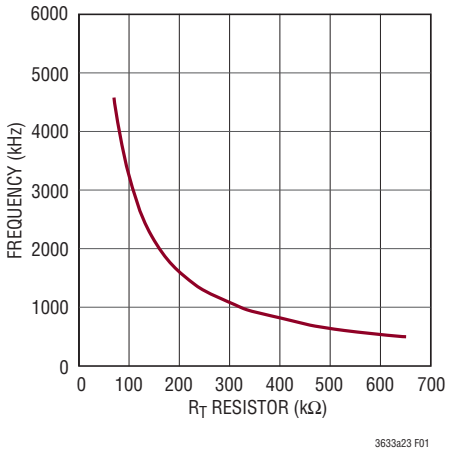

Figure 1. Switching Frequency vs R_T

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where ΔI_L = inductor ripple current, f = operating frequency L = inductor value and V_{IN} is the input power supply voltage applied to the PV_{IN} inputs. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater inductor core loss, greater ESR loss in the output capacitor, and larger output voltage ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

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APPLICATIONS INFORMATION

A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$. Note that the largest ripple current occurs at the highest PV_{IN}. Exceeding 60% of $I_{OUT(MAX)}$ is not recommended. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor ripple current also must not be so large that its valley current level exceeds the negative current limit, which can be as small as –1.2A. If the negative current limit is exceeded while the part is in the forced continuous mode of operation, V_{OUT} can get charged up to above its regulation level – until the inductor current no longer exceeds the negative current limit. In such instances, choose a larger inductor value to reduce the inductor ripple current. The alternative is to reduce the inductor ripple current by decreasing the R_T resistor value which will increase the switching frequency.

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire, leading to increased DCR and copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard”, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current, so it is important to ensure that the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don’t radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. Table 1 gives a sampling of available surface mount inductors.

Table 1. Inductor Selection Table

INDUCTANCE (µH)	DCR (mΩ)	MAX CURRENT (A)	DIMENSIONS (mm)	HEIGHT (mm)
Würth Electronik WE-HC 744312 Series				
0.25	2.5	18	7 × 7.7	3.8
0.47	3.4	16		
0.72	7.5	12		
1.0	9.5	11		
1.5	10.5	9		
Vishay IHLP-2020BZ-01 Series				
0.22	5.2	15	5.2 × 5.5	2
0.33	8.2	12		
0.47	8.8	11.5		
0.68	12.4	10		
1	20	7		
Toko FDV0620 Series				
0.20	4.5	12.4	7 × 7.7	2.0
0.47	8.3	9.0		
1.0	18.3	5.7		
Coilcraft D01813H Series				
0.33	4	10	6 × 8.9	5.0
0.56	10	7.7		
1.2	17	5.3		
TDK RLF7030 Series				
1.0	8.8	6.4	6.9 × 7.3	3.2
1.5	9.6	6.1		

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

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APPLICATIONS INFORMATION

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3633A-2 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is approximated by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

When using low-ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3 \bullet \Delta I_{OUT}}{f \bullet V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are available in small case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the PV_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at PV_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

$INTV_{CC}$ Regulator Bypass Capacitor

An internal low dropout (LDO) regulator draws power from the SV_{IN} input and produces the 3.3V supply that powers the internal bias circuitry and drives the gate of the internal MOSFET switches. The $INTV_{CC}$ pin connects to the output of this regulator and must have a minimum of 1µF ceramic decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the $INTV_{CC}$ and PGND pins to provide the transient currents required by the LTC3633A-2. This supply is intended only to supply additional DC load currents as desired and not intended to regulate large transient or AC behavior, as this may impact LTC3633A-2 operation.

As long as the $INTV_{CC}$ rail is powered by SV_{IN}, the regulator control circuitry will operate, regardless of the PV_{IN} voltages. Thus, the SV_{IN} input can be powered from a different supply voltage than either PV_{IN1} or PV_{IN2}. This characteristic makes the LTC3633A-2/LTC3633A-3 very flexible and easy to use in systems with multiple power sources.

Operating from Multiple Power Sources

Channel 1 and channel 2 may be operated from separate input power sources. In cases where one power source is disconnected, the other regulator can continue to operate provided that SV_{IN} remain powered. This can be done with a simple diode-OR circuit, as shown in Figure 2.

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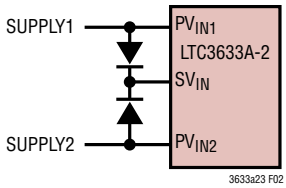

Figure 2. Diode-OR Circuit

Furthermore, as long as SV_{IN} is powered, the LTC3633A-2/LTC3633A-3 operates as a step-down regulator with PV_{IN} voltages as low as 1.5V (subject to minimum off-time constraints). However, at PV_{IN} voltages less than 3V, internal on-time calculation errors increase, and controlled on-time operation is not guaranteed. If this occurs, the output voltages will remain in regulation, but the switching frequency of each channel may deviate from the programmed frequency under these conditions and phase lock between the two channels may be lost.

Boost Capacitor

The LTC3633A-2 uses a "bootstrap" circuit to create a voltage rail above the applied input voltage PV_{IN}. Specifically, a boost capacitor, C_{BOOST}, is charged to a voltage approximately equal to $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately PV_{IN} + 3.3V. For most applications, a 0.1µF ceramic capacitor closely connected between the BOOST and SW pins will provide adequate performance.

Output Voltage Programming

Each regulator's output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right)$$

The desired output voltage is set by appropriate selection of resistors R1 and R2 as shown in Figure 3. Choosing large values for R1 and R2 will result in improved zero-load efficiency but may lead to undesirable noise coupling or phase margin reduction due to stray capacitances at the V_{FB} node. Care should be taken to route the V_{FB} trace away from any noise source, such as the SW trace. To improve the frequency response of the main control loop, a feedforward capacitor, C_F, may be used as shown in Figure 3.

Connecting the V_{ON} pin to the output voltage makes the on-time proportional the output voltage and allows the internal on-time servo loop to lock the converter's switching frequency to the programmed value. If the output voltage is outside the V_{ON} sense range (0.6V – 6V for LTC3633A-2, 1.5V – 12V for LTC3633A-3), the output voltage will stay in regulation, but the switching frequency may deviate from the programmed frequency.

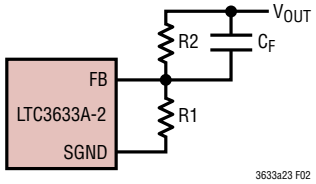

Figure 3. Setting the Output Voltage

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3633A-2 can turn on the bottom power MOSFET, trip the current comparator and turn the power MOSFET back off. This time is typically 45ns. For the controlled on-time architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{(MAX)} = 1 - f \bullet \left(t_{OFF(MIN)} + 2 \bullet t_{DEAD}\right)$$

where f is the switching frequency, t_{DEAD} is the nonoverlap time, or "dead time" (typically 10ns) and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1 - f \bullet \left(t_{OFF(MIN)} + 2 \bullet t_{DEAD}\right)}$$

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Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{(MIN)} = \left(f \bullet t_{ON(MIN)}\right)$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, but the switching frequency will decrease from its programmed value. This constraint may not be of critical importance in most cases, so high switching frequencies may be used in the design without any fear of severe consequences. As the sections on Inductor and Capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

Internal/External Loop Compensation

The LTC3633A-2 provides the option to use a fixed internal loop compensation network to reduce both the required external component count and design time. The internal loop compensation network can be selected by connecting the ITH pin to the $INTV_{CC}$ pin. To ensure stability it is recommended that internal compensation only be used with applications with f_{SW} > 1MHz. Alternatively, the user may choose specific external loop compensation components to optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the ITH pin.

Suggested compensation component values are shown in Figure 4. For a 2MHz application, an R-C network of 220pF and 13kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 10pF bypass capacitor on the ITH pin is recommended for the purposes of filtering out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor C_F can be added to improve the high frequency response, as previously shown in Figure 3. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

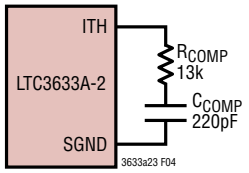

Figure 4. Compensation Component

Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time, and settling behavior at this test point reflect the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external components shown in Figure 4 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of ~1µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its

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APPLICATIONS INFORMATION

steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft starting.

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Floating this pin or connecting it to $INTV_{CC}$ enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is tied to ground, forced continuous mode operation is selected, creating the lowest fixed output ripple at the expense of light load efficiency.

The LTC3633A-2 will detect the presence of the external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place both regulators into forced continuous mode operation.

Output Voltage Tracking and Soft-Start

The LTC3633A-2 allows the user to control the output voltage ramp rate by means of the TRACKSS pin. From 0 to 0.6V, the TRACKSS voltage will override the internal 0.6V reference input to the error amplifier, thus regulating the feedback voltage to that of the TRACKSS pin. When TRACKSS is above 0.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

The voltage at the TRACKSS pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4µA pull-up current source to implement a soft-start function by connecting an external capacitor (C_{SS}) from the TRACKSS pin to ground. The relationship between output rise time and TRACKSS capacitance is given by:

$$t_{SS} = 430000\Omega \bullet C_{SS}$$

A default internal soft-start ramp forces a minimum soft-start time of 400µs by overriding the TRACKSS pin input during this time period. Hence, capacitance values less than approximately 1000pF will not significantly affect soft-start behavior.

When driving the TRACKSS pin from another source, each channel's output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 5. In the following discussions, V_{OUT1} refers to the LTC3633A-2 output 1 as a master channel and V_{OUT2} refers to output 2 as a slave channel. In practice, either channel can be used as the master.

To implement the coincident tracking in Figure 5a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TRACKSS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 6a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking, the feedback pin of the master channel should connect to the TRACKSS pin of the slave channel (as in Figure 6b). By selecting different resistors, the LTC3633A-2 can achieve different modes of tracking including the two in Figure 5.

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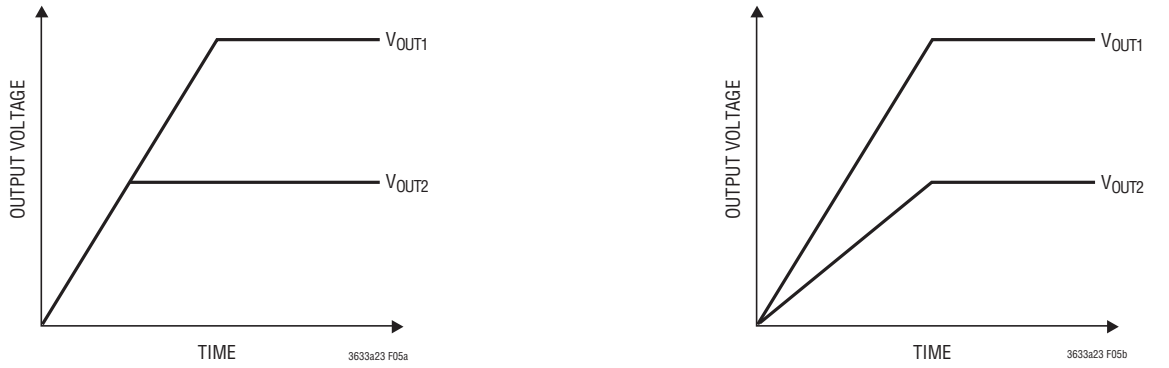
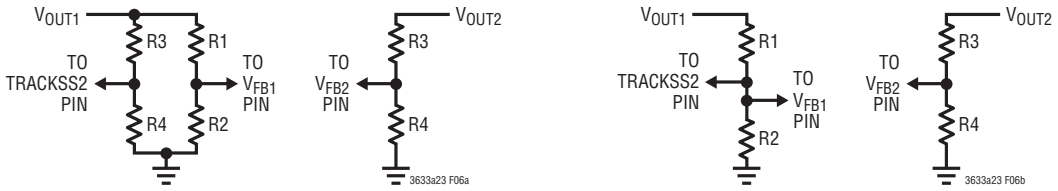


(5a) Coincident Tracking **(5b) Ratiometric Tracking**

Figure 5. Two Different Modes of Output Voltage Tracking



(6a) Coincident Tracking Setup **(6b) Ratiometric Tracking Setup**

Figure 6. Setup for Coincident and Ratiometric Tracking

Upon start-up, the regulator defaults to Burst Mode operation until the output exceeds 80% of its final value (V_{FB} > 0.48V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value (as it may when tracking down, for instance), the regulator will automatically switch to Burst Mode operation to prevent inductor saturation and improve TRACKSS pin accuracy.

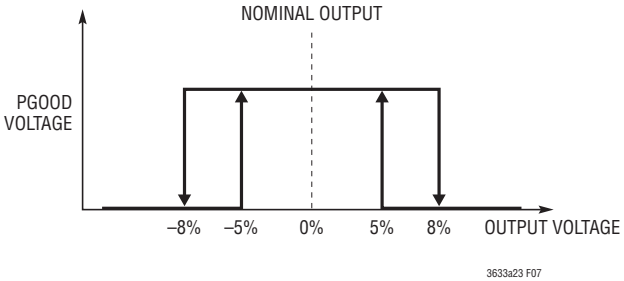


Figure 7. PGOOD Pin Behavior

Output Power Good

The PGOOD output of the LTC3633A-2 is driven by a 20Ω (typical) open-drain pull-down device. This device will be turned off once the output voltage is within 5% (typical) of the target regulation point, allowing the voltage at PGOOD to rise via an external pull-up resistor. If the output voltage exits an 8% (typical) regulation window around the target regulation point, the open-drain output will pull down with 20Ω output resistance to ground, thus dropping the PGOOD pin voltage. This behavior is described in Figure 7.

A filter time of 40µs (typical) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. As a result, the output voltage must be within the target regulation window of 5% for 40µs before the PGOOD pin pulls high. Conversely, the output voltage must exit the 8% regulation window for 40µs before the PGOOD pin pulls to ground.

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APPLICATIONS INFORMATION

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC3633A-2 circuits: 1) I^2R losses, 2) switching losses and quiescent power loss 3) transition losses and other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}{}^2(R_{SW} + R_L)$$

2. The internal LDO draws power from the SV_{IN} input to regulate the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

   Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on each LTC3633A-2 regulator channel is approximately 2.3nC.

   To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by the voltage applied to SV_{IN}:

   $$P_{LDO} = (I_{GATECHG} + I_Q) \bullet SV_{IN}$$

3. Other "hidden" losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC3633A-2 internal power devices switch quickly enough that these losses are not significant compared to other sources.

   Other losses, including diode conduction losses during dead-time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3633A-2 requires the exposed package backplane metal (PGND) to be well soldered to the PC board to provide good thermal contact. This gives the QFN and TSSOP packages exceptional thermal properties, which are necessary to prevent excessive self-heating of the part in normal operation.

In a majority of applications, the LTC3633A-2 does not dissipate much heat due to its high efficiency and low thermal resistance of its exposed-back QFN package. However, in applications where the LTC3633A-2 is running at high ambient temperature, high input supply voltage, high switching frequency, and maximum output current load, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off until temperature returns to 140°C.

To prevent the LTC3633A-2 from exceeding the maximum junction temperature of 125°C, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

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APPLICATIONS INFORMATION

As an example, consider the case when one of the regulators is used in an application where V_{IN} = SV_{IN} = 12V, I_{OUT} = 2A, frequency = 2MHz, V_{OUT} = 1.8V. From the $R_{DS(ON)}$ graphs in the Typical Performance Characteristics section, the top switch on-resistance is nominally 145mΩ and the bottom switch on-resistance is nominally 70mΩ at 70°C ambient. The equivalent power MOSFET resistance R_{SW} is:

$$R_{DS(ON)TOP} \bullet \frac{1.8V}{12V} + R_{DS(ON)BOT} \bullet \frac{10.2V}{12V} = 81.3m\Omega$$

From the previous section's discussion on gate drive, we estimate the total gate drive current through the LDO to be 2MHz • 2.3nC = 4.6mA, and I_Q of one channel is 0.65mA (see Electrical Characteristics). Therefore, the total power dissipated by a single regulator is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + SV_{IN} \bullet (I_{GATECHG} + I_Q)$$

$$P_D = (2A)^2 \bullet (0.0813\Omega) + (12V) \bullet (4.6mA + 0.65mA) = 0.388W$$

Running two regulators under the same conditions would result in a power dissipation of 0.776W. The QFN 5mm × 4mm package junction-to-ambient thermal resistance, θ_{JA}, is around 43°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.776W \bullet 43°C/W + 70°C = 103°C$$

which is below the maximum junction temperature of 125°C. With higher ambient temperatures, a heat sink or cooling fan should be considered to drop the junction-to-ambient thermal resistance. Alternatively, the TSSOP package may be a better choice for high power applications, since it has better thermal properties than the QFN package.

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 70°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. Redoing the calculation assuming that R_{SW} increased 12% at 103°C yields a new junction temperature of 107°C. If the application calls for a higher ambient temperature and/or higher load currents, care should be taken to reduce the temperature rise of the part by using a heat sink or air flow.

Figure 8 is a temperature derating curve based on the DC1347 demo board (QFN package). It can be used to estimate the maximum allowable ambient temperature for given DC load currents in order to avoid exceeding the maximum operating junction temperature of 125°C.

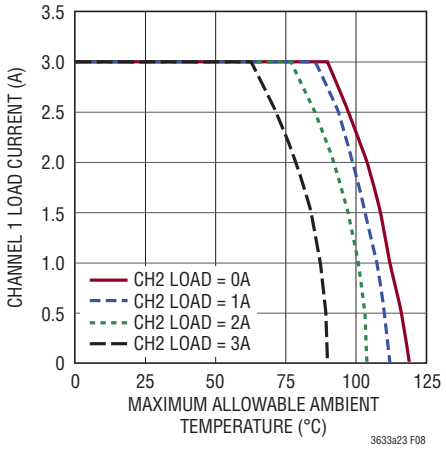

Figure 8. Temperature Derating Curve for DC1347 Demo Circuit

Junction Temperature Measurement

The junction-to-ambient thermal resistance will vary depending on the size and amount of heat sinking copper on the PCB board where the part is mounted, as well as the amount of air flow on the device. In order to properly evaluate this thermal resistance, the junction temperature needs to be measured. A clever way to measure the junction temperature directly is to use the internal junction diode on one of the pins (PGOOD) to measure its diode voltage change based on ambient temperature change.

First remove any external passive component on the PGOOD pin, then pull out 100µA from the PGOOD pin to turn on its internal junction diode and bias the PGOOD pin to a negative voltage. With no output current load, measure the PGOOD voltage at an ambient temperature of 25°C, 75°C and 125°C to establish a slope relationship between the delta voltage on PGOOD and delta ambient temperature. Once this slope is established, then the junction temperature rise can be measured as a function of power loss in the package with corresponding output load current. Although making this measurement with this method does violate absolute maximum voltage ratings on the PGOOD pin, the applied power is so low that there should be no significant risk of damaging the device.

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APPLICATIONS INFORMATION

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3633A-2. Check the following in your layout:

1) Do the input capacitors connect to the PV_{IN} and PGND pins as close as possible? These capacitors provide the AC current to the internal power MOSFETs and their drivers.

2) The output capacitor, C_{OUT}, and inductor L should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to both PGND and the (–) plate of C_{IN}.

3) The resistive divider, (e.g. R1 to R4 in Figure 9) must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal V_{FB} should be routed away from noisy components and traces, such as the SW line, and its trace length should be minimized. In addition, the R_T resistor and loop compensation components should be terminated to SGND.

4) Keep sensitive components away from the SW pin. The R_T resistor, the compensation components, the feedback resistors, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor L.

5) A ground plane is preferred, but if not available, the signal and power grounds should be segregated with both connecting to a common, low noise reference point. The connection to the PGND pin should be made with a minimal resistance trace from the reference point.

6) Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside of the package (PGND).

Refer to Figures 10 and 11 for board layout examples.

Design Example

As a design example, consider using the LTC3633A-2 in an application with the following specifications: $V_{IN(MAX)}$ = 13.2V, V_{OUT1} = 1.8V, V_{OUT2} = 3.3V, $I_{OUT(MAX)}$ = 3A, $I_{OUT(MIN)}$ = 10mA, f = 2MHz, V_{DROOP} ~ (5% • V_{OUT}). The following discussion will use equations from the previous sections.

Because efficiency is important at both high and low load current, Burst Mode operation will be utilized.

First, the correct R_T resistor value for 2MHz switching frequency must be chosen. Based on the equation discussed earlier, R_T should be 160k; the closest standard value is 162k. RT can be tied to $INTV_{CC}$ if switching frequency accuracy is not critical.

Next, determine the channel 1 inductor value for about 40% ripple current at maximum V_{IN}:

$$L1=\left(\frac{1.8V}{2MHz \bullet 1.2A}\right)\left(1-\frac{1.8V}{13.2V}\right)=0.64\mu H$$

A standard value of 0.68µH should work well here. Solving the same equation for channel 2 results in a 1µH inductor.

C_{OUT} will be selected based on the charge storage requirement. For a V_{DROOP} of 90mV for a 3A load step:

$$C_{OUT1} \approx \frac{3 \bullet \Delta I_{OUT}}{f \bullet V_{DROOP}} = \frac{3 \bullet (3A)}{(2MHz)(90mV)} = 50\mu F$$

A 47µF ceramic capacitor should be sufficient for channel 1. Solving the same equation for channel 2 (using 5% of V_{OUT} for V_{DROOP}) results in 27µF of capacitance (22µF is the closest standard value).

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 3A\frac{\sqrt{1.8V(13.2V-1.8V)}}{13.2V} = 1A$$

Solving this equation for channel 2 results in an RMS input current of 1.3A. Decoupling each PV_{IN} input with a 47µF ceramic capacitor should be adequate for most applications.

Lastly, the feedback resistors must be chosen. Picking R1 and R3 to be 12.1k, R2 and R4 are calculated to be:

$$R2 = (12.1k) \bullet \left(\frac{1.8V}{0.6V}-1\right) = 24.2k$$

$$R4 = (12.1k) \bullet \left(\frac{3.3V}{0.6V}-1\right) = 54.5k$$

The final circuit is shown in Figure 9.

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APPLICATIONS INFORMATION

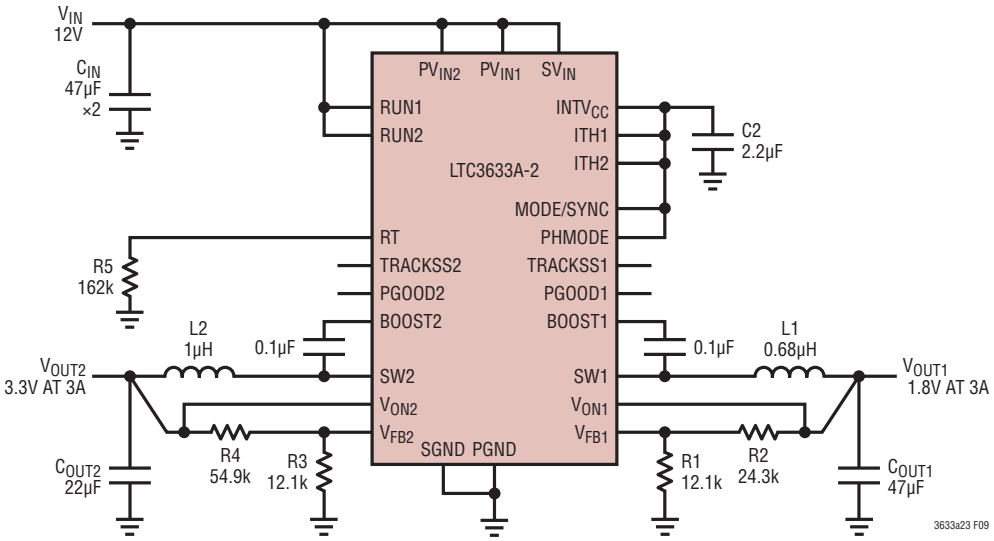

Figure 9. Design Example Circuit

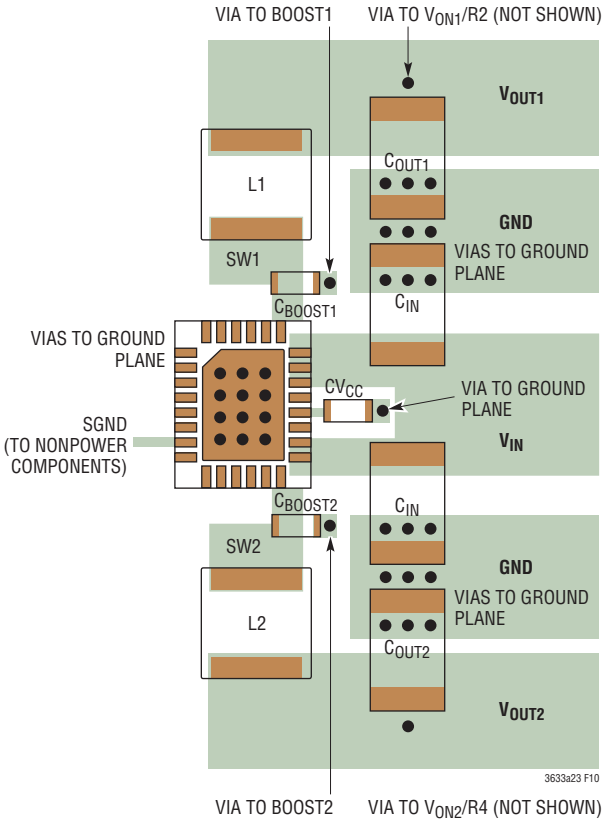

Figure 10. Example of Power Component Layout for QFN Package

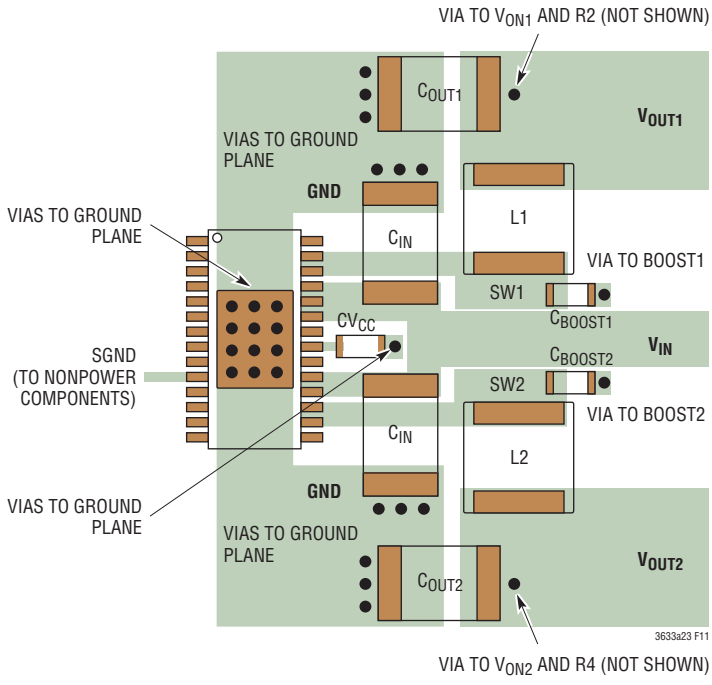

Figure 11. Example of Power Component Layout for TSSOP Package

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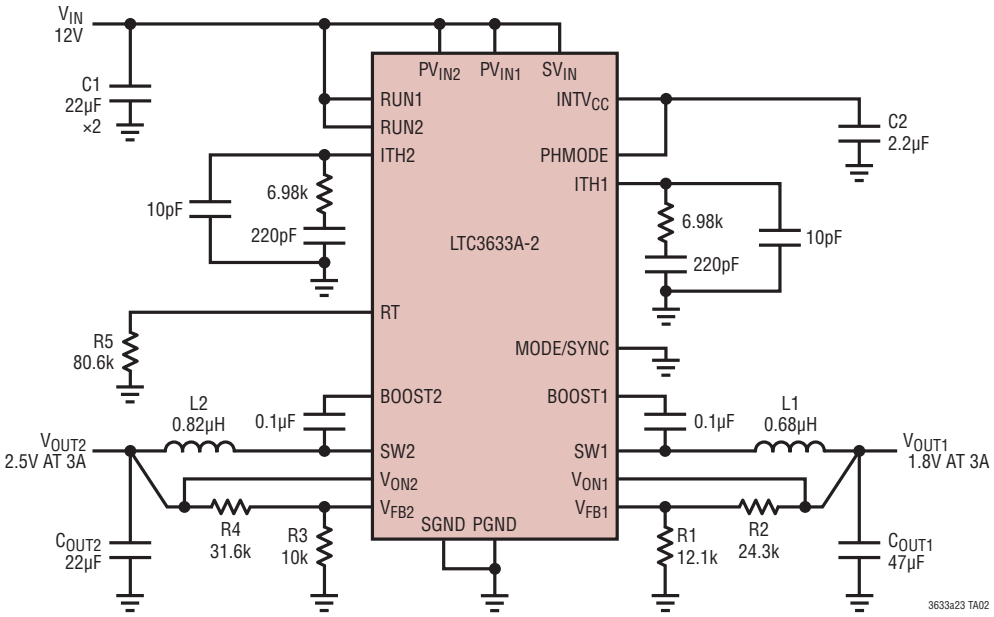
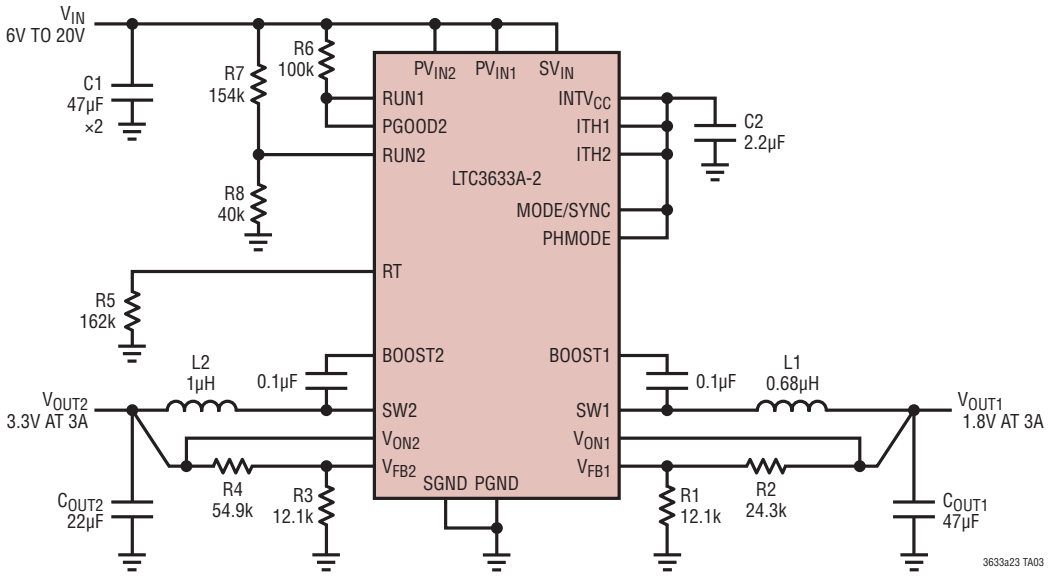
TYPICAL APPLICATIONS

1.8V/2.5V 4MHz Buck Regulator



3.3V/1.8V Sequenced Regulator with 6V Input UVLO (V_{OUT1} Enabled After V_{OUT2})



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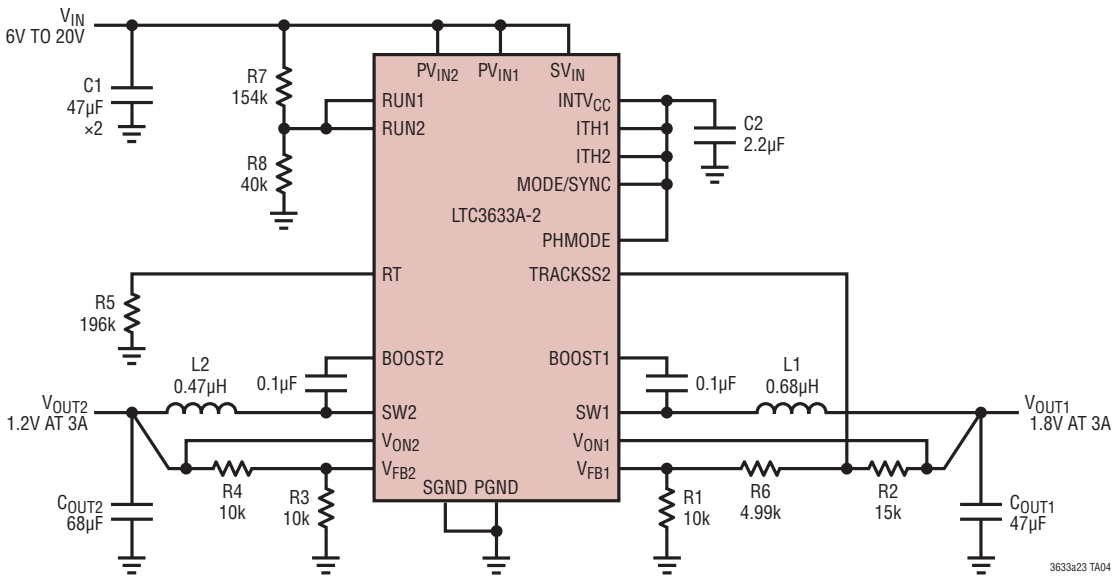
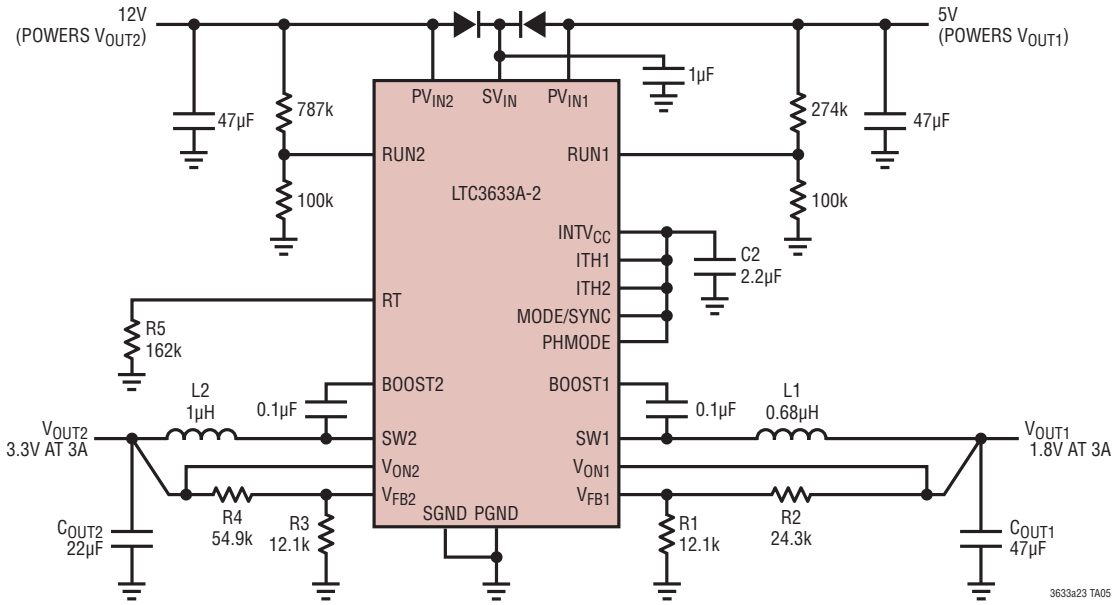
TYPICAL APPLICATIONS

1.2V/1.8V Buck Regulator with Coincident Tracking and 6V Input UVLO



Dual Output Regulator From Multiple Input Supplies



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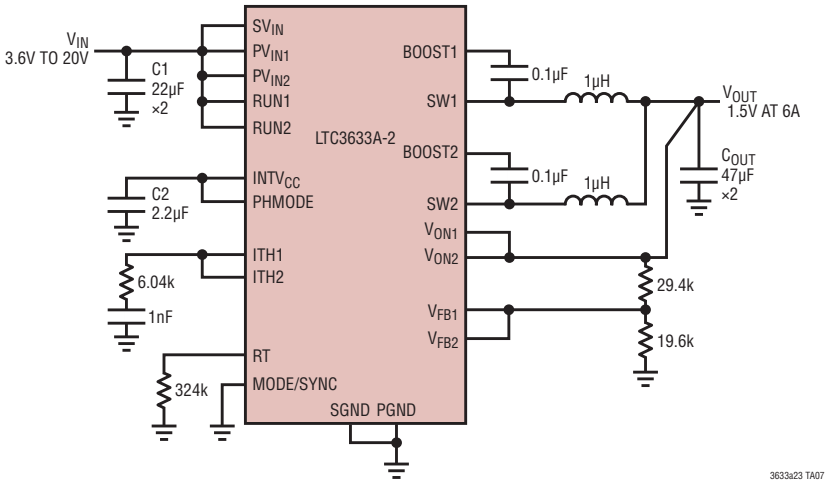
TYPICAL APPLICATIONS

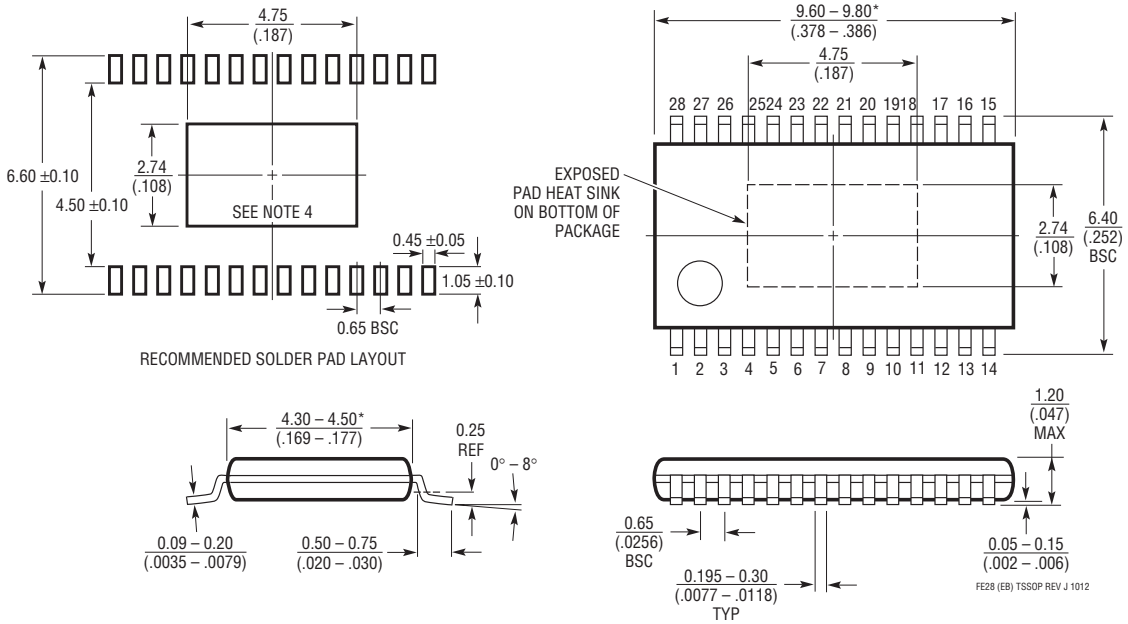
6A 1MHz 2-Phase Buck Regulator



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation EB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

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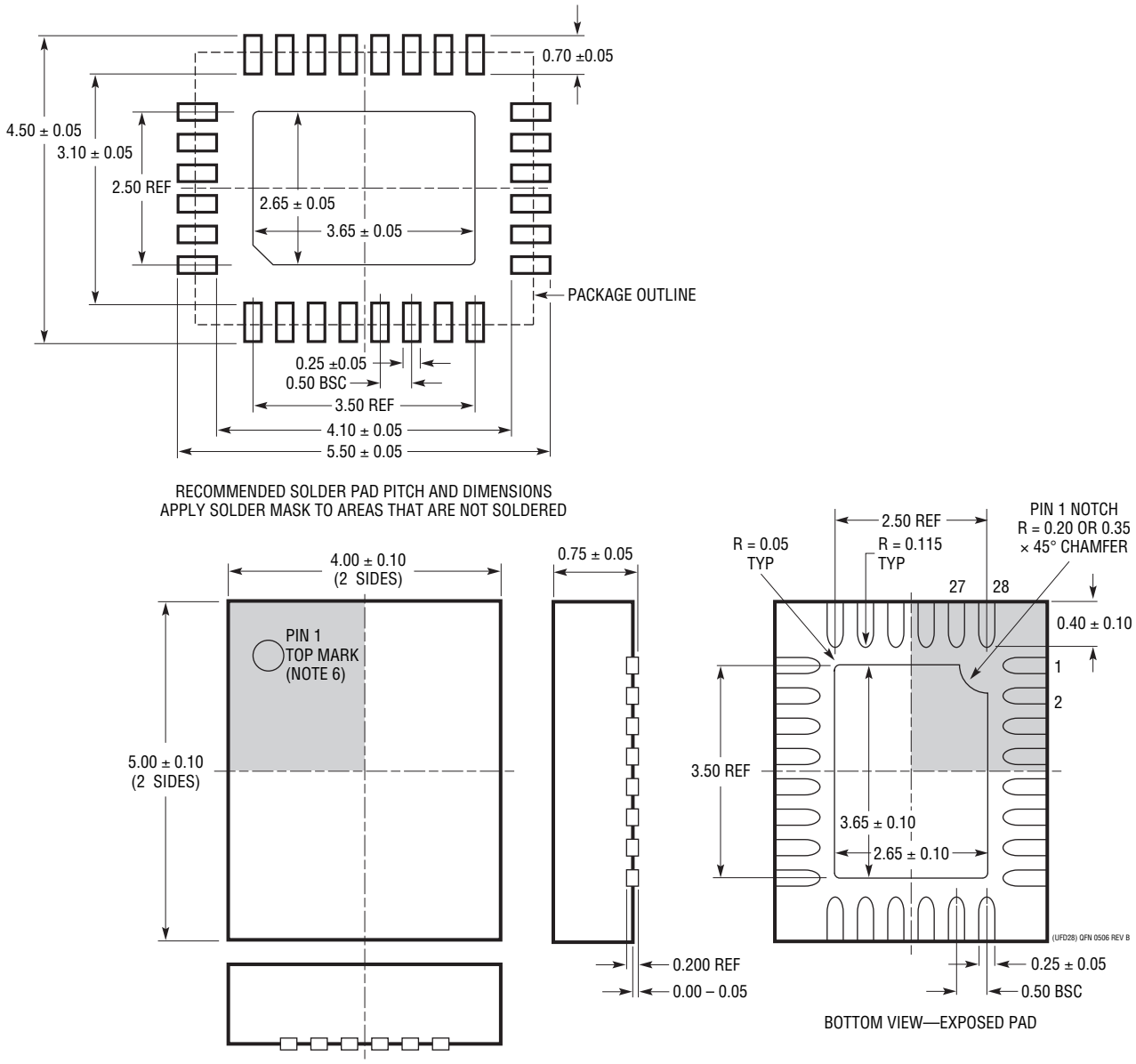
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UFD Package
28-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1712 Rev B)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/13	Clarified Absolute Maximum Ratings	2
B	5/15	Clarified I_{LIM} limits. Clarified Inductor Selection.	3 13

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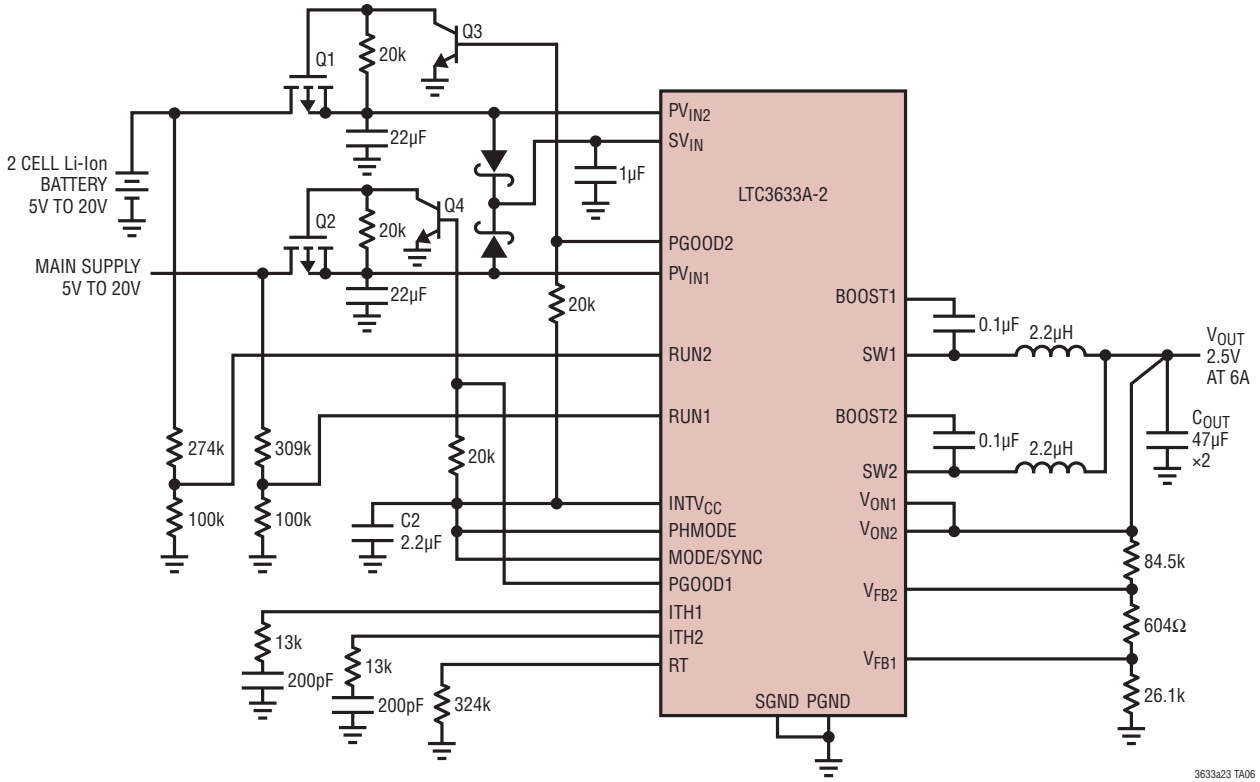
TYPICAL APPLICATION

2.5V Regulator with Battery Backup



Q1, Q2: VISHAY SILICONIX P-CHANNEL MOSFET SI4953ADY
Q3, Q4: ROHM SEMICONDUCTOR NPN TRANSISTOR IMX1T110

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3633	15V, Dual 3A (I_{OUT}), 4MHz Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 13µA, 4mm × 5mm QFN-28, TSSOP-28E
LTC3605	15V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3602	10V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 10V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 3mm × 3mm QFN-16, MSOP-16E
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3605A	20V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 3mm QFN-16, MSOP-16E
LTC3626	20V, 2.5A Synchronous Monolithic Step-Down Regulator with Current and Temperature Monitoring	95% Efficiency, V_{IN}: 3.6V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 4mm QFN-20

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