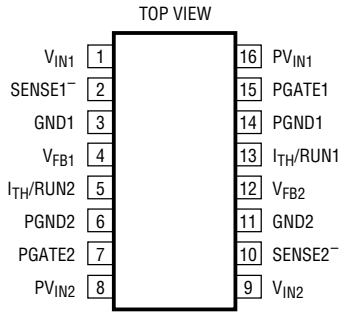
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}, PV_{IN}) .....–0.3V to 10V
$SENSE^-$, PGATE Voltages .....–0.3V to (V_{IN} + 0.3V)
V_{FB}, I_{TH}/RUN Voltages .....–0.3V to 2.4V
PGATE Peak Output Current (<10µs) 1A
Storage Ambient Temperature Range ... –65°C to 150°C
Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Note 3) ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 150°C, θ_{JA} = 135°C/W

ORDER PART NUMBER
LTC1874EGN
GN PART MARKING
1874

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

All specifications apply to each controller. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 4.2V unless otherwise specified. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input DC Supply Current (Per Controller)	Typicals at V_{IN} = 4.2V (Note 4)					
Normal Operation	2.4V ≤ V_{IN} ≤ 9.8V			270	420	µA
Sleep Mode	2.4V ≤ V_{IN} ≤ 9.8V			230	370	µA
Shutdown	2.4V ≤ V_{IN} ≤ 9.8V, V_{ITH}/RUN = 0V			8	22	µA
UVLO	V_{IN} < UVLO Threshold			6	10	µA
Undervoltage Lockout Threshold	V_{IN} Falling	●	1.55	2.0	2.35	V
	V_{IN} Rising		1.85	2.3	2.40	V
Shutdown Threshold (at I_{TH}/RUN)		●	0.15	0.35	0.55	V
Start-Up Current Source	V_{ITH}/RUN = 0V		0.25	0.5	0.85	µA
Regulated Feedback Voltage	T_A = 0°C to 70°C (Note 5)	●	0.780	0.800	0.820	V
	T_A = –40°C to 85°C (Note 5)	●	0.770	0.800	0.830	V
Output Voltage Line Regulation	2.4V ≤ V_{IN} ≤ 9.8V (Note 5)			0.05		mV/V
Output Voltage Load Regulation	I_{TH}/RUN Sinking 5µA (Note 5)			2.5		mV/µA
	I_{TH}/RUN Sourcing 5µA (Note 5)			2.5		mV/µA
V_{FB} Input Current	(Note 5)			10	50	nA
Overvoltage Protect Threshold	Measured at V_{FB}		0.820	0.860	0.895	V
Overvoltage Protect Hysteresis				20		mV
Oscillator Frequency	V_{FB} = 0.8V		500	550	650	kHz
	V_{FB} = 0V			120		kHz
Gate Drive Rise Time	C_{LOAD} = 3000pF			40		ns
Gate Drive Fall Time	C_{LOAD} = 3000pF			40		ns
Peak Current Sense Voltage	(Note 6)			120		mV

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1874E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$

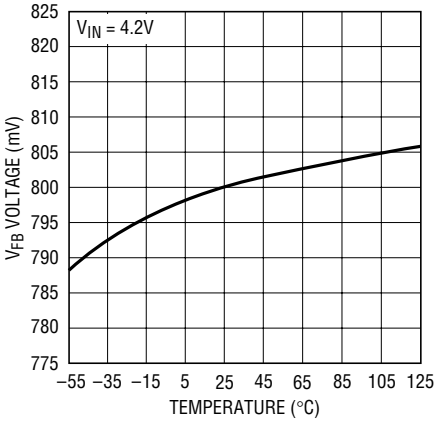
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: Each controller in the LTC1874 is individually tested in a feedback loop that servos V_{FB} to the output of the error amplifier.

Note 6: Peak current sense voltage is reduced dependent upon duty cycle to a percentage of value as given in Figure 2.

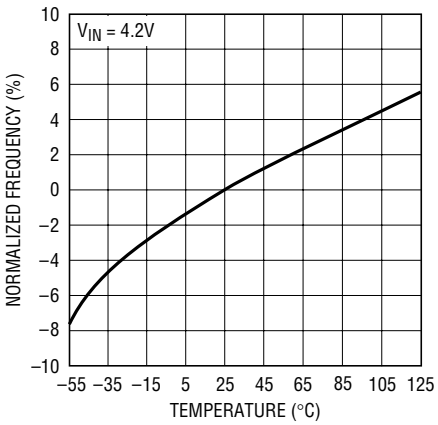
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Voltage vs Temperature



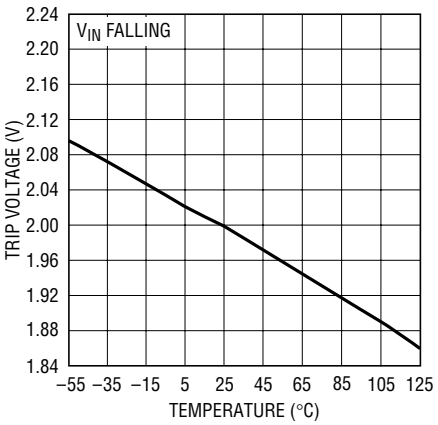
1874 G01

Normalized Oscillator Frequency vs Temperature



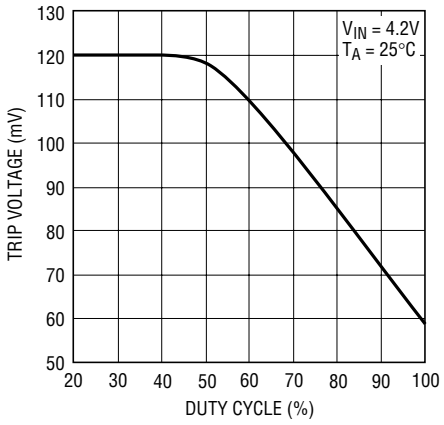
1874 G02

Undervoltage Lockout Trip Voltage vs Temperature



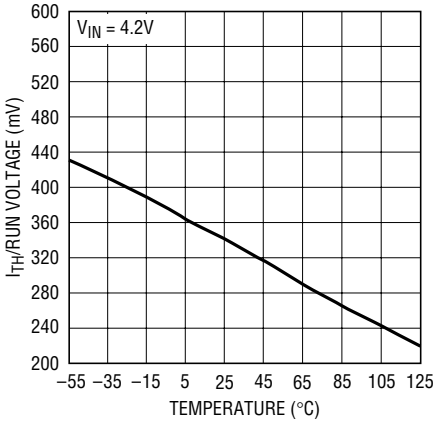
1874 G03

Maximum (V_{IN} – SENSE$^-$) Voltage vs Duty Cycle



1874 G04

Shutdown Threshold vs Temperature



1874 G05

PIN FUNCTIONS

V_{IN1} (Pin 1): Main Supply Pin for Controller #1. This pin delivers the Input DC Supply Current (listed in the Electrical Characteristics table) plus a small amount of logic switching current. Must be connected to PV_{IN1} (Pin 16) and closely decoupled to GND1 (Pin 3).

SENSE1$^-$ (Pin 2): The Negative Input to the Current Comparator of Controller #1.

GND1 (Pin 3): Signal Ground for Controller #1. Must be connected to PGND1 (Pin 14).

V_{FB1} (Pin 4): Receives the feedback voltage from an external resistive divider across the output of Controller #1.

I_{TH}/RUN2 (Pin 5): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input of Controller #2. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.35V causes Controller #2 to be shut down. In shutdown, all functions of Controller #2 are disabled and PGATE2 (Pin 7) is held high.

PGND2 (Pin 6): Power Ground for Controller #2. Must be connected to GND2 (Pin 11).

PGATE2 (Pin 7): Gate Drive for the External P-Channel MOSFET of Controller #2. This pin swings from 0V to the voltage of PV_{IN2}.

PV_{IN2} (Pin 8): Power Supply Pin for Controller #2. This pin delivers the dynamic switching current that drives the gate of the external P-channel MOSFET of Controller #2. Must be connected to V_{IN2} (Pin 9) and closely decoupled to PGND2 (Pin 6).

V_{IN2} (Pin 9): Main Supply Pin for Controller #2. This pin delivers the Input DC Supply Current (listed in the Electrical Characteristics table) plus a small amount of logic switching current. Must be connected to PV_{IN2} (Pin 8) and closely decoupled to GND2 (Pin 11).

SENSE2$^-$ (Pin 10): The Negative Input to the Current Comparator of Controller #2.

GND2 (Pin 11): Signal Ground for Controller #2. Must be connected to PGND2 (Pin 6).

V_{FB2} (Pin 12): Receives the feedback voltage from an external resistive divider across the output of Controller #2.

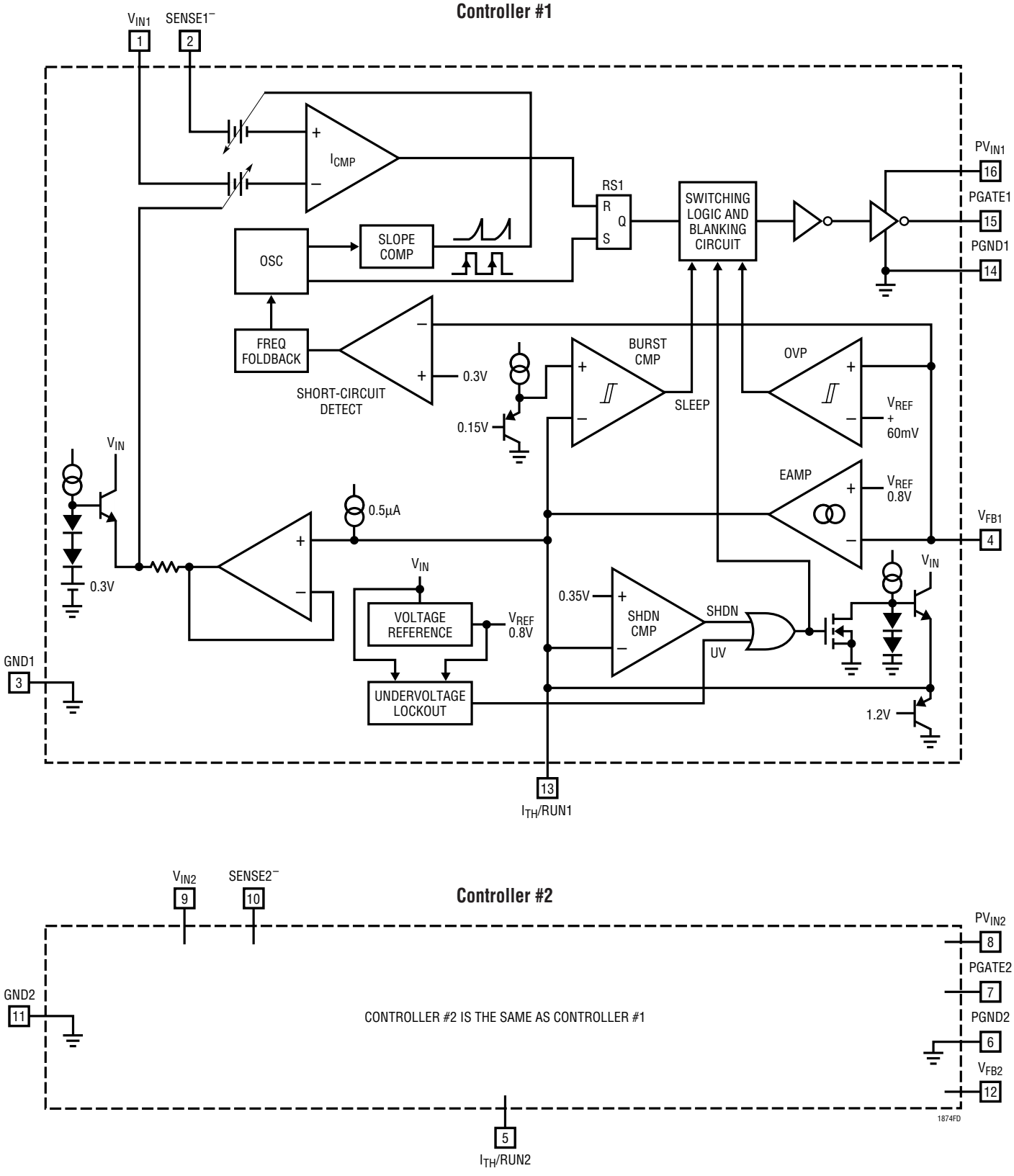
I_{TH}/RUN1 (Pin 13): This pin performs two functions. It serves as the error amplifier compensation point as well as the run control input of Controller #1. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0.7V to 1.9V. Forcing this pin below 0.35V causes Controller #1 to be shut down. In shutdown, all functions of Controller #1 are disabled and PGATE1 (Pin 15) is held high.

PGND1 (Pin 14): Power Ground for Controller #1. Must be connected to GND1 (Pin 3).

PGATE1 (Pin 15): Gate Drive for the External P-Channel MOSFET of Controller #1. This pin swings from 0V to the voltage of PV_{IN1}.

PV_{IN1} (Pin 16): Power Supply Pin for Controller #1. This pin delivers the dynamic switching current that drives the gate of the external P-channel MOSFET of Controller #1. Must be connected to V_{IN1} (Pin 1) and closely decoupled to PGND1 (Pin 14).

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

The LTC1874 is a dual, constant frequency current mode switching regulator. The two switching regulators function identically but independent of each other. The following description of operation is written for a single switching regulator.

Main Control Loop

During normal operation, the external P-channel power MOSFET is turned on by the oscillator and turned off when the current comparator (I_{CMP}) resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH}/RUN pin, which is the output of the error amplifier EAMP. An external resistive divider connected between V_{OUT} and ground allows the EAMP to receive an output feedback voltage V_{FB}. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the I_{TH}/RUN voltage to increase until the average inductor current matches the new load current.

The main control loop is shut down by pulling the I_{TH}/RUN pin low. Releasing I_{TH}/RUN allows an internal 0.5µA current source to charge up the external compensation network. When the I_{TH}/RUN pin reaches 0.35V, the main control loop is enabled with the I_{TH}/RUN voltage then pulled up to its zero current level of approximately 0.7V. As the external compensation network continues to charge up, the corresponding output current trip level follows, allowing normal operation.

Comparator OVP guards against transient overshoots greater than 7.5% by turning off the external P-channel power MOSFET and keeping it off until the fault is removed.

Burst Mode Operation

The controller enters Burst Mode operation at low load currents. In this mode, the peak current of the inductor is set as if V_{ITH}/RUN = 1V (at low duty cycles) even though the voltage at the I_{TH}/RUN pin is at a lower value. If the inductor's average current is greater than the load requirement, the voltage at the I_{TH}/RUN pin will drop. When the I_{TH}/RUN voltage goes below 0.85V, the sleep signal goes high, turning off the external MOSFET. The sleep signal goes low when the I_{TH}/RUN voltage goes above 0.925V and the controller resumes normal operation. The next oscillator cycle will turn the external MOSFET on and the switching cycle repeats.

Dropout Operation

When the input supply voltage decreases towards the output voltage, the rate of change of inductor current during the ON cycle decreases. This reduction means that the external P-channel MOSFET will remain on for more than one oscillator cycle since the inductor current has not ramped up to the threshold set by EAMP. Further reduction in input supply voltage will eventually cause the P-channel MOSFET to be turned on 100%, i.e., DC. The output voltage will then be determined by the input voltage minus the voltage drop across the MOSFET, the sense resistor and the inductor.

Undervoltage Lockout

To prevent operation of the P-channel MOSFET below safe input voltage levels, an undervoltage lockout is incorporated into the controller. When the input supply voltage drops below approximately 2.0V, the P-channel MOSFET and all circuitry is turned off except the undervoltage block, which draws only several microamperes.

Short-Circuit Protection

When the output is shorted to ground, the frequency of the oscillator will be reduced to about 120kHz. This lower frequency allows the inductor current to safely discharge, thereby preventing current runaway. The oscillator's frequency will gradually increase to its designed rate when the feedback voltage again approaches 0.8V.

Overvoltage Protection

As a further protection, the overvoltage comparator in the controller will turn the external MOSFET off when the feedback voltage has risen 7.5% above the reference voltage of 0.8V. This comparator has a typical hysteresis of 20mV.

OPERATION

Slope Compensation and Inductor's Peak Current

The inductor's peak current is determined by:

$$I_{PK} = \frac{V_{ITH} - 0.7}{10(R_{SENSE})}$$

when the controller is operating below 40% duty cycle. However, once the duty cycle exceeds 40%, slope compensation begins and effectively reduces the peak inductor current. The amount of reduction is given by the curves in Figure 2.

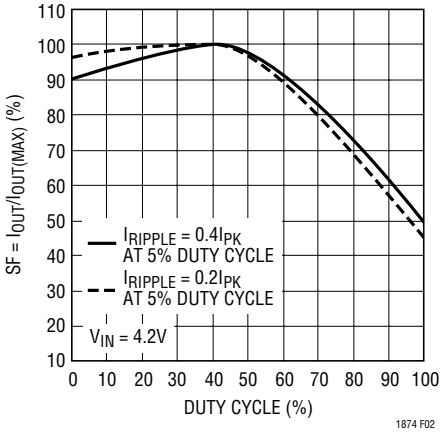


Figure 2. Percentage of Maximum Output Current vs Duty Cycle

APPLICATIONS INFORMATION

The basic LTC1874 application circuit is shown in Figure 1. External component selection for each controller is driven by the load requirement and begins with the selection of L1 and R_{SENSE} (= R1). Next, the power MOSFET (M1) and the output diode (D1) are selected followed by C_{IN} and C_{OUT} (= C1).

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE}, the threshold of the comparator determines the inductor's peak current. The output current the controller can provide is given by:

$$I_{OUT} = \frac{0.12V}{R_{SENSE}} - \frac{I_{RIPPLE}}{2}$$

where I_{RIPPLE} is the inductor peak-to-peak ripple current (see Inductor Value Calculation section).

A reasonable starting point for setting ripple current is $I_{RIPPLE} = (0.4)(I_{OUT})$. Rearranging the above equation, it becomes:

$$R_{SENSE} = \frac{1}{(10)(I_{OUT})} \text{ for Duty Cycle } < 40\%$$

However, for operation that is above 40% duty cycle, slope compensation effect has to be taken into consideration to select the appropriate value to provide the required amount of current. Using Figure 2, the value of R_{SENSE} is:

$$R_{SENSE} = \frac{SF}{(10)(I_{OUT})(100)}$$

where SF is the "slope factor."

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies permit the use of a smaller inductor for the same amount of inductor ripple current. However, this is at the expense of efficiency due to an increase in MOSFET gate charge losses.

The inductance value also has a direct effect on ripple current. The ripple current, I_{RIPPLE}, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}. The inductor's peak-to-peak ripple current is given by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f(L)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

where f is the operating frequency. Accepting larger values of I_{RIPPLE} allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is

APPLICATIONS INFORMATION

$I_{RIPPLE} = 0.4(I_{OUT(MAX)})$. Remember, the maximum I_{RIPPLE} occurs at the maximum input voltage.

In Burst Mode operation on an LTC1874 controller, the ripple current is normally set such that the inductor current is continuous during the burst periods. Therefore, the peak-to-peak ripple current must not exceed:

$$I_{RIPPLE} \leq \frac{0.03V}{R_{SENSE}}$$

This implies a minimum inductance of:

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f\left(\frac{0.03}{R_{SENSE}}\right)}\left(\frac{V_{OUT} + V_D}{V_{IN} + V_D}\right)$$

(Use $V_{IN(MAX)} = V_{IN}$)

A smaller value than L_{MIN} could be used in the circuit; however, the inductor current will not be continuous during burst periods.

Inductor Core Selection

Once the value of inductor is known, an off the shelf inductor can be selected. The inductor should be rated for the calculated peak current. Some manufacturers specify both peak saturation current and peak RMS current. Make sure that the RMS current meets your continuous load requirements. Also, you may want to compare the DC resistance of different inductors in order to optimize the efficiency.

Inductor core losses are usually not specified and you will need to evaluate them yourself. Usually, the core losses are not a problem because the inductors operate with relatively low magnetic flux swings. The best way to evaluate the core losses is by measuring the converters efficiency. Converter efficiency will reveal the difference in both DC current losses and core losses.

Off the shelf inductors are available from numerous manufacturers. Some of the most common manufacturers are Coilcraft, Coiltronics, Panasonic, Toko, Tokin, Murata and Sumida.

Power MOSFET Selection

The main selection criteria for the power MOSFET are the threshold voltage $V_{GS(TH)}$, the "on" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS} and total gate charge.

Since the controller is designed for operation down to low input voltages, a logic level threshold MOSFET ($R_{DS(ON)}$ guaranteed at $V_{GS} = 2.5V$) is required for applications that work close to this voltage. When these MOSFETs are used, make sure that the input supply to the controller is less than the absolute maximum V_{GS} rating, typically 8V.

The required minimum $R_{DS(ON)}$ of the MOSFET is governed by its allowable power dissipation. For applications that may operate the controller in dropout, i.e., 100% duty cycle, at its worst case the required $R_{DS(ON)}$ is given by:

$$R_{DS(ON)_{DC=100\%}} = \frac{P_P}{\left(I_{OUT(MAX)}\right)^2\left(1+\delta p\right)}$$

where P_P is the allowable power dissipation and δp is the temperature dependency of $R_{DS(ON)}$. $(1 + \delta p)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta p = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

In applications where the maximum duty cycle is less than 100% and the controller is in continuous mode, the $R_{DS(ON)}$ is governed by:

$$R_{DS(ON)} \cong \frac{P_P}{\left(DC\right)I_{OUT}{}^2\left(1+\delta p\right)}$$

where DC is the maximum operating duty cycle of the controller.

Output Diode Selection

The catch diode carries load current during the off-time. The average diode current is therefore dependent on the MOSFET duty cycle. At high input voltages the diode conducts most of the time. As V_{IN} approaches V_{OUT} the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is

APPLICATIONS INFORMATION

short-circuited. Under this condition the diode must safely handle I_{PEAK} at close to 100% duty cycle. Therefore, it is important to adequately specify the diode peak current and average power dissipation so as not to exceed the diode ratings.

Under normal load conditions, the average current conducted by the diode is:

$$I_D = \left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) I_{OUT}$$

The allowable forward voltage drop in the diode is calculated from the maximum short-circuit current as:

$$V_F \approx \frac{P_D}{I_{SC(MAX)}}$$

where P_D is the allowable power dissipation and will be determined by efficiency and/or thermal requirements.

Schottky diodes are a good choice for low forward drop and fast switching times. Remember to keep lead length short and observe proper grounding (see Board Layout Checklist) to avoid ringing and increased dissipation.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle $(V_{OUT} + V_D)/(V_{IN} + V_D)$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Several capacitors may be paralleled to meet the size or height requirements in the design. Due to the high operating frequency of the controller, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{4fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. An excellent choice of tantalum capacitors are the AVX TPS and KEMET T510 series of surface mount tantalum capacitors.

APPLICATIONS INFORMATION

Low Supply Operation

Although the controller can function down to approximately 2.0V, the maximum allowable output current is reduced when V_{IN} decreases below 3V. Figure 3 shows the amount of change as the supply is reduced down to 2V. Also shown in Figure 3 is the effect of V_{IN} on V_{REF} as V_{IN} goes below 2.3V.

Setting Output Voltage

The controller develops a 0.8V reference voltage between the feedback (V_{FB}) terminal and ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right)$$

For most applications, an 80k resistor is suggested for R1. To prevent stray pickup, locate resistors R1 and R2 close to the LTC1874.

Foldback Current Limiting

As described in the Output Diode Selection, the worst-case dissipation occurs with a short-circuited output when the diode conducts the current limit value almost continuously. To prevent excessive heating in the diode, foldback current limiting can be added to reduce the current in proportion to the severity of the fault.

Foldback current limiting is implemented by adding diodes D_{FB1} and D_{FB2} between the output and the I_{TH}/RUN pin as shown in Figure 5. In a hard short (V_{OUT} = 0V), the current will be reduced to approximately 50% of the maximum output current.

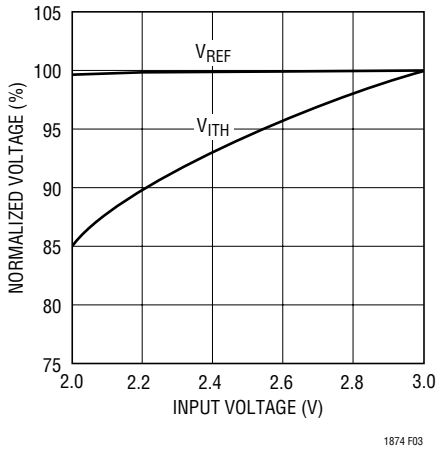


Figure 3. Line Regulation of V_{REF} and V_{ITH}

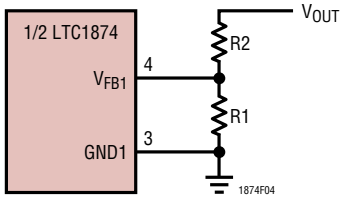


Figure 4. Setting Output Voltage

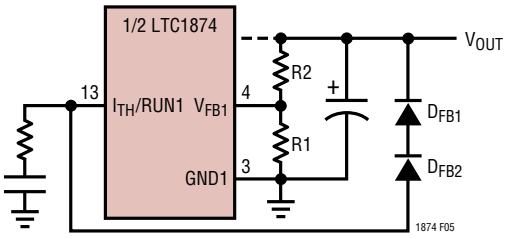


Figure 5. Foldback Current Limiting

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1874. These items are illustrated graphically for a single controller in the layout diagram in Figure 6. Check the following in your layout:

1. Is the Schottky diode closely connected between power ground (PGND) and the drain of the external MOSFET?
2. Does the (+) plate of C_{IN} connect to the sense resistor as closely as possible? This capacitor provides AC current to the MOSFET.
3. Is the input decoupling capacitor (0.1µF) connected closely between V_{IN} and signal ground (GND)?
4. Connect the end of R_{SENSE} as close to V_{IN} as possible. The V_{IN} pin is the SENSE$^+$ of the current comparator.
5. Is the trace from SENSE$^-$ to the SENSE resistor kept short? Does the trace connect close to R_{SENSE}?
6. Keep the switching node PGATE away from sensitive small signal nodes.
7. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.
8. PV_{IN} must connect to V_{IN} and PGND must connect to GND. Isolate high current power paths from signal power and signal ground where possible in the layout. An unbroken ground plane is recommended.

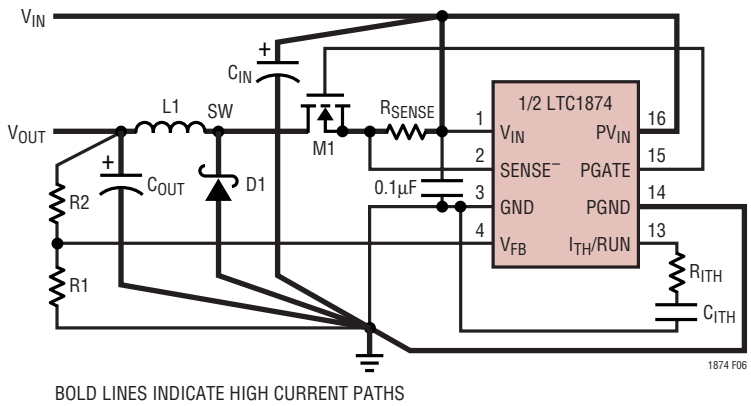
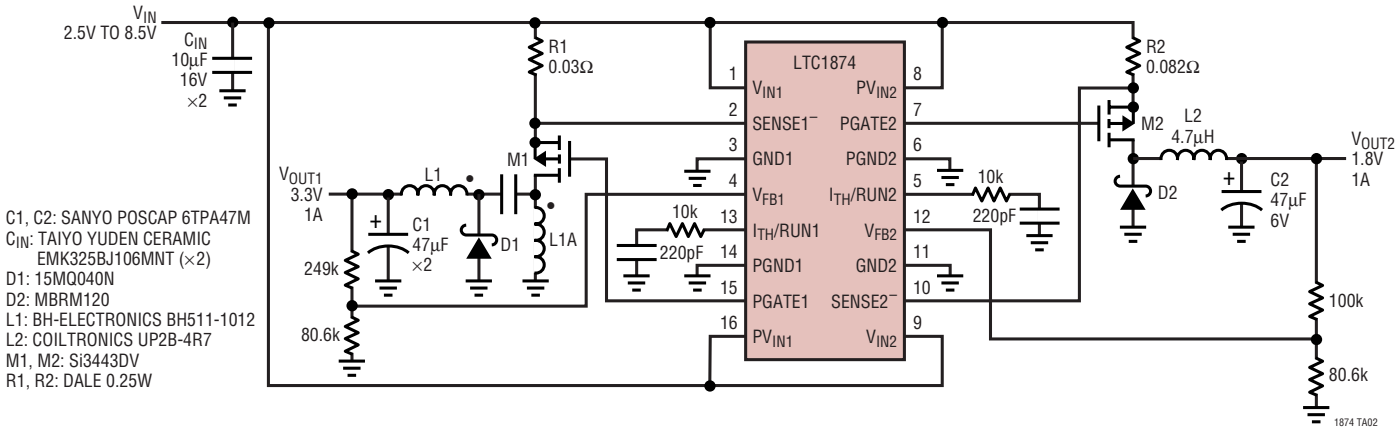


Figure 6. LTC1874 Layout Diagram (See PC Board Layout Checklist)

TYPICAL APPLICATION

LTC1874 2.5V–8.5V Input to 3.3V/1A and 1.8V/1A Dual Converter

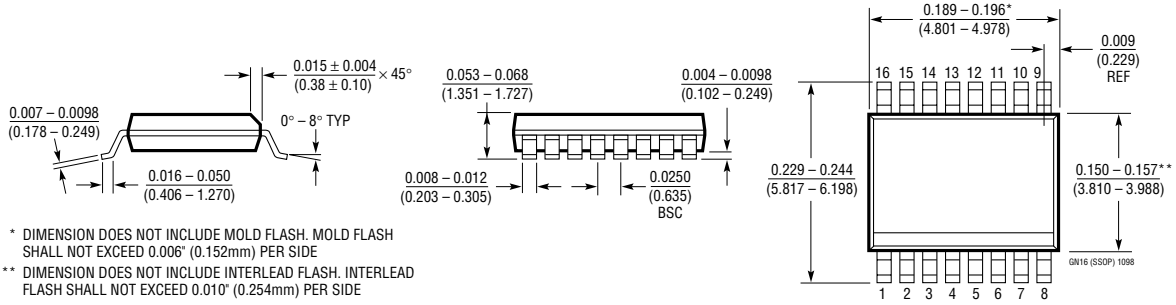


C1, C2: SANYO POSCAP 6TPA47M
C_{IN}: TAIYO YUDEN CERAMIC EMK325BJ106MNT (×2)
D1: 15MQ040N
D2: MBRM120
L1: BH-ELECTRONICS BH511-1012
L2: COILTRONICS UP2B-4R7
M1, M2: Si3443DV
R1, R2: DALE 0.25W

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1147 Series	High Efficiency Step-Down Switching Regulator Controllers	100% Duty Cycle, 3.5V ≤ V_{IN} ≤ 16V
LTC1622	Synchronizable Low Input Voltage Current Mode Step-Down DC/DC Controller	V_{IN} 2V to 10V, I_{OUT} Up to 4.5A, Burst Mode Operation Optional, 8-Lead MSOP
LTC1624	High Efficiency SO-8 N-Channel Switching Regulator Controller	8-Pin N-Channel Drive, 3.5V ≤ V_{IN} ≤ 36V
LTC1625	No R_{SENSE}™ Synchronous Step-Down Regulator	97% Efficiency, No Sense Resistor; Up to 10A
LTC1626	Low Voltage, High Efficiency Step-Down DC/DC Converter	Monolithic, Constant Off-Time, Low Voltage Range: 2.5V to 6V
LTC1628	Dual, 2-Phase Synchronous Step-Down Controller	Minimum C_{IN} and C_{OUT}, 3.5V ≤ V_{IN} ≤ 36V
LTC1735	Single, High Efficiency, Low Noise Synchronous Switching Controller	High Efficiency 5V to 3.3V Conversion at up to 15A
LT1767	1.5A, 500kHz Step-Down Switching Regulators	High Frequency, Small Inductor, High Efficiency
LTC1772	Constant Frequency Current Mode Step-Down DC/DC Controller	V_{IN} 2.5V to 9.8V, I_{OUT} Up to 4A, SOT-23 Package
LTC1773	Synchronous Step-Down Controller	V_{IN} 2.65V to 8.5V, I_{OUT} up to 4A
LTC1877/LTC1878	Low Voltage, Monolithic Synchronous Step-Down Regulator	Low Supply Voltage Range: 2.65V to 8V, I_{OUT} = 0.5A

No R_{SENSE} is a trademark of Linear Technology Corporation.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
1874f LT/TP 0201 4K • PRINTED IN USA