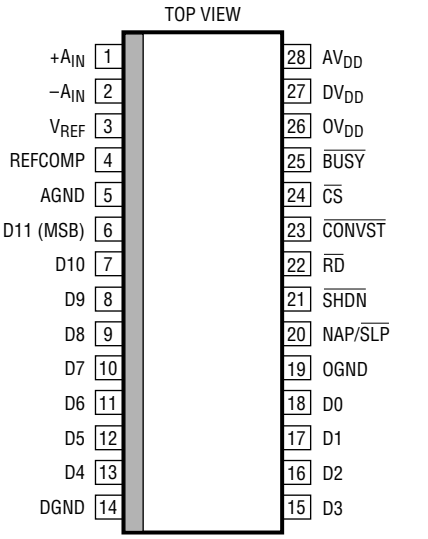
ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} =OV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Analog Input Voltage (Note 3) ..... – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... – 0.3V to 12V
Digital Output Voltage ..... – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1415C ..... 0°C to 70°C
LTC1415I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 110°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER

LTC1415CG
LTC1415CSW
LTC1415IG
LTC1415ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 7)	●		0.35	±1	LSB
Differential Linearity Error		●		0.25	±1	LSB
Offset Error	(Note 8)	 ●		±1	±6 ±8	LSB LSB
Full-Scale Error					±20	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0			±15		ppm/°C

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V	●		4.096		V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions During Conversions			19 5		pF pF
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	150	ns
t_{AP}	Sample-and-Hold Aperture Delay Time				–1.5		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				2		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	0V < V_{CM} < V_{DD}, DC to MHz			60		dB

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-(Noise + Distortion) Ratio	100kHz Input Signal 600kHz Input Signal			72 69		dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First 5 Harmonics 600kHz Input Signal, First 5 Harmonics			–80 –72		dB dB
SFDR	Spurious Free Dynamic Range	600kHz Input Signal			–75		dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			–84		dB
	Full-Power Bandwidth				18		MHz
	Full-Linear Bandwidth	S/(N + D) ≥ 68dB			1		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0			±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V			0.01		LSB/V
V_{REF} Output Resistance	$\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
REFCOMP Output Voltage	I_{OUT} = 0			4.096		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = –10µA I_O = –200µA	 ●	 4.0	 4.5 	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●	 	 0.05 0.10	 0.4	 V V
I_{OZ}	Hi-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage	(Notes 10, 11)		4.75		5.25	V
I_{DD}	Supply Current Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V (Note 12) $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V (Note 12)	● ●		11 1.5 1.0	20 2.3	mA mA µA
P_D	Power Dissipation Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V			55 7.5 0.01	100 12	mW mW mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	1.25			MHz
	Conversion and Acquisition Time		●			800	ns
t_{CONV}	Conversion Time		●			700	ns
t_{ACQ}	Acquisition Time		●			150	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 10)	●	10			ns
t_3	NAP/$\overline{SLP}\uparrow$ to $\overline{SHDN}\downarrow$ Setup Time	(Notes 9, 10)			200		ns
t_4	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	Nap Mode (Note 10)			200		ns
		Sleep Mode, $C_{REFCOMP}$ = 10µF (Note 10)			10		ms
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	50			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			10		ns
			●			60	ns
t_7	Data Ready Before $\overline{BUSY}\uparrow$			20	35		ns
			●	15			ns
t_8	Delay Between Conversions	(Note 10)	●	50			ns
t_9	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 10)	●	–5			ns
t_{10}	Data Access Time After $\overline{RD}\downarrow$	C_L = 25pF			20	35	ns
			●			45	ns
		C_L = 100pF			25	45	ns
			●			60	ns
t_{11}	Bus Relinquish Time				10	30	ns
		0°C = T_A = 70°C	●			35	ns
		–40°C = T_A = 85°C	●			40	ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	50			ns
t_{14}	Aperture Delay of Sample-and-Hold				–1.5		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together unless otherwise noted.

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below ground or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below ground, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SAMPLE} = 1.25MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $-A_{IN}$ grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

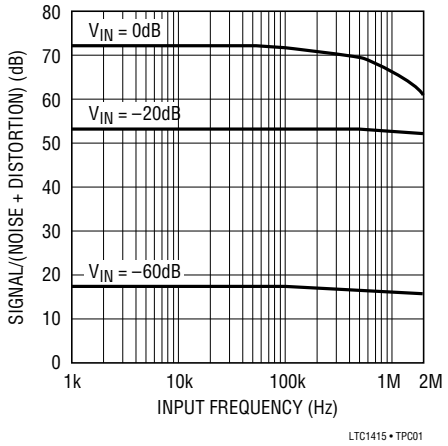
Note 10: Recommended operating conditions.

Note 11: The falling edge of $\overline{CONVST}$ starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 425ns after the start of the conversion or after $\overline{BUSY}$ rises.

Note 12: $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V.

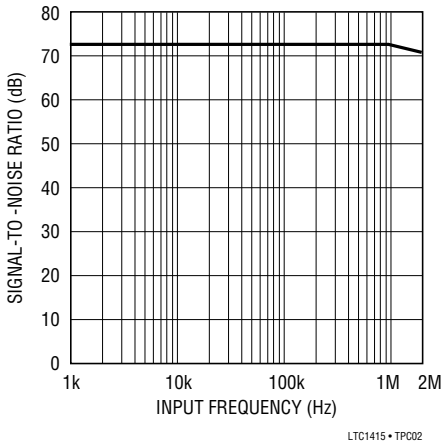
TYPICAL PERFORMANCE CHARACTERISTICS

S/(N + D) vs Input Frequency and Amplitude



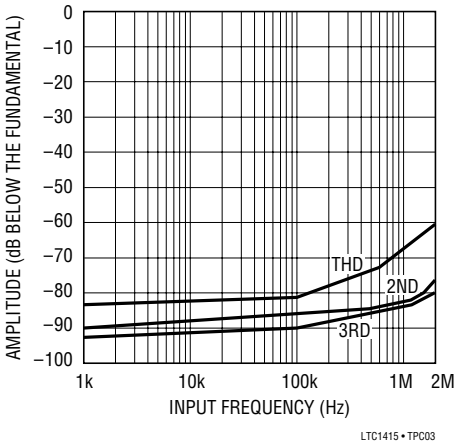
LTC1415 • TPC01

Signal-to-Noise Ratio vs Input Frequency



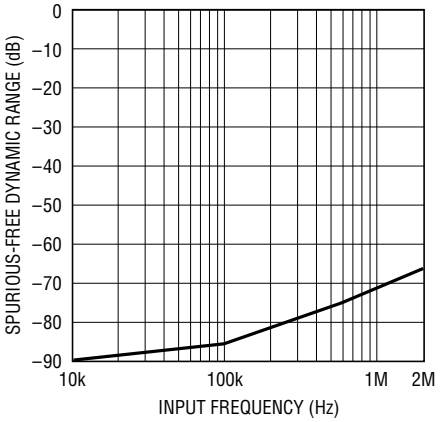
LTC1415 • TPC02

Distortion vs Input Frequency



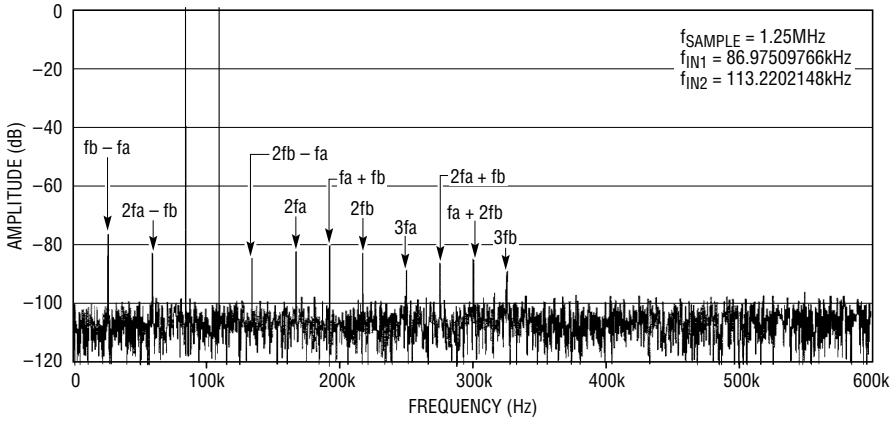
LTC1415 • TPC03

Spurious-Free Dynamic Range vs Input Frequency



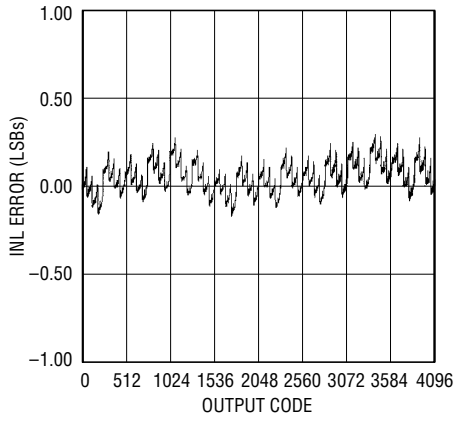
LTC1415 • TPC04

Intermodulation Distortion Plot



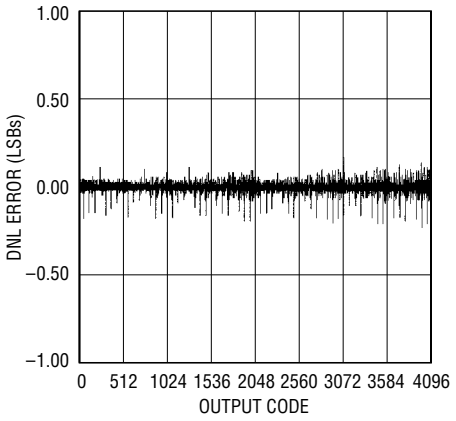
LTC1415 • TPC05

Integral Nonlinearity vs Output Code



LTC1415 • TPC07

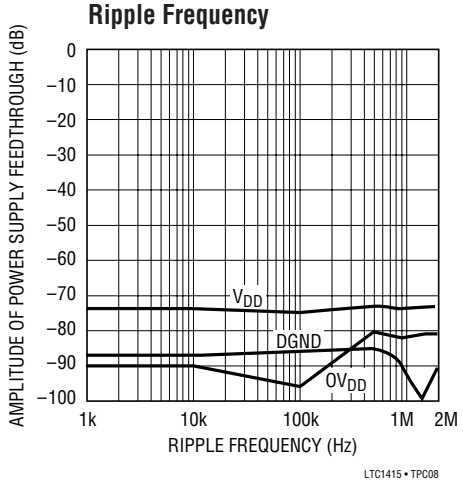
Differential Nonlinearity vs Output Code



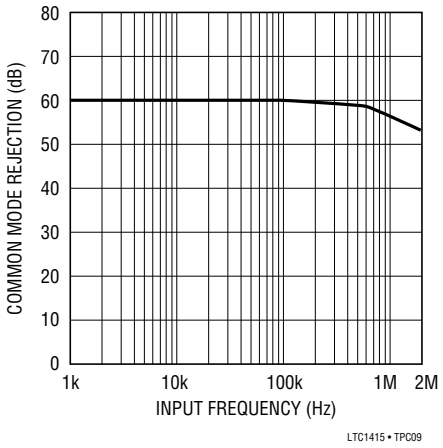
LTC1415 • TPC06

TYPICAL PERFORMANCE CHARACTERISTICS

Power Supply Feedthrough vs Ripple Frequency



Input Common Mode Rejection vs Input Frequency



PIN FUNCTIONS

$+A_{IN}$ (Pin 1): Positive Analog Input, 0V to 4.096V.

$-A_{IN}$ (Pin 2): Negative Analog Input, 0V to 4.096V.

V_{REF} (Pin 3): 2.50V Reference Output.

REFCOMP (Pin 4): Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

OGND (Pin 19): Digital Output Buffer Ground.

NAP/$\overline{SLP}$ (Pin 20): Power Shutdown Mode. High for quick wake-up Nap mode.

$\overline{SHDN}$ (Pin 21): Power Shutdown Input. A low logic level will invoke the Shutdown mode selected by the NAP/$\overline{SLP}$ pin. Tie high if unused.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge.

$\overline{CS}$ (Pin 24): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

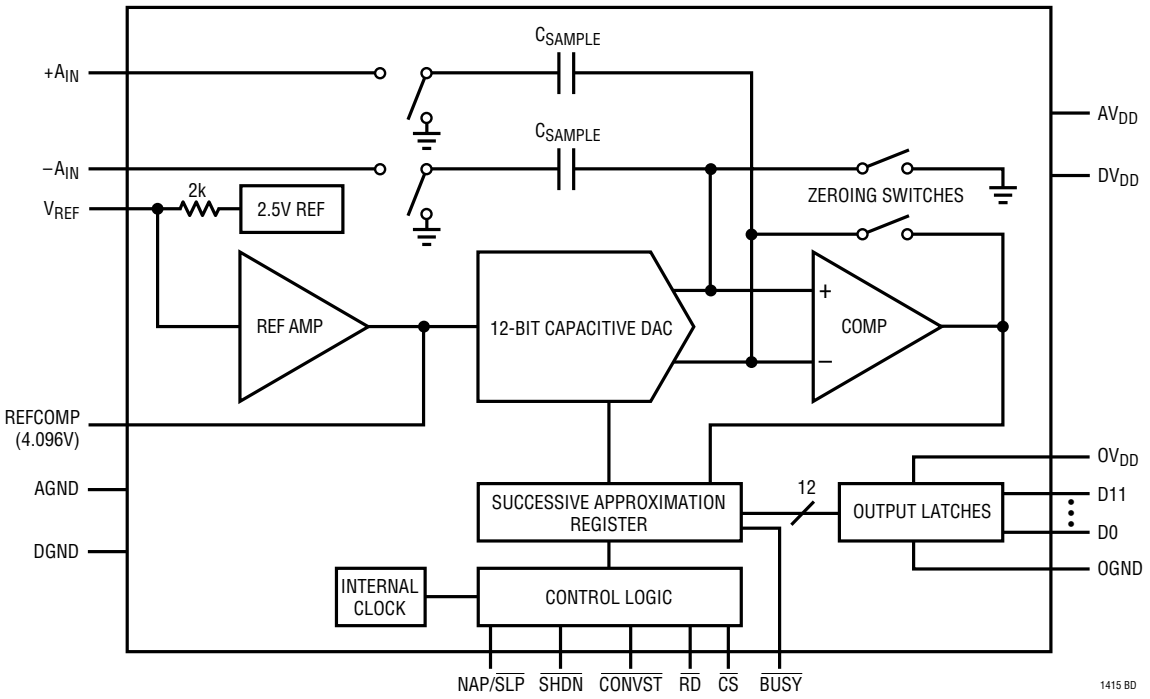
$\overline{BUSY}$ (Pin 25): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. Its rising edge may be used to latch the output data.

OV_{DD} (Pin 26): Digital output buffer supply. Short to Pin 28 for 5V output. Tie to 3V for driving 3V logic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to Pin 28.

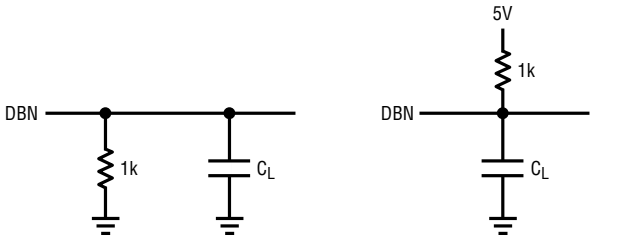
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS

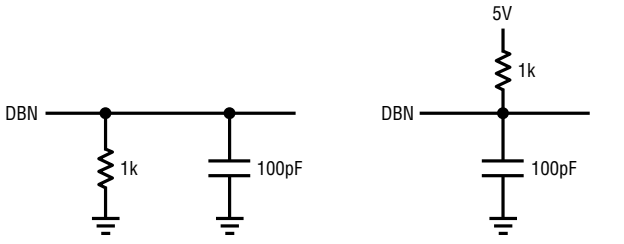
Load Circuits for Access Timing



(A) Hi-Z TO V_{OH} AND V_{OL} TO V_{OH} (B) Hi-Z TO V_{OL} AND V_{OH} TO V_{OL}

1415 TC01

Load Circuits for Bus Relinquish Time



(A) V_{OH} TO Hi-Z (B) V_{OL} TO Hi-Z

1415 TC02

APPLICATIONS INFORMATION

CONVERSION DETAILS

The LTC1415 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs (please refer to Digital Interface section for the data format).

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of the conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During the conversion, the internal differential 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the $+A_{IN}$ and $-A_{IN}$ inputs are connected to the sample-and-hold capacitors (C_{SAMPLE}) during the acquire phase and the comparator offset is nulled by the zeroing switches. In this acquire phase, a minimum delay of 150ns will provide enough time for the sample-and-hold capacitors to acquire the analog signal. During the convert phase the comparator zeroing switches open, putting the comparator into compare mode. The input switches the connect C_{SAMPLE} capacitors to ground, transferring the differential analog input charge onto the summing junction. This input charge is successively compared with the binary weighted charges supplied by the differential capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the differential DAC output balances the $+A_{IN}$ and $-A_{IN}$ input charges. The SAR contents (a 12-bit data word) which represents the difference of $+A_{IN}$ and $-A_{IN}$ are loaded into the 12-bit output latches.

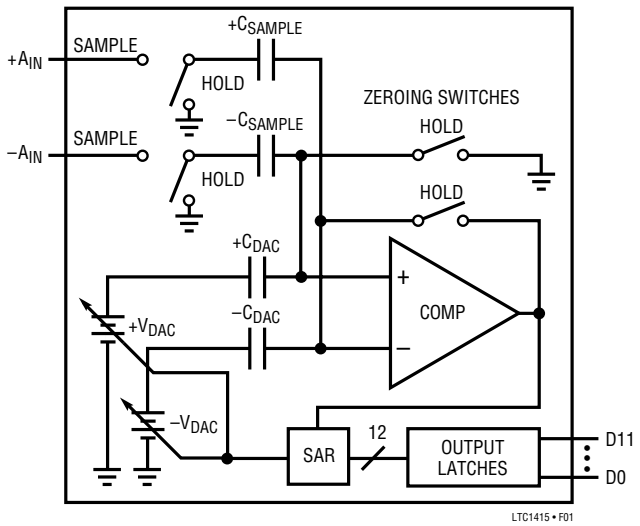


Figure 1. Simplified Block Diagram

DYNAMIC PERFORMANCE

The LTC1415 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using a FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1415 FFT plot.

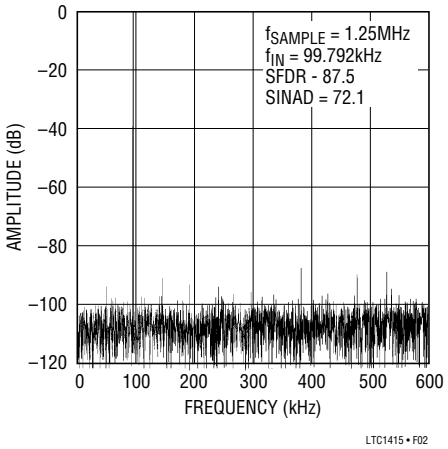


Figure 2. LTC1415 Nonaveraged, 4096 Point FFT

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] or SINAD is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies from above DC and below half the sampling frequency. Figure 2 shows a typical spectral content with a 1.25MHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 625kHz.

APPLICATIONS INFORMATION

Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 1.25MHz the LTC1415 maintains very good ENOBs up to the Nyquist input frequency of 625kHz (refer to Figure 3).

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20Log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots Vn^2}}{V1}$$

where V1 is the RMS amplitude of the fundamental frequency and V2 through Vn are the amplitudes of the second through nth harmonics. THD vs input frequency is shown in Figure 4. The LTC1415 has good distortion performance up to the Nyquist frequency and beyond.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by

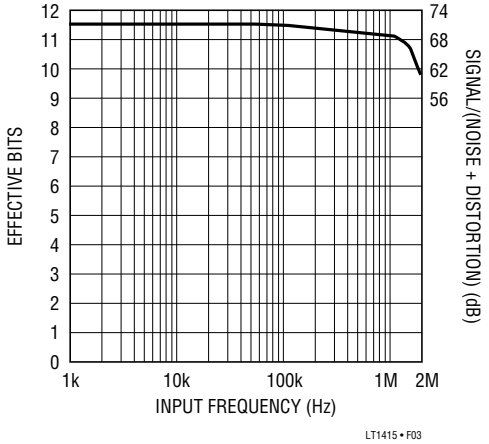


Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

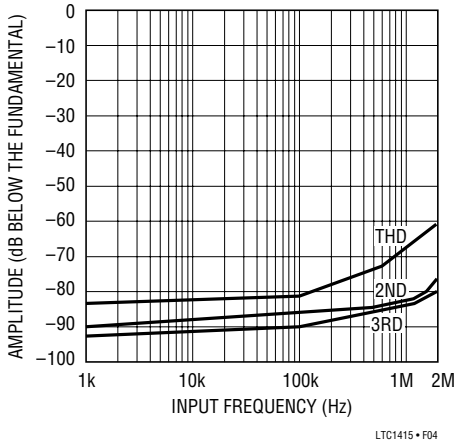


Figure 4. Distortion vs Input Frequency

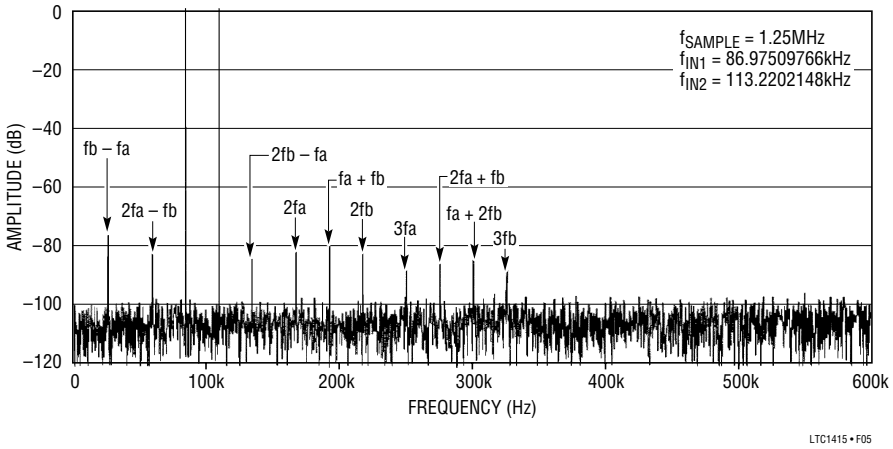


Figure 5. Intermodulation Distortion Plot

APPLICATIONS INFORMATION

the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa + – nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(fa + fb) = 20Log \frac{\text{Amplitude at (fa + fb)}}{\text{Amplitude at fa}}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal.

The full-linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1415 has been designed to optimize input bandwidth, allowing the ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The differential analog inputs of the LTC1415 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $–A_{IN}$ input is grounded). The $+A_{IN}$ and $–A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common mode to both inputs will be reduced by the common mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1415 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 6). For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 150ns for full throughput rate).

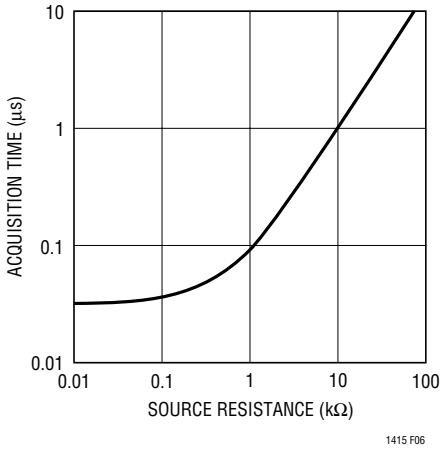


Figure 6. Acquisition Time vs Source Resistance

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz should be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions.

The best choice for an op amp to drive the LTC1415 will depend on the application. Generally applications fall into two categories: AC applications where dynamic specifications are most critical and time domain applications where DC accuracy and settling time are most critical.

APPLICATIONS INFORMATION

The following list is a summary of the op amps that are suitable for driving the LTC1415, more detailed information is available in the Linear Technology databooks and the LinearView™ CD-ROM.

LT®1215/LT1216: Dual and quad 23MHz, 50V/µs single supply op amps. Single 5V to ±15V supplies, 6.6mA specifications, 90ns settling to 0.5LSB.

LT1223: 100MHz video current feedback amplifier. ±5V to ±15V supplies, 6mA supply current. Low distortion up to and above 400kHz. Low noise. Good for AC applications.

LT1227: 140MHz video current feedback amplifier. ±5V to ±15V supplies, 10mA supply current. Lowest distortion at frequencies above 400kHz. Low noise. Best for AC applications.

LT1229/LT1230: Dual and quad 100MHz current feedback amplifiers. ±2V to ±15V supplies, 6mA supply current each amplifier. Low noise. Good AC specs.

LT1360: 37MHz voltage feedback amplifier. ±5V to ±15V supplies. 3.8mA supply current. Good AC and DC specs. 70ns settling to 0.5LSB.

LT1363: 50MHz, 450V/µs op amps. ±5V to ±15V supplies. 6.3mA supply current. Good AC and DC specs. 60ns settling to 0.5LSB.

LT1364/LT1365: Dual and quad 50MHz, 450V/µs op amps. ±5V to ±15V supplies, 6.3mA supply current per amplifier. 60ns settling to 0.5LSB.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1415 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example Figure 7 shows a 1000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor to limit the input bandwidth to 1.6MHz. The 1000pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

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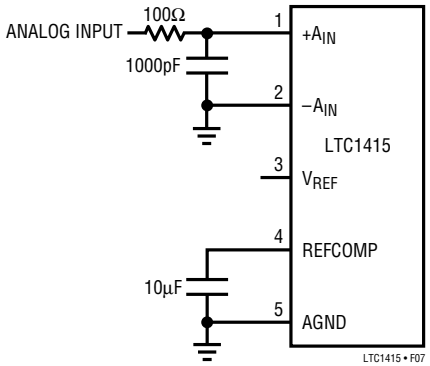

Figure 7. RC Input Filter

Input Range

The 4.096V input range of the LTC1415 is optimized for low noise. Most single supply op amps also perform well over this same range, allowing direct coupling to the analog inputs and eliminating the need for special translation circuitry.

Some applications may require other input ranges. The LTC1415 differential inputs and reference circuitry can accommodate other input ranges often with little or no additional circuitry. The following sections describe the reference and input circuitry and how they affect the input range.

Internal Reference

The LTC1415 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.500V. It is connected internally to a reference amplifier and is available at V_{REF} (Pin 3) see Figure 8a. A 2k resistor is in series with the output so that it can be easily overdriven by an external reference or other

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circuitry. The reference amplifier gains the voltage at the V_{REF} pin by 1.638 to create the required internal reference voltage of 4.096V. This provides buffering between the V_{REF} pin and the high speed capacitive DAC. The reference amplifier compensation pin (REFCOMP, Pin 4) must be bypassed with a capacitor to ground. The reference amplifier is stable with capacitors of 1µF or greater. For the best noise performance a 10µF ceramic or tantalum in parallel with a 0.1µF ceramic is recommended.

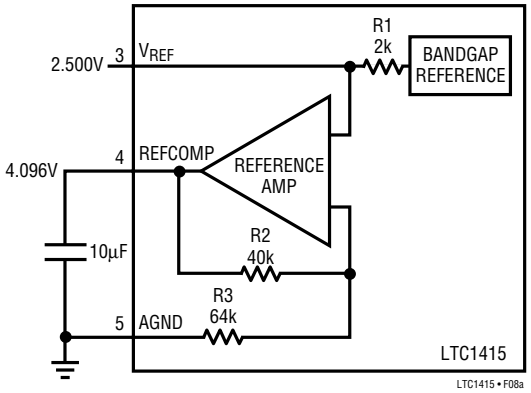

Figure 8a. LTC1415 Reference Circuit

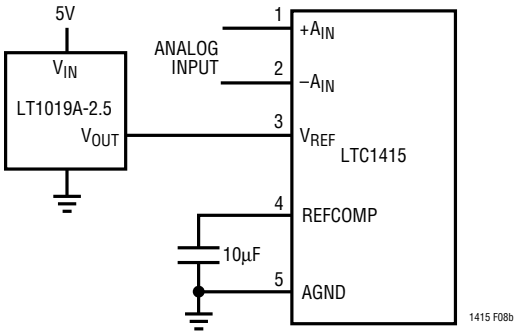

Figure 8b. Using the LT1019-2.5 as an External Reference

The V_{REF} pin can be driven with a DAC or other means shown in Figure 9. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio. The filtering of the internal LTC1415 reference amplifier will limit the bandwidth and settling time of this circuit. A settling time of 5ms should be allowed for after a reference adjustment.

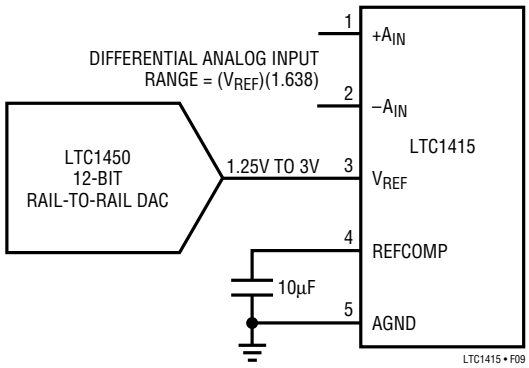

Figure 9. Driving V_{REF} with a DAC to Adjust Full Scale

Differential Inputs

The LTC1415 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The ADC will always convert the difference of $+A_{IN} – (–A_{IN})$ independent of the common mode voltage. The common mode rejection is constant from DC to 1MHz, see Figure 10a. The only requirement is that both inputs can not exceed the AV_{DD} or AGND power supply voltages. Integral nonlinearity errors (INL) and differential nonlinearity errors (DNL) are independent of the common mode voltage, however, the bipolar zero error (BZE) will vary. The change in BZE is typically less than 0.1% of the common mode voltage.

Differential inputs allow greater flexibility for accepting different input ranges. Figure 10b shows a circuit that shifts the input range up in voltage by 200mV. This can be useful in applications where the amplifier driving the ADC input is not able to swing all the way to ground, because of output loading or settling time issues.

Some AC applications may have their performance limited by distortion. Most circuits exhibit higher distortion when signals approach the supply or ground. Distortion can be reduced by reducing the signal amplitude and keeping the common mode voltage at approximately midsupply. The circuit of Figure 10c reduces the ADC full scale from

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4.096V to 2.048V and shifts the common mode voltage from half of full scale to 2.274V.

AC Coupled Inputs

The analog inputs can be AC coupled for applications where the input has no DC information. The input of the ADC does need to be DC biased at midscale. Figures 10d and 10e demonstrate AC coupling and the required biasing. Figure 10d shows the ADC with a full scale of 4.096V, a common mode voltage of 2.048V and an input that swings from 0V to 4.096V. This circuit has the lowest noise (SINAD = 72dB to 100kHz) but will have distortion

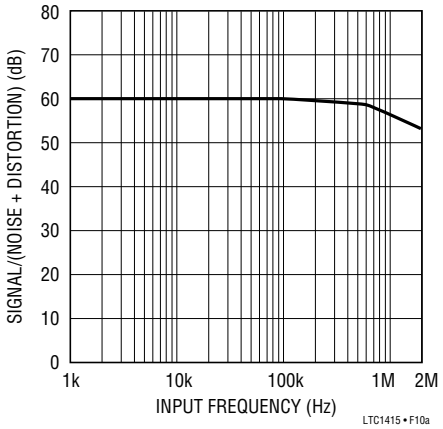

Figure 10a. CMRR vs Input Frequency

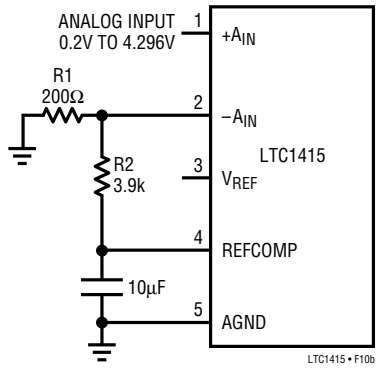

Figure 10b. Shifting the Input Range Up from Ground by 200mV

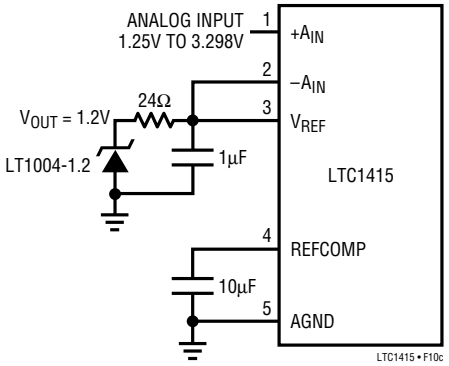

Figure 10c. 2.048V Input Range with a Common Mode Voltage of 2.274V. For Low Distortion AC Applications

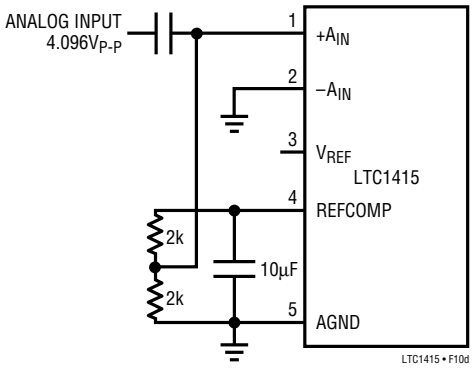

Figure 10d. 4.096V_{P-P} Input Range with AC Coupling. For Low Noise AC Applications

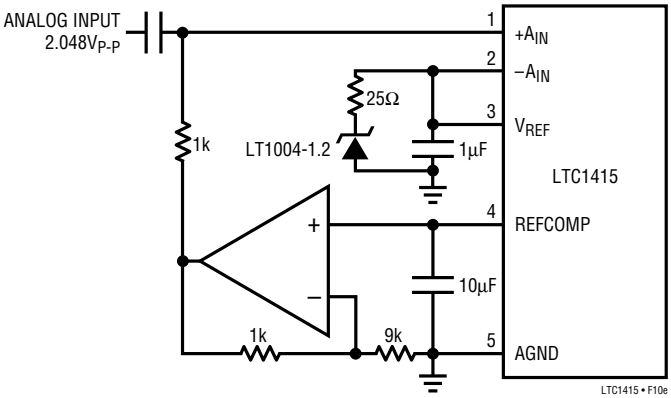

Figure 10e. 2.048V_{P-P} Input Range with AC Coupling. For Low Distortion AC Applications

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limitations at high input frequencies (THD = 75dB at 600kHz). The ADC in Figure 10e has a full scale of 2.048V and a common mode of 2.27V. The reduced signal swing of this circuit results in improved distortion at higher input frequencies (THD = 82dB at 600kHz) but with worse SINAD at low frequencies (SINAD = 70dB at 100kHz).

Full-Scale and Offset Adjustment

Figure 11a shows the ideal input/output characteristics for the LTC1415. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB,... FS – 1.5LSB, FS – 0.5LSB). The output is straight binary with 1LSB = FS/4096 = 4.096V/4096 = 1mV.

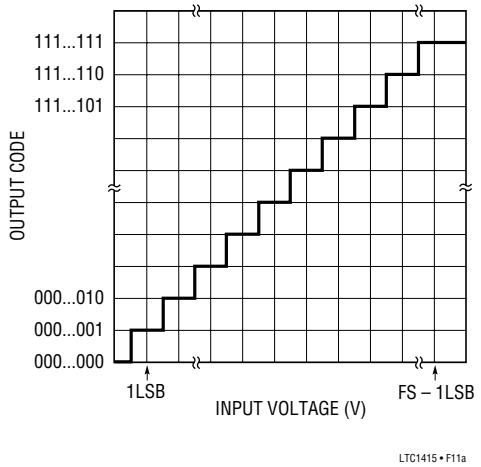

Figure 11a. LTC1415 Transfer Characteristics

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 11b shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the $-A_{IN}$ input. For zero offset error apply 0.5mV (i.e., 0.5LSB) at $+A_{IN}$ and adjust the offset at the $-A_{IN}$ input (R8) until the output code flickers between 0000 0000 0000 and 0000 0000 0001. For full-scale adjustment, an input voltage of 4.0945V (FS – 1.5LSBs) is applied to the analog input and R7 is adjusted until

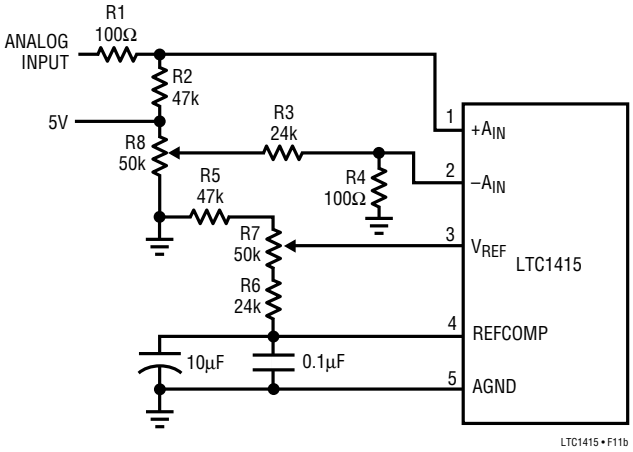

Figure 11b. Offset and Full-Scale Adjust Circuit

the output code flickers between 1111 1111 1110 and 1111 1111 1111.

BOARD LAYOUT AND GROUNDING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1415, a printed circuit board with ground plane is required. The ground plane under the ADC area should be as free of breaks and holes as possible, such that a low impedance path between all ADC grounds and all ADC decoupling capacitors is provided. It is critical to prevent digital noise from being coupled to the analog input, reference or analog power supply lines. Layout should ensure that digital and analog signal lines are separated as much as possible. Particular care should be taken not to run any digital track alongside an analog signal track.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 5 (AGND), Pin 14 and Pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. The REFCOMP bypass capacitor and the DV_{DD} bypass capacitor should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil

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width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1415 has differential inputs to minimize noise coupling. Common mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1415 will hold and convert the difference voltage between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (Pin 1) and $-A_{IN}$ (Pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

SUPPLY BYPASSING

High quality, low series resistance ceramic, 10µF bypass capacitors should be used at the V_{DD} and REFCOMP pins as shown in the Typical Application on the fist page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively 10µF tantalum capacitors in parallel with 0.1µF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figures 13a, 13b, 13c and 13d show the schematic and layout of a suggested evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a two layer printed circuit board.

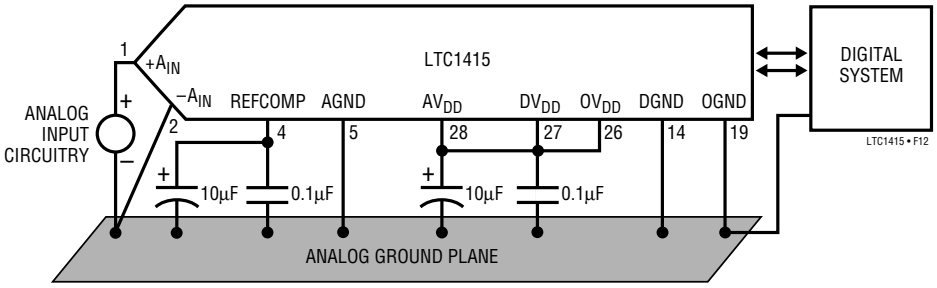

Figure 12. Power Supply Grounding Practice

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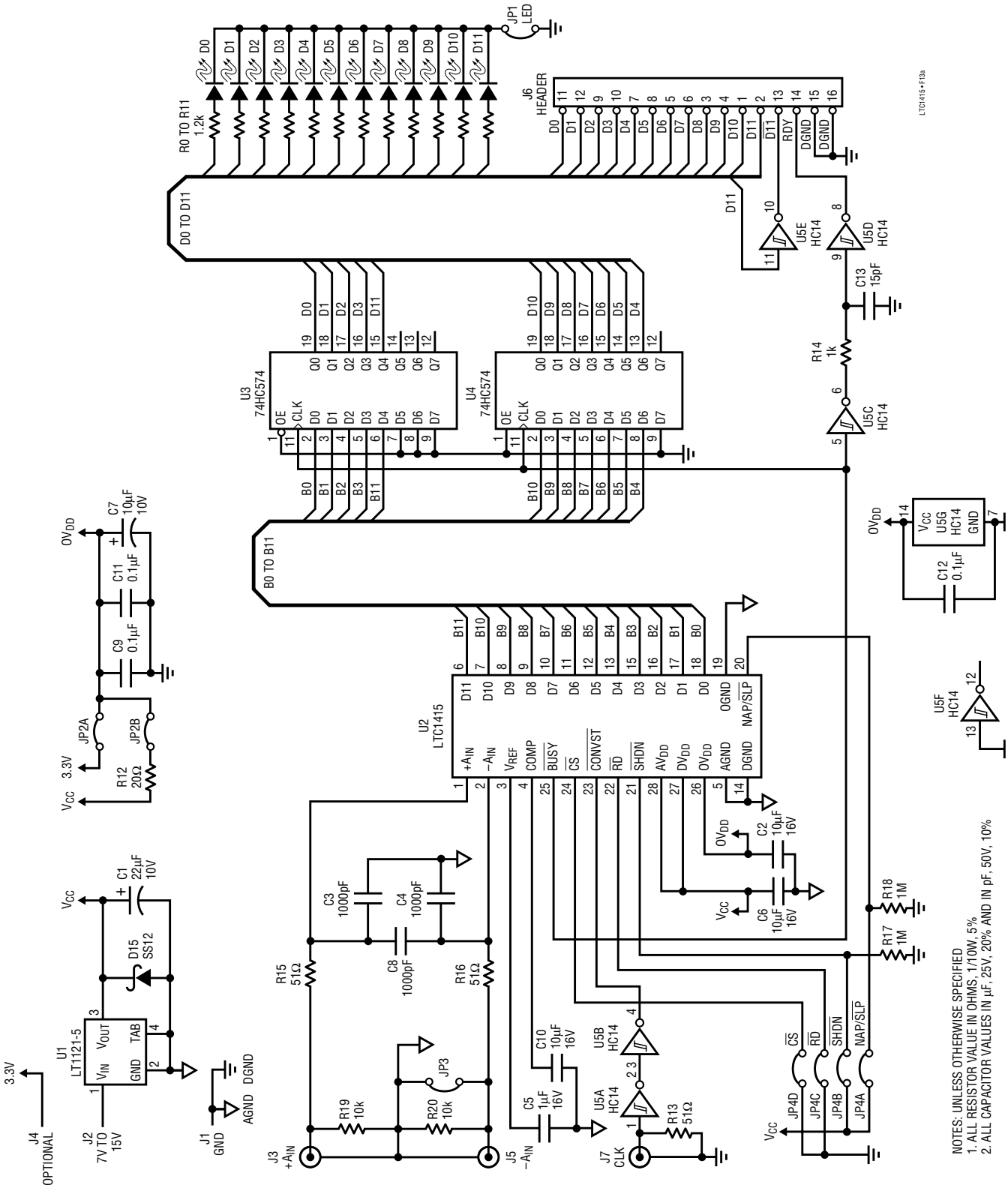

Figure 13a. Suggested Evaluation Circuit Schematic

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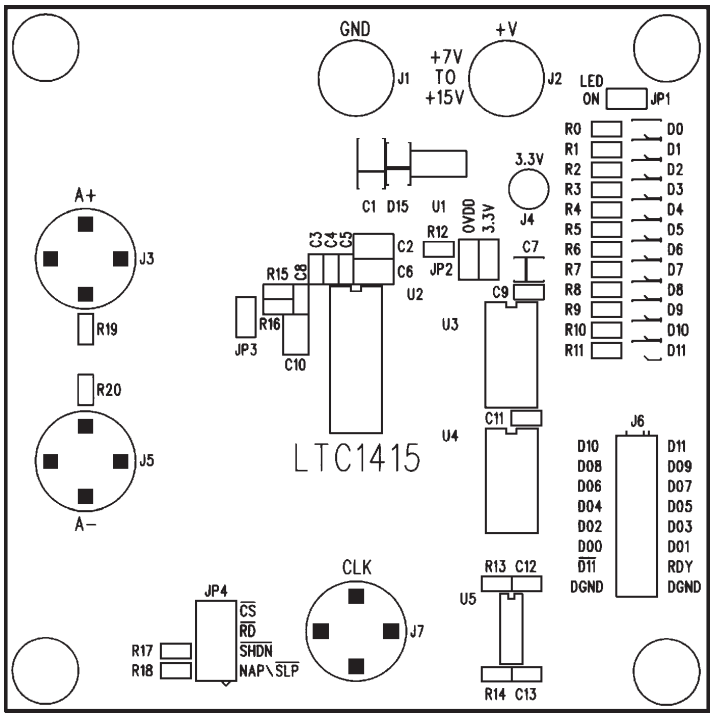

Figure 13b. Suggested Evaluation Circuit Board Component Side Silkscreen

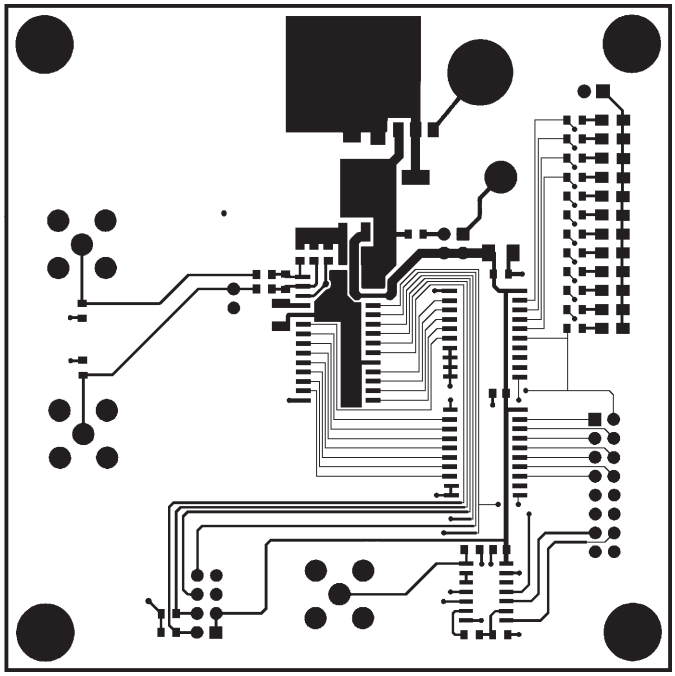

Figure 13c. Suggested Evaluation Circuit Board Component Side Layout

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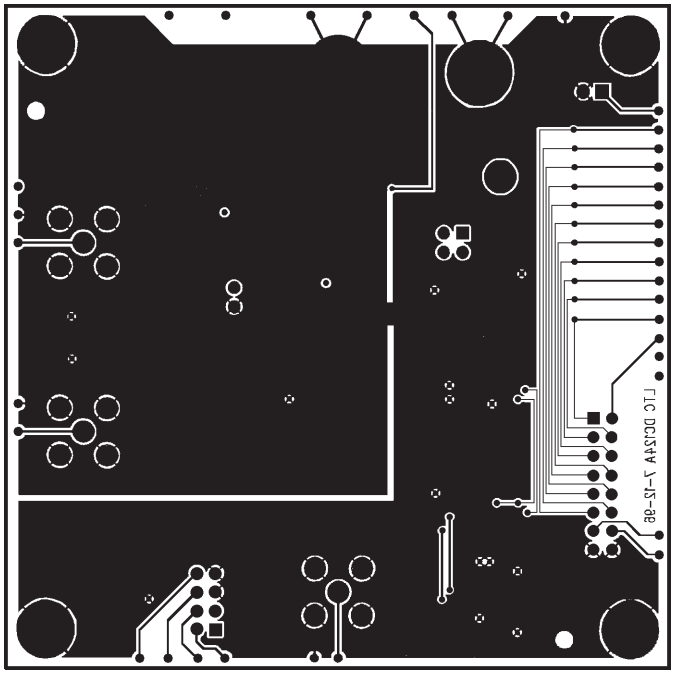

Figure 13d. Suggested Evaluation Circuit Board Solder Side Layout

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.70µs and a maximum conversion time over the full operating temperature range of 0.75µs. No external adjustments are required. The guaranteed maximum acquisition time is 150ns. In addition, a throughput time of 800ns and a minimum sampling rate of 1.25Msps are guaranteed.

Power Shutdown

The LTC1415 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 87% and leaves only the digital logic and reference powered up. The wake-up time from Nap to active is 200ns. Follow the setup time shown in Figure 14a to avoid inadvertently invoking Sleep mode. In Sleep mode all bias currents are shut down and only leakage current remains, about 1µA. Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle to 0.01% for full 12-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (Pin 4). The wake-up time is 10ms with the recommended 10µF capacitor. Shutdown is controlled by Pin 21 ($\overline{SHDN}$); the ADC is in shutdown when it is low. The shutdown mode is selected with Pin 20 (NAP/$\overline{SLP}$); high selects Nap.

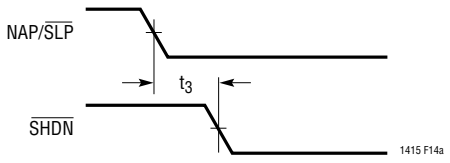

Figure 14a. NAP/$\overline{SLP}$ to $\overline{SHDN}$ Timing

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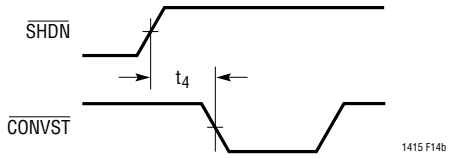


Figure 14b. SHDN to CONVST Wake-Up Timing

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: CONVST, CS and RD. A logic "0" applied to the CONVST pin will start a conversion after the ADC has been selected (i.e., CS is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the BUSY output. BUSY is low during a conversion.

Figures 16 through 20 show several different modes of operation. In modes 1a and 1b (Figures 16 and 18) CS and RD are both tied low. The falling edge of CONVST starts the conversion. The data outputs are always enabled and data can be latched with the BUSY rising edge. Mode 1a shows operation with a narrow logic low CONVST pulse. Mode 1b shows a narrow logic high CONVST pulse.

In mode 2 (Figure 18) CS is tied low. The falling edge of the CONVST signal again starts the conversion. Data outputs are in three-state until read by the MPU with the RD signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 19 and 20) CS is tied low and CONVST and RD are tied together. The MPU starts the conversion and reads the output with the RD signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to RD (= CONVST), starting the conversion. BUSY goes low, forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; BUSY goes high, releasing the processor and the processor takes RD (= CONVST) back high and reads the new conversion data.

In ROM mode, the processor takes RD (= CONVST) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

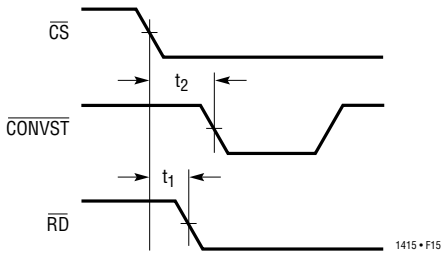


Figure 15. CS to CONVST Setup Timing

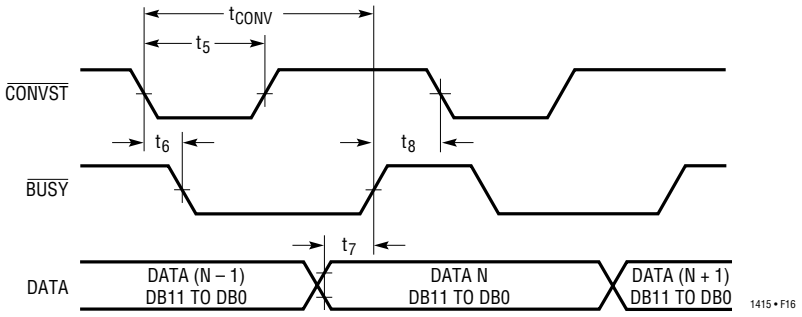


Figure 16. Mode 1a CONVST Starts a Conversion. Data Outputs Always Enabled

APPLICATIONS INFORMATION

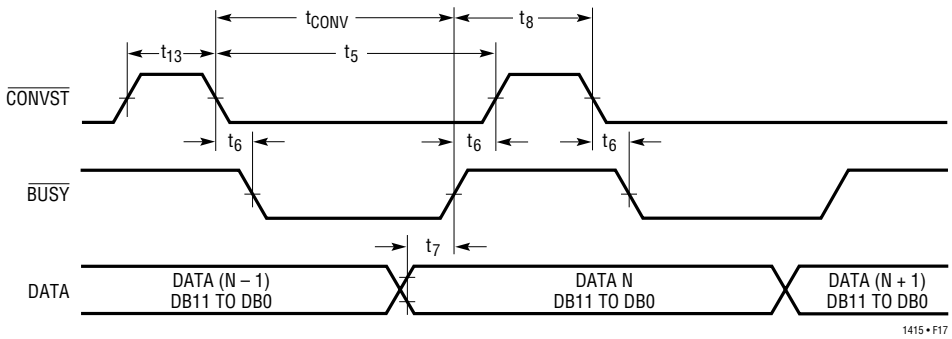


Figure 17. Mode 1b $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

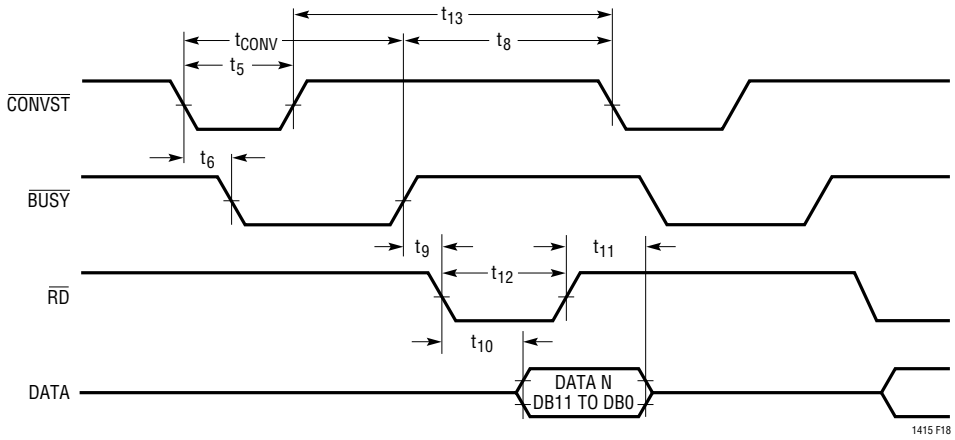


Figure 18. Mode 2 $\overline{\text{CONVST}}$ Starts a Conversion. Data is Read by $\overline{\text{RD}}$

APPLICATIONS INFORMATION

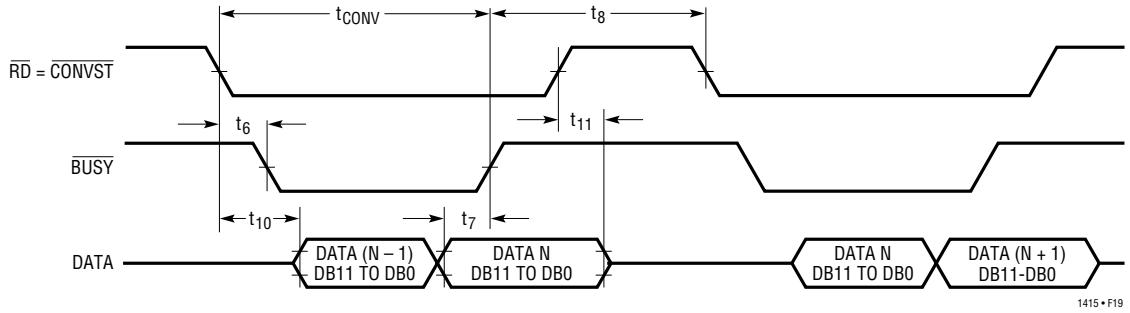


Figure 19. Slow Memory Mode Timing

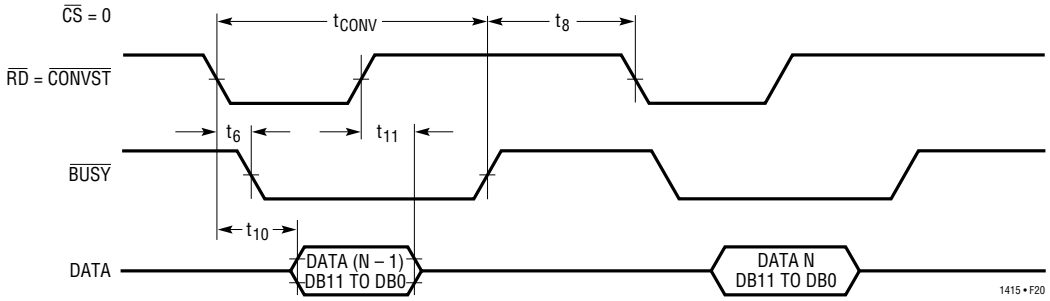
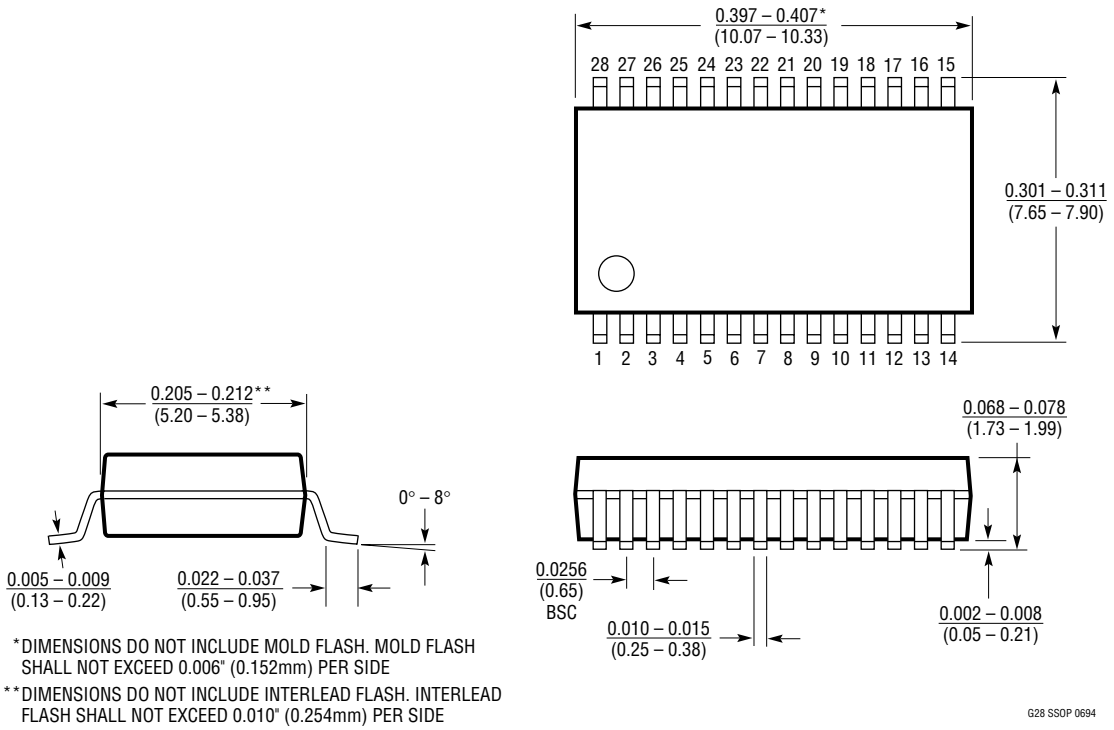


Figure 20. ROM Mode Timing

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



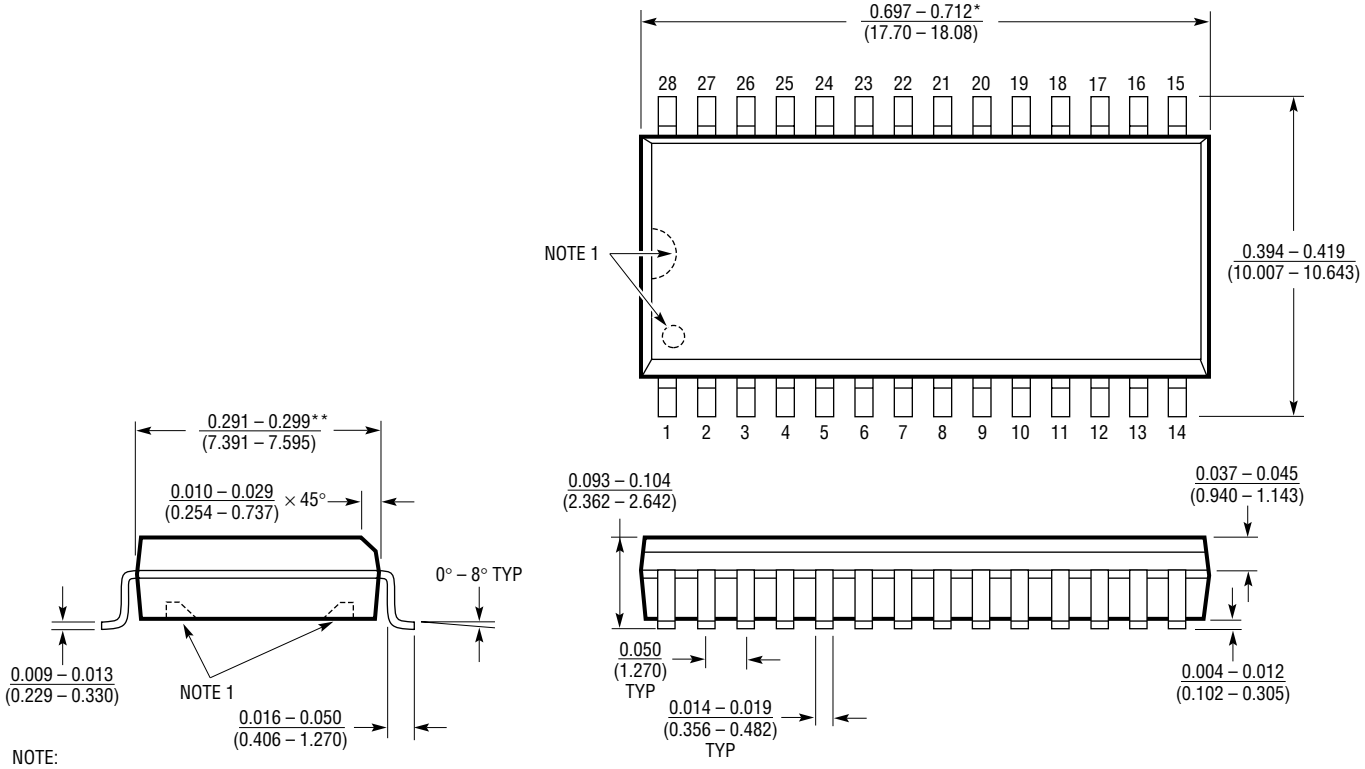
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

SW Package
28-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS. THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S28 (WIDE) 0996

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1273/75/76	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	Lower Power 75mW and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/77	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power (10mW) for $f_{SAMPLE} \leq 100$ksps
LTC1278/79	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs with Convert Start Input Best for 300ksps < $f_{SAMPLE} \leq 600$ksps
LTC1282	Complete 3V 12-Bit ADC with 12mW Power Dissipation	Fully Specified for 3V-Powered Applications, $f_{SAMPLE} \leq 140$ksps
LTC1409	Low Power 12-Bit, 800ksps Sampling ADC	Best Dynamic Performance, $f_{SAMPLE} \leq 800$ksps, 80mW Dissipation
LTC1410	12-Bit, 1.25Msps Sampling ADC with Shutdown	Best Dynamic Performance, THD = 84 and SINAD = 71 at Nyquist
LTC1419	14-Bit, 800ksps Sampling ADC	81.5dB SINAD, 150mW from ±5V Supplies
LTC1605	16-Bit, 100ksps Sampling ADC	Single Supply, ±10V Input Range, Low Power

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