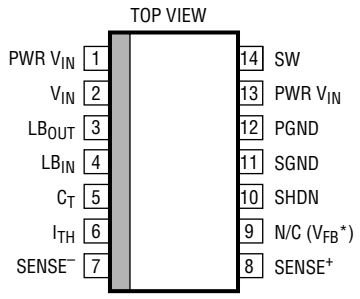
ABSOLUTE MAXIMUM RATINGS

(Voltages Refer to GND Pin) (Note 1)

Input Supply Voltage (Pins 1, 2, 13) ..... –0.3V to 13V
DC Switch Current (Pin 14) 1.2A
Peak Switch Current (Pin 14) 1.6A
Switch Voltage (Pin 14) ..... V_{IN} – 13.0
Operating Temperature Range
LTC1265C ..... 0° to 70°C
LTC1265I ..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... –65° to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
14-LEAD PLASTIC SO

*ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1265CS
LTC1265CS-5
LTC1265CS-3.3
LTC1265IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, V_{SHDN} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	Feedback Current into Pin 9	LTC1265			0.2	1	µA
V_{FB}	Feedback Voltage	LTC1265C	●	1.22	1.25	1.28	V
		V_{IN} = 9V, LTC1265I	●	1.20	1.25	1.30	V
V_{OUT}	Regulator Output Voltage	LTC1265-3.3: I_{LOAD} = 800mA	●	3.22	3.3	3.40	V
		LTC1265-5: I_{LOAD} = 800mA	●	4.9	5	5.2	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 6.5V to 10V, I_{LOAD} = 800mA		–40	0	40	mV
	Output Voltage Load Regulation	LTC1265-3.3: 10mA < I_{LOAD} < 800mA			40	65	mV
		LTC1265-5: 10mA < I_{LOAD} < 800mA			60	100	mV
	Burst Mode Operation Output Ripple	I_{LOAD} = 0mA			50		mV_{P-P}
I_Q	Input DC Supply Current (Note 3)	Active Mode: 3.5V < V_{IN} < 10V			1.8	2.4	mA
		Sleep Mode: 3.5V < V_{IN} < 10V			160	230	µA
		Sleep Mode: 5V < V_{IN} < 10V (LTC1265-5)			160	230	µA
		Shutdown: V_{SHDN} = V_{IN}, 3.5V < V_{IN} < 10V			5	15	µA
V_{LBTRIP}	Low-Battery Trip Point			1.15	1.25	1.35	V
I_{LBIN}	Current into Pin 4					0.5	µA
I_{LBOUT}	Current Sunk by Pin 3	V_{LBOUT} = 0.4V, V_{LBIN} = 0V		0.5	1.0	1.5	mA
		V_{LBOUT} = 5V, V_{LBIN} = 10V				1.0	µA
$V_8 – V_7$	Current Sense Threshold Voltage	LTC1265: V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE}^- = 5V, V_9 = V_{OUT}/4 – 25mV (Forced)		130	150	180	mV
		LTC1265-3.3: V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)		130	150	180	mV
		LTC1265-5: V_{SENSE}^- = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)		130	150	180	mV
R_{ON}	ON Resistance of Switch	LTC1265C	●		0.3	0.60	Ω
		LTC1265I			0.3	0.70	Ω
I_5	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE}^- = V_{OUT}		40	60	100	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Switch Off Time (Note 4)	C_T = 390pF, I_{LOAD} = 800mA (LTC1265C)	●	4	5	6	µs
		C_T = 390pF, I_{LOAD} = 800mA (LTC1265I)	●	3.5	5	7	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 10V, V_{SHDN} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Shutdown Pin High	Min Voltage at Pin 10 for Device to be in Shutdown		1.2			V
V_{IL}	Shutdown Pin Low	Max Voltage at Pin 10 for Device to be Active				0.6	V
I_{10}	Shutdown Pin Input Current	V_{SHDN} = 8V				0.5	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

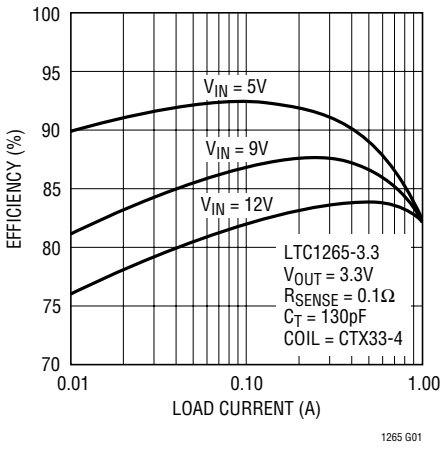
Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1265CS, LTC1265CS-3.3, LTC1265CS-5:
$T_J = T_A + (P_D \bullet 110°C/W)$

Note 3: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

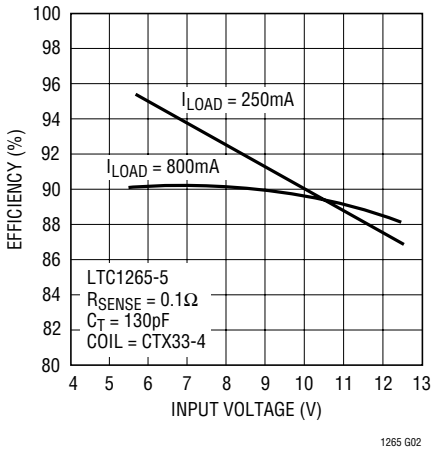
Note 4: In applications where R_{SENSE} is placed at ground potential, the off time increases by approximately 40%.

TYPICAL PERFORMANCE CHARACTERISTICS

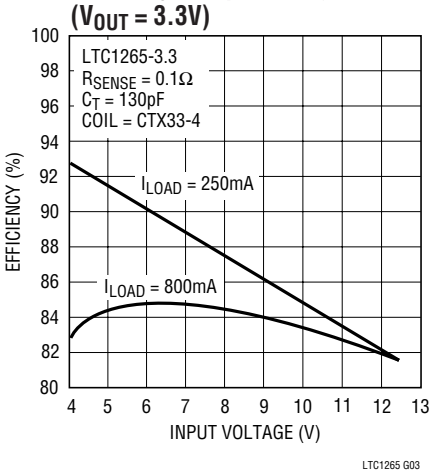
Efficiency vs Load Current



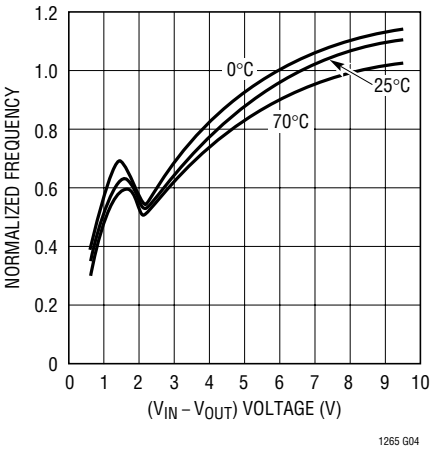
Efficiency vs Input Voltage (V_{OUT} = 5V)



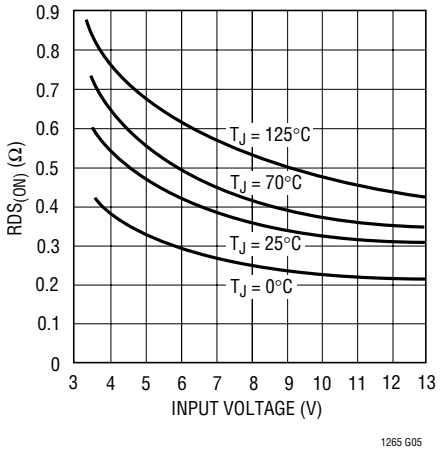
Efficiency vs Input Voltage (V_{OUT} = 3.3V)



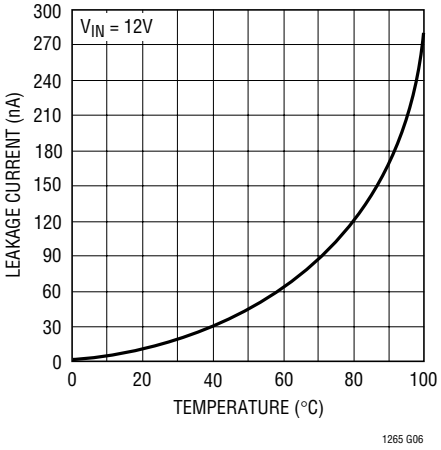
Operating Frequency vs (V_{IN} – V_{OUT})



Switch Resistance

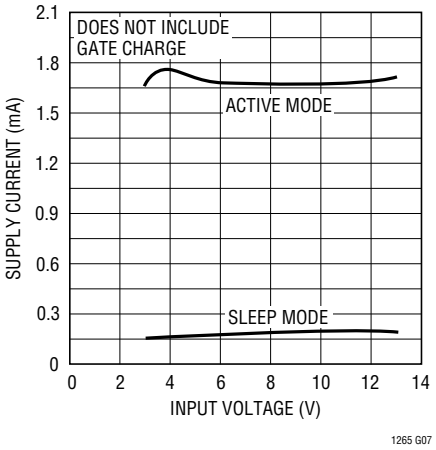


Switch Leakage Current

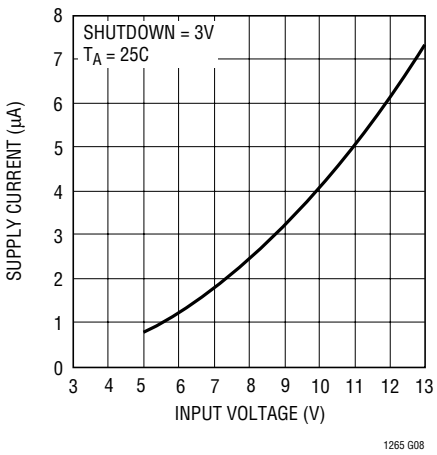


TYPICAL PERFORMANCE CHARACTERISTICS

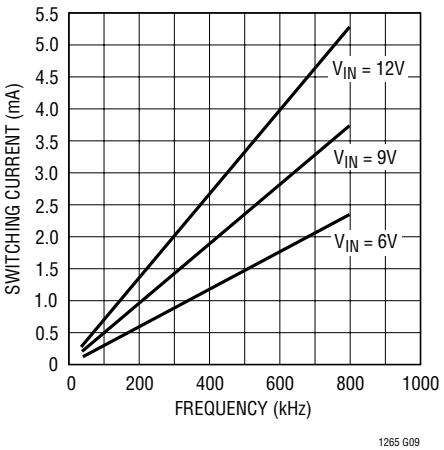
DC Supply Current



Supply Current in Shutdown



Gate Charge Losses



PIN FUNCTIONS

PWR V_{IN} (Pins 1, 13): Supply for the Power MOSFET and its Driver. Must decouple this pin properly to ground. Must always tie Pins 1 and 13 together.

V_{IN} (Pin 2): Main Supply for All the Control Circuitry in the LTC1265.

LB_{OUT} (Pin 3): Open-Drain Output of the Low-Battery Comparator. This pin will sink current when Pin 4 (LB_{IN}) goes below 1.25V. During shutdown, this pin is high impedance.

LB_{IN} (Pin 4): The (–) Input of the Low-Battery Comparator. The (+) input is connected to a reference voltage of 1.25V.

C_T (Pin 5): External capacitor C_T from Pin 5 to ground sets the switch off time. The operating frequency is dependent on the input voltage and C_T.

I_{TH} (Pin 6): Feedback Amplifier Decoupling Point. The current comparator threshold is proportional to Pin 6 voltage.

$SENSE^-$ (Pin 7): Connect to the (–) input of the current comparator. For LTC1265-3.3 and LTC1265-5, it also connects to an internal resistive divider which sets the output voltage.

$SENSE^+$ (Pin 8): The (+) Pin to the Current Comparator. A built-in offset between Pins 7 and 8 in conjunction with R_{SENSE} sets the current trip threshold.

N/C, V_{FB} (Pin 9): For the LTC1265 adjustable version, this pin serves as the feedback pin from an external resistive divider used to set the output voltage. On the LTC1265-3.3 and LTC1265-5 versions, this pin is not used.

SHDN (Pin 10): Pulling this pin HIGH keeps the internal switch off and puts the LTC1265 in micropower shutdown. Do not float this pin.

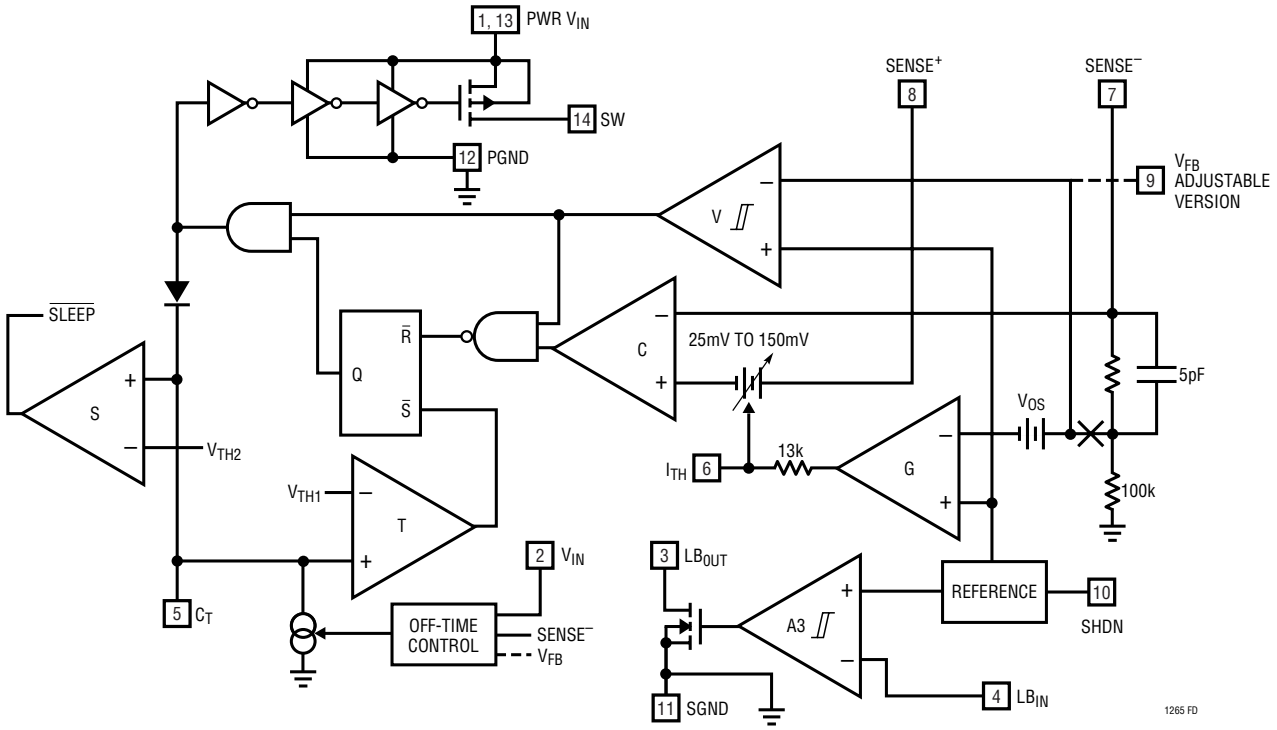
SGND (Pin 11): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGND (Pin 12): Switch Driver Ground. Connects to the (–) terminal of C_{IN}. Anode of the Schottky diode must be connected close to this pin.

SW (Pin 14): Drain of the P-Channel MOSFET Switch. Cathode of the Schottky diode must be connected close to this pin.

FUNCTIONAL DIAGRAM

(Pin 9 connection shown for LTC1265-3.3 and LTC1265-5; change create LTC1265)



OPERATION

(Refer to Functional Diagram)

The LTC1265 uses a constant off-time architecture to switch its internal P-channel power MOSFET. The off time is set by an external timing capacitor at C_T (Pin 5). The operating frequency is then determined by the off time and the difference between V_{IN} and V_{OUT}.

The output voltage is set by an internal resistive divider (LTC1265-3.3 and LTC1265-5) connected to SENSE$^-$ (Pin 7) or an external divider returned to V_{FB} (Pin 9 for LTC1265). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V.

To optimize efficiency, the LTC1265 automatically switches between continuous and Burst Mode operation. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

When the load is heavy, the LTC1265 is in continuous operation. During the switch ON time, current comparator C monitors the voltage between Pins 7 and 8 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches the comparator's threshold value, its output signal will change state, setting the flip flop and turning the internal P-channel MOSFET off. The timing capacitor connected to Pin 5 is now allowed to discharge at a rate determined by the off-time controller.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, sets the flip flop and causes the switch to turn on. Also, the timing capacitor is recharged. The inductor current will again ramp up until the current comparator C trips. The cycle then repeats.

When the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (Pin 6) to increase the current comparator threshold, thus tracking the load current.

When the load is relatively light, the LTC1265 automatically goes into Burst Mode operation. The current loop is interrupted when the output voltage exceeds the desired regulated value. The hysteretic voltage comparator V trips when V_{OUT} is above the desired output voltage, shutting off the switch and causing the capacitor to discharge. This

OPERATION (Refer to Functional Diagram)

capacitor discharges past V_{TH1} until its voltage drops below V_{TH2}. Comparator S then trips and a sleep signal is generated. The circuit now enters into sleep mode with the power MOSFET turned off. In sleep mode, the LTC1265 is in standby and the load current is supplied by the output capacitor. All unused circuitry is shut off, reducing quiescent current from 2mA to 160µA. When the output capacitor discharges by the amount of the hysteresis of the comparator V, the P-channel switch turns on again and the process repeats itself. During Burst Mode operation the peak inductor current is set at 25mV/R_{SENSE}.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture, the operating frequency is a function of the voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 2V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle) providing low dropout operation with $V_{OUT} \cong V_{IN}$.

APPLICATIONS INFORMATION

The basic LTC1265 application circuit is shown in Figure 1. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the Schottky diode D1 is selected followed by C_{IN} and C_{OUT}.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. With the current comparator monitoring the voltage developed across R_{SENSE}, the threshold of the comparator determines the peak inductor current. Depending on the load current condition, the threshold of the comparator lies between 25mV/R_{SENSE} and 150mV/R_{SENSE}. The maximum output current of the LTC1265 is:

$$I_{OUT(MAX)} = \frac{150mV}{R_{SENSE}} - \frac{I_{RIPPLE}}{2} \text{ (Amps)}$$

where I_{RIPPLE} is the peak-to-peak inductor ripple current.

At a relatively light load, the LTC1265 is in Burst Mode operation. In this mode the peak inductor current is set at 25mV/R_{SENSE}. To fully benefit from Burst Mode operation, the inductor current should be continuous during burst periods. Hence, the peak-to-peak inductor ripple current must not exceed 25mV/R_{SENSE}.

To account for light and heavy load conditions, the $I_{OUT(MAX)}$ is then given by:

$$I_{OUT(MAX)} = \frac{150mV}{R_{SENSE}} - \frac{25mV}{2 \bullet R_{SENSE}} \text{ (Amps)}$$

$$= \frac{137.5mV}{R_{SENSE}} \text{ (Amps)}$$

Solving for R_{SENSE} and allowing a margin of variations in the LTC1265 and extended component values yields:

$$R_{SENSE} = \frac{100mV}{I_{OUT(MAX)}} (\Omega)$$

The LTC1265 is rated with a capability to supply a maximum of 1.2A of output current. *Therefore, the minimum value of R_{SENSE} that can be used is 0.083Ω.* A graph for selecting R_{SENSE} versus maximum output is given in Figure 2.

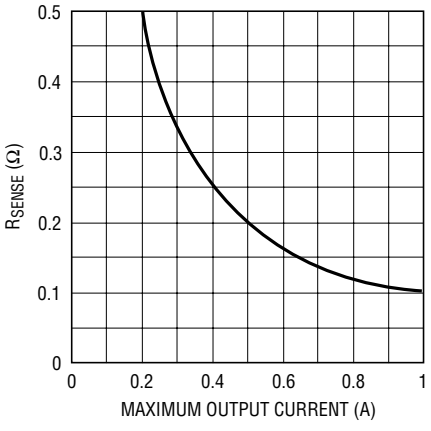


Figure 2. Selecting R_{SENSE}

APPLICATIONS INFORMATION

Under short-circuit condition, the peak inductor current is determined by:

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}} \text{ (Amps)}$$

In this condition, the LTC1265 automatically extends the off time of the P-channel MOSFET to allow the inductor current to decay far enough to prevent any current build-up. The resulting ripple current causes the average short-circuit current to be approximately $I_{OUT(MAX)}$.

C_T and L Selection for Operating Frequency

The LTC1265 uses a constant off-time architecture with t_{OFF} determined by an external capacitor C_T. Each time the P-channel MOSFET turns on, the voltage on C_T is reset to approximately 3.3V. During the off time, C_T is discharged by a current that is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise, decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3(10^4)f}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) \text{ (Farads)}$$

where V_D is the drop across the Schottky diode.

As the operating frequency is increased, the gate charge losses will reduce efficiency. The complete expression for operating frequency is given by:

$$f \approx \frac{1}{t_{OFF}}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) \text{ (Hz)}$$

where:

$$t_{OFF} = 1.3(10^4)C_T\left(\frac{V_{REG}}{V_{OUT}}\right) \text{ (sec)}$$

V_{REG} is the desired output voltage (i.e. 5V, 3.3V). V_{OUT} is the measured output voltage. Thus V_{REG}/V_{OUT} = 1 in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input-to-output voltage differential drops below 2V, the LTC1265 reduces t_{OFF} by increasing the discharge current in C_T. This prevents audible operation prior to dropout. (See shelving effect shown in the Operating Frequency curve under Typical Performance Characteristics.)

To maintain continuous inductor current at light load, the inductor must be chosen to provide no more than 25mV/R_{SENSE} of peak-to-peak ripple current. This results in the following expression for L:

$$L \geq 5.2(10^5)R_{SENSE}(C_T)V_{REG}$$

Using an inductance smaller than the above value will result in the inductor current being discontinuous. A consequence of this is that the LTC1265 will delay entering Burst Mode operation and efficiency will be degraded at low currents.

Inductor Core Selection

With the value of L selected, the type of inductor must be chosen. Basically, there are two kinds of losses in an inductor; core and copper losses.

Core losses are dependent on the peak-to-peak ripple current and core material. However it is independent of the physical size of the core. By increasing the inductance, the peak-to-peak inductor ripple current will decrease, therefore reducing core loss. Utilizing low core loss material, such as molypermalloy or Kool Mμ® will allow user to concentrate on reducing copper loss and preventing saturation.

Although higher inductance reduces core loss, it increases copper loss as it requires more windings. When space is not at a premium, larger wire can be used to reduce the wire resistance. This also prevents excessive heat dissipation.

CATCH DIODE SELECTION

Losses in the catch diode depend on forward drop and switching times. Therefore Schottky diodes are a good choice for low drop and fast switching times.

The catch diode carries load current during the off time. The average diode current is therefore dependent on the

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APPLICATIONS INFORMATION

P-channel switch duty cycle. At high input voltages, the diode conducts most of the time. As V_{IN} approaches V_{OUT}, the diode conducts only a small fraction of the time. The most stressful condition for the diode is when the output is short circuited. Under this condition, the diode must safely handle $I_{SC(PK)}$ at close to 100% duty cycle. Most LTC1265 circuits will be well served by either a 1N5818 or a MBRS130LT3 Schottky diode. An MBRS0520 is a good choice for $I_{OUT(MAX)} \leq 500mA$.

C_{IN}

In continuous mode, the input current of the converter is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor must be used. In addition, the capacitor must handle a high RMS current. The C_{IN} RMS current is given by:

$$I_{RMS} \approx \frac{I_{OUT}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}} \left(A_{RMS}\right)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. **Do not underspecify this component**. An additional 0.1µF ceramic capacitor is also required on PWR V_{IN} for high frequency decoupling.

C_{OUT}

The selection of C_{OUT} is based upon the effective series resistance (ESR) for proper operation of the LTC1265. The required ESR of C_{OUT} is:

$$ESR_{COUT} < 50mV/I_{RIPPLE}$$

where I_{RIPPLE} is the ripple current of the inductor. For the case where the I_{RIPPLE} is $25mV/R_{SENSE}$, the required ESR of C_{OUT} is:

$$ESR_{COUT} < 2(R_{SENSE})$$

To avoid overheating, the output capacitor must be sized to handle the ripple current generated by the inductor. The worst-case RMS ripple current in the output capacitor is given by:

$$I_{RMS} \approx \frac{150mV}{2(R_{SENSE})} \left(A_{RMS}\right)$$

Generally, once the ESR requirement for C_{OUT} has been met, the RMS current rating far exceeds the $I_{RIPPLE(P-P)}$ requirement.

ESR is a direct function of the volume of the capacitor. Manufacturers such as Nichicon, AVX and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolyte and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are both available in surface mount configuration and are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Consult the manufacturer for other specific recommendations.

When the capacitance of C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1265 would normally be in continuous operation. The effect will be most pronounced with low value of R_{SENSE} and can be improved at higher frequencies with lower values of L.

Low-Battery Detection

The low-battery comparator senses the input voltage through an external resistive divider. This divided voltage connects to the (–) input of a voltage comparator (Pin 4) which is compared with a 1.25V reference voltage. Neglecting Pin 4 bias current, the following expression is used for setting the trip limit:

$$V_{LB\_TRIP} = 1.25\left(1 + \frac{R4}{R3}\right)$$

APPLICATIONS INFORMATION

The output, Pin 3, is an N-channel open drain that goes low when the battery voltage is below the threshold set by R3 and R4. In shutdown, the comparator is disabled and Pin 3 is in a high impedance state.

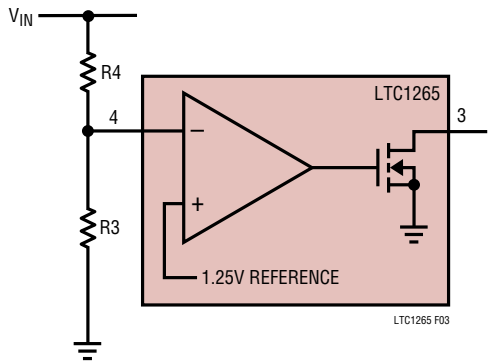


Figure 3. Low-Battery Comparator

LTC1265 ADJUSTABLE APPLICATIONS

The LTC1265 develops a 1.25V reference voltage between the feedback (Pin 9) terminal and signal ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

For most applications a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1265.

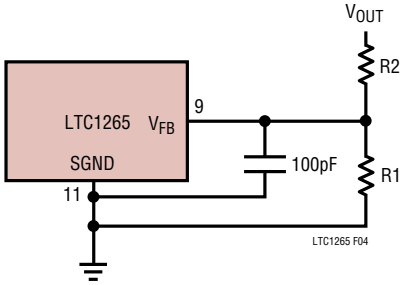


Figure 4. LTC1265 Adjustable Configuration

Absolute Maximum Ratings and Latchup Prevention

The absolute maximum ratings specify that SW (Pin 14) can never exceed V_{IN} (Pins 1, 2, 13) by more than 0.3V. Normally this situation should never occur. It could, however, if the output is held up while the V_{IN} supply is pulled down. A condition where this could potentially occur is when a battery is supplying power to an LTC1265 regulator and also to one or more loads in parallel with the the regulator's V_{IN}. If the battery is disconnected while the LTC1265 regulator is supplying a light load and one of the parallel circuits has a heavy load, the input capacitor of the LTC1265 regulator could be pulled down faster than the output capacitor, causing the absolute maximum ratings to be exceeded. The result is often a latchup which can be destructive if V_{IN} is reapplied quickly. Battery disconnect is possible as a result of mechanical stress, bad battery contacts or use of a lithium-ion battery with a built-in internal disconnect. The user needs to assess his/her application to determine whether this situation could occur. If so, additional protection is necessary.

Prevention against latchup can be accomplished by simply connecting a Schottky diode across the SW and V_{IN} pins as shown in Figure 5. The diode will normally be reverse biased unless V_{IN} is pulled below V_{OUT} at which time the diode will clamp the ($V_{OUT} - V_{IN}$) potential to less than the 0.6V required for latchup. Note that a low leakage Schottky should be used to minimize the effect on no-load supply current. Schottky diodes such as MBR0530, BAS85 and BAT84 work well. Another more serious effect of the protection diode leakage is that at no load with nothing to provide a sink for this leakage current, the

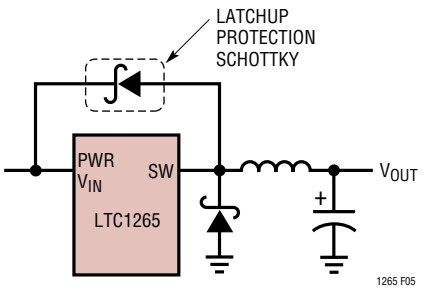


Figure 5. Preventing Absolute Maximum Ratings from Being Exceeded

APPLICATIONS INFORMATION

output voltage can potentially float above the maximum allowable tolerance. To prevent this from occuring, a resistor must be connected between V_{OUT} and ground with a value low enough to sink the maximum possible leakage current.

THERMAL CONSIDERATIONS

In a majority of applications, the LTC1265 does not dissipate much heat due to its high efficiency. However, in applications where the switching regulator is running at high duty cycles or the part is in dropout with the switch turned on continuously (DC), the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated by the regulator exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P(\theta_{JA})$$

where P is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is simply given by:

$$T_J = T_R + T_A$$

As an example, consider the LTC1265 is in dropout at an input voltage of 4V with a load current of 0.5A. From the Typical Performance Characteristics graph of Switch Resistance, the ON resistance of the P-channel is 0.55Ω. Therefore power dissipated by the part is:

$$P = I^2(R_{DSON}) = 0.1375W$$

For the SO package, the θ_{JA} is 110°C/W.

Therefore the junction temperature of the regulator when it is operating in ambient temperature of 25°C is:

$$T_J = 0.1375(110) + 25 = 40.1°C$$

Remembering that the above junction temperature is obtained from a R_{DSON} at 25°C, we need to recalculate the junction temperature based on a higher R_{DSON} since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Now consider the case of a 1A regulator with V_{IN} = 4V and T_A = 65°C. Starting with the same 0.55Ω assumption for R_{DSON}, the T_J calculation will yield 125°C. But from the graph, this will increase the R_{DSON} to 0.76Ω, which when used in the above calculation yields an actual T_J > 148°C. Therefore the LTC1265 would be unsuitable for a 4V input, 1A output regulator operating at T_A = 65°C.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1265. These items are also illustrated graphically in the layout diagram of Figure 6. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1265 signal ground (Pin 11) must return to the (–) plate of C_{OUT}. The power ground (Pin 12) returns to the anode of the Schottky diode, and the (–) plate of C_{IN}, whose leads should be as short as possible.
2. Does the (+) plate of the C_{IN} connect to the power V_{IN} (Pins 1,13) as close as possible? This capacitor provides the AC current to the internal P-channel MOSFET and its driver.
3. Is the input decoupling capacitor (0.1μF) connected closely between power V_{IN} (Pins 1,13) and power ground (Pin 12)? This capacitor carries the high frequency peak currents.
4. Is the Schottky diode closely connected between the power ground (Pin 12) and switch (Pin 14)?
5. Does the LTC1265 $SENSE^-$ (Pin 7) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and signal ground.
6. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 7 and 8 should be as close as possible to the LTC1265.
7. Is SHDN (Pin 10) actively pulled to ground during normal operation? The SHDN pin is high impedance and must not be allowed to float.

APPLICATIONS INFORMATION

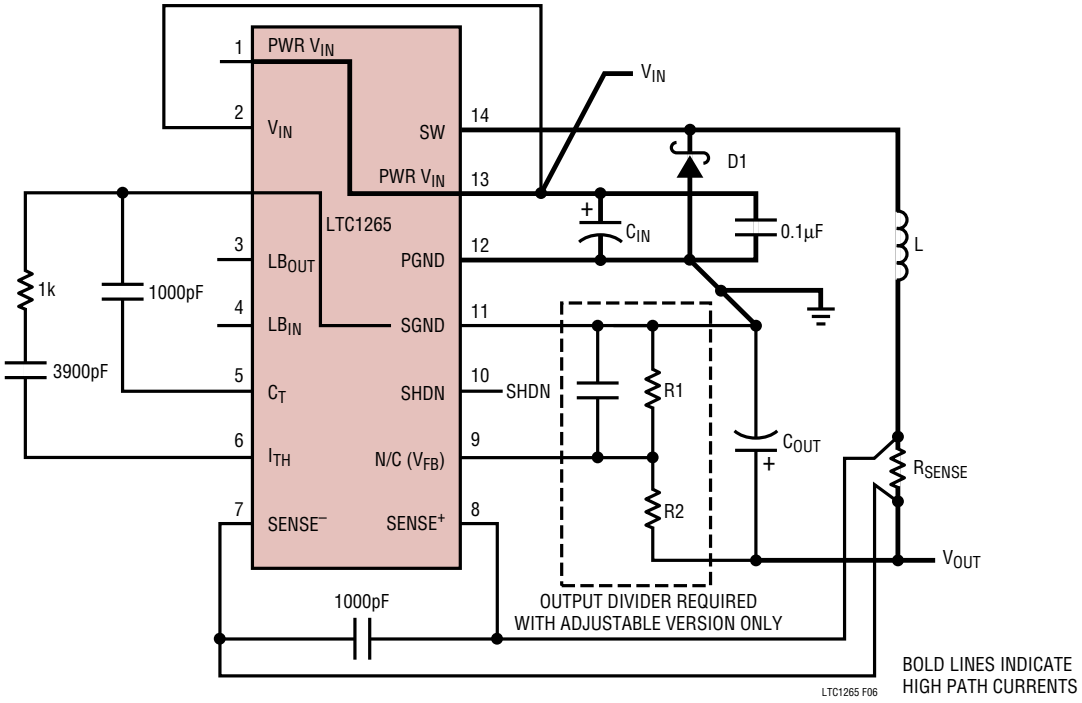


Figure 6. LTC1265 Layout Diagram (See Board Layout Checklist)

Troubleshooting Hints

Since efficiency is critical to LTC1265 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. As the LTC1265 is highly tolerant of poor layout, the output voltage will still be regulated. Therefore, monitoring the output voltage will not tell you whether you have a good or bad layout. The waveform to monitor is the voltage on the timing capacitor Pin 5.

In continuous mode the voltage on the C_T pin is a sawtooth with approximately $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 7a.

When the load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on C_T pin now falls to ground for periods of time as shown in Figure 7b. During this time the LTC1265 is in sleep mode with quiescent current reduced to 160µA.

The inductor current should also be monitored. If the circuit is poorly decoupled, the peak inductor current will be haphazard as in Figure 8a. A well decoupled LTC1265 has a clean inductor current as in Figure 8b.

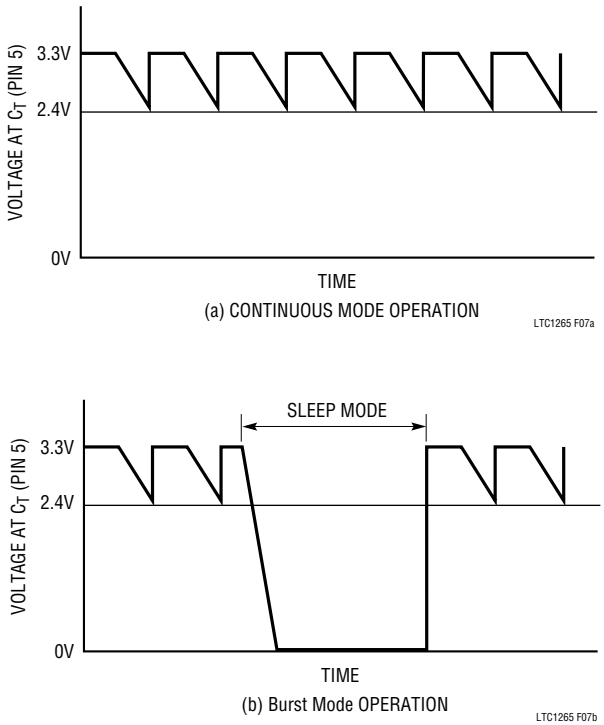
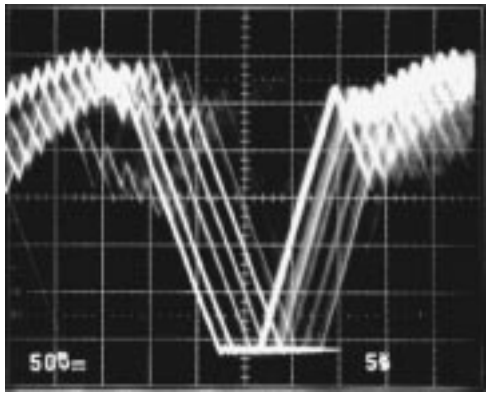
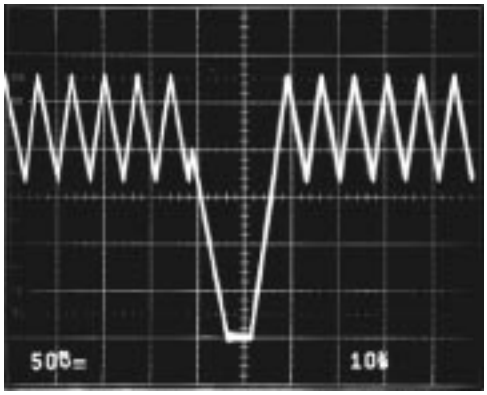


Figure 7. C_T Waveforms

APPLICATIONS INFORMATION



(a) POORLY DECOUPLED LTC1265



(b) WELL DECOUPLED LTC1265

Figure 8. Inductor Waveforms

Design Example

As a design example, assume V_{IN} = 5V, V_{OUT} = 3.3V, I_{MAX} = 0.8A and f = 250kHz. With this information we can easily calculate all the important components.

From (1),

$R_{SENSE} = 100mV/0.8 = 0.125\Omega$

From (2) and assuming V_D = 0.4V,

$C_T \cong 100pF$

Using (3), the value of the inductor is:

$L \geq 5.2(10^5)(0.125)(100pF)3.3V = 22\mu H$

For the catch diode, a MBRS130LT3 or 1N5818 will be sufficient in this application.

C_{IN} will require an RMS current rating of at least 0.4A at temperature, and C_{OUT} will require an ESR of (from 5):

$ESR_{COUT} < 0.25\Omega$

The inductor ripple current is given by:

$$I_{RIPPLE} = \left(\frac{V_{OUT} + V_D}{L}\right) t_{OFF} = 0.22A$$

At light loads the peak inductor current is at:

$I_{PEAK} = 25mV/0.125 = 0.2A$

Therefore, at load current less than 0.1A the LTC1265 will be in Burst Mode operation. Figure 9 shows the complete circuit and Figure 10 shows the efficiency curve with the above calculated component values.

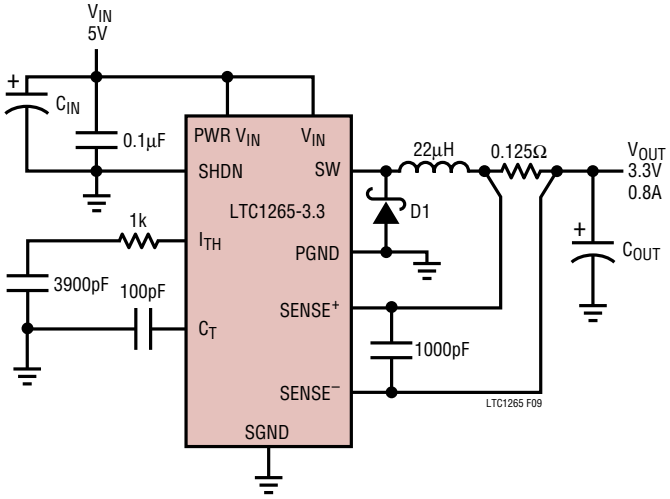


Figure 9. Design Example Circuit

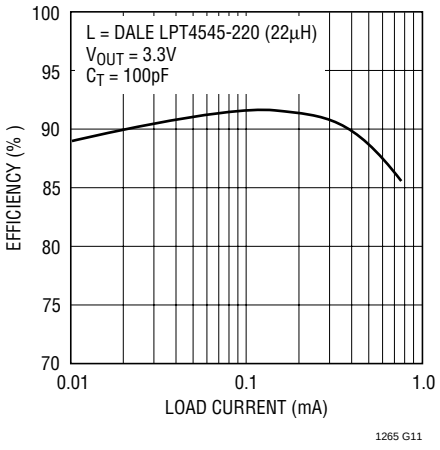
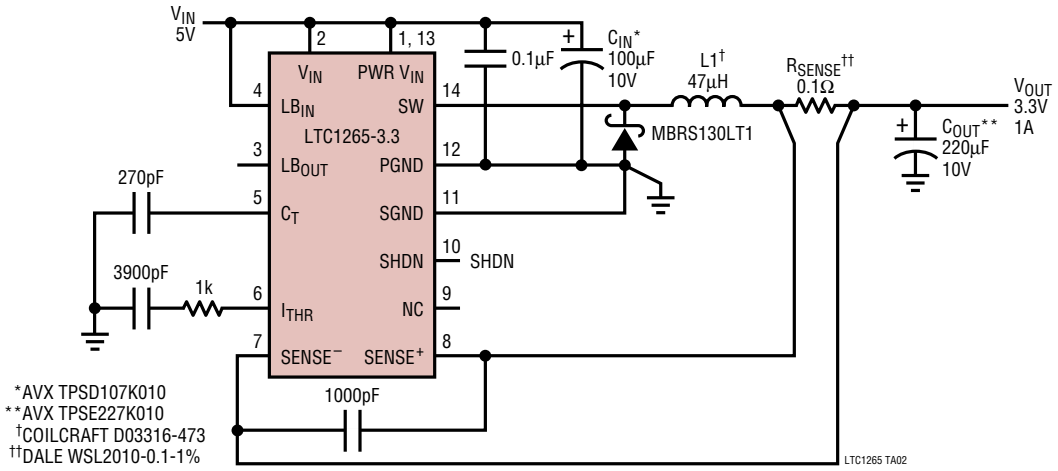


Figure 10. Design Example Efficiency Curve

TYPICAL APPLICATIONS

High Efficiency 5V to 3.3V Converter



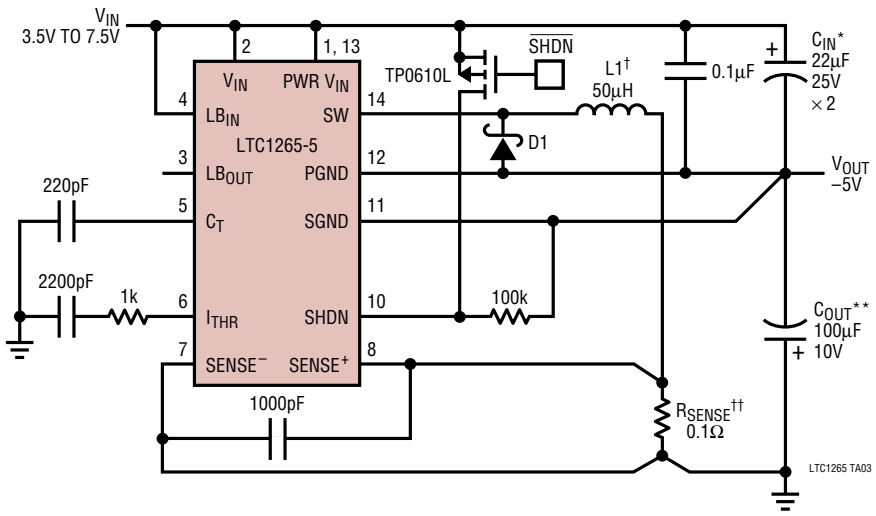
Positive-to-Negative (–5V) Converter

*AVX TPSD226K025
**AVX TPSD107K010
†L1 SELECTION

MANUFACTURER	PART NO.
COILCRAFT	DO3316-473
COILTRONICS	CTX50-4
DALE	LPT4545-500LA
SUMIDA	CD74-470

††IRC LRC2010-01-R100-J
D1= MBRS130LT3

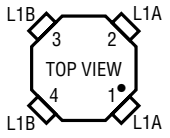
V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
3.5	360
4.0	430
5.0	540
6.0	630
7.0	720
7.5	740



TYPICAL APPLICATIONS

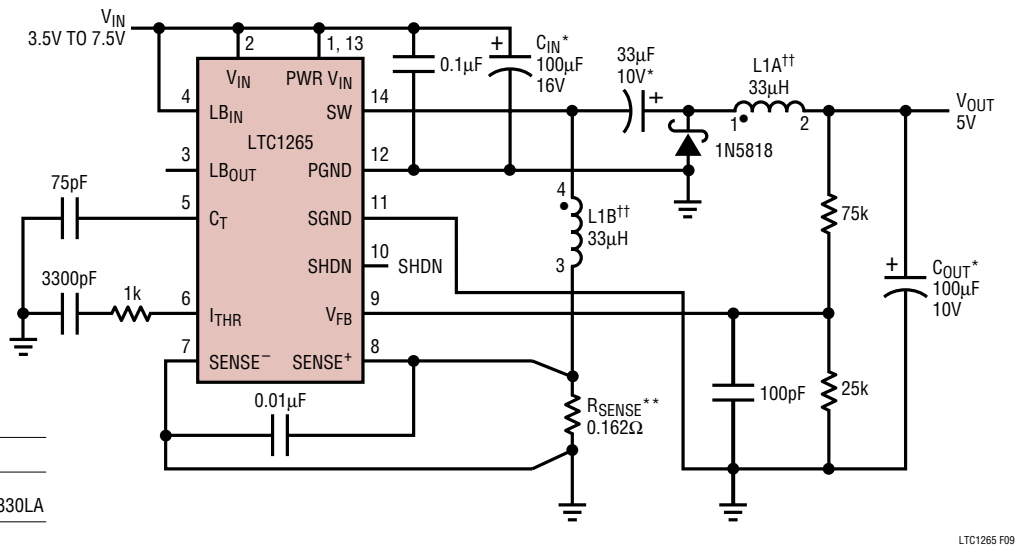
5V Buck-Boost Converter

V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
3.5	240
4.0	275
5.0	365
6.0	490
7.0	610
7.5	665



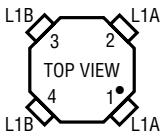
*SANYO OS-CON CAPACITOR
**IRC LRC2010-01-R162-J
†L1A, L2A SELECTION

MANUFACTURER	PART NO.
COILTRONICS	CTX33-4
DALE	LPT4545-330LA



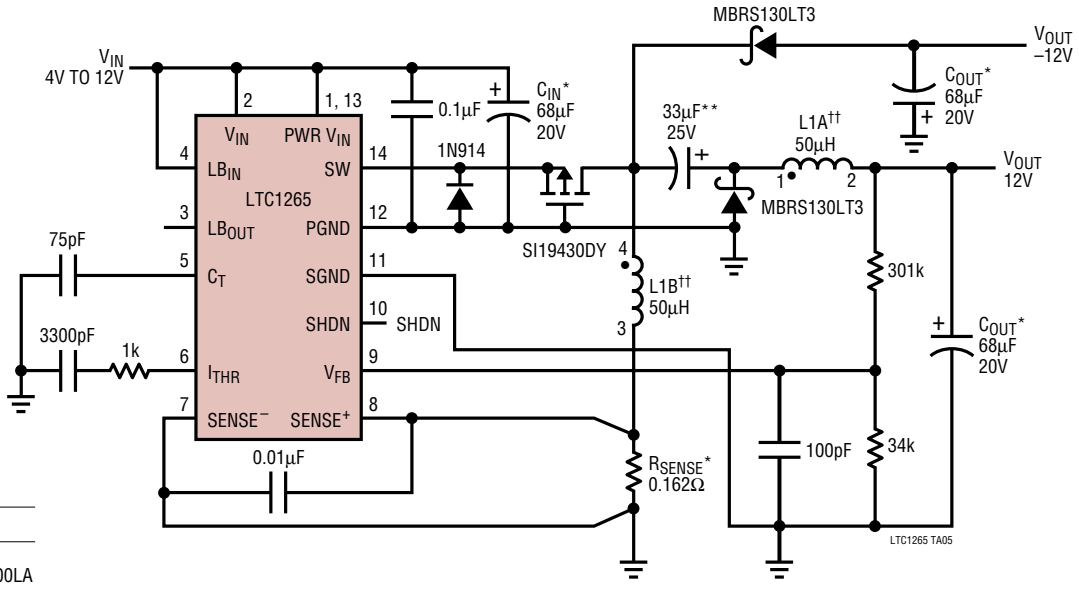
9V to 12V and – 12V Outputs

V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
4.0	40
5.0	60
6.0	80
7.0	100
8.0	115
9.0	130
10.0	150
11.0	165
12.0	180



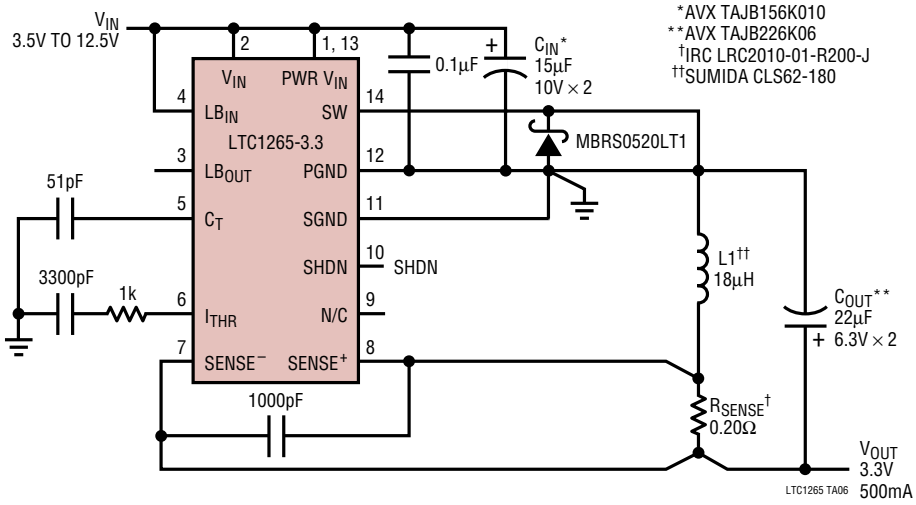
*AVX TPSE686K020
**AVX TPSE336K025
†IRC LRC2010-01-R162-J
††L1A,L2A SELECTION

MANUFACTURER	PART NO.
COILTRONICS	CTX50-4
DALE	LPT4545-500LA

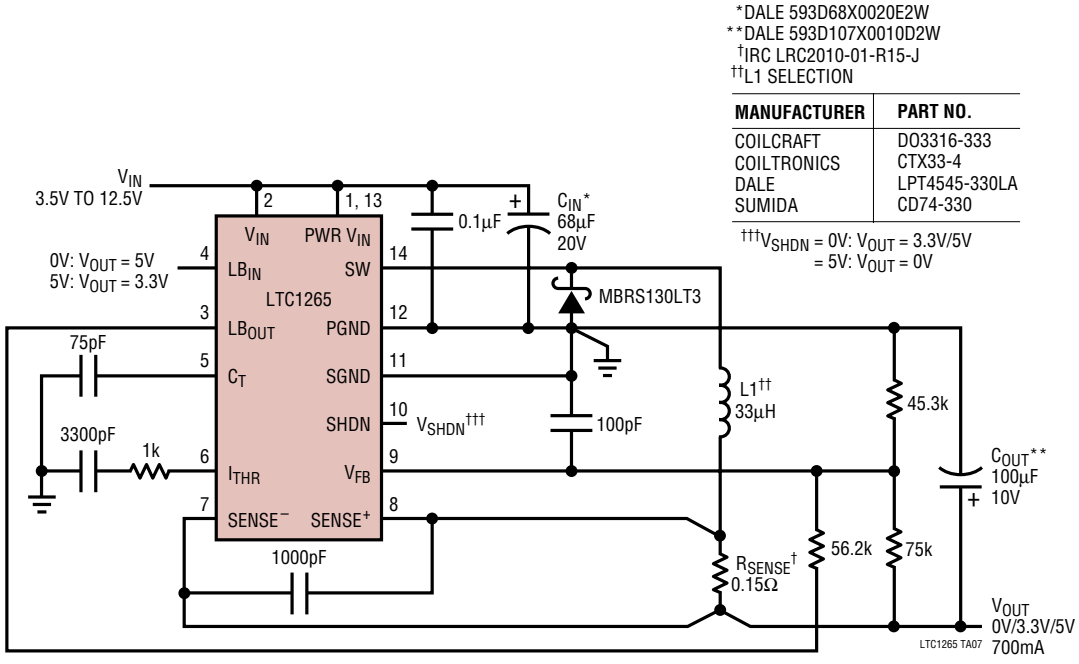


TYPICAL APPLICATIONS

2.5mm Max Height 5V-to-3.3V (500mA)

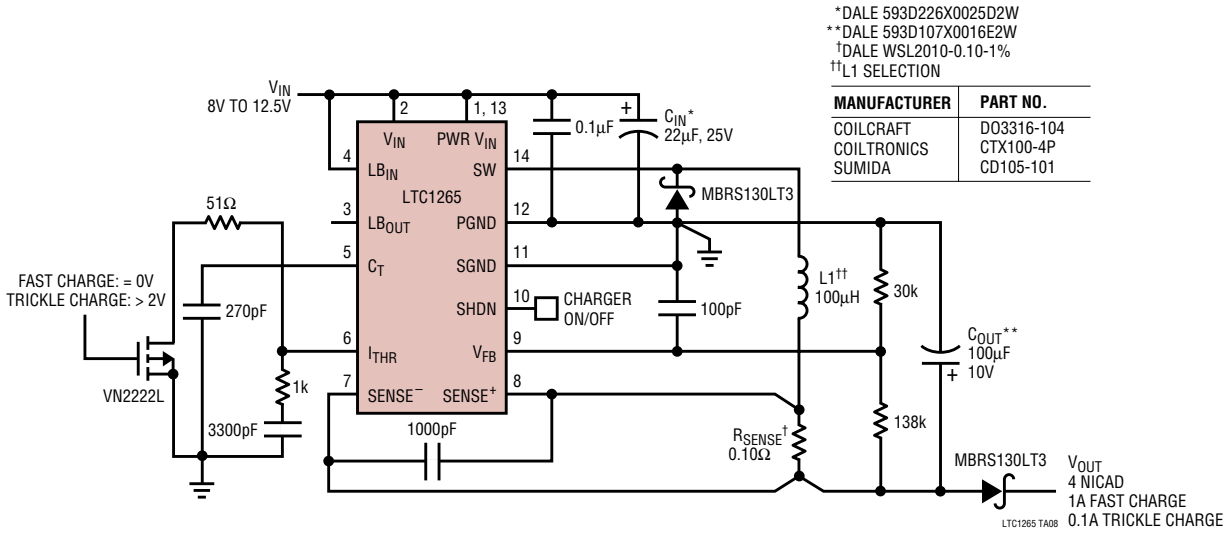


Logic Selectable 0V/3.3V/5V 700mA Regulator



TYPICAL APPLICATIONS

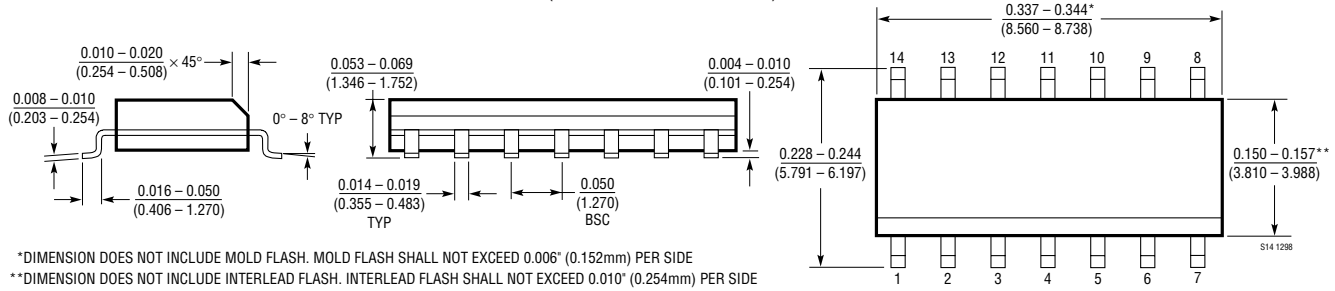
4-NiCad Battery Charger



PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1143	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	Step-Down Switching Regulator Controller	Nonsynchronous, 8-Pin, $V_{IN} \leq 16V$
LTC1148HV	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1174	Step-Down Switching Regulator with Internal 0.5A Switch	$V_{IN} \leq 18.5V$, Comparator/Low Battery Detector
LTC1474/LTC1475	Low Quiescent Current Step-Down Regulators	Monolithic, $I_Q = 40\mu A$, 400mA, MS8
LTC1574	Step-Down Switching Regulator with Internal 0.5A Switch and Schottky Diode	$V_{IN} \leq 18.5V$, Comparator
LTC1622	Low Input Voltage Step-Down DC/DC Controller	Constant Frequency, 2V to 10V V_{IN}, MS8
LTC1627	Monolithic Synchronous Step-Down Switching Regulator	Constant Frequency, I_{OUT} to 500mA, 2.65V to 8.5V V_{IN}
LTC1772	Constant Frequency Step-Down DC/DC Controller	SOT-23, 2.2V to 9.8V V_{IN}

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