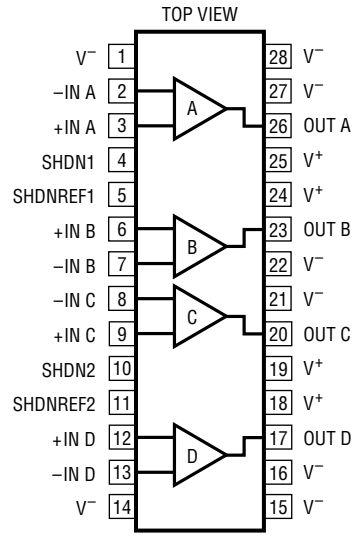
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+ to V^-) ..... ±13.5V
Input Current ..... ±10mA
Output Short-Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range ..... –40°C to 85°C
Specified Temperature Range (Note 3) .. –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
28-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 25°C/W (NOTE 4)
UNDERSIDE METAL CONNECTED TO V^-

ORDER PART NUMBER
LT6301CFE
LT6301IFE

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, pulse tested, ±5V ≤ V_S ≤ ±12V, $V_{SHDNREF}$ = 0V, R_{BIAS} = 24.9k between V^+ and SHDN unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		 ●		1	5.0 7.5	mV mV
	Input Offset Voltage Matching	(Note 6)	 ●		0.3	5.0 7.5	mV mV
	Input Offset Voltage Drift		●		10		µV/°C
I_{OS}	Input Offset Current		 ●		100	500 800	nA nA
I_B	Input Bias Current		 ●		±0.1	±4 ±6	µA µA
	Input Bias Current Matching	(Note 6)	 ●		100	500 800	nA nA
e_n	Input Noise Voltage Density	f = 10kHz			8		nV/√Hz
i_n	Input Noise Current Density	f = 10kHz			0.8		pA/√Hz
R_{IN}	Input Resistance	V_{CM} = (V^+ – 2V) to (V^- + 2V) Differential	●	5	50 6.5		MΩ MΩ
C_{IN}	Input Capacitance				3		pF
	Input Voltage Range (Positive) Input Voltage Range (Negative)	(Note 5) (Note 5)	● ●	V^+ – 2	V^+ – 1 V^- + 1	 V^- + 2	V V
CMRR	Common Mode Rejection Ratio	V_{CM} = (V^+ – 2V) to (V^- + 2V)	 ●	74 66	83		dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full specified temperature range, otherwise specifications are at T_A = 25°C. V_{CM} = 0V, pulse tested, ±5V ≤ V_S ≤ ±12V, $V_{SHDNREF}$ = 0V, R_{BIAS} = 24.9k between V⁺ and SHDN unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PSRR	Power Supply Rejection Ratio	V_S = ±4V to ±12V		74	88		dB
			●	66			dB
A_{VOL}	Large-Signal Voltage Gain	V_S = ±12V, V_{OUT} = ±10V, R_L = 40Ω		63	76		dB
			●	57			dB
		V_S = ±5V, V_{OUT} = ±3V, R_L = 25Ω		60	70		dB
			●	54			dB
V_{OUT}	Output Swing	V_S = ±12V, R_L = 100Ω		10.9	11.1		±V
			●	10.7			±V
		V_S = ±12V, I_L = 250mA		10.6	10.9		±V
			●	10.4			±V
		V_S = ±5V, R_L = 25Ω		3.7	4		±V
			●	3.5			±V
		V_S = ±5V, I_L = 250mA		3.6	3.9		±V
			●	3.4			±V
I_{OUT}	Maximum Output Current	V_S = ±12V, R_L = 1Ω		500	1200		mA
I_S	Supply Current per Amplifier	V_S = ±12V, R_{BIAS} = 24.9k (Note 7)		8.0	10	13.5	mA
			●	6.7		15.0	mA
		V_S = ±12V, R_{BIAS} = 32.4k (Note 7)			8		mA
		V_S = ±12V, R_{BIAS} = 43.2k (Note 7)			6		mA
		V_S = ±12V, R_{BIAS} = 66.5k (Note 7)			4		mA
		V_S = ±5V, R_{BIAS} = 24.9k (Note 7)		2.2	3.4	5.0	mA
			●	1.8		5.8	mA
	Supply Current in Shutdown	V_{SHDN} = 0.4V			0.1	1	mA
	Output Leakage in Shutdown	V_{SHDN} = 0.4V			0.3	1	mA
	Channel Separation	V_S = ±12V, V_{OUT} = ±10V, R_L = 40Ω (Note 8)		80	110		dB
			●	77			dB
SR	Slew Rate	V_S = ±12V, A_V = –10, (Note 9)		300	600		V/µs
		V_S = ±5V, A_V = –10, (Note 9)		100	200		V/µs
HD2	Differential 2nd Harmonic Distortion	V_S = ±12V, A_V = 10, $2V_{P-P}$, R_L = 50Ω, 1MHz			–85		dBc
HD3	Differential 3rd Harmonic Distortion	V_S = ±12V, A_V = 10, $2V_{P-P}$, R_L = 50Ω, 1MHz			–82		dBc
GBW	Gain Bandwidth	f = 1MHz			200		MHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Applies to short circuits to ground only. A short circuit between the output and either supply may permanently damage the part when operated on supplies greater than ±10V.

Note 3: The LT6301C is guaranteed to meet specified performance from 0°C to 70°C and is designed, characterized and expected to meet these extended temperature limits, but is not tested at –40°C and 85°C. The LT6301I is guaranteed to meet the extended temperature limits.

Note 4: Thermal resistance varies depending upon the amount of PC board metal attached to Pins 1, 14, 15, 28 and the exposed bottom side metal of the device. If the maximum dissipation of the package is exceeded, the device will go into thermal shutdown and be protected.

Note 5: Guaranteed by the CMRR tests.

Note 6: Matching is between amplifiers A and B or between amplifiers C and D.

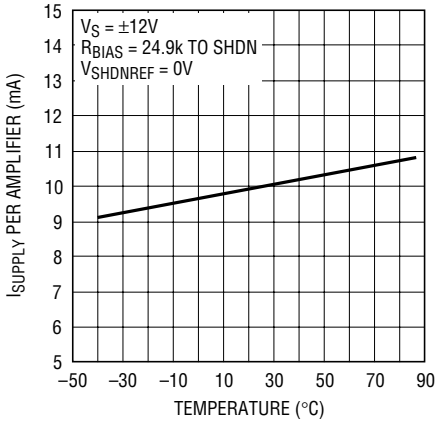
Note 7: R_{BIAS} is connected between V⁺ and each SHDN pin, with each SHDNREF pin grounded.

Note 8: Channel separation is measured between amplifiers A and B and between amplifiers C and D. Channel separation between any other combination of amplifiers is guaranteed by design as two separate die are used in the package.

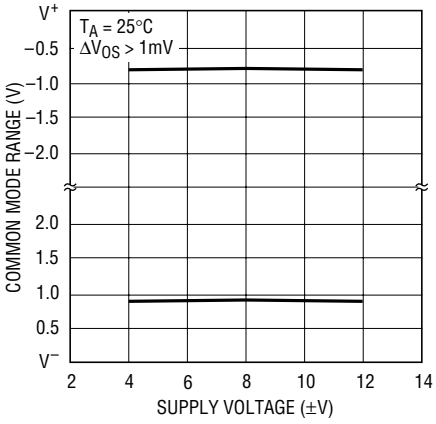
Note 9: Slew rate is measured at ±5V on a ±10V output signal while operating on ±12V supplies and ±1V on a ±3V output signal while operating on ±5V supplies.

TYPICAL PERFORMANCE CHARACTERISTICS

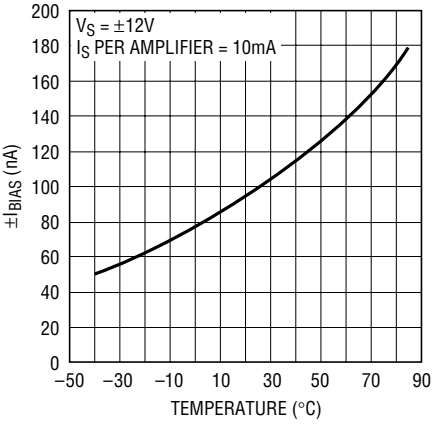
Supply Current vs Ambient Temperature



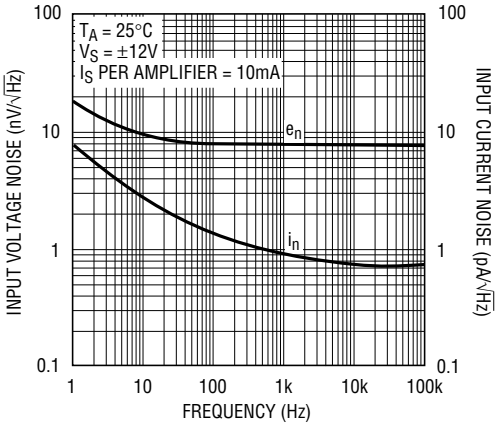
Input Common Mode Range vs Supply Voltage



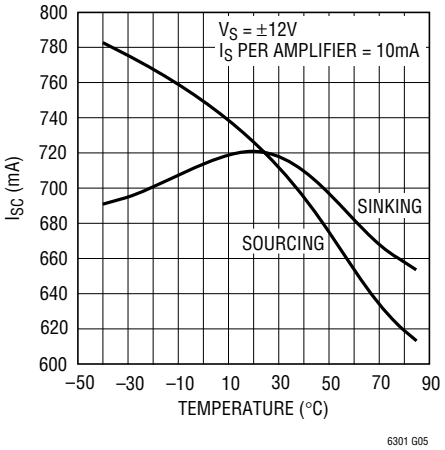
Input Bias Current vs Ambient Temperature



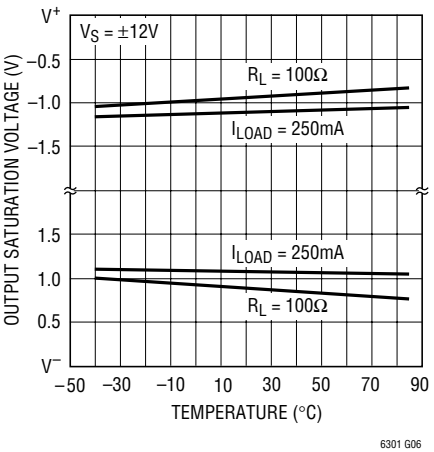
Input Noise Spectral Density



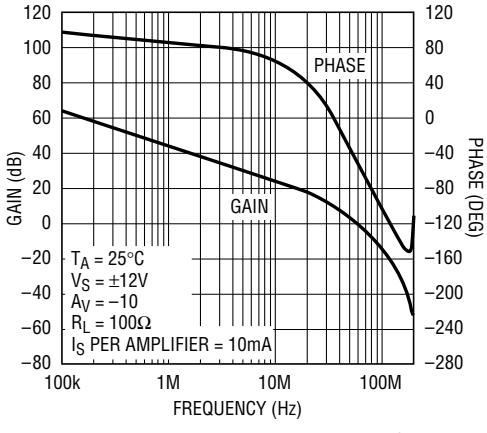
Output Short-Circuit Current vs Ambient Temperature



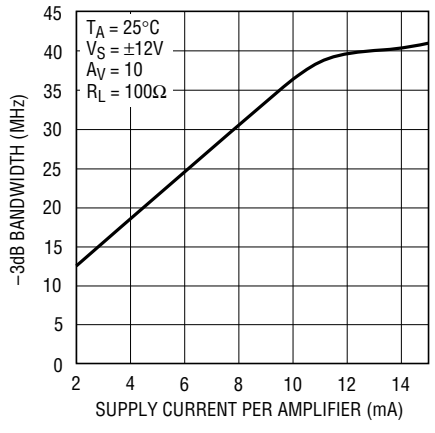
Output Saturation Voltage vs Ambient Temperature



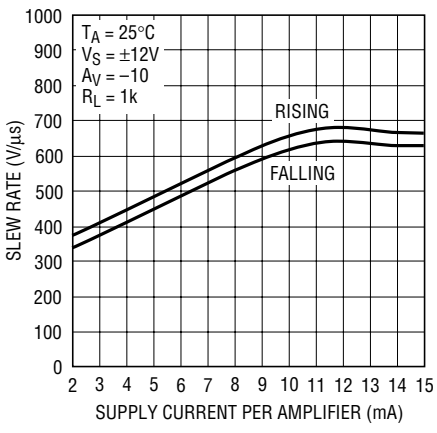
Open-Loop Gain and Phase vs Frequency



–3dB Bandwidth vs Supply Current

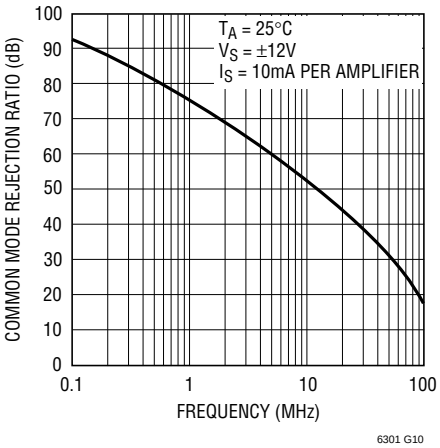


Slew Rate vs Supply Current

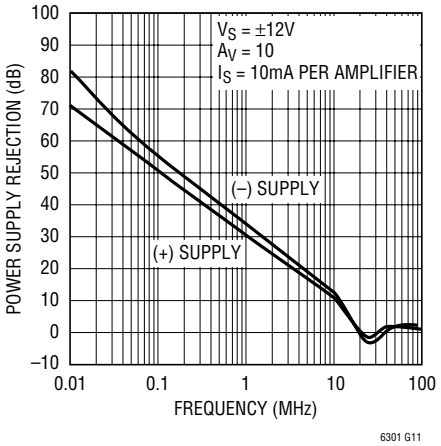


TYPICAL PERFORMANCE CHARACTERISTICS

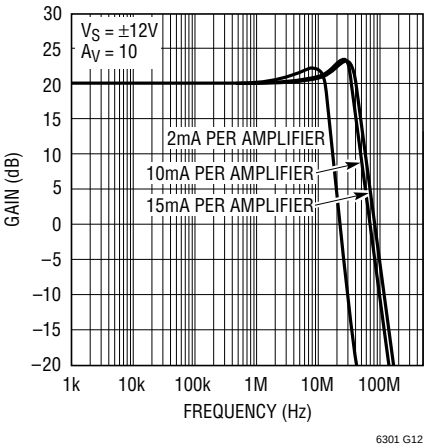
CMRR vs Frequency



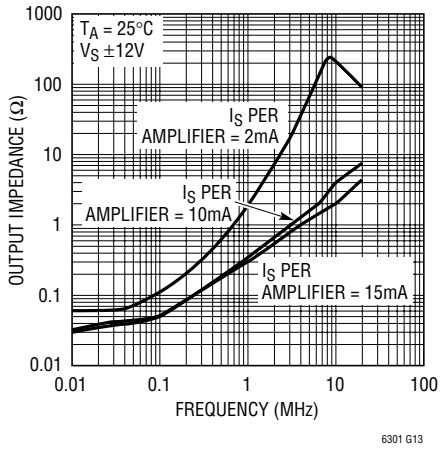
PSRR vs Frequency



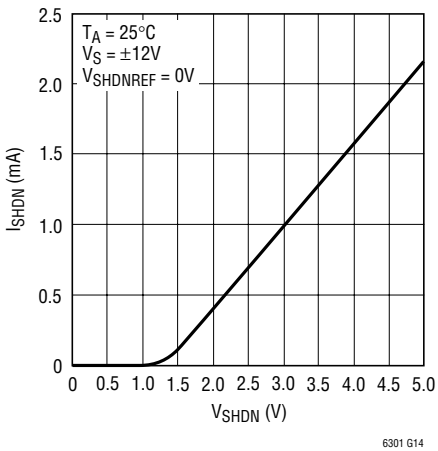
Frequency Response vs Supply Current



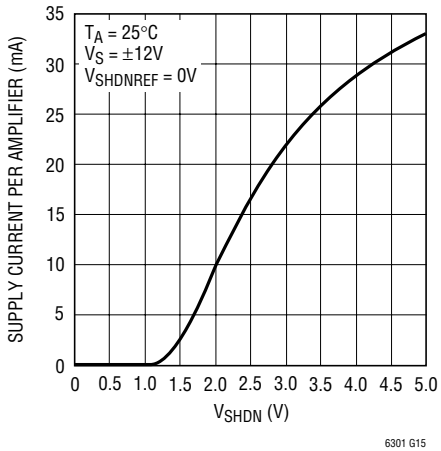
Output Impedance vs Frequency



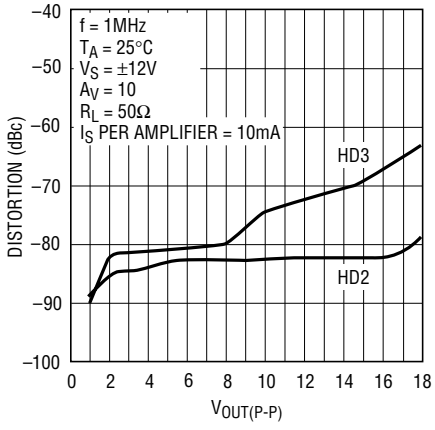
I_{SHDN} vs V_{SHDN}



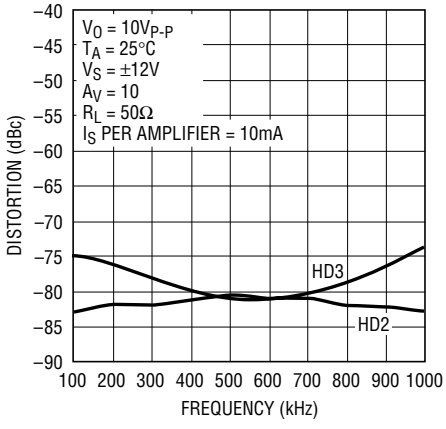
Supply Current vs V_{SHDN}



Differential Harmonic Distortion vs Output Amplitude

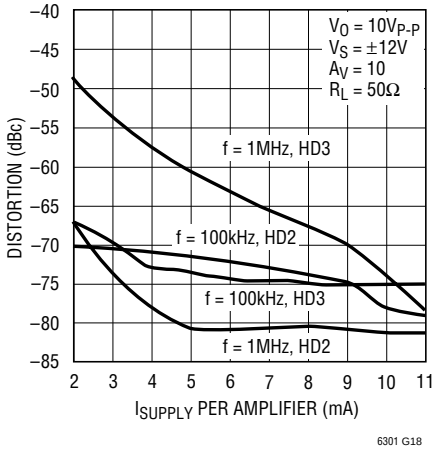


Differential Harmonic Distortion vs Frequency

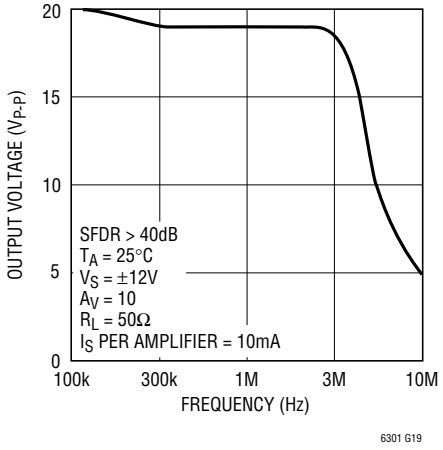


TYPICAL PERFORMANCE CHARACTERISTICS

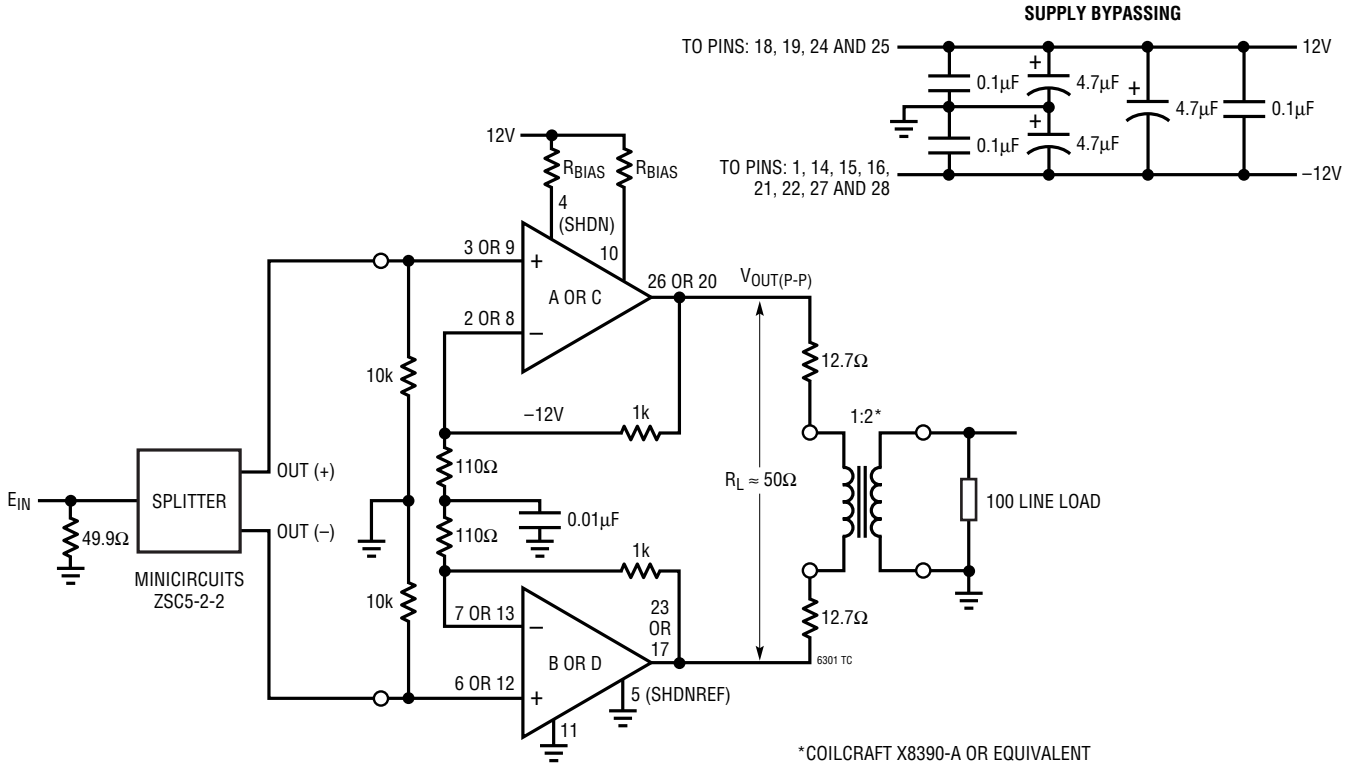
Differential Harmonic Distortion vs Supply Current



Undistorted Output Swing vs Frequency



TEST CIRCUIT



*COILCRAFT X8390-A OR EQUIVALENT
V_{OUTP-P} AMPLITUDE SET AT EACH AMPLIFIER OUTPUT
DISTORTION MEASURED ACROSS LINE LOAD
FOR MATCHING, USE AMPLIFIERS A AND B,
OR AMPLIFIERS C AND D

APPLICATIONS INFORMATION

The LT6301 is a high speed, 200MHz gain bandwidth product, quad voltage feedback amplifier with high output current drive capability, 500mA source and sink. The LT6301 is ideal for use as a line driver in xDSL data communication applications. The output voltage swing has been optimized to provide sufficient headroom when operating from ±12V power supplies in full-rate ADSL applications. The LT6301 also allows for an adjustment of the operating current to minimize power consumption. In addition, the LT6301 is available in a small footprint surface mount package to minimize PCB area.

To minimize signal distortion, the LT6301 amplifiers are decompensated to provide very high open-loop gain at high frequency. As a result each amplifier is frequency stable with a closed-loop gain of 10 or more. If a closed-loop gain of less than 10 is desired, external frequency compensating components can be used.

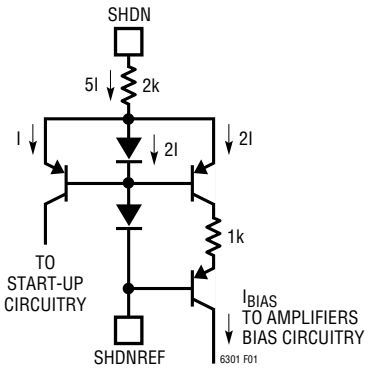


Figure 1. Internal Current Biasing Circuitry

Setting the Quiescent Operating Current

Power consumption and dissipation are critical concerns in multiport xDSL applications. Two pins, Shutdown (SHDN) and Shutdown Reference (SHDNREF), are provided to control quiescent power consumption and allow for the complete shutdown of the drivers. The quiescent current should be set high enough to prevent distortion induced errors in a particular application, but not so high that power is wasted in the driver unnecessarily. A good starting point to evaluate the LT6301 is to set the quiescent current to 10mA per amplifier. Pins 4 and 5 set the current for amplifiers A and B and Pins 10 and 11 set the current for amplifers C and D. Each amplifier pair should be controlled separately.

The internal biasing circuitry is shown in Figure 1. Grounding the SHDNREF pin and directly driving the SHDN pin with a voltage can control the operating current as seen in the Typical Performance Characteristics. When the SHDN pin is less than SHDNREF + 0.4V, the driver is shut down and consumes typically only 100µA of supply current and the outputs are in a high impedance state. Part to part variations, however, will cause inconsistent control of the quiescent current if direct voltage drive of the SHDN pin is used.

Using an external resistor, R_{BIAS}, connected in one of two ways provides a much more predictable control of the quiescent supply current. Figure 2 illustrates the effect on supply current per amplifier with R_{BIAS} connected between the SHDN pin and the 12V V^+ supply of the LT6301 and the approximate design equations. Figure 3 illustrates the same control with R_{BIAS} connected between the SHDNREF pin and ground while the SHDN pin is tied to V^+. Either approach is equally effective.

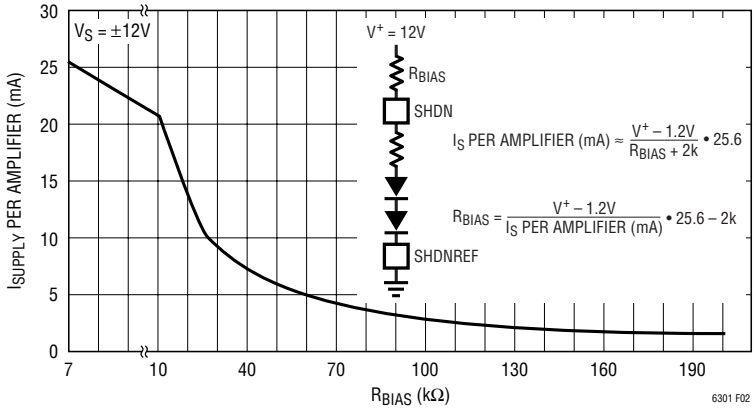


Figure 2. R_{BIAS} to V^+ Current Control

APPLICATIONS INFORMATION

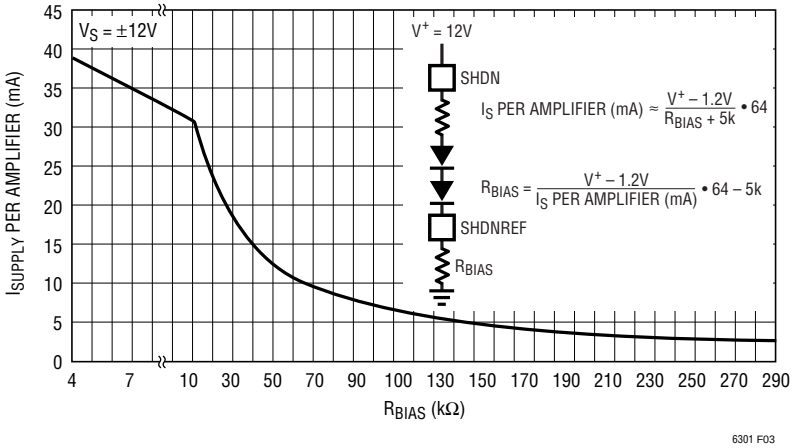


Figure 3. R_{BIAS} to Ground Current Control

Two Control Inputs

		RESISTOR VALUES (kΩ)					
		R_{SHDN} TO V_{CC} (12V)			R_{SHDN} TO V_{LOGIC}		
	V_{LOGIC}	3V	3.3V	5V	3V	3.3V	5V
	R_{SHDN}	40.2	43.2	60.4	4.99	6.81	19.6
	R_{C1}	11.5	13.0	21.5	8.66	10.7	20.5
	R_{C0}	19.1	22.1	36.5	14.3	17.8	34.0
V_{C1}	V_{C0}	SUPPLY CURRENT PER AMPLIFIER (mA)					
H	H	10	10	10	10	10	10
H	L	7	7	7	7	7	7
L	H	5	5	5	5	5	5
L	L	2	2	2	2	2	2

One Control Input

		RESISTOR VALUES (kΩ)					
		R_{SHDN} TO V_{CC} (12V)			R_{SHDN} TO V_{LOGIC}		
	V_{LOGIC}	3V	3.3V	5V	3V	3.3V	5V
	R_{SHDN}	40.2	43.2	60.4	4.99	6.81	19.6
	R_C	7.32	8.25	13.7	5.49	6.65	12.7
	V_C	SUPPLY CURRENT PER AMPLIFIER (mA)					
	H	10	10	10	10	10	10
	L	2	2	2	2	2	2

6301 F04

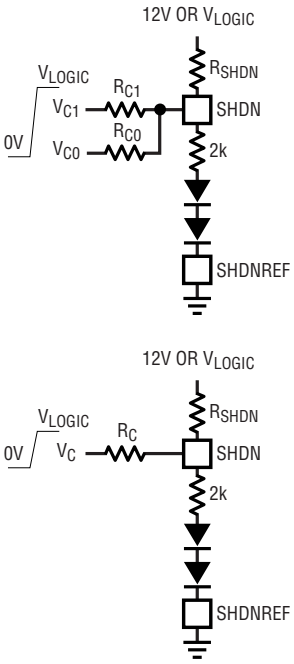


Figure 4. Providing Logic Input Control of Operating Current

Logic Controlled Operating Current

The DSP controller in a typical xDSL application can have I/O pins assigned to provide logic control of the LT6301 line driver operating current. As shown in Figure 4 one or two logic control inputs can control two or four different operating modes. The logic inputs add or subtract current to the SHDN input to set the operating current. The one logic input example selects the supply current to be either full power, 10mA per amplifier or just 2mA per amplifier, which significantly reduces the driver power consumption while maintaining less than 2Ω output impedance to frequencies less than 1MHz. This low power mode retains termination impedance at the amplifier outputs and the line driving back termination resistors. With this termination, while a DSL port is not transmitting data, it can still sense a received signal from the line across the back-termination resistors and respond accordingly.

The two logic input control provides two intermediate (approximately 7mA per amplifier and 5mA per amplifier) operating levels between full power and termination modes.

APPLICATIONS INFORMATION

These modes can be useful for overall system power management when full power transmissions are not necessary. Contact LTC Applications for single supply design information.

Shutdown and Recovery

The ultimate power saving action on a completely idle port is to fully shut down the line driver by pulling the SHDN pin to within 0.4V of the SHDNREF potential. As shown in Figure 5 complete shutdown occurs in less than 10µs and, more importantly, complete recovery from the shut down state to full operation occurs in less than 2µs. The biasing circuitry in the LT6301 reacts very quickly to bring the amplifiers back to normal operation.

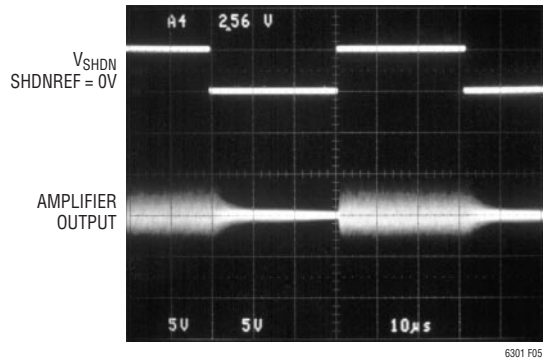


Figure 5. Shutdown and Recovery Timing

Power Dissipation and Heat Management

xDSL applications require the line driver to dissipate a significant amount of power and heat compared to other components in the system. The large peak to RMS variations of DMT and CAP ADSL signals require high supply voltages to prevent clipping, and the use of a step-up transformer to couple the signal to the telephone line can require high peak current levels. These requirements result in the driver package having to dissipate significant amounts of power. Several multiport cards inserted into a rack in an enclosed central office box can add up to many, many watts of power dissipation in an elevated ambient temperature environment. The LT6301 has built-in thermal shutdown circuitry that will protect the amplifiers if operated at excessive temperatures, however data transmissions will be seriously impaired. It is important in the design of the PCB and card enclosure to take measures to spread the heat developed in the driver away to the ambient environment to prevent thermal shutdown (which occurs when the junction temperature of the LT6301 exceeds 165°C).

Estimating Line Driver Power Dissipation

Figure 6 is a typical ADSL application shown for the purpose of estimating the power dissipation in the line driver. Due to the complex nature of the DMT signal,

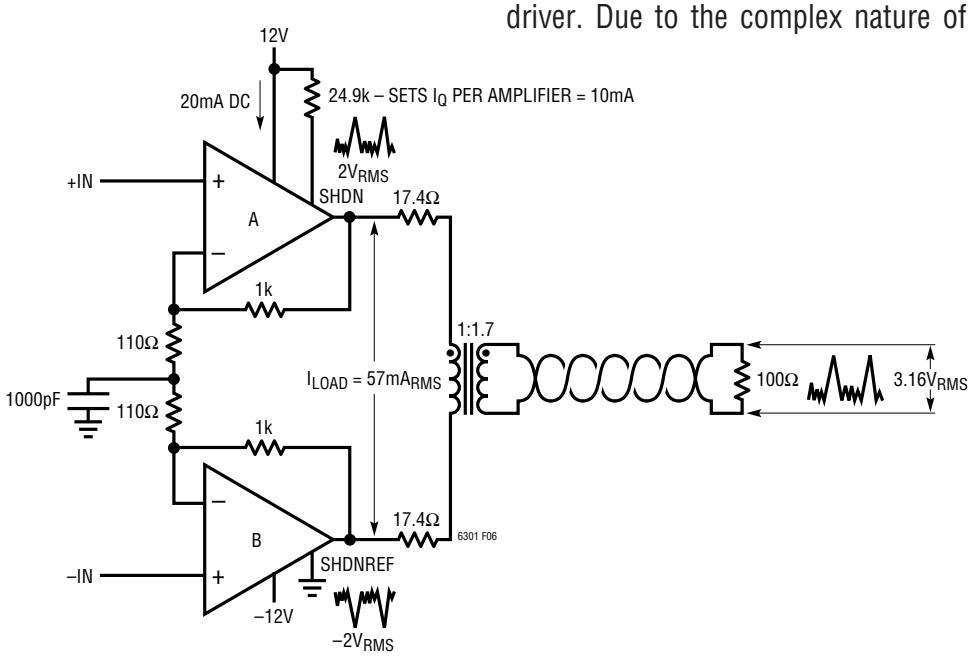


Figure 6. Estimating Line Driver Power Dissipation

APPLICATIONS INFORMATION

which looks very much like noise, it is easiest to use the RMS values of voltages and currents for estimating the driver power dissipation. The voltage and current levels shown for this example are for a full-rate ADSL signal driving 20dBm or $100mW_{RMS}$ of power on to the 100Ω telephone line and assuming a 0.5dBm insertion loss in the transformer. The quiescent current for the LT6301 is set to 10mA per amplifier.

The power dissipated in the LT6301 is a combination of the quiescent power and the output stage power when driving a signal. The two pairs of amplifiers are configured to place a differential signal on two lines. The Class AB output stage in each amplifier will simultaneously dissipate power in the upper power transistor of one amplifier, while sourcing current, and the lower power transistor of the other amplifier, while sinking current. The total device power dissipation is then:

$$P_D = P_{QUIESCENT} + P_{Q(UPPER)} + P_{Q(LOWER)}$$

$$P_D = (V^+ - V^-) \bullet I_Q + (V^+ - V_{OUTARMS}) \bullet I_{LOAD} + (V^- - V_{OUTBRMS}) \bullet I_{LOAD}$$

With no signal being placed on the line and the amplifier biased for 10mA per amplifier supply current, the quiescent driver power dissipation is:

$$P_{DQ} = [24V \bullet 10mA] \bullet 4 = 960mW$$

This can be reduced in many applications by operating with a lower quiescent current value or shutting down the part during idle conditions.

When driving a load, a large percentage of the amplifier quiescent current is diverted to the output stage and becomes part of the load current. Figure 7 illustrates the total amount of biasing current flowing between the + and – power supplies through the amplifiers as a function of load current for one differential driver. As much as 60% of the quiescent no load operating current is diverted to the load.

At full power to both lines the total package power dissipation is:

$$P_{D(FULL)} = [24V \bullet 8mA + (12V - 2V_{RMS}) \bullet 57mA_{RMS} + [|-12V - (-2V_{RMS})|] \bullet 57mA_{RMS}] \bullet 2$$

$$P_{D(FULL)} = [192mW + 570mW + 570mW] \bullet 2 = 2.664W^*$$

The junction temperature of the driver must be kept less than the thermal shutdown temperature when processing a signal. The junction temperature is determined from the following expression:

$$T_J = T_{AMBIENT}\ (°C) + P_{D(FULL)}\ (W) \bullet \theta_{JA}\ (°C/W)$$

θ_{JA} is the thermal resistance from the junction of the LT6301 to the ambient air, which can be minimized by heat-spreading PCB metal and airflow through the enclosure as required. For the example given, assuming a maximum ambient temperature of 50°C and keeping the junction temperature of the LT6301 to 150°C maximum, the maximum thermal resistance from junction to ambient required is:

$$\theta_{JA(MAX)} = \frac{150°C - 50°C}{2.664W} = 37.5°C/W$$

*Design techniques exist to significantly reduce this value (See Line Driving Back Termination).

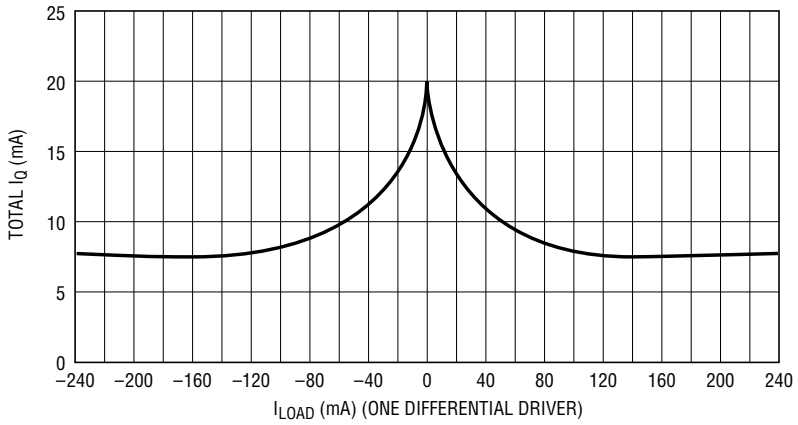


Figure 7. I_Q vs I_{LOAD}

APPLICATIONS INFORMATION

Heat Sinking Using PCB Metal

Designing a thermal management system is often a trial and error process as it is never certain how effective it is until it is manufactured and evaluated. As a general rule, the more copper area of a PCB used for spreading heat away from the driver package, the more the operating junction temperature of the driver will be reduced. The limit to this approach however is the need for very compact circuit layout to allow more ports to be implemented on any given size PCB.

To best extract heat from the FE28 package, a generous area of top layer PCB metal should be connected to the four corner pins (Pins 1, 14, 15 and 28). These pins are fused to the leadframe where the LT6301 die are attached. The package also has an exposed metal heat sinking pad on the bottom side which, when soldered to the PCB top layer metal, directly conducts heat away from the IC junction. Soldering the thermal pad to the board produces a thermal resistance from junction to case, θ_{JC}, of approximately 3°C/W.

Important Note: The metal planes used for heat sinking the LT6301 are electrically connected to the negative supply potential of the driver, typically –12V. These planes must be isolated from any other power planes used in the board design.

Fortunately xDSL circuit boards use multiple layers of metal for interconnection of components. Areas of metal beneath the LT6301 connected together through several small 13 mil vias can be effective in conducting heat away from the driver package. The use of inner layer metal can free up top and bottom layer PCB area for external component placement.

When PCB cards containing multiple ports are inserted into a rack in an enclosed cabinet, it is often necessary to provide airflow through the cabinet and over the cards. This is also very effective in reducing the junction-to-ambient thermal resistance of each line driver. To a limit, this thermal resistance can be reduced approximately 5°C/W for every 100lfpm of laminar airflow.

Layout and Passive Components

With a gain bandwidth product of 200MHz the LT6301 requires attention to detail in order to extract maximum performance. Use a ground plane, short lead lengths and a combination of RF-quality supply bypass capacitors (i.e., 0.1µF). As the primary applications have high drive current, use low ESR supply bypass capacitors (1µF to 10µF).

The four V^+ pins (Pins 18, 19, 24, 25) separately provide power to each amplifier and should be shorted together with leads as short as possible to the bypass capacitors.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole that can cause frequency peaking. In general, use feedback resistors of 1k or less.

Compensation

The LT6301 is stable in a gain 10 or higher for any supply and resistive load. It is easily compensated for lower gains with a single resistor or a resistor plus a capacitor.

Figure 8 shows that for inverting gains, a resistor from the inverting node to AC ground guarantees stability if the parallel combination of R_C and R_G is less than or equal to $R_F/9$. For lowest distortion and DC output offset, a series capacitor, C_C, can be used to reduce the noise gain at lower frequencies. The break frequency produced by R_C and C_C should be less than 5MHz to minimize peaking.

Figure 9 shows compensation in the noninverting configuration. The R_C, C_C network acts similarly to the inverting case. The input impedance is not reduced because the network is bootstrapped. This network can also be placed between the inverting input and an AC ground.

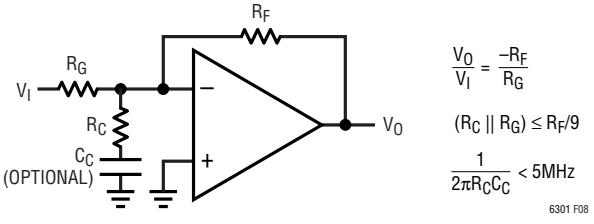


Figure 8. Compensation for Inverting Gains

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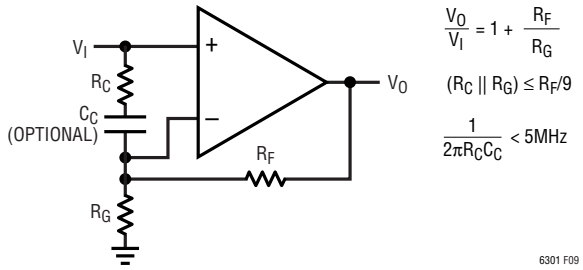


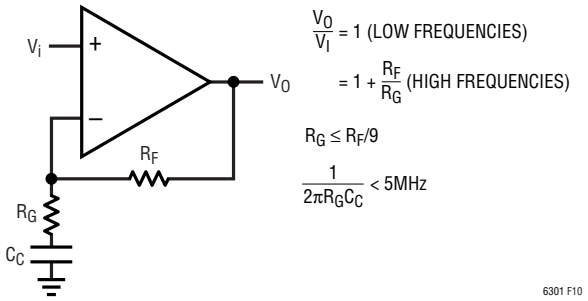
$$\frac{V_O}{V_I} = 1 + \frac{R_F}{R_G}$$

$$(R_C \parallel R_G) \leq R_F/9$$

$$\frac{1}{2\pi R_C C_C} < 5MHz$$

Figure 9. Compensation for Noninverting Gains

Another compensation scheme for noninverting circuits is shown in Figure 10. The circuit is unity gain at low frequency and a gain of $1 + R_F/R_G$ at high frequency. The DC output offset is reduced by a factor of ten. The techniques of Figures 9 and 10 can be combined as shown in Figure 11. The gain is unity at low frequencies, $1 + R_F/R_G$ at mid-band and for stability, a gain of 10 or greater at high frequencies.



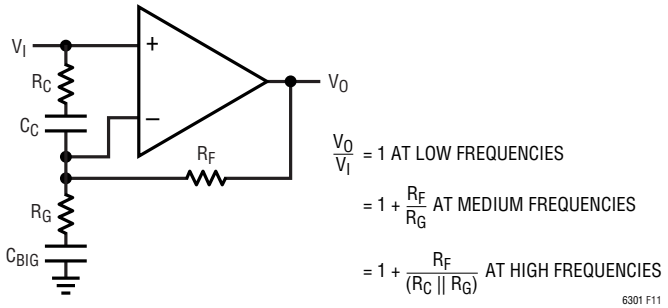
$$\frac{V_O}{V_I} = 1 \text{ (LOW FREQUENCIES)}$$

$$= 1 + \frac{R_F}{R_G} \text{ (HIGH FREQUENCIES)}$$

$$R_G \leq R_F/9$$

$$\frac{1}{2\pi R_G C_C} < 5MHz$$

Figure 10. Alternate Noninverting Compensation



$$\frac{V_O}{V_I} = 1 \text{ AT LOW FREQUENCIES}$$

$$= 1 + \frac{R_F}{R_G} \text{ AT MEDIUM FREQUENCIES}$$

$$= 1 + \frac{R_F}{(R_C \parallel R_G)} \text{ AT HIGH FREQUENCIES}$$

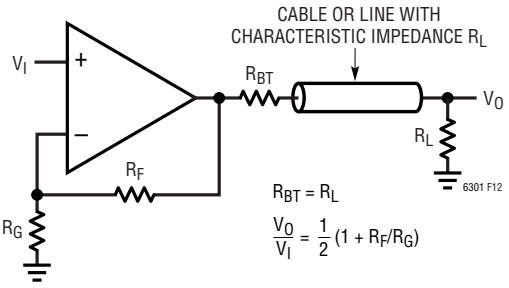
Figure 11. Combination Compensation

In differential driver applications, as shown on the first page of this data sheet, it is recommended that the gain setting resistor be comprised of two equal value resistors connected to a good AC ground at high frequencies. This ensures that the feedback factor of each amplifier remains less than 0.1 at any frequency. The midpoint of the resistors can be directly connected to ground, with the resulting DC gain to the V_{OS} of the amplifiers, or just bypassed to ground with a 1000pF or larger capacitor.

Line Driving Back-Termination

The standard method of cable or line back-termination is shown in Figure 12. The cable/line is terminated in its characteristic impedance (50Ω, 75Ω, 100Ω, 135Ω, etc.). A back-termination resistor also equal to the chararacteristic impedance should be used for maximum pulse fidelity of outgoing signals, and to terminate the line for incoming signals in a full-duplex application. There are three main drawbacks to this approach. First, the power dissipated in the load and back-termination resistors is equal so half of the power delivered by the amplifier is wasted in the termination resistor. Second, the signal is halved so the gain of the amplifer must be doubled to have the same overall gain to the load. The increase in gain increases noise and decreases bandwidth (which can also increase distortion). Third, the output swing of the amplifier is doubled which can limit the power it can deliver to the load for a given power supply voltage.

An alternate method of back-termination is shown in Figure 13. Positive feedback increases the effective back-termination resistance so R_{BT} can be reduced by a factor



$$R_{BT} = R_L$$

$$\frac{V_O}{V_I} = \frac{1}{2}(1 + R_F/R_G)$$

Figure 12. Standard Cable/Line Back Termination

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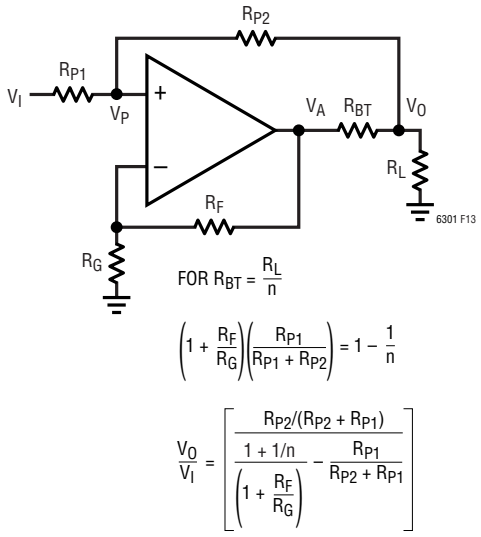

Figure 13. Back Termination Using Postive Feedback

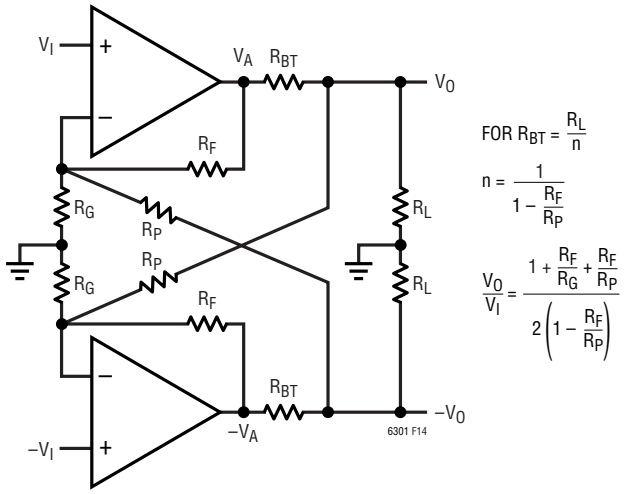

Figure 14. Back Termination Using Differential Postive Feedback

of n. To analyze this circuit, first ground the input. As $R_{BT} = R_L/n$, and assuming $R_{P2} >> R_L$ we require that:

$V_A = V_O (1 – 1/n)$ to increase the effective value of R_{BT} by n.

$V_P = V_O (1 – 1/n)/(1 + R_F/R_G)$

$V_O = V_P (1 + R_{P2}/R_{P1})$

Eliminating V_P, we get the following:

$(1 + R_{P2}/R_{P1}) = (1 + R_F/R_G)/(1 – 1/n)$

For example, reducing R_{BT} by a factor of n = 4, and with an amplifer gain of $(1 + R_F/R_G) = 10$ requires that $R_{P2}/R_{P1} = 12.3$.

Note that the overall gain is increased:

$$\frac{V_O}{V_I} = \frac{R_{P2}/(R_{P2}+R_{P1})}{\left[(1+1/n)/(1+R_F/R_G)\right] - \left[R_{P1}/(R_{P2}+R_{P1})\right]}$$

A simpler method of using positive feedback to reduce the back-termination is shown in Figure 14. In this case, the drivers are driven differentially and provide complementary outputs. Grounding the inputs, we see there is inverting gain of $–R_F/R_P$ from $–V_O$ to V_A

$V_A = V_O (R_F/R_P)$

and assuming $R_P >> R_L$, we require

$V_A = V_O (1 – 1/n)$

solving

$R_F/R_P = 1 – 1/n$

So to reduce the back-termination by a factor of 3 choose $R_F/R_P = 2/3$. Note that the overall gain is increased to:

$V_O/V_I = (1 + R_F/R_G + R_F/R_P)/[2(1 – R_F/R_P)]$

Using positive feedback is often referred to as active termination.

Figure 16 shows a full-rate ADSL line driver incorporating positive feedback to reduce the power lost in the back termination resistors by 40% yet still maintains the proper impedance match to the100Ω characteristic line impedance. This circuit also reduces the transformer turns ratio over the standard line driving approach resulting in lower peak current requirements. With lower current and less power loss in the back termination resistors, this driver dissipates only 1W of power, a 30% reduction.

While the power savings of positive feedback are attractive there is one important system consideration to be addressed, received signal sensitivity. The signal received

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from the line is sensed across the back termination resistors. With positive feedback, signals are present on both ends of the R_{BT} resistors, reducing the sensed amplitude. Extra gain may be required in the receive channel to compensate, or a completely separate receive path may be implemented through a separate line coupling transformer.

Considerations for Fault Protection

The basic line driver design, shown on the front page of this data sheet, presents a direct DC path between the outputs of the two amplifiers. An imbalance in the DC biasing potentials at the noninverting inputs through either a fault condition or during turn-on of the system can create a DC voltage differential between the two amplifier outputs. This condition can force a considerable amount of current to flow as it is limited only by the small valued back-termination resistors and the DC resistance of the transformer primary. This high current can possibly cause the power supply voltage source to drop significantly impacting overall system performance. If left unchecked, the high DC current can heat the LT6301 to thermal shutdown.

Using DC blocking capacitors, as shown in Figure 15, to AC couple the signal to the transformer eliminates the possibility for DC current to flow under any conditions. These capacitors should be sized large enough to not impair the frequency response characteristics required for the data transmission.

Another important fault related concern has to do with very fast high voltage transients appearing on the telephone line (lightning strikes for example). TransZorbs®, varistors and other transient protection devices are often used to absorb the transient energy, but in doing so also create fast voltage transitions themselves that can be coupled through the transformer to the outputs of the line driver. Several hundred volt transient signals can appear at the primary windings of the transformer with current into the driver outputs limited only by the back termination resistors. While the LT6301 has clamps to the supply rails at the output pins, they may not be large enough to handle the significant transient energy. External clamping diodes, such as BAV99s, at each end of the transformer primary help to shunt this destructive transient energy away from the amplifier outputs.

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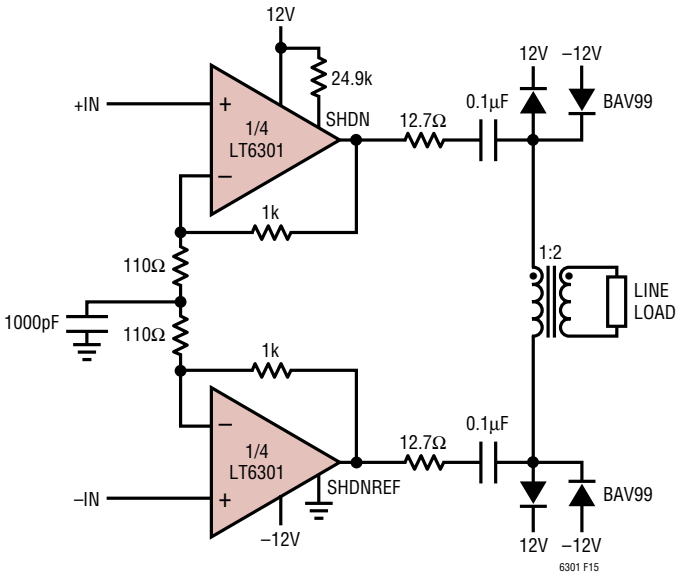
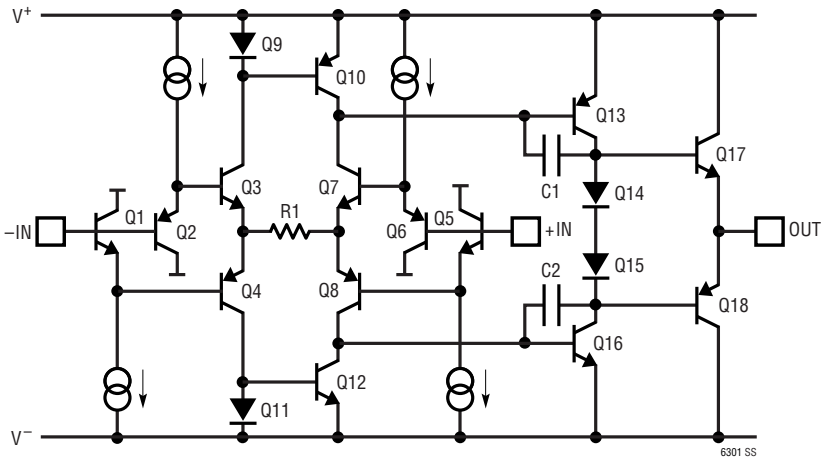


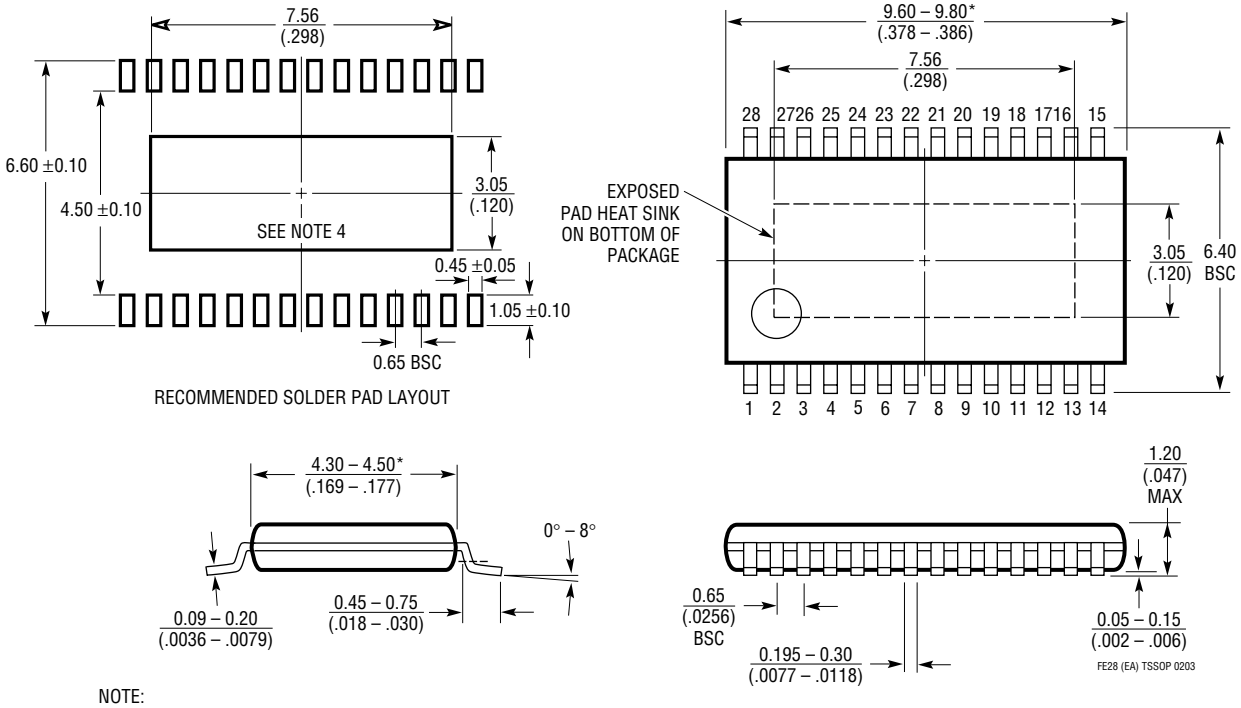
Figure 15. Protecting the Driver Against Load Faults and Line Transients

SIMPLIFIED SCHEMATIC (one amplifier shown)



PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

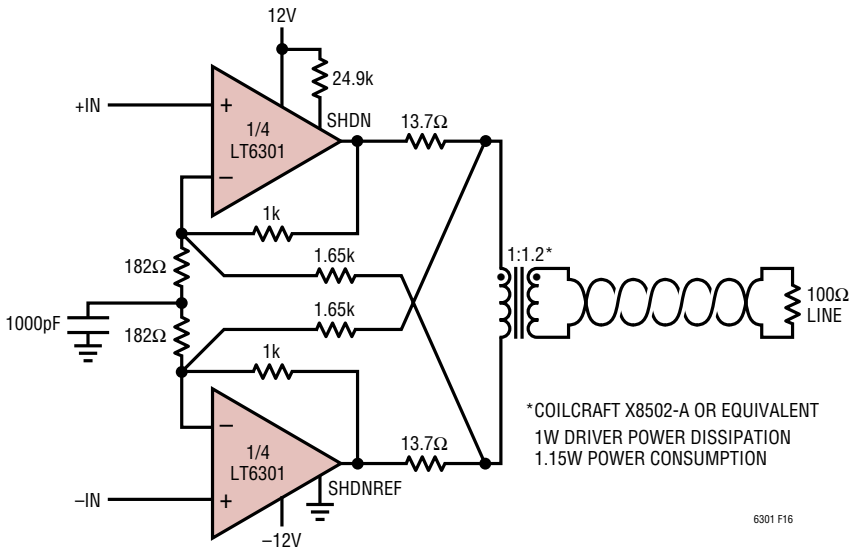


Figure 16. ADSL Line Driver Using Active Termination

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1361	Dual 50MHz, 800V/µs Op Amp	±15V Operation, 1mV V_{OS}, 1µA I_B
LT1739	Dual 500mA, 200MHz xDSL Line Driver	Low Cost ADSL CO Driver, Low Power
LT1794	Dual 500mA, 200MHz xDSL Line Driver	ADSL CO Driver, Extended Output Swing, Low Power
LT1795	Dual 500mA, 50MHz Current Feedback Amplifier	Shutdown/Current Set Function, ADSL CO Driver
LT1813	Dual 100MHz, 750V/µs, 8nV/$\sqrt{Hz}$ Op Amp	Low Noise, Low Power Differential Receiver, 4mA/Amplifier
LT1886	Dual 200mA, 700MHz Op Amp	12V Operation, 7mA/Amplifier, ADSL CPE Modem Line Driver
LT1969	Dual 200mA, 700MHz Op Amp with Power Control	12V Operation, MSOP Package, ADSL CPE Modem Line Driver
LT6300	Dual 500mA, 200MHz, xDSL Line Driver	ADSL CO Driver in SSOP Package

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