ABSOLUTE MAXIMUM RATINGS

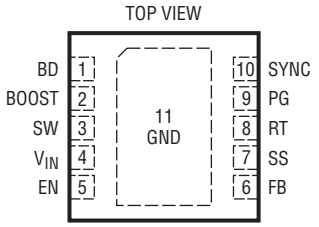
(Note 1)

V_{IN}, EN Voltage 55V
BOOST Pin Voltage 75V
BOOST Pin Above SW Pin.....30V
FB, V_{OUT}, RT, SYNC, SS Voltage 6V
PG, BD Voltage 30V
Boost Diode Current.....1A

Operating Junction Temperature Range (Note 2)
LT3991E..... –40°C to 125°C
LT3991I..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
(MSE Only) ..... 300°C

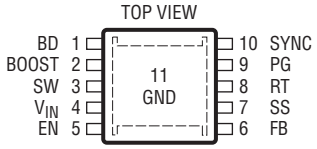
PIN CONFIGURATION

LT3991



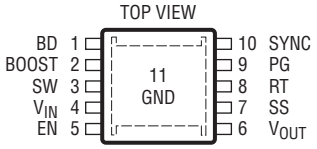
DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
θ_{JA} = 45°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

LT3991



MSE PACKAGE
10-LEAD PLASTIC MSOP
θ_{JA} = 45°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

LT3991-3.3, LT3991-5



MSE PACKAGE
10-LEAD PLASTIC MSOP
θ_{JA} = 45°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3991EDD#PBF	LT3991EDD#TRPBF	LFJR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3991IDD#PBF	LT3991IDD#TRPBF	LFJR	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C
LT3991EMSE#PBF	LT3991EMSE#TRPBF	LTFJS	10-Lead Plastic MSOP	–40°C to 125°C
LT3991IMSE#PBF	LT3991IMSE#TRPBF	LTFJS	10-Lead Plastic MSOP	–40°C to 125°C
LT3991EMSE-3.3#PBF	LT3991EMSE-3.3#TRPBF	LTFRS	10-Lead Plastic MSOP	–40°C to 125°C
LT3991IMSE-3.3#PBF	LT3991IMSE-3.3#TRPBF	LTFRS	10-Lead Plastic MSOP	–40°C to 125°C
LT3991EMSE-5#PBF	LT3991EMSE-5#TRPBF	LTFRV	10-Lead Plastic MSOP	–40°C to 125°C
LT3991IMSE-5#PBF	LT3991IMSE-5#TRPBF	LTFRV	10-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{EN} = 12V, V_{BD} = 3.3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	(Note 4)	●		4	4.3	V
Quiescent Current from V_{IN}	V_{EN} Low V_{EN} High, V_{SYNC} Low V_{EN} High, V_{SYNC} Low	 ●		0.7 1.7	1.2 2.7 4.5	µA µA µA
LT3991 FB Pin Current	V_{FB} = 1.19V	●		0.1	12	nA
Internal Feedback Resistor Divider				10		MΩ
Feedback Voltage		 ●	1.175 1.165	1.19 1.19	1.205 1.215	V V
LT3991-3.3 Output Voltage		 ●	3.25 3.224	3.3 3.3	3.35 3.376	V V
LT3991-5 Output Voltage		 ●	4.93 4.89	5 5	5.07 5.11	V V
FB Voltage Line Regulation	4.3V < V_{IN} < 40V (Note 4)			0.0002	0.01	%/V
Switching Frequency	R_T = 11k R_T = 35.7k R_T = 255k		1.6 0.8 160	2 1 200	2.4 1.2 240	MHz MHz kHz
Minimum Switch On Time				110		ns
Minimum Switch Off Time				150	200	ns
Switch Current Limit			1.7	2.3	2.9	A
Switch V_{CESAT}	I_{SW} = 1A			440		mV
Switch Leakage Current				0.02	1	µA
Boost Schottky Forward Voltage	I_{SH} = 100mA			800		mV
Boost Schottky Reverse Leakage	$V_{REVERSE}$ = 12V			0.02	1	µA
Minimum Boost Voltage (Note 3)	V_{IN} = 5V	●		1.4	1.8	V
BOOST Pin Current	I_{SW} = 1A, V_{BOOST} = 15V			25	33	mA
EN Voltage Threshold	EN Rising	●	0.95	1.01	1.07	V
EN Voltage Hysteresis				30		mV
EN Pin Current				0.2	20	nA
LT3991 PG Threshold Offset from V_{FB}	V_{FB} Rising		60	100	140	mV
LT3991 PG Hysteresis				20		mV
LT3991-X PG Threshold Offset from V_{OUT}	V_{OUT} Rising		5.5	9	12.5	%
LT3991X PG Hysteresis				1.3		%
PG Leakage	V_{PG} = 3V			0.02	1	µA
PG Sink Current	V_{PG} = 0.4V	●	300	570		µA
SYNC Threshold			0.6	0.8	1.0	V
SYNC Pin Current				0.1		nA
SS Source Current	V_{SS} = 1V		0.6	1	1.6	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3991E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3991I is guaranteed over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the switch.

Note 4: Minimum input voltage depends on application circuit.

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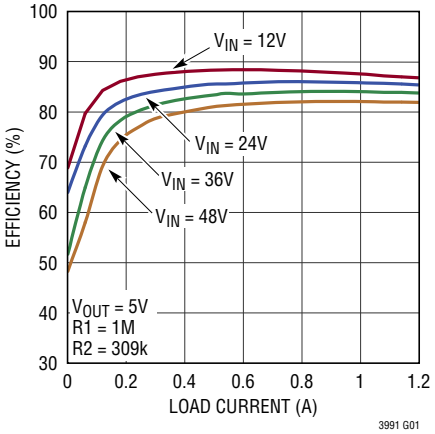
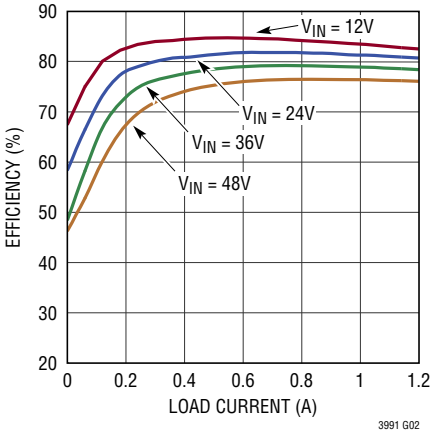
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

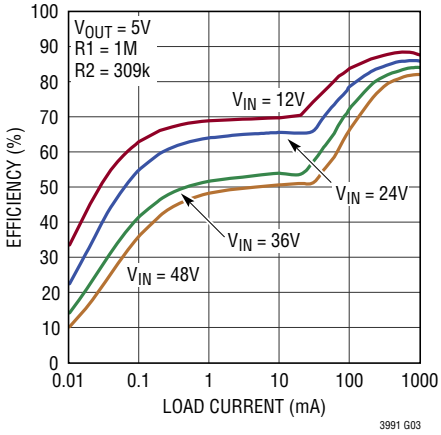
Efficiency, V_{OUT} = 5V



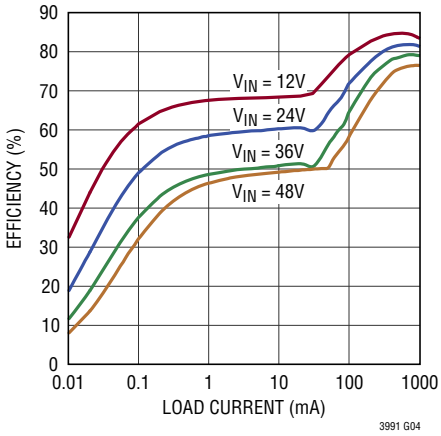
Efficiency, V_{OUT} = 3.3V



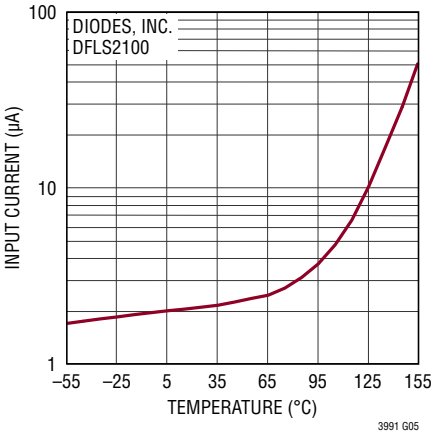
Efficiency, V_{OUT} = 5V



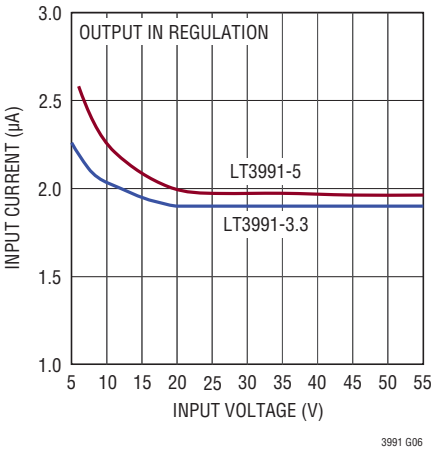
Efficiency, V_{OUT} = 3.3V



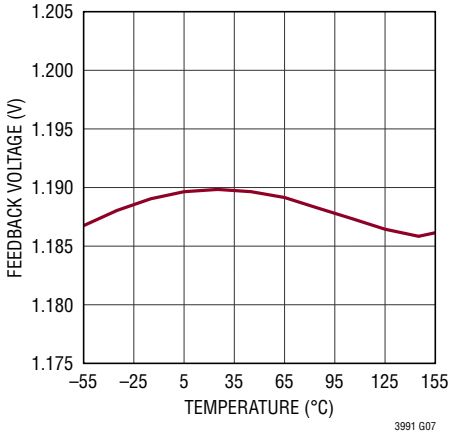
No Load Supply Current



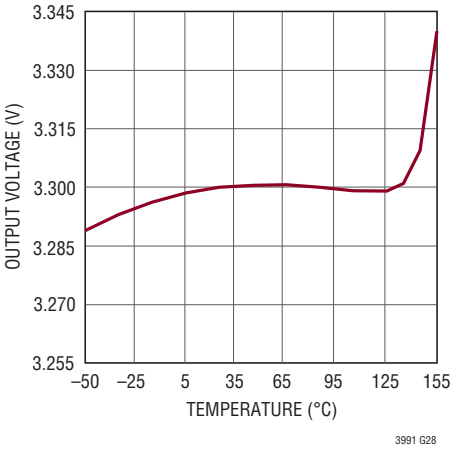
No Load Supply Current



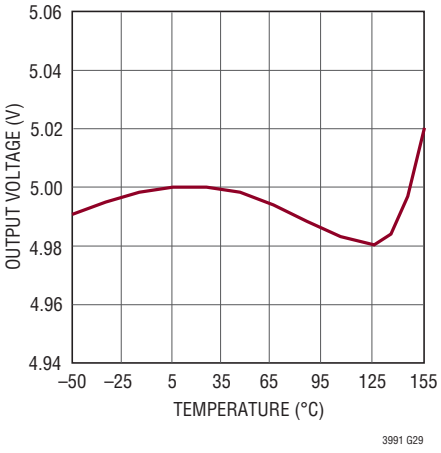
LT3991 Feedback Voltage



LT3991-3.3 Output Voltage



LT3991-5 Output Voltage



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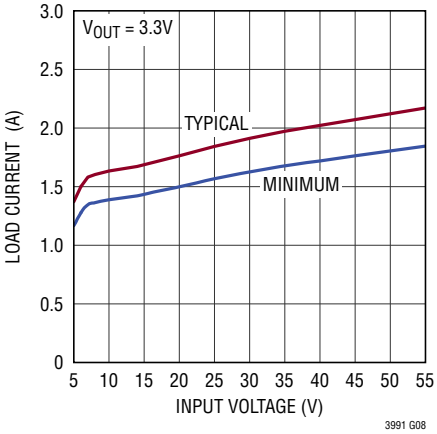
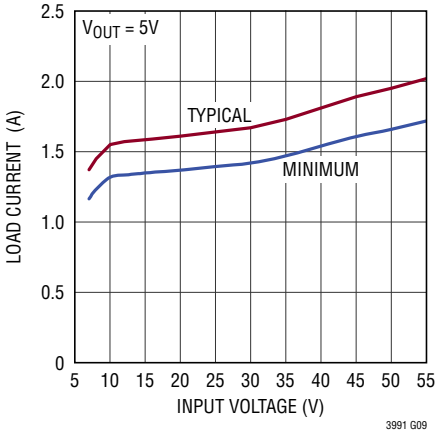
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

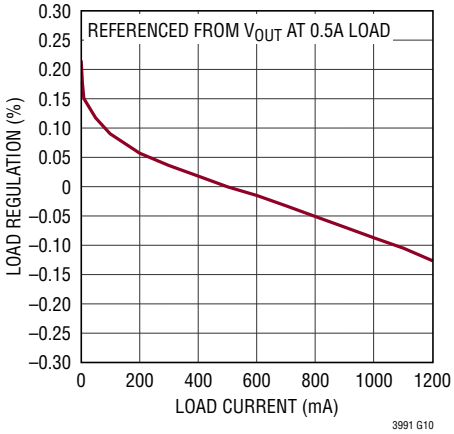
Maximum Load Current



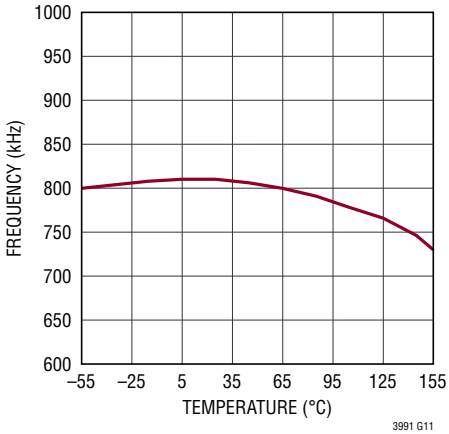
Maximum Load Current



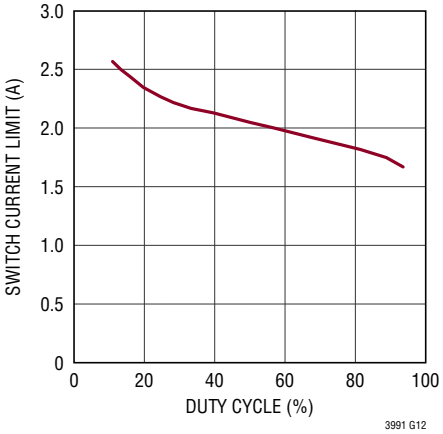
Load Regulation



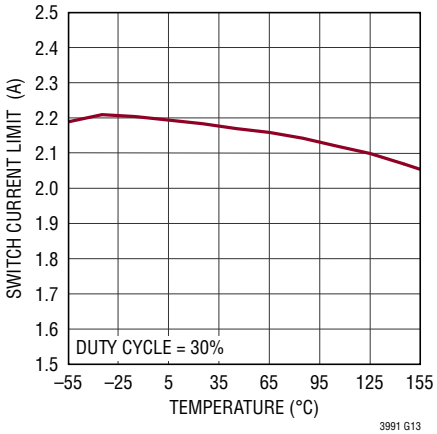
Switching Frequency



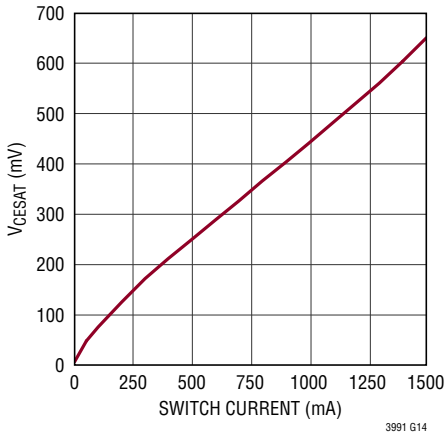
Switch Current Limit



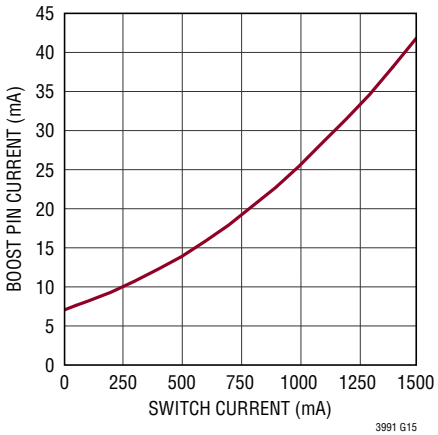
Switch Current Limit



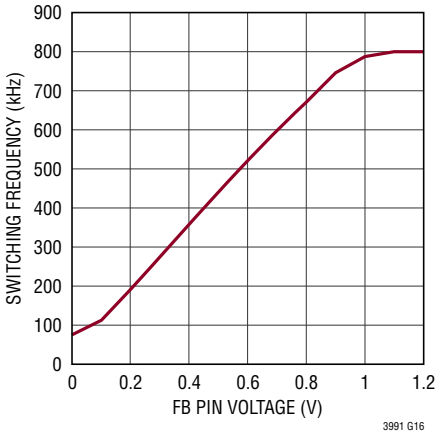
Switch V_{CESAT}



Boost Pin Current



LT3991 Frequency Foldback



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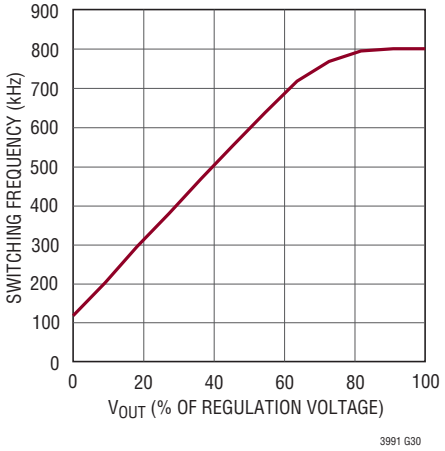
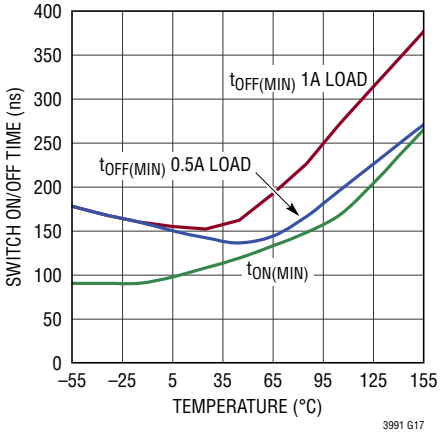
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

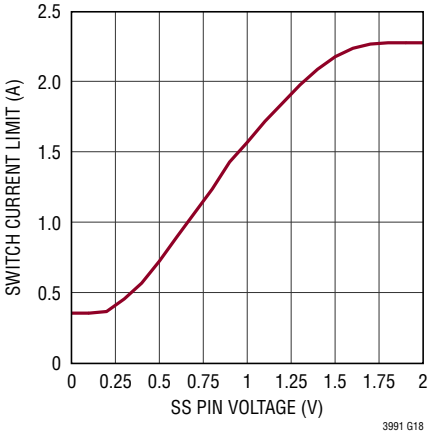
LT3991-X Frequency Foldback



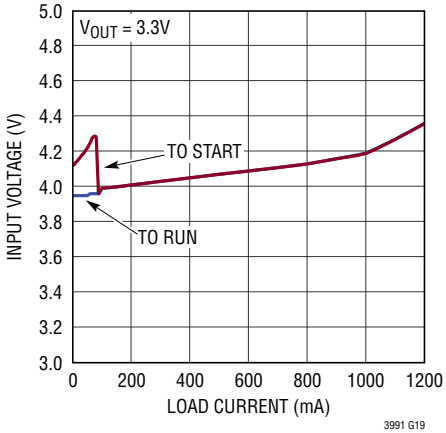
Minimum Switch On-Time/ Switch Off-Time



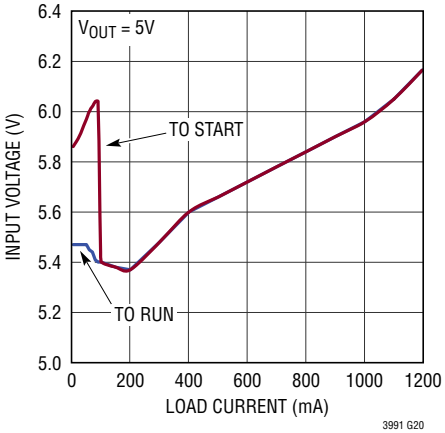
Soft-Start



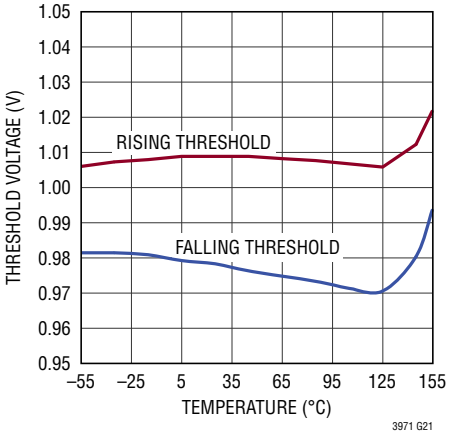
Minimum Input Voltage



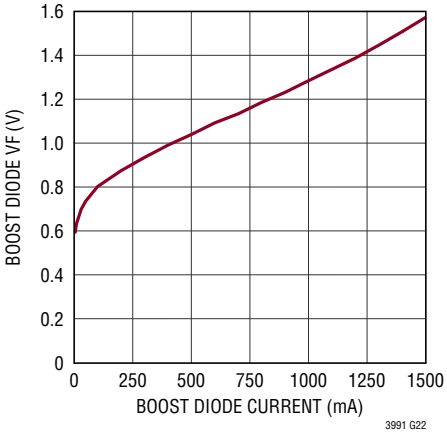
Minimum Input Voltage



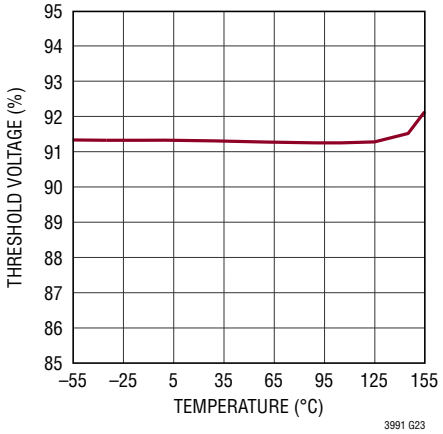
EN Threshold



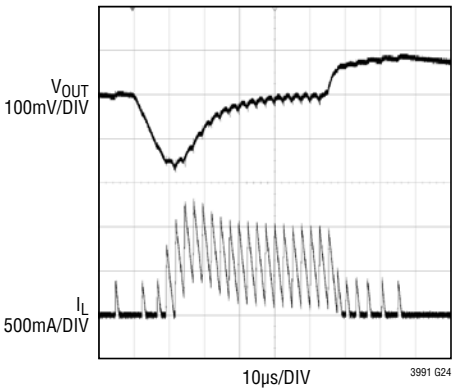
Boost Diode Forward Voltage



Power Good Threshold



Transient Load Response, Load Current Stepped from 25mA (Burst Mode Operation) to 525mA



V_{IN} = 48V, V_{OUT} = 3.3V
C_{OUT} = 47µF

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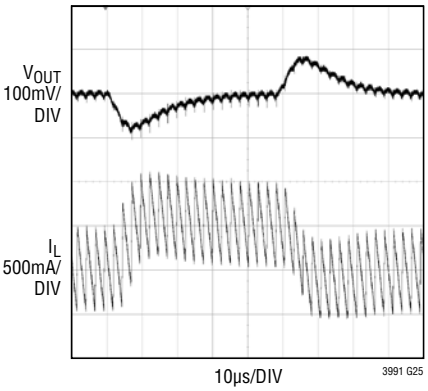
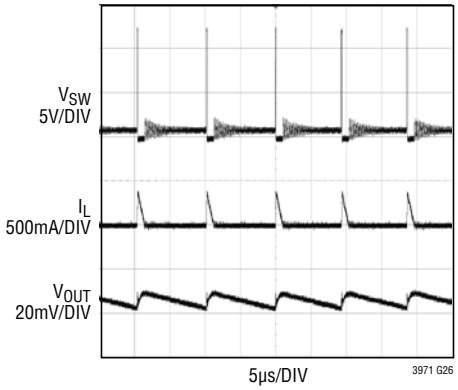
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Transient Load Response, Load Current Stepped from 0.5A to 1A



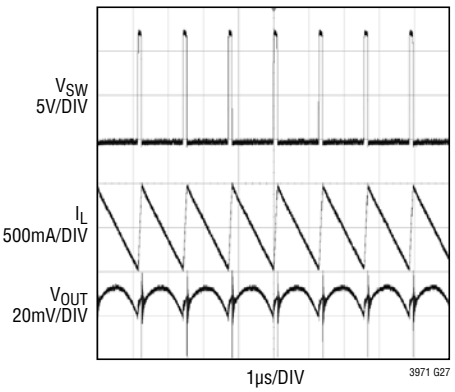
V_{IN} = 48V, V_{OUT} = 3.3V
C_{OUT} = 47µF

Switching Waveforms; Burst Mode Operation



V_{IN} = 48V, V_{OUT} = 3.3V
I_{LOAD} = 20mA
C_{OUT} = 47µF

Switching Waveforms; Full Frequency Continuous Operation



V_{IN} = 48V, V_{OUT} = 3.3V
I_{LOAD} = 1A
C_{OUT} = 47µF

PIN FUNCTIONS

BD (Pin 1): This pin connects to the anode of the boost diode. The BD pin is normally connected to the output.

BOOST (Pin 2): This pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch.

SW (Pin 3): The SW pin is the output of an internal power switch. Connect this pin to the inductor, catch diode, and boost capacitor.

V_{IN} (Pin 4): The V_{IN} pin supplies current to the LT3991's internal circuitry and to the internal power switch. This pin must be locally bypassed.

EN (Pin 5): The part is in shutdown when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.005V going up and 0.975V going down. The EN threshold is only accurate when V_{IN} is above 4.3V. If V_{IN} is lower than 4.3V, ground EN to place the part in shutdown. Tie to V_{IN} if shutdown feature is not used.

FB (Pin 6, LT3991 Only): The LT3991 regulates the FB pin to 1.19V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically this capacitor is 10pF.

V_{OUT} (Pin 6, LT3991-3.3/LT3991-5 Only): The LT3991-3.3 and LT3991-5 regulate the V_{OUT} pin to 3.3V and 5V respectively. This pin connects to the internal 10MΩ feedback divider that programs the fixed output voltage.

SS (Pin 7): A capacitor and a series resistor are tied between SS and ground to slowly ramp up the peak current limit of the LT3991 on start-up. The soft-start capacitor is only actively discharged when EN is low. The SS pin is released when the EN pin goes high. Float this pin to disable soft-start. The soft-start resistor has a typical value of 100k.

RT (Pin 8): A resistor is tied between RT and ground to set the switching frequency.

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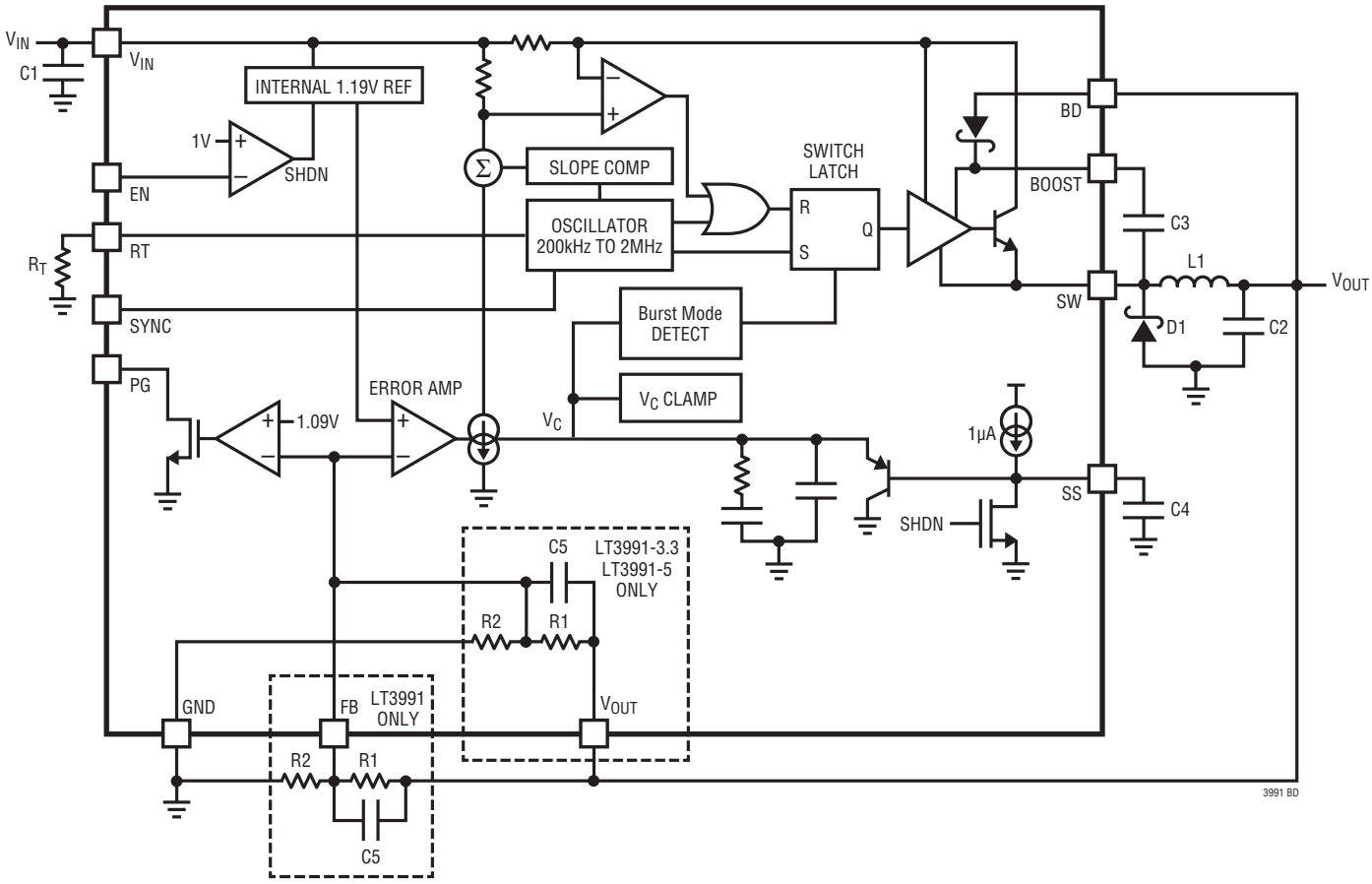
PIN FUNCTIONS

PG (Pin 9): The PG pin is the open-drain output of an internal comparator. PGOOD remains low until the FB pin is within 9% of the final regulation voltage. PGOOD is valid when the LT3991 is enabled and V_{IN} is above 4.3V.

SYNC (Pin 10): This is the external clock synchronization input. Ground this pin for low ripple Burst Mode operation at low output loads. Tie to a clock source for synchronization, which will include pulse-skipping at low output loads. When in pulse-skipping mode, quiescent current increases to 1.5mA.

GND (Exposed Pad Pin 11): Ground. The exposed pad must be soldered to PCB.

BLOCK DIAGRAM



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OPERATION

The LT3991 is a constant frequency, current mode step-down regulator. An oscillator, with frequency set by RT, sets an RS flip-flop, turning on the internal power switch. An amplifier and comparator monitor the current flowing between the V_{IN} and SW pins, turning the switch off when this current reaches a level determined by the voltage at V_C (see Block Diagram). An error amplifier measures the output voltage through an external resistor divider tied to the FB pin and servos the V_C node. If the error amplifier's output increases, more current is delivered to the output; if it decreases, less current is delivered. An active clamp on the V_C node provides current limit. The V_C node is also clamped by the voltage on the SS pin; soft-start is implemented by generating a voltage ramp at the SS pin using an external capacitor and resistor.

If the EN pin is low, the LT3991 is shut down and draws 700nA from the input. When the EN pin exceeds 1.01V, the switching regulator will become active.

The switch driver operates from either V_{IN} or from the BOOST pin. An external capacitor is used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to fully saturate the internal bipolar NPN power switch for efficient operation.

To further optimize efficiency, the LT3991 automatically switches to Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA. In a typical application, 2.8µA will be consumed from the supply when regulating with no load.

The oscillator reduces the LT3991's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the output current during start-up and overload.

The LT3991 contains a power good comparator which trips when the FB pin is at 91% of its regulated value. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. Power good is valid when the LT3991 is enabled and V_{IN} is above 4.3V.

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Achieving Ultralow Quiescent Current

To enhance efficiency at light loads, the LT3991 operates in low ripple Burst Mode, which keeps the output capacitor charged to the desired output voltage while minimizing the input quiescent current. In Burst Mode operation the LT3991 delivers single pulses of current to the output capacitor followed by sleep periods where the output power is supplied by the output capacitor. When in sleep mode the LT3991 consumes 1.7µA, but when it turns on all the circuitry to deliver a current pulse, the LT3991 consumes 1.5mA of input current in addition to the switch current. Therefore, the total quiescent current will be greater than 1.7µA when regulating.

As the output load decreases, the frequency of single current pulses decreases (see Figure 1) and the percentage of time the LT3991 is in sleep mode increases, resulting in much higher light load efficiency. By maximizing the time between pulses, the converter quiescent current gets closer to the 1.7µA ideal. Therefore, to optimize the quiescent current performance at light loads, the current in the feedback resistor divider and the reverse current in the catch diode must be minimized, as these appear to the output as load currents. Use the largest possible feedback resistors and a low leakage Schottky catch diode in applications utilizing the ultralow quiescent current

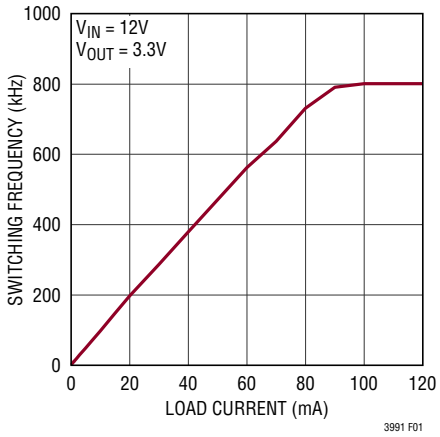

Figure 1. Switching Frequency in Burst Mode Operation

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performance of the LT3991. The feedback resistors should preferably be on the order of MΩ and the Schottky catch diode should have less than 1µA of typical reverse leakage at room temperature. These two considerations are reiterated in the FB Resistor Network and Catch Diode Selection sections.

It is important to note that another way to decrease the pulse frequency is to increase the magnitude of each single current pulse. However, this increases the output voltage ripple because each cycle delivers more power to the output capacitor. The magnitude of the current pulses was selected to ensure less than 15mV of output ripple in a typical application. See Figure 2.

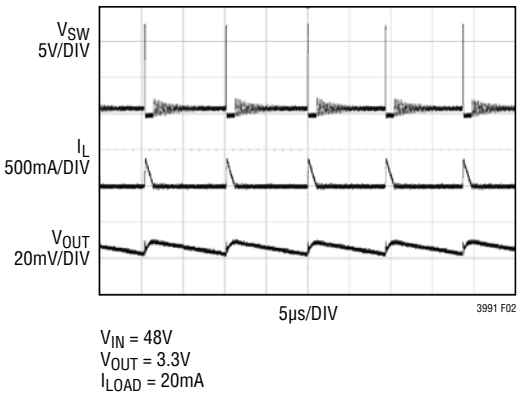

Figure 2. Burst Mode Operation

While in Burst Mode operation, the burst frequency and the charge delivered with each pulse will not change with output capacitance. Therefore, the output voltage ripple will be inversely proportional to the output capacitance. In a typical application with a 47µF output capacitor, the output ripple is about 8mV, and with a 100µF output capacitor the output ripple is about 4mV. The output voltage ripple can continue to be decreased by increasing the output capacitance.

At higher output loads (above 86mA for the front page application) the LT3991 will be running at the frequency programmed by the R_T resistor, and will be operating in standard PWM mode. The transition between PWM and low ripple Burst Mode operation will exhibit slight frequency jitter, but will not disturb the output voltage.

To ensure proper Burst Mode operation, the SYNC pin must be grounded. When synchronized with an external clock, the LT3991 will pulse skip at light loads. The quiescent current will significantly increase to 1.5mA in light load situations when synchronized with an external clock. Holding the SYNC pin high yields no advantages in terms of output ripple or minimum load to full frequency, so is not recommended.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{1.19V} - 1\right)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

The total resistance of the FB resistor divider should be selected to be as large as possible to enhance low current performance. The resistor divider generates a small load on the output, which should be minimized to optimize the low supply current at light loads.

When using large FB resistors, a 10pF phase lead capacitor should be connected from V_{OUT} to FB.

The LT3991-3.3 and LT3991-5 control an internal 10M FB resistor divider as well as an internal lead capacitor.

Setting the Switching Frequency

The LT3991 uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

Table 1. Switching Frequency vs R_T Value

SWITCHING FREQUENCY (MHz)	R_T VALUE (kΩ)
0.2	255
0.4	118
0.6	71.5
0.8	49.9
1.0	35.7
1.2	28.0
1.4	22.1
1.6	17.4
1.8	14.0
2.0	11.0

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Operating Frequency Tradeoffs

Selection of the operating frequency is a tradeoff between efficiency, component size, minimum dropout voltage, and maximum input voltage. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency, lower maximum input voltage, and higher dropout voltage. The highest acceptable switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_D}{t_{ON(MIN)}(V_{IN} - V_{SW} + V_D)}$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V), and V_{SW} is the internal switch drop (~0.5V at max load). This equation shows that slower switching frequency is necessary to safely accommodate high V_{IN}/V_{OUT} ratio. Also, as shown in the Input Voltage Range section, lower frequency allows a lower dropout voltage. The input voltage range depends on the switching frequency because the LT3991 switch has finite minimum on and off times. The minimum switch on and off times are strong functions of temperature. Use the typical minimum on and off curves to design for an application's maximum temperature, while adding about 30% for part-to-part variation. The minimum and maximum duty cycles that can be achieved taking minimum on and off times into account are:

$$DC_{MIN} = f_{SW}\, t_{ON(MIN)}$$

$$DC_{MAX} = 1 - f_{SW}\, t_{OFF(MIN)}$$

where f_{SW} is the switching frequency, the $t_{ON(MIN)}$ is the minimum switch on-time, and the $t_{OFF(MIN)}$ is the minimum switch off-time. These equations show that duty cycle range increases when switching frequency is decreased. See the Electrical Characteristics section for $t_{ON(MIN)}$ and $t_{OFF(MIN)}$ values.

A good choice of switching frequency should allow adequate input voltage range (see Input Voltage Range section) and keep the inductor and capacitor values small.

Input Voltage Range

The minimum input voltage is determined by either the LT3991's minimum operating voltage of 4.3V or by its maximum duty cycle (see equation in Operating Frequency Tradeoffs section). The minimum input voltage due to duty cycle is:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_D}{1 - f_{SW}\, t_{OFF(MIN)}} - V_D + V_{SW}$$

where $V_{IN(MIN)}$ is the minimum input voltage, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V), V_{SW} is the internal switch drop (~0.5V at max load), f_{SW} is the switching frequency (set by R_T), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage. If a lower dropout voltage is desired, a lower switching frequency should be used.

The maximum input voltage for LT3991 applications depends on switching frequency, the Absolute Maximum Ratings of the V_{IN} and BOOST pins, and the operating mode. For a given application where the switching frequency and the output voltage are already selected, the maximum input voltage ($V_{IN(OP-MAX)}$) that guarantees optimum output voltage ripple for that application can be found by applying the following equation:

$$V_{IN(OP-MAX)} = \frac{V_{OUT} + V_D}{f_{SW} \bullet t_{ON(MIN)}} - V_D + V_{SW}$$

where $t_{ON(MIN)}$ is the minimum switch on-time. Note that a higher switching frequency will decrease the maximum operating input voltage. Conversely, a lower switching frequency will be necessary to achieve normal operation at higher input voltages.

The circuit will tolerate inputs above the maximum operating input voltage and up to the Absolute Maximum Ratings of the V_{IN} and BOOST pins, regardless of chosen switching frequency. However, during such transients where V_{IN} is higher than $V_{IN(OP-MAX)}$, the LT3991 will enter pulse-skipping operation where some switching pulses are skipped to maintain output regulation. The output voltage ripple and inductor current ripple will be higher than in typical operation. Do not overload when V_{IN} is greater than $V_{IN(OP-MAX)}$.

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Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = \frac{V_{OUT} + V_D}{f_{SW}}$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, V_D is the catch diode drop (~0.5V) and L is the inductor value in µH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start-up or short-circuit) and high input voltage (>30V), the saturation current should be above 2.8A. To keep the efficiency high, the series resistance (DCR) should be less than 0.1Ω, and the core material should be intended for high frequency applications. Table 2 lists several vendors and suitable types.

The inductor value must be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2}$$

The LT3991 limits its peak switch current in order to protect itself and the system from overload faults. The LT3991's switch current limit (I_{LIM}) is at least 2.33A at low duty cycles and decreases linearly to 1.8A at DC = 0.8.

Table 2. Inductor Vendors

VENDOR	URL	PART SERIES	TYPE
Murata	www.murata.com	LQH55D	Open
TDK	www.componenttdk.com	SLF7045 SLF10145	Shielded Shielded
Toko	www.toko.com	D62CB D63CB D73C D75F	Shielded Shielded Shielded Open
Coilcraft	www.coilcraft.com	MSS7341 MSS1038	Shielded Shielded
Sumida	www.sumida.com	CR54 CDRH74 CDRH6D38 CR75	Open Shielded Shielded Open

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = \frac{(1-DC) \bullet (V_{OUT} + V_D)}{L \bullet f_{SW}}$$

where f_{SW} is the switching frequency of the LT3991, DC is the duty cycle and L is the value of the inductor. Therefore, the maximum output current that the LT3991 will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. If your load is lower than the maximum load current, than you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that if the inductance differs from the simple rule above, then the maximum load current will depend on the input voltage. In addition, low inductance may result in discontinuous mode operation, which further reduces maximum load current. For details of maximum output current and discontinuous operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN}>0.5$), a minimum inductance is required to avoid sub-harmonic oscillations. See Application Note 19.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use the equations above to check that the LT3991 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

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Input Capacitor

Bypass the input of the LT3991 circuit with a ceramic capacitor of X7R or X5R type. Y5V types have poor performance over temperature and applied voltage, and should not be used. A 4.7µF to 10µF ceramic capacitor is adequate to bypass the LT3991 and will easily handle the ripple current. Note that larger input capacitance is required when a lower switching frequency is used (due to longer on-times). If the input power source has high impedance, or there is significant inductance due to long wires or cables, additional bulk capacitance may be necessary. This can be provided with a low performance electrolytic capacitor.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT3991 and to force this very high frequency switching current into a tight local loop, minimizing EMI. A 4.7µF capacitor is capable of this task, but only if it is placed close to the LT3991 (see the PCB Layout section). A second precaution regarding the ceramic input capacitor concerns the maximum input voltage rating of the LT3991. A ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3991 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3991's voltage rating. This situation is easily avoided (see the Hot Plugging Safely section).

Output Capacitor and Output Ripple

The output capacitor has two essential functions. Along with the inductor, it filters the square wave generated by the LT3991 to produce the DC output. In this role it determines the output ripple, so low impedance (at the switching frequency) is important. The second function is to store energy in order to satisfy transient loads and stabilize the LT3991's control loop. Ceramic capacitors have very low equivalent series resistance (ESR) and provide the best ripple performance. A good starting value is:

$$C_{OUT} = \frac{100}{V_{OUT} f_{SW}}$$

where f_{SW} is in MHz, and C_{OUT} is the recommended output capacitance in µF. Use X5R or X7R types. This choice will provide low output ripple and good transient response. Transient performance can be improved with a higher value capacitor. Increasing the output capacitance will also decrease the output voltage ripple. A lower value of output capacitor can be used to save space and cost but transient performance will suffer.

When choosing a capacitor, look carefully through the data sheet to find out what the actual capacitance is under operating conditions (applied voltage and temperature). A physically larger capacitor or one with a higher voltage rating may be required. Table 3 lists several capacitor vendors.

Table 3. Recommended Ceramic Capacitor Vendors

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Catch Diode Selection

The catch diode (D1 from Block Diagram) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output load current. The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current. Peak reverse voltage is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage.

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Table 4. Schottky Diodes. The Reverse Current Values Listed Are Estimates Based Off of Typical Curves for Reverse Current vs Reverse Voltage at 25°C.

PART NUMBER	V_R (V)	I_{AVE} (A)	V_F at 1A (mV)	V_F at 2A (mV)	I_R at V_R = 20V 25°C (µA)
On Semiconductor					
MBR0520L	20	0.5			30
MBR0540	40	0.5	620		0.4
MBRM120E	20	1	530	595	0.5
MBRM140	40	1	550		20
Diodes Inc.					
B0530W	30	0.5			15
B0540W	40	0.5	620		1
B120	20	1	500		1.1
B130	30	1	500		1.1
B140	40	1	500		1.1
B150	50	1	700		0.4
B220	20	2		500	20
B230	30	2		500	0.6
B140HB	40	1			1
DFLS240L	40	2		500	4
DFLS140	40	1.1	510		1
DFLS160	60	1	500		2.5
DFLS2100	100	2	770	860	0.01
B240	40	2		500	0.45
Central Semiconductor					
CMSH1 - 40M	40	1	500		
CMSH1 - 60M	60	1	700		
CMSH1 - 40ML	40	1	400		
CMSH2 - 40M	40	2		550	
CMSH2 - 60M	60	2		700	
CMSH2 - 40L	40	2		400	
CMSH2 - 40	40	2		500	
CMSH2 - 60M	60	2		700	

An additional consideration is reverse leakage current. When the catch diode is reversed biased, any leakage current will appear as load current. When operating under light load conditions, the low supply current consumed by the LT3991 will be optimized by using a catch diode with minimum reverse leakage current. Low leakage Schottky diodes often have larger forward voltage drops at a given current, so a trade-off can exist between low load and high load efficiency. Often Schottky diodes with larger reverse bias ratings will have less leakage at a given output voltage than a diode with a smaller reverse bias rating. Therefore, superior leakage performance can be achieved at the expense of diode size. Table 4 lists several Schottky diodes and their manufacturers.

Ceramic Capacitors

Ceramic capacitors are small, robust and have very low ESR. However, ceramic capacitors can cause problems when used with the LT3991 due to their piezoelectric nature. When in Burst Mode operation, the LT3991's switching frequency depends on the load current, and at very light loads the LT3991 can excite the ceramic capacitor at audio frequencies, generating audible noise. Since the LT3991 operates at a lower current limit during Burst Mode operation, the noise is typically very quiet to a casual ear. If this is unacceptable, use a high performance tantalum or electrolytic capacitor at the output.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LT3991. As previously mentioned, a ceramic input capacitor combined with trace or cable inductance forms a high quality (under damped) tank circuit. If the LT3991 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the LT3991's rating. This situation is easily avoided (see the Hot Plugging Safely section).

BOOST and BD Pin Considerations

Capacitor C3 and the internal boost Schottky diode (see the Block Diagram) are used to generate a boost voltage that is higher than the input voltage. In most cases a 0.47µF capacitor will work well. Figure 3 shows three ways to arrange the boost circuit. The BOOST pin must be more than 2.3V above the SW pin for best efficiency. For outputs of 3V and above, the standard circuit (Figure 3a) is best. For outputs between 2.8V and 3V, use a 1µF boost capacitor. A 2.5V output presents a special case because it is marginally adequate to support the boosted drive stage

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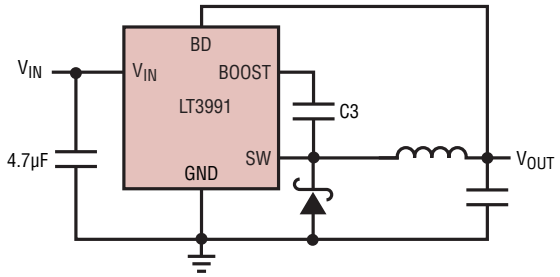
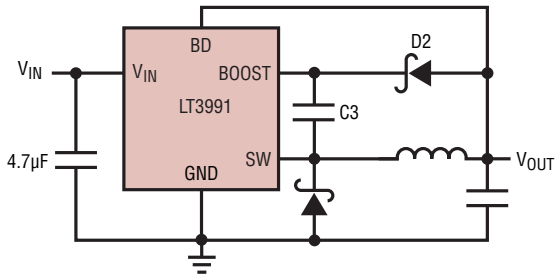
while using the internal boost diode. For reliable BOOST pin operation with 2.5V outputs use a good external Schottky diode (such as the ON Semi MBR0540), and a 1µF boost capacitor (Figure 3b). For output voltages below 2.5V, the boost diode can be tied to the input (Figure 3c), or to another external supply greater than 2.8V. However, the circuit in Figure 3a is more efficient because the BOOST pin current comes from a lower voltage source. You must also be sure that the maximum voltage ratings of the BOOST and BD pins are not exceeded.

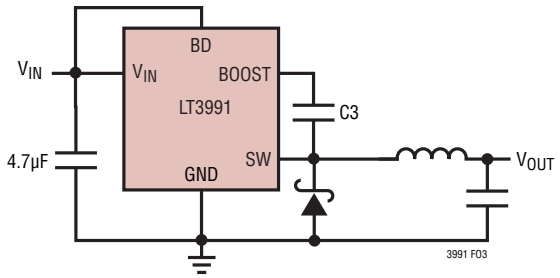
The minimum operating voltage of an LT3991 application is limited by the minimum input voltage (4.3V) and by the maximum duty cycle as outlined in the Input Voltage Range section. For proper start-up, the minimum input voltage is also limited by the boost circuit. If the input voltage is ramped slowly, the boost capacitor may not be fully charged. Because the boost capacitor is charged with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages, and on the arrangement of the boost circuit. The minimum load generally goes to zero once the circuit has started. Figure 4 shows a plot of minimum load to start and to run as a function of input voltage. In many cases the discharged output capacitor will present a load to the switcher, which will allow it to start. The plots show the worst-case situation where V_{IN} is ramping very slowly. For lower start-up voltage, the boost diode can be tied to V_{IN}; however, this restricts the input range to one-half of the absolute maximum rating of the BOOST pin.



(3a) For V_{OUT} > 2.8V

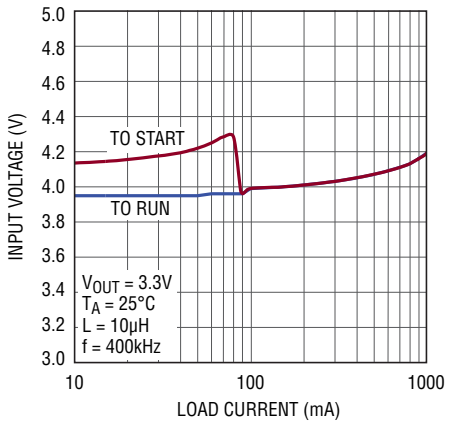


(3b) For 2.5V < V_{OUT} < 2.8V



(3c) For V_{OUT} < 2.5V; $V_{IN(MAX)}$ = 27V

Figure 3. Three Circuits for Generating the Boost Voltage



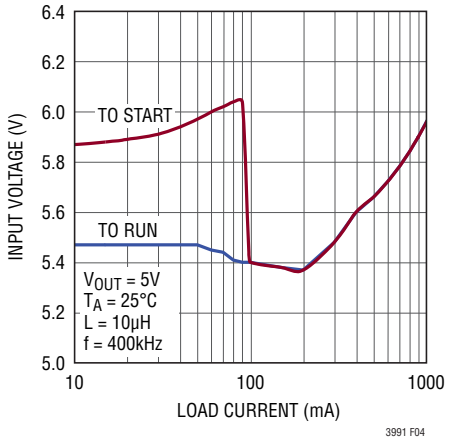


Figure 4. The Minimum Input Voltage Depends on Output Voltage, Load Current and Boost Circuit

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At light loads, the inductor current becomes discontinuous and this reduces the minimum input voltage to approximately 400mV above V_{OUT}. At higher load currents, the inductor current is continuous and the duty cycle is limited by the maximum duty cycle of the LT3991, requiring a higher input voltage to maintain regulation.

Enable Pin

The LT3991 is in shutdown when the EN pin is low and active when the pin is high. The rising threshold of the EN comparator is 1.01V, with 30mV of hysteresis. The EN pin can be tied to V_{IN} if the shutdown feature is not used.

Adding a resistor divider from V_{IN} to EN programs the LT3991 to regulate the output only when V_{IN} is above a desired voltage (see Figure 5). Typically, this threshold, $V_{IN(EN)}$, is used in situations where the input supply is current limited, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \frac{R3}{R4} + 1$$

where output regulation should not start until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, regulation will not stop until the input falls slightly below $V_{IN(EN)}$.

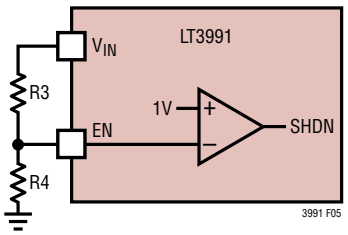
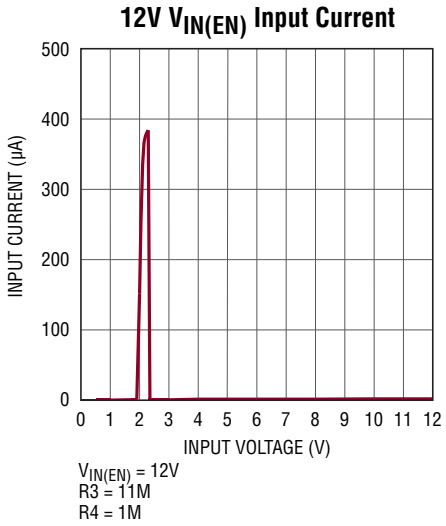


Figure 5. Programmed Enable Threshold

Be aware that when the input voltage is below 4.3V, the input current may rise to several hundred µA. And the part may be able to switch at cold or for $V_{IN(EN)}$ thresholds less than 7V. Figure 6 shows the magnitude of the increased input current in a typical application with different programmed $V_{IN(EN)}$.

When operating in Burst Mode for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT3991. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.



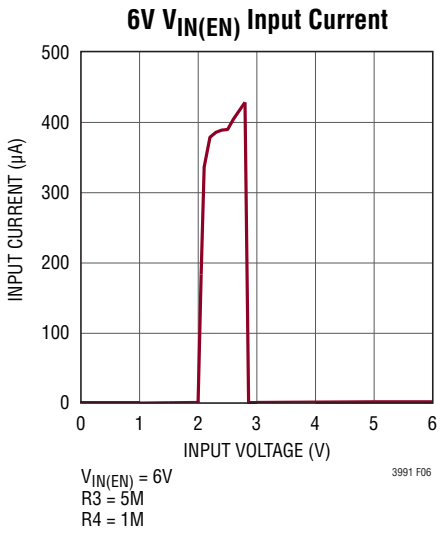


Figure 6. Input Current vs Input Voltage for a Programmed $V_{IN(EN)}$ of 6V and 12V

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Soft-Start

The SS pin can be used to soft-start the LT3991 by throttling the maximum input current during start-up. An internal 1µA current source charges an external capacitor generating a voltage ramp on the SS pin. The SS pin clamps the internal V_C node, which slowly ramps up the current limit. Maximum current limit is reached when the SS pin is about 1.5V or higher. By selecting a large enough capacitor, the output can reach regulation without overshoot. A 100k resistor in series with the soft-start capacitor is recommended. Figure 7 shows start-up waveforms for a typical application with a 10nF capacitor and a 100k resistor on SS for a 3.3Ω load when the EN pin is pulsed high for 10ms.

The external SS capacitor is only actively discharged when EN is low. With EN low, the external SS cap is discharged through approximately 150Ω. The EN pin needs to be low long enough for the external cap to completely discharge through the 150Ω pull-down and external series resistor prior to start-up.

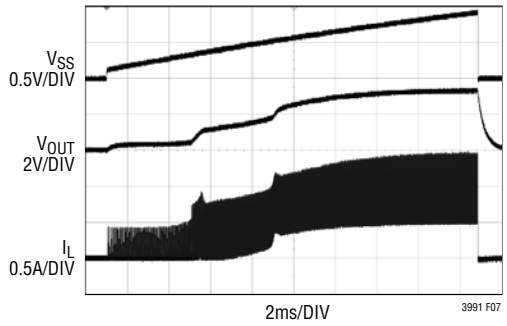

Figure 7. Soft-Start Waveforms for Front-Page Application with 10nF Capacitor and 100k Series Resistor on SS. EN is Pulsed High for About 10ms with a 3.3Ω Load Resistor

Synchronization

To select low ripple Burst Mode operation, tie the SYNC pin below 0.6V (this can be ground or a logic low output).

Synchronizing the LT3991 oscillator to an external frequency can be done by connecting a square wave (with 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys that are below 0.6V and peaks above 1.0V (up to 6V).

The LT3991 will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse skip to maintain regulation.

The LT3991 may be synchronized over a 250kHz to 2MHz range. The R_T resistor should be chosen to set the LT3991 switching frequency 20% below the lowest synchronization input. For example, if the synchronization signal will be 250kHz and higher, the R_T should be selected for 200kHz. To assure reliable and safe operation the LT3991 will only synchronize when the output voltage is near regulation as indicated by the PG flag. It is therefore necessary to choose a large enough inductor value to supply the required output current at the frequency set by the R_T resistor (see the Inductor Selection section). The slope compensation is set by the R_T value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by R_T, than the slope compensation will be sufficient for all synchronization frequencies.

Shorted and Reversed Input Protection

If the inductor is chosen so that it won't saturate excessively, an LT3991 buck regulator will tolerate a shorted output. There is another situation to consider in systems where the output will be held high when the input to the LT3991 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with the LT3991's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT3991's internal circuitry will pull its quiescent current through its SW pin. This is fine if your system can tolerate a few µA in this state. If you ground the EN pin, the SW pin current will drop to essentially zero. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic diodes inside the LT3991 can pull current from the output through the SW pin and the V_{IN} pin. Figure 8 shows a circuit that will run only when the input voltage is present and that protects against a shorted or reversed input.

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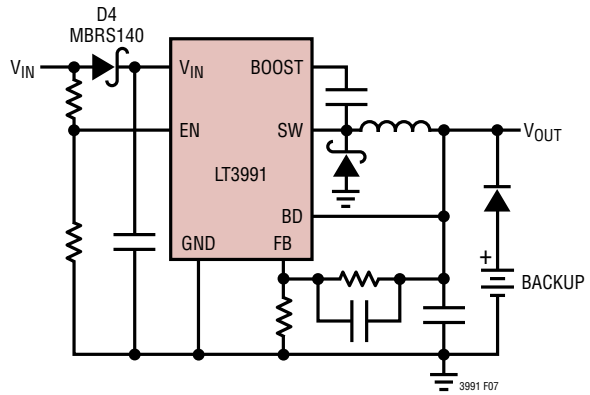

Figure 8. Diode D4 Prevents a Shorted Input from Discharging a Backup Battery Tied to the Output. It Also Protects the Circuit from a Reversed Input. The LT3991 Runs Only When the Input is Present

PCB Layout

For proper operation and minimum EMI, care must be taken during printed circuit board layout. Figure 9 shows the recommended component placement with trace, ground plane and via locations. Note that large, switched currents flow in the LT3991's V_{IN} and SW pins, the catch diode (D1), and the input capacitor (C1). The loop formed by these components should be as small as possible. These components, along with the inductor and output capacitor, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane below these components. The SW and BOOST nodes should be as small as possible. Finally, keep the FB and R_T nodes small so that the ground traces will shield them from the SW and BOOST nodes. The Exposed Pad on the bottom of the package must be soldered to ground so that the pad acts as a heat sink. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the LT3991 to additional ground planes within the circuit board and on the bottom side.

Hot Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LT3991 circuits. However, these capacitors can cause problems if the LT3991 is plugged into a live supply. The low loss ceramic capacitor, combined with stray inductance in series with the power source, forms an under damped tank circuit, and the voltage at

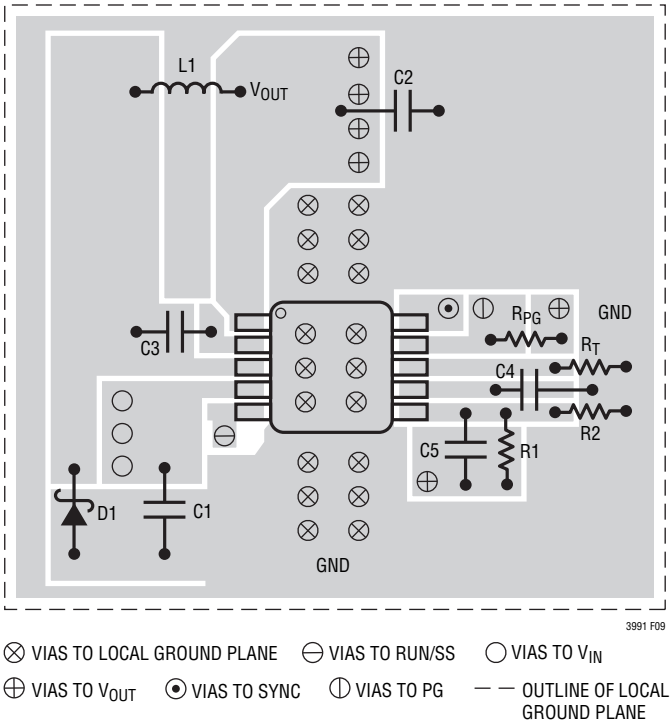

Figure 9. A Good PCB Layout Ensures Proper, Low EMI Operation

the V_{IN} pin of the LT3991 can ring to twice the nominal input voltage, possibly exceeding the LT3991's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LT3991 into an energized supply, the input network should be designed to prevent this overshoot. See Linear Technology Application Note 88 for a complete discussion.

High Temperature Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT3991. The Exposed Pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT3991. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating.

Power dissipation within the LT3991 can be estimated by calculating the total power loss from an efficiency measurement and subtracting the catch diode loss and inductor

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loss. The die temperature is calculated by multiplying the LT3991 power dissipation by the thermal resistance from junction to ambient.

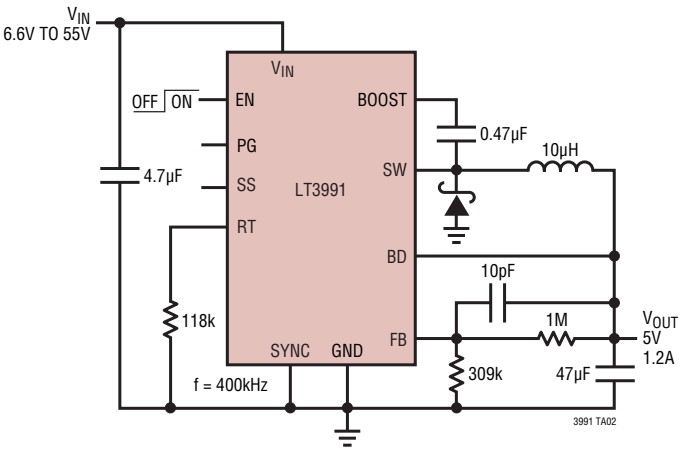
Also keep in mind that the leakage current of the power Schottky diode goes up exponentially with junction temperature. When the power switch is closed, the power Schottky diode is in parallel with the power converter's output filter stage. As a result, an increase in a diode's leakage current results in an effective increase in the load, and a corresponding increase in input power. Therefore, the catch Schottky diode must be selected with care to avoid excessive increase in light load supply current at high temperatures.

Other Linear Technology Publications

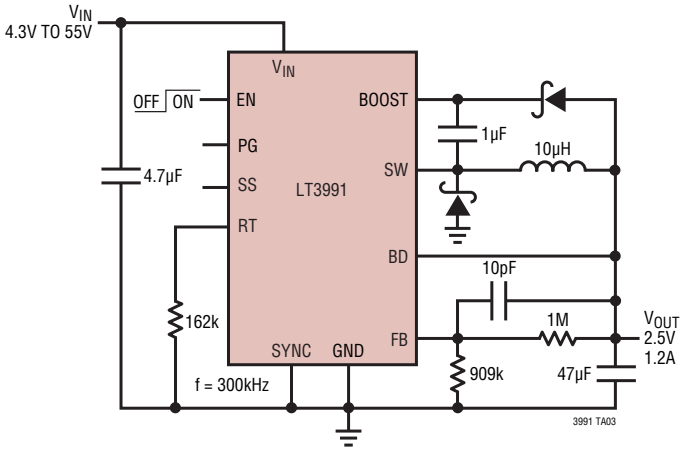
Application Notes 19, 35 and 44 contain more detailed descriptions and design information for buck regulators and other switching regulators. The LT1376 data sheet has a more extensive discussion of output ripple, loop compensation and stability testing. Design Note 318 shows how to generate a bipolar output supply using a buck regulator.

TYPICAL APPLICATIONS

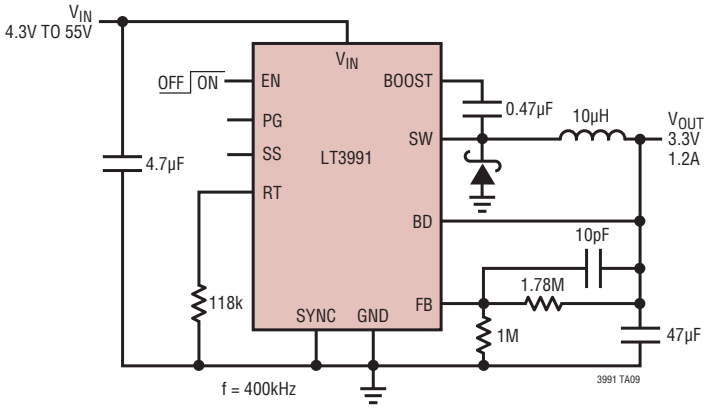
5V Step-Down Converter



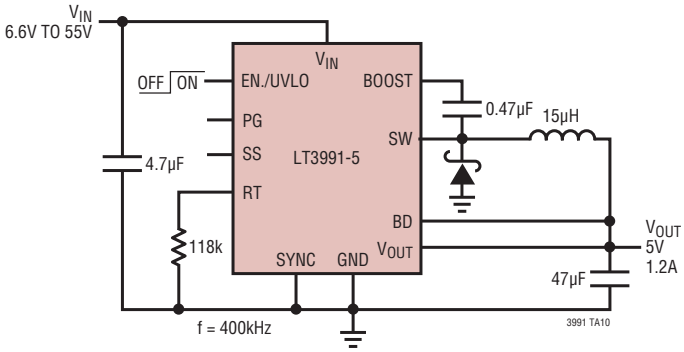
2.5V Step-Down Converter



3.3V Step-Down Converter



5V Step-Down Converter



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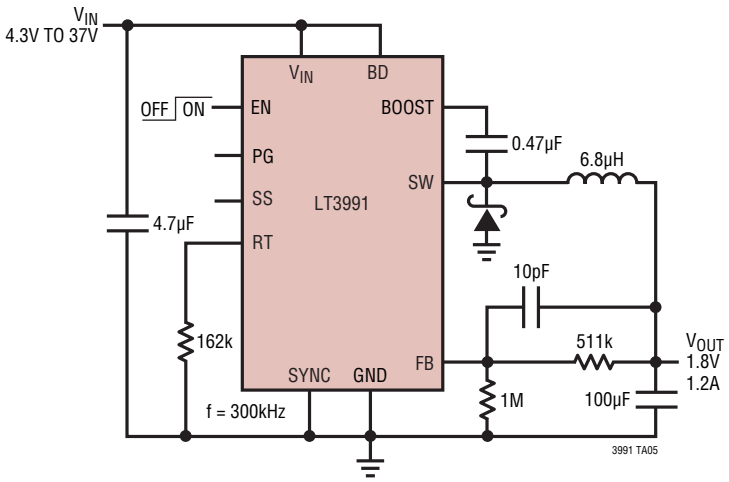
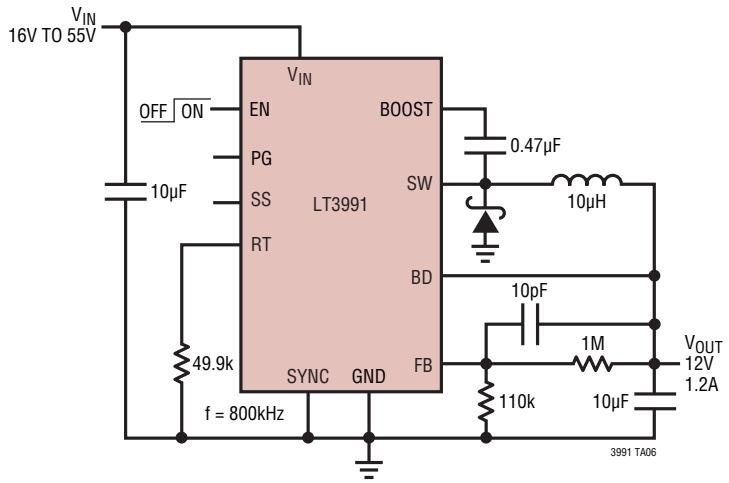
TYPICAL APPLICATIONS

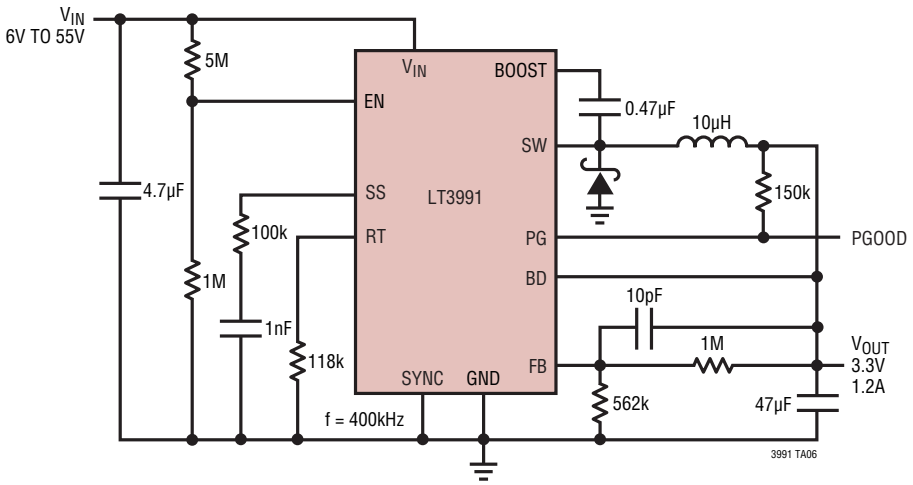
1.8V Step-Down Converter



12V Step-Down Converter



3.3V Step-Down Converter with Undervoltage Lockout, Soft-Start, and Power Good



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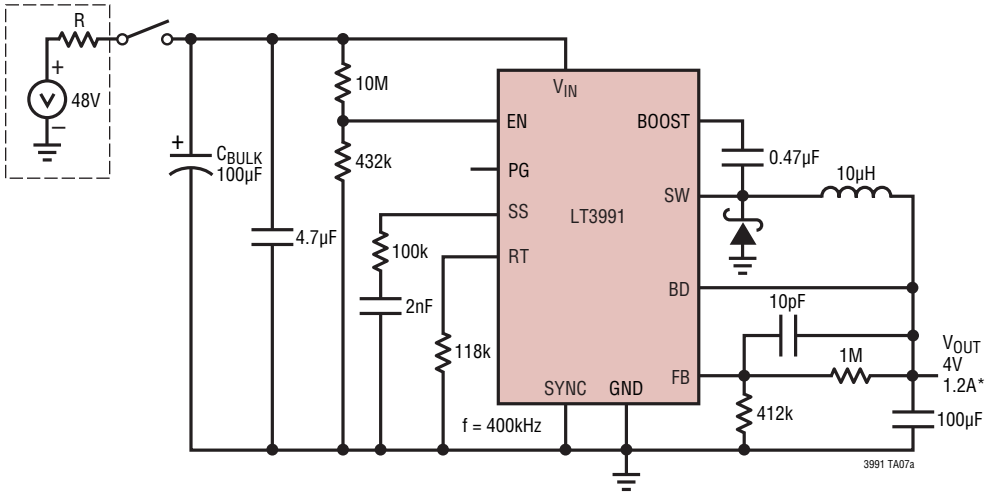
TYPICAL APPLICATIONS

4V Step-Down Converter with a High Impedance Input Source

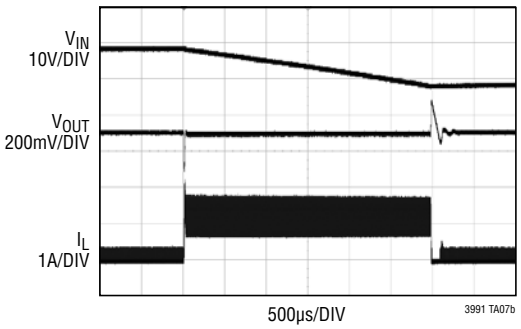


* AVERAGE OUTPUT POWER CANNOT EXCEED THAT WHICH CAN BE PROVIDED BY HIGH IMPEDANCE SOURCE. NAMELY,

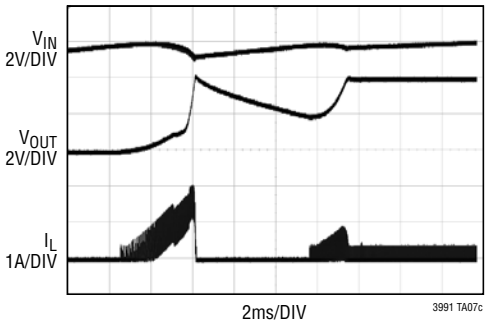
$$P_{OUT(MAX)} = \frac{V^2}{4R} \bullet \eta$$

WHERE V IS VOLTAGE OF SOURCE, R IS INTERNAL SOURCE IMPEDANCE, AND η IS LT3971 EFFICIENCY. MAXIMUM OUTPUT CURRENT OF 1.2A CAN BE SUPPLIED FOR A SHORT TIME BASED ON THE ENERGY WHICH CAN BE SOURCED BY THE BULK INPUT CAPACITANCE.

Sourcing a Maximum Load Pulse



Start-Up from High Impedance Input Source



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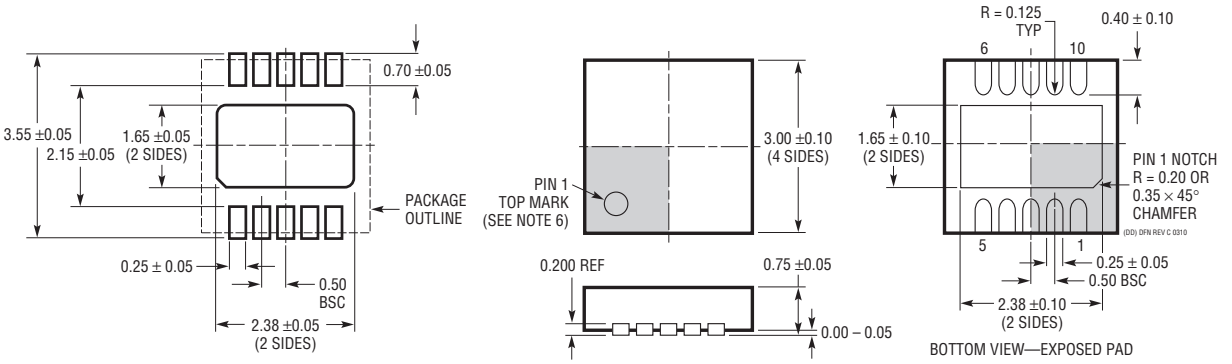
PACKAGE DESCRIPTION

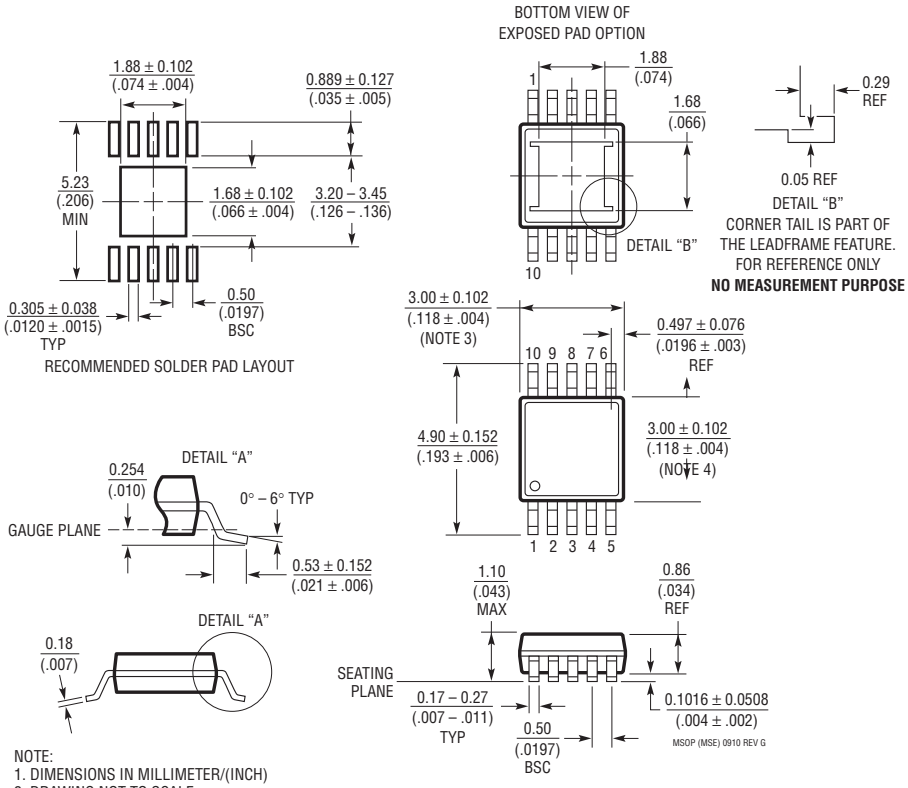
DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev G)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

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REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	01/11	Added 3.3V and 5V fixed voltage options reflected throughout the data sheet.	1-24

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

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RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT3970	40V, 350mA, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 4.2V to 40V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} <1 µA, 3mm × 2mm DFN-10, MSOP-10 Packages
LT3990	62V, 350mA, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.5µA	V_{IN} = 4.2V to 62V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.5µA, I_{SD} <1 µA, 3mm × 2mm DFN-10, MSOP-10 Packages
LT3971	38V, 1.2A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with I_Q = 2.8µA	V_{IN} = 4.3V to 38V, $V_{OUT(MIN)}$ = 1.21V, I_Q = 2.8µA, I_{SD} <1 µA, 3mm × 3mm DFN-10, MSOP-10E Packages
LT3682	36V, 60V Max, 1A, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter	V_{IN} = 3.6V to 36V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1 µA, 3mm × 3mm DFN-12 Package
LT3689	36V, 60V Transient Protection, 800mA, 2.2MHz High Efficiency Micropower Step-Down DC/DC Converter with POR Reset and Watchdog Timer	V_{IN} = 3.6V to 36V (Transient to 60V), $V_{OUT(MIN)}$ = 0.8V, I_Q = 75µA, I_{SD} <1 µA, 3mm × 3mm QFN-16 Package
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 36V (Transient to 60V), $V_{OUT(MIN)}$ = 0.78V, I_Q = 70µA, I_{SD} <1 µA, 3mm × 3mm DFN-10, MSOP-10E Packages
LT3980	58V with Transient Protection to 80V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN} = 3.6V to 58V (Transient to 60V), $V_{OUT(MIN)}$ = 0.78V, I_Q = 85µA, I_{SD} <1 µA, 3mm × 4mm DFN-16, MSOP-16E Packages

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