

Revision History

Below are the changes from the September 2007 version to the June 2011 version.

Page	Item	Description
1	Ordering Information	Obsoleted Le57D111DJC package.

Table of Contents

1.0 Product Description	5
2.0 Block Descriptions	5
2.1 Two-Wire Interface	5
2.2 Signal Transmission	5
2.3 Power Feed Controller and Common Bias	5
2.4 Input Decoder and Control	5
2.5 Off-Hook Detector	5
2.6 Ring-Trip Detector	5
3.0 Connection Diagrams	6
4.0 Pin Descriptions	7
5.0 Electrical Characteristics	9
5.1 Absolute Maximum Ratings	9
5.2 Operating Ranges	10
6.0 Specifications	11
6.1 Transmission Performance	11
6.2 Crosstalk Between Channels	11
6.3 Longitudinal Capability	11
6.4 Insertion Loss	12
6.5 Line Characteristics	13
6.6 Power Supply Rejection Ratio at the Two-Wire Interface, Active Normal State	13
6.7 Power Dissipation	13
6.8 Supply Currents	13
6.9 RFI Rejection	14
6.10 Logic Inputs	14
6.11 Logic Output	14
6.12 Ring-Trip Detector Input	14
6.13 Loop Detector	15
6.14 SLIC Device Decoding	15
6.15 User-Programmable Components	16
6.16 DC Feed Characteristics	17
6.17 Test Circuits	18
7.0 Application Circuit	21
8.0 Line card Parts List	22
9.0 Physical Dimensions	23
9.1 44-Pin eTQFP	23

List of Figures

Figure 1 - Block Diagram	1
Figure 2 - Feed Programming	18
Figure 3 - Two-to-Four Wire Insertion Loss	18
Figure 4 - Four-to-Two Wire Insertion Loss and Balance Return Signals	18
Figure 5 - Longitudinal Balance	19
Figure 6 - Two-Wire Return Loss Test Circuit	19
Figure 7 - RFI Test Circuit	19
Figure 8 - Le5711 Test Circuit	20

1.0 Product Description

The Le5711 device is designed for long loop high-density POTS applications requiring a low power, small footprint SLIC. The Le5711 device increases linecard density by integrating two SLIC devices into a single 32 pin package. This reduction in board space allows for higher density linecard, which allows for amortizing common hardware across more channels. The Le5711 device gives linecard designers a simple control interface that supports four states: Active, Reverse Polarity, Standby, and Disconnect (Ringing). The Le5711 device is low cost and high performance, providing key features required for POTS markets requiring only loop start. The device includes a thermal management resistor for reducing power dissipation.

2.0 Block Descriptions

2.1 Two-Wire Interface

The two-wire interfaces provide DC current and send voice signals to a telephone apparatus connected to the linecard with a two-wire line. The two-wire interface also receives the returning voice signals from the telephone transmitter.

2.2 Signal Transmission

The RSN input current controls the receive current sent to the two-wire interface. The AC line voltage is sensed by a differential amplifier between the A_i (TIP) and HP_i leads.* The output of this amplifier is equal to the AC metallic components of the line voltages and is output at VTX_i . The transmission circuit also contains a longitudinal feedback circuit to shunt longitudinal signals to a DC bias voltage. The longitudinal feedback does not affect metallic signals.

***Note:**

"i" denotes channel number

2.3 Power Feed Controller and Common Bias

The power feed controllers have three sections: (1) the battery feed circuit, (2) the reverse polarity circuit, and (3) the common bias circuit. The battery feed circuit regulates the amount of DC current and voltage supplied to the telephone over a wide range of loop resistance. The reverse polarity circuit provides the capability to reverse the loop current for pay telephone key pad disable and other applications. The bias circuit provides a filtered reference voltage, which is offset from the subscriber line voltage, and a signal which sets the current limit.

2.4 Input Decoder and Control

The input decoder and control block provides a means for a microprocessor or SLAC IC to control such system states as Active, Standby, Disconnect (Ringing), and Reverse Polarity. The input decoder and control block has TTL-compatible inputs, which set the operating states of the SLIC device. It also provides the supervision signal sent back to the controller.

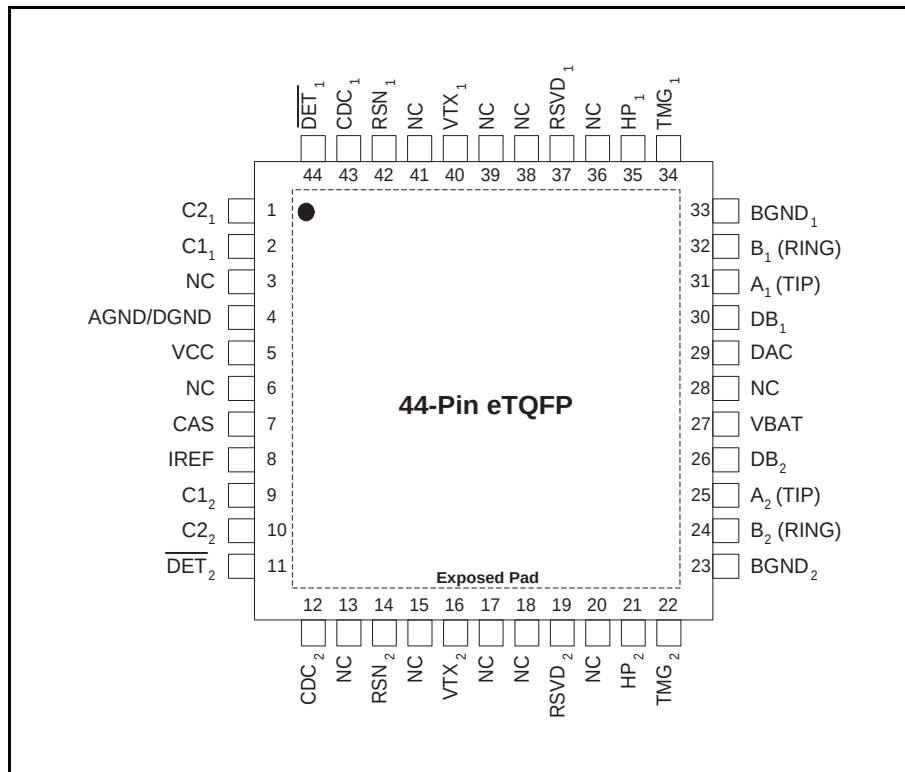
2.5 Off-Hook Detector

The most important loop monitoring function is off-hook detection. Loop current is programmed for both channels by a single resistor. Loop detect threshold is typically 1/3 of the programmed Loop current in the Active and Reverse Polarity states.

2.6 Ring-Trip Detector

In the Disconnect state, the ring-trip detector is active. While the DB_i pin is more negative than the DAC pin, the DET pin will be high to indicate on hook. When an off hook condition occurs, the DB_i pin becomes more positive than the DAC pin, and the DET pin will go low to indicate off hook during ringing (ring-trip) has been detected. The system implements the Ringing state using external control of a ring relay in combination with the Disconnect SLIC state, which enables the ring-trip detector.

3.0 Connection Diagrams



Note:

1. Pin 1 is marked for orientation.
2. NC = No Connect
3. The exposed heat sink pad on the bottom of the eTQFP package is connected to the battery supply (VBAT pin). Do not connect to GND.

4.0 Pin Descriptions

Pin Name	Type	Description
A ₁ (TIP)	Output	Output of A (TIP) power amplifier of channel 1.
A ₂ (TIP)	Output	Output of A (TIP) power amplifier of channel 2.
AGND/DGND	Ground	Analog and digital ground.
B ₁ (RING)	Output	Output of B (RING) power amplifier of channel 1.
B ₂ (RING)	Output	Output of B (RING) power amplifier of channel 2.
BGND ₁	Ground	Battery (power) ground of channel 1
BGND ₂	Ground	Battery (power) ground of channel 2.
C1 ₁	Input	State decoder inputs of channel 1.
C2 ₁	Input	
C1 ₂	Input	State decoder inputs of channel 2.
C2 ₂	Input	
CAS	Capacitor	Pin for capacitor to filter reference voltage when operating in anti-saturation region.
CDC ₁	Capacitor	DC feed filter capacitor of channel 1.
CDC ₂	Capacitor	DC feed filter capacitor of channel 2.
RSVD ₁	Input	Reserved. Connect to V _{CC} .
RSVD ₂	Input	Reserved. Connect to V _{CC} .
DAC	Input	Ring-trip negative of both channels. Negative input to ring-trip comparator.
DB ₁	Input	Ring-trip positive of channel 1. Positive input to ring-trip comparator.
DB ₂	Input	Ring-trip positive of channel 2. Positive input to ring-trip comparator.
DET ₁	Output	Switch-hook/Ring-trip detector output of channel1. Logic low indicates that a detector is tripped.
DET ₂	Output	Switch-hook/Ring-trip detector output of channel 2. Logic low indicates that a detector is tripped.
HP ₁	Capacitor	Connect High-pass filter capacitor from HP ₁ to B ₁ (RING).
HP ₂	Capacitor	Connect High-pass filter capacitor from HP ₂ to B ₂ (RING).
IREF	Resistor	Connection for reference resistor that programs loop detector threshold and DC feed current of both channels.
NC	—	No Connect. This pin is not internally connected.
RSN ₁	Input	Receive Summing Node of channel 1. In the Active and Polarity Reversed states, the current (both AC and DC) between A ₁ (TIP) and B ₁ (RING) is equal to 500 times the current into this pin. The networks that program receive gain and two-wire impedance of channel 1 connect to this node.

Pin Name	Type	Description
RSN ₂	Input	Receive Summing Node of channel 2. In the Active and Polarity Reversed states, the current (both AC and DC) between A ₂ (TIP) and B ₂ (RING) is equal to 500 times the current into this pin. The networks that program receive gain and two-wire impedance of channel 2 connect to this node.
TMG ₁	Output	Thermal management of channel 1. External resistor connects from TMG ₁ to VBAT to offload power from the SLIC device.
TMG ₂	Output	Thermal management of channel 2. External resistor connects from TMG ₂ to VBAT to offload power from the SLIC device.
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VTX ₁	Output	Transmit audio signal of channel 1. This output is a scaled version of the A and B metallic voltage. VTX also sources the two-wire input impedance programming network.
VTX ₂	Output	Transmit audio signal of channel 2. This output is a scaled version of the A and B metallic voltage. VTX ₂ also sources the two-wire input impedance programming network.
Exposed Pad	Battery	The exposed thermal management pad must be in thermal contact with an exposed copper plate with an electrical potential of battery supply (VBAT pin).

5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Storage temperature	–55 to +150° C
V _{CC} with respect to AGND	–0.4 to +7.0 V
V _{BAT} with respect to AGND	+0.4 to –61V
BGND ₁ , BGND ₂ with respect to AGND	+3 to –3 V
A ₁ (TIP), A ₂ (TIP), B ₁ (RING), B ₂ (RING) with respect to BGND: Continuous 10 ms (F = 0.1 Hz) 1 μs (F = 0.1 Hz) 250 ns (F = 0.1 Hz)	V _{BAT} to + 1 V –70 to +5 V –80 to +8 V –90 to +12 V
Current from A ₁ (TIP), A ₂ (TIP), B ₁ (RING), B ₂ (RING)	±150 mA
DB ₁ , DB ₂ , and DAC inputs: Voltage on ring-trip inputs	V _{BAT} to 0 V
Current into ring-trip inputs	±10 mA
C1 ₁ , C2 ₁ , C1 ₂ , C2 ₂ Input Voltage	–0.4 to V _{CC} + 0.4 V
Maximum power dissipation, continuous: T _A = 70° C, No heat sink In 44-pin eTQFP	(see note 1)
Thermal Data (Junction to Ambient): In 44-pin eTQFP package	θ _{JA} (see note 2)
Thermal Data (Junction to Case): In 44-pin eTQFP package	θ _{JC} (see note 2)
ESD Immunity (Human Body Model)	JESD22 Class 1C compliant

Notes:

1. Thermal limiting circuitry on the chip will shut down the circuit at a junction temperature of about 165°C. Continuous operation above 145°C junction temperature may degrade device reliability.
2. The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Refer to the Thermal Management for the Le5711 and Le5712 Dual SLIC Devices Application Note for details.

Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 245°C during printed circuit board assembly.

Refer to IPC/JEDEC J-Std-020B Table 5-2 for the recommended solder reflow temperature profile.

5.2 Operating Ranges

Zarlink guarantees the performance of this device over commercial (0 to 70°C) and industrial (-40 to 85°C) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with section 4.6.2 of Bellcore GR-357-CORE Component Reliability Assurance Requirements for Telecommunications Equipment.

Ambient Temperature	-40° to 85°C
V _{CC}	4.75 to 5.25 V
V _{BAT}	-39 to -58 V
DB1, DB2, and DAC	V _{BAT} to -2 V
AGND	0 V
BGND1, BGND2 with respect to AGND	-100 to + 100 mV
Load resistance on VTX to ground	20 kΩ minimum

Note:

The operating ranges define those limits between which the device operates and is guaranteed under the noted test conditions.

6.0 Specifications

6.1 Transmission Performance

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
2-wire return loss	200 Hz to 3.4 kHz (See Figure 6 on page 19)	26			dB	3, 5
Analog output (VTX) impedance			3	20	Ω	3
Analog (VTX) output offset voltage		−50		+50	mV	
Overload level, 2-wire	Active or Reverse Polarity state	2.5			V _{pk}	2a
Overload level	On hook	1.1				2b
THD (Total Harmonic Distortion)	0 dBm		−64	−50	dB	4
	+7 dBm		−55	−40		
THD, On hook	0 dBm			−36		

6.2 Crosstalk Between Channels

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
Crosstalk coupling loss	F = 200 Hz to 3.4 kHz		80		dB	3

6.3 Longitudinal Capability

(See Figure 5 on page 19.)

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
Longitudinal to metallic L-T, L-4 balance	200 Hz to 3.4 kHz, 0° C to +70° C	50			dB	3
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40				
Longitudinal current per pin (A or B)	Active state (off hook)	8.5	20		mArms	6
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω /pin	
Idle Channel Noise	C-Message, $R_L = 600 \Omega$		7	12	dBrnC	3
	Psophometric, 600 Ω		−83	−78	dBmp	

6.4 Insertion Loss

(See Figure 3 and Figure 4 on page 18.)

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
Gain accuracy, 4-to-2-wire	0 dBm, 1 kHz	−0.20	0	+0.20	dB	
Gain accuracy, 2-to-4-wire and 4-to-4-wire	0 dBm, 1 kHz	−9.74	−9.54	−9.34		
Gain accuracy, 4-to-2-wire	On hook	−0.35		+0.35		
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz	−0.15		+0.15		
Gain tracking	+3 dBm to −55 dBm relative to 0 dBm	−0.15		+0.15		3
Gain tracking, On hook	0 dBm to −37 dBm +3 dBm to 0 dBm	−0.15 −0.35		+0.15 +0.35		

6.5 Line Characteristics

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
I_L , Short Loops, Active state		26.4	30	33.6	mA	
I_L , Long Loops, Active state	$R_{LDC} = 1930\ \Omega$, $BAT = -42.75\ V$, $T_A = 25^\circ C$	18	19			
I_L , Accuracy, Standby state	$I_L = \left(\frac{ V_{BAT} - 3V}{(R_L + 3.2\ k)} \right)$, $T_A = 25^\circ C$	$0.7I_L$	I_L	$1.3I_L$		
I_L , Loop current, Disconnect state	$R_L = 0$			100	μA	
VAB, Open Circuit voltage	$V_{BAT} = -48\ V$	+38.3	+40.3		V	

6.6 Power Supply Rejection Ratio at the Two-Wire Interface, Active Normal State

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
V_{CC}	50 Hz to 3.4 kHz $V_{RIPPLE} = 100\ mV_{RMS}$	30	40		dB	4
V_{BAT}	50 Hz to 3.4 kHz $V_{RIPPLE} = 500\ mV_{PP}$	28	50			

6.7 Power Dissipation

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
On hook, both channels, Standby state			40	100	mW	
On hook, both channels, Active state			380	540		
Off hook, both channels, Active state	$R_L = 300\ \Omega$, $R_{TMG} = 1600\ \Omega$		1400	1700		
One channel, Active state One channel, Standby state	$R_L = 300\ \Omega$, $R_{TMG} = 1600\ \Omega$		720	1050		

6.8 Supply Currents

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
I_{CC} , On-hook V_{CC} supply current	Both channels, Standby state		2.5	4.0	mA	
	Both channels, Active state, $BAT = -48\ V$		9.0	12.0		
I_{BAT} , On-hook V_{BAT} supply current	Both channels, Standby state		0.5	1.5		
	Both channels, Active state, $BAT = -48\ V$		6.5	8.5		

6.9 RFI Rejection

(See Figure 7 on page 19.)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
VTX1 or VTX2	f = .01 to 100 MHz HF gen output = 1.5 Vrms $C_{AXi} = C_{BXi} = 33 \text{ nF}$			1	mVrms	3
	$C_{AXi} = C_{BXi} = 2.2 \text{ nF}$			3		

6.10 Logic Inputs

(Applies to C1₁, C1₂, C2₁, and C2₂.)

Description	Test Conditions	Min.	Typ.	Max.	Unit	Note
V _{IH} , Input High voltage		2.0			V	
V _{IL} , Input Low voltage				0.8		
I _{IH} , Input High current		−75		40	μA	
I _{IL} , Input Low current		−400				

6.11 Logic Output

(Applies to $\overline{\text{DET1}}$ and $\overline{\text{DET2}}$.)

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
V _{OL} , Output Low voltage	I _{OUT} = 0.3 mA			0.40	V	
V _{OH} , Output High voltage	I _{OUT} = −0.1 mA	2.4				

6.12 Ring-Trip Detector Input

(Applies to DAC, DB1, and DB2.)

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
Bias Current		−500	−50		nA	
Common Mode Range		V _{BAT+} 1		−2	V	

6.13 Loop Detector

Description	Test Conditions (See Note 1)	Min.	Typ.	Max.	Unit	Note
Off-hook threshold Active		9		11	mA	
On-hook threshold Active		8.5		10.5		
Off-hook threshold Standby		4		6		
On-hook threshold Standby		3.8		5.8		
Hysteresis		0		2		

Notes:

- Unless otherwise noted, the test conditions are set up by the Le5711 device test circuit as illustrated in Figure 8 on page 20.
- Overload level is defined as THD = 1%.
 - Overload level is defined when THD = 1.5%.
- Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
- This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
- Group delay can be greatly reduced by using a Z_T network such as that shown in Figure 6. The network reduces the group delay to less than 2 μ s and increases 2WRL. The effect of group delay on linecard performance also may be compensated by synthesizing complex impedance with the QLSLAC™ device.
- Minimum current level guaranteed not to cause a false loop detect.

6.14 SLIC Device Decoding

(For i, Channel = 1 or 2)

State	C2 _i	C1 _i	Two-Wire Status	$\overline{\text{DET}}_x$ Output
0	0	0	Disconnect	Ring-Trip Detector
1	0	1	Active	Loop Detector
2	1	1	Polarity Reversed	Loop Detector
3	1	0	Standby	Loop Detector

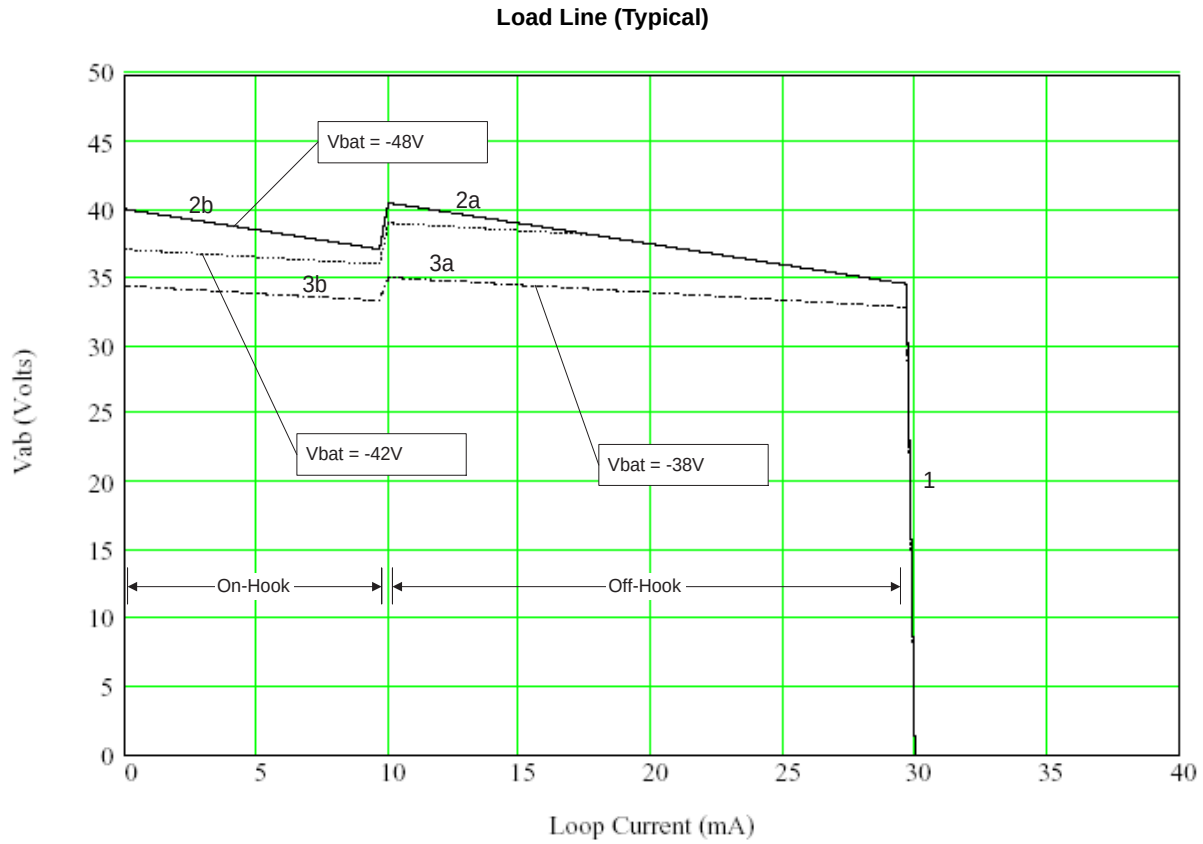
6.15 User-Programmable Components

Equation	Description
$Z_{Ti} = 166.7(Z_{2WIN} - 2R_F)$	Z_{Ti}^* is connected between the VTX and RSN pins. The fuse resistors are R_F , and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_{Ti} , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RXi} = \frac{Z_L}{G_{42L}} \cdot \frac{500Z_T}{Z_T + 166.7(Z_L + 2R_F)}$	Z_{RXi}^* is connected from VRX to RSN. Z_{Ti} is defined above, and G_{42L} is the desired receive gain.
$R_{REF} = \frac{450}{I_{LOOP}}$ $C_{DC} = 1.5 \mu F$	I_{LOOP} is the desired loop current in the constant-current region. Loop detect threshold is typically 1/3 of programmed Loop current.
$C_{CAS} = \frac{1}{170 \text{ k}\Omega \cdot 2\pi \cdot f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{ V_{BAT} - 3 \text{ V}}{3200 \Omega + R_L}$	Standby loop current (resistive region).
Thermal Management Equations (Active, and Reverse Polarity states for one channel)	
$R_{TMG} \geq \frac{ V_{BATMAX} - 6 \text{ V} - I_{LMIN}(2R_F + R_{LMIN})}{I_{LMIN}} - 40 \Omega$	R_{TMG} is connected from TMG to VBAT and limits power within the SLIC device in Active and Off-Hook states.
$P_{RTMG} = \frac{(V_{BAT} - 6 \text{ V} - [I_L \cdot (R_L + 2R_F)])^2}{(R_{TMG} + 40 \Omega)^2} \cdot R_{TMG}$	Power dissipated in the TMG resistor, R_{TMG} , during Active and Off-Hook states.
$P_{SLIC} = V_{BAT} \cdot I_L - P_{RTMG} - R_L(I_L)^2 + 0.12 \text{ W}$	Power dissipated per channel in the SLIC device while in Active state.

Note:

* "i" denotes channel number

6.16 DC Feed Characteristics



Switch-hook Threshold: $I_{SWTH} = \frac{150}{R_{REF}}$ $R_{REF} = 15\text{ k}$

Regions:

1. Constant current region: $V_{AB1} = I_L R_L' = \frac{(450)}{R_{REF}} R_L'$, where $R_L' = R_L + 2R_F$
- 2a. Battery-independent anti-sat (Off-hook): $V_{AB2a} = 43.6\text{ V} - I_L 303\ \Omega$
- 2b. Battery-independent anti-sat (On-hook): $V_{AB2b} = V_{AB2a} - 3.5\text{ V}$
- 3a. Battery tracking anti-sat (Off-hook): $V_{AB3a} = |V_{BAT}| - 1.8\text{ V} - I_L 111\ \Omega$
- 3b. Battery tracking anti-sat (On-hook): $V_{AB3b} = V_{AB3a} - 0.33 \cdot |V_{BAT}| + 10.8$

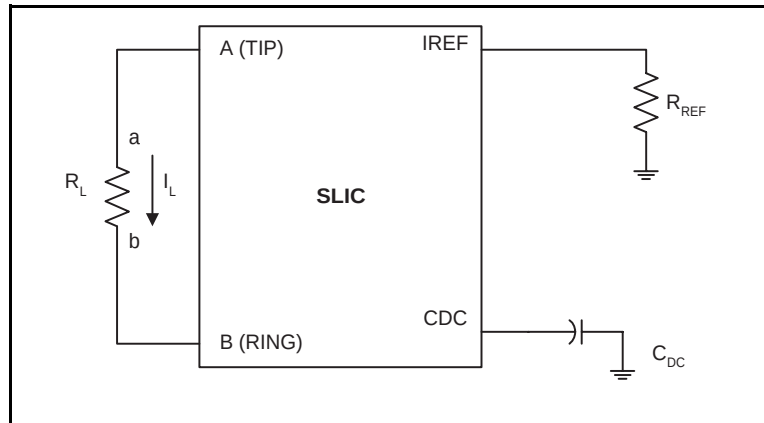


Figure 2 - Feed Programming

6.17 Test Circuits

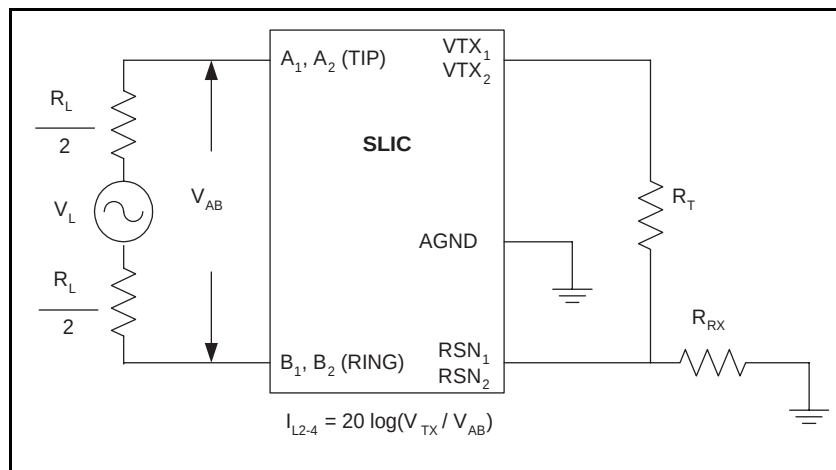


Figure 3 - Two-to-Four Wire Insertion Loss

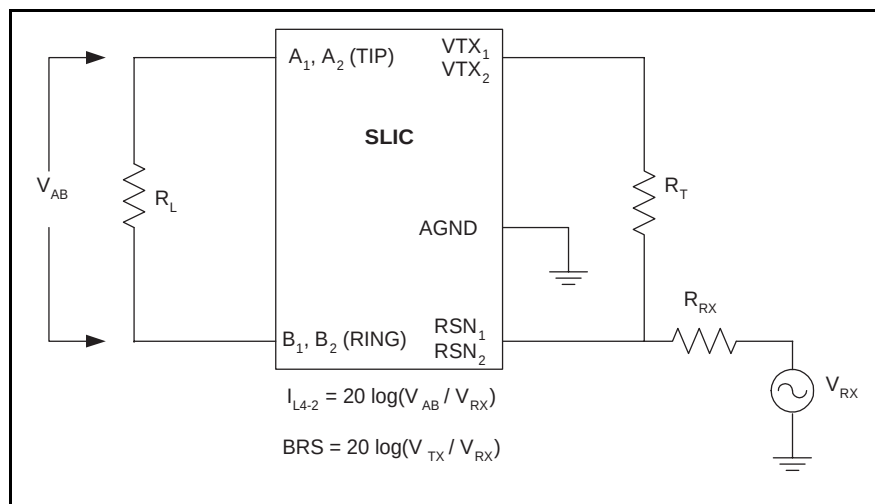


Figure 4 - Four-to-Two Wire Insertion Loss and Balance Return Signals

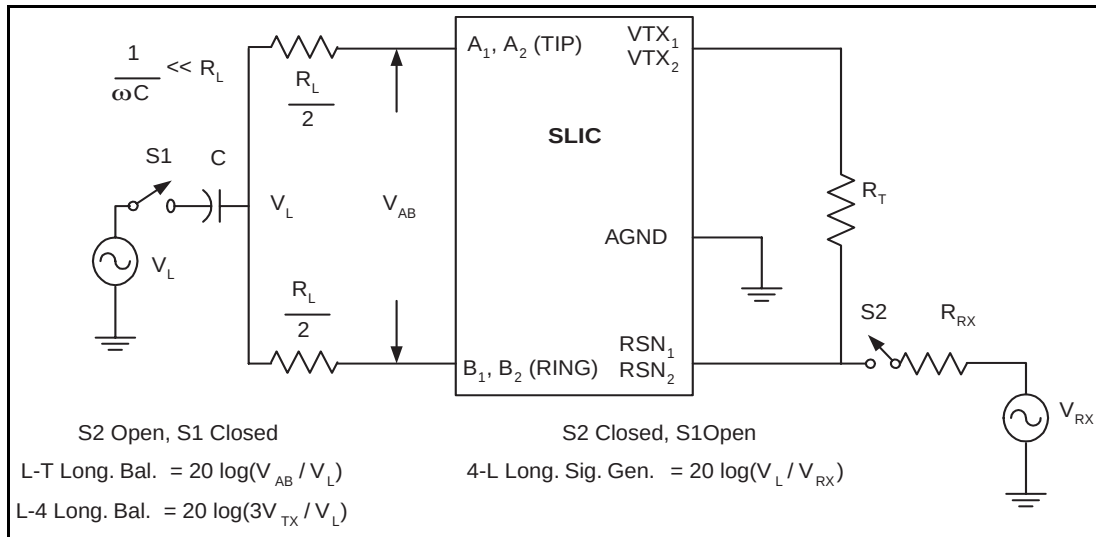


Figure 5 - Longitudinal Balance

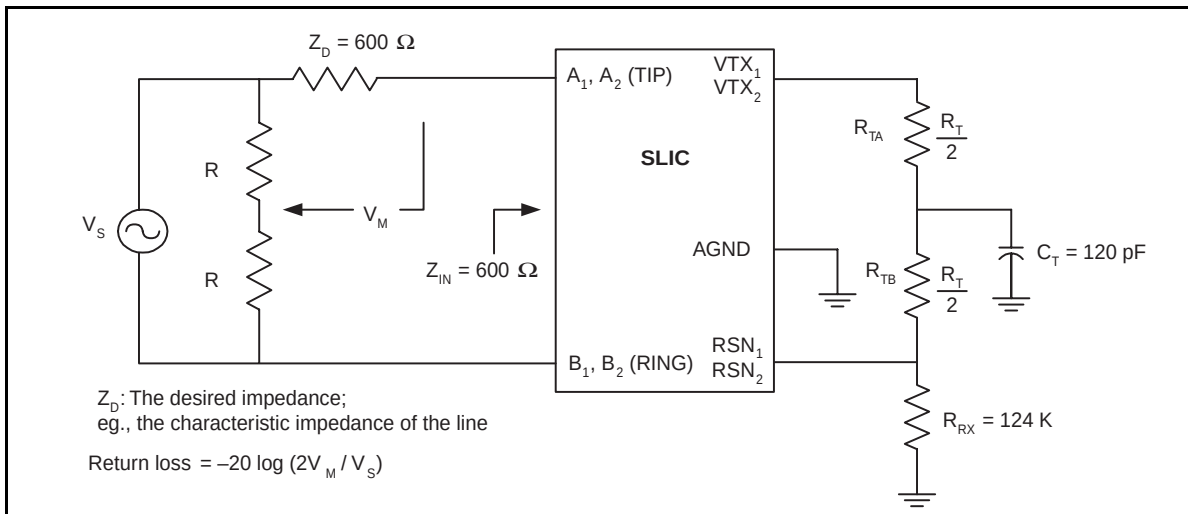


Figure 6 - Two-Wire Return Loss Test Circuit

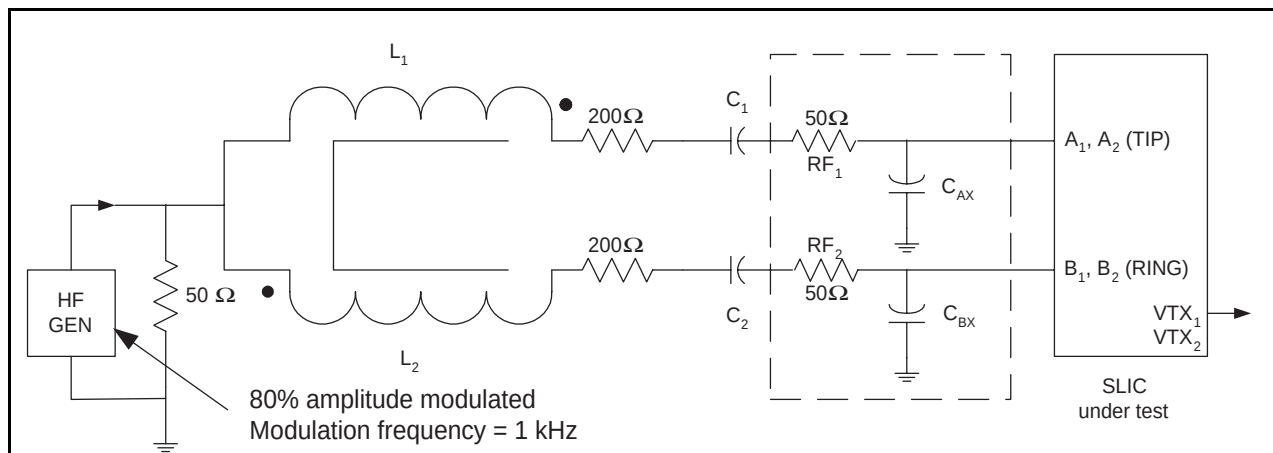


Figure 7 - RFI Test Circuit

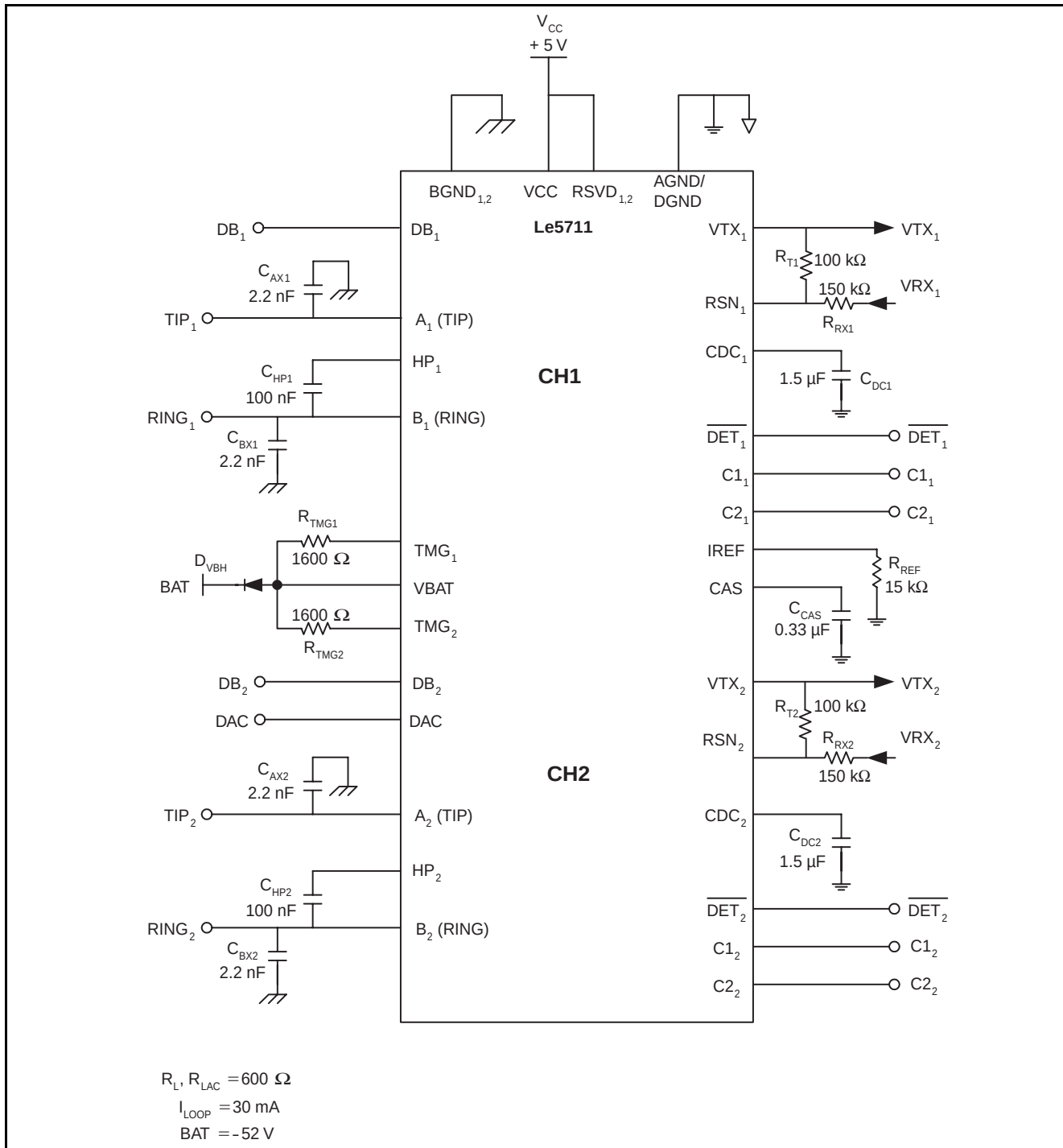
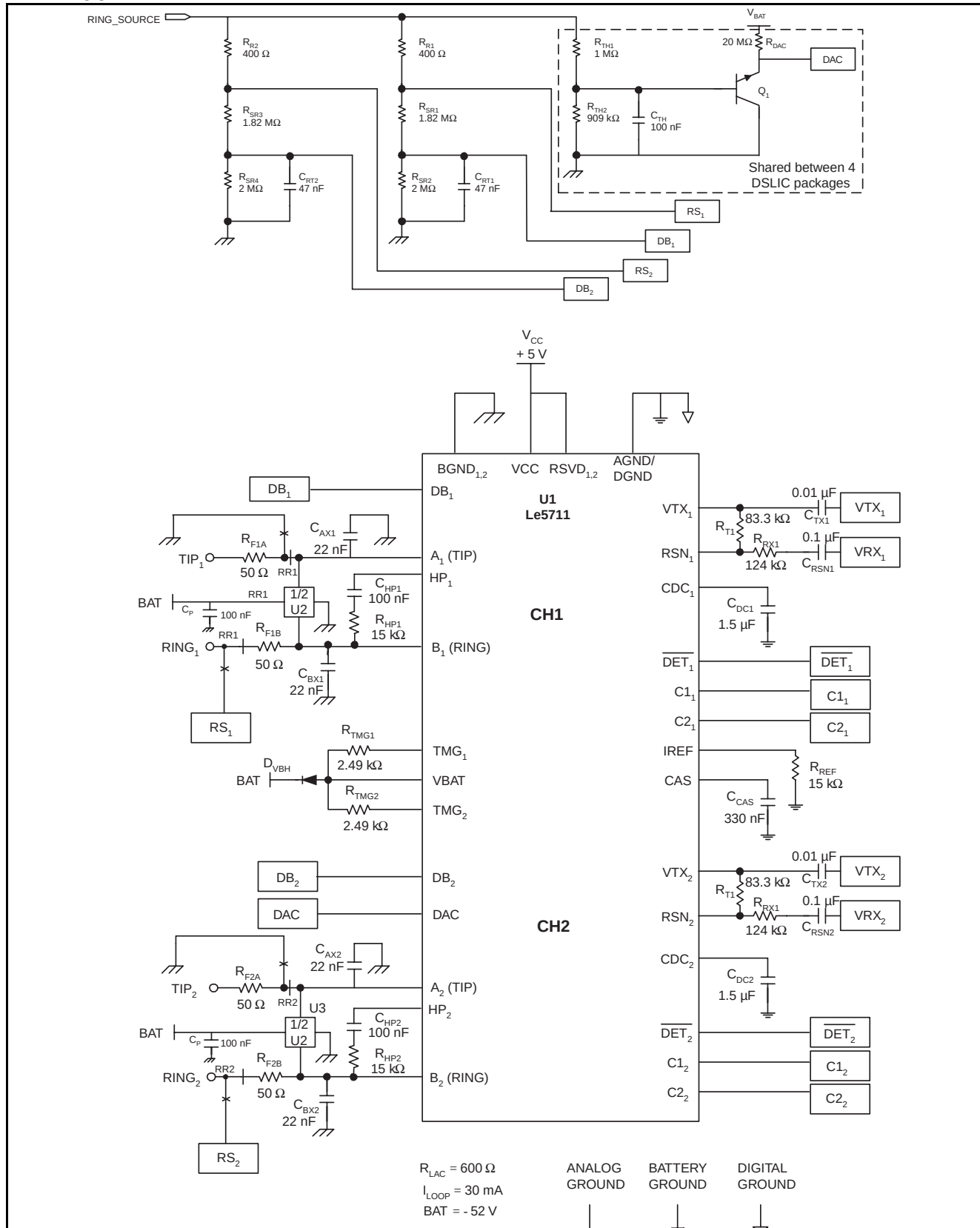


Figure 8 - Le5711 Test Circuit

7.0 Application Circuit



8.0 Line card Parts List

The following list defines the parts and part values required to meet target specification limits for channel i of the line card (i = 1,2).

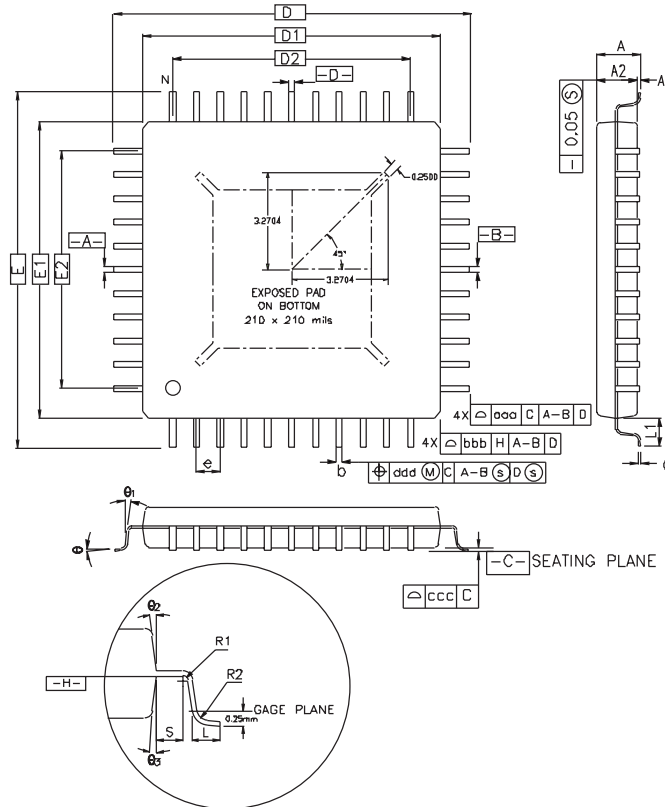
Item	Quantity	Type	Value	Tol.	Rating	Comments	Note
C _{AX1} , C _{BX1} , C _{AX2} , C _{BX2}	4	Capacitor (X7R)	22 nF	20%	100 V		
C _{HP1} , C _{HP2} , C _P	3	Capacitor (X7R)	100 nF	20%	100 V		
C _{TH}		Capacitor (X7R)	100 nF	20%	50 V		1
C _{RT1} , C _{RT2}	2	Capacitor (X7R)	47 nF	20%	50 V		
C _{DC1} , C _{DC2}	2	Capacitor (X7R)	1.5 μ F	20%	5 V		
C _{TX1} , C _{TX2}	2	Capacitor (X7R)	0.01 μ F	20%	5 V		
C _{RSN1} , C _{RSN2}	2	Capacitor (X7R)	0.1 μ F	20%	5 V		
R _{F1A} , R _{F1B} , R _{F2A} , R _{F2B}	2	PTC or Fusible	50 Ω				
R _{REF}	1	SMT	15 k Ω	1%	1/10 W		
R _{T1} , R _{T2}	2	SMT	83.3 k Ω	1%	1/10 W		
R _{RX1} , R _{RX2}	2	SMT	124 k Ω	1%	1/10 W		
R _{HP1} , R _{HP2}	2	SMT	15 k Ω	1%	1/10 W		
D _{VBH}	1	MURS 120 (D0-41) DIODE					
R _{R1} , R _{R2}	2	SMT	400 Ω	5 Ω	1 W		
U2	1	TISP6NTP2A					
R _{SR2} , R _{SR4}	2	SMT	2 M Ω	1%	1/10 W		
R _{SR1} , R _{SR3}	2	SMT	1.82 M Ω	1%	1/10 W		
U1	1	Le5711 device					
R _{TMG1} R _{TMG2}	2	SMT	1.8 k Ω	5%	1 W		2
C _{CAS}	1	Capacitor (X7R)	330 nF	20%	100 V		
R _{TH1}	*	SMT	1 M Ω	1%	1/10 W		
R _{TH2}	*	SMT	909 k Ω	1%	1/10 W		
R _{DAC}	*	SMT	20 M Ω	5%	1/10 W		
Q ₁	*	NPN	BC639		50 V		

Note:

- * Shared between four DualSLIC device packages
- Refer to the Thermal Management for the Le5711 and Le5712 Dual Devices Application Note for particular conditions.

9.0 Physical Dimensions

9.1 44-Pin eTQFP



Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
A	-	-	1.20	c	0.09	-	0.20
A1	0.05	-	0.15	L	0.45	0.60	0.75
A2	0.95	1.00	1.05	L1	1.00 REF		
D	12 BSC			S	0.20	-	-
D1	10 BSC			b	0.17	0.20	0.27
E	12 BSC			e	0.80 BSC		
E1	10 BSC			D2	8.00		
R2	0.08	-	0.20	E2	8.00		
R1	0.08	-	-	aaa	0.20		
Θ	0 deg	3.5 deg	7 deg	bbb	0.20		
Θ 1	0 deg	-	-	ccc	0.10		
Θ 2	11 deg	12 deg	13 deg	ddd	0.20		
Θ 3	11 deg	12 deg	13 deg	N	44		

Notes:

- Controlling dimension in millimeter unless otherwise specified.
- Dimensions "D1" and "E1" do not include mold protrusion. Allowable protrusion is 0.25mm per side.
"D1" and "E1" are maximum plastic body size dimensions including mold mismatch.
- Dimension "b" does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08mm.
- Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07mm for 0.4mm and 0.5mm pitch packages.
- Square dotted line is E-Pad outline.
- "N" is the total number of terminals.

Note:

Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.



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