LB1980JH

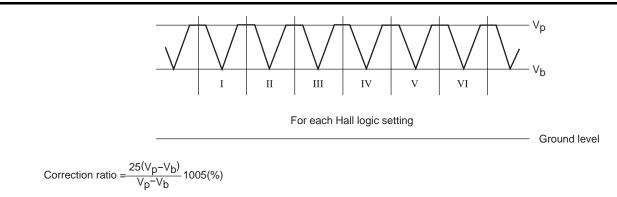
Allowable Operating Ranges at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VS		5 to 22	V
	VCC		4.5 to 5.5	V
Hall input amplitude	V _{HALL}	Between the hall inputs	±30 to ±80	mVo-p
GSENSE pin input range	VGSENSE	With respect to the control system ground	-0.20 to +0.20	V

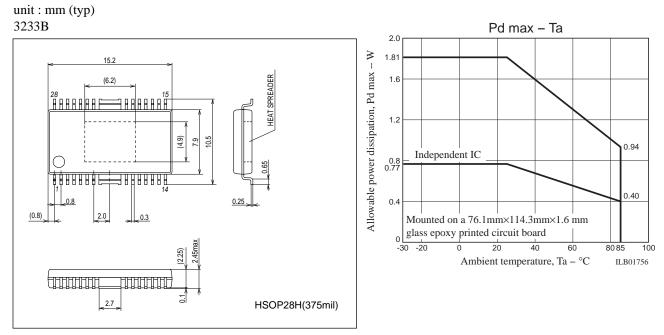
Electrical Characteristics at Ta = 25° C, V_{CC} = 5V,V_S = 15V

Parameter	Symbol Conditions		Ratings			Unit
	0,		min	typ	max	0.111
V _{CC} supply current	lcc	$R_{L=\infty}$, $V_{CTL}=0V$, $V_{LIM}=0V$ (Quiescent)		12	18	mA
Outputs						
Output saturation voltage	VO sat1	I_{O} =500mA, Rf=0.5 Ω , Sink+Source V_{CTL} = V_{LIM} =5 V (With saturation prevention)		2.1	2.6	V
	VO sat2	I _O =1.0mA, Rf=0.5Ω, Sink+Source V _{CTL} =V _{LIM} =5V(With saturation prevention)		2.6	3.5	V
Output leakage current	IO leak				1.0	mA
FR						
FR pin input threshold voltage	V _{FSR}		2.25	2.50	2.75	V
FR pin input bias current	I _B (FSR)		-5.0			mA
Control						
CTLREF pin voltage	VCREF		2.05	2.15	2.25	V
CTLREF pin input range	VCREFIN		1.50		3.50	V
CTL pin input bias current	I _B (CTL)	With V _{CTL} =5V and the CTLREF pin open			4.0	μA
CTL pin control start voltage	V _{CTL} (ST)	With Rf=0.5 Ω , V _{LIM} =5V, I _O ≥10mA, Hall input logic fixed (U, V, W=H, H, L)	2.00	2.15	2.30	V
CTL pin control Gm	Gm(CTL)	With Rf=0.5 Ω , ΔI_O =200mA, Hall input logic fixed (U, V, W=H, H, L)	0.46	0.58	0.70	A / \
Current Limiter						
LIM current limit offset voltage	Voff(LIM)	With Rf=0.5 Ω , V _{CTL} =5V, I _O ≥10mA, Hall input logic fixed (U, V, W=H, H, L)	140	200	260	mV
LIM pin input bias current	I _B (LIM)	With V _{CTL} =5V and the V _{CREF} pin open	-2.5			μA
LIM pin current control level	ILIM	With Rf=0.5Ω, V _{CTL} =5V, V _{LIM} =2.06V Hall input logic fixed (U, V, W=H, H, L)	830	900	970	mA
Hall Amplifier						
Hall amplifier input offset voltage	Voff(HALL)		-6		+6	mA
Hall amplifier input bias current	I _B (HALL)			1.0	3.0	μA
Hall amplifier common-mode	V _{CM} (HALL)			1.3	3.3	V
input voltage range						
TRC		1				
Torque ripple correction ratio	TRC	For the high and low peaks in the Rf waveform when $I_O=200$ mA. (Rf=0.5 Ω , with the ADJ pin open) *1		9		%
ADJ pin voltage	V _{ADJ}		2.37	2.50	2.63	V
FG Amplifier	-					
FG amplifier input offset voltage	Voff(FG)		-8		+8	mV
FG amplifier input bias current	I _B (FG)		-100			nA
FG amplifier output saturation voltage	V _O sat (FG)	Sink side, for the load provided by the internal pull-up resistor			0.5	V
FG amplifier voltage gain	V _G (FG)	For the open loop state with f=10kHz	41.5	44.5	47.5	dB
FG amplifier common-mode	V _{GM} (FG)		0.5		4.0	V
input voltage						
Saturation						
Saturation prevention circuit lower side voltage setting	VO sat(DET)	The voltages between each OUT and Rf pair when $I_O{=}10\text{mA},$ Rf=0.5 $\Omega,$ and $V_{CTL}{=}V_{LIM}{=}5V$	0.175	0.25	0.325	V
TSD						
TSD operating temperature	TSD	Design target value *2		180		°C
Hysteresis width	∆TSD	Design target value *2		20		°C

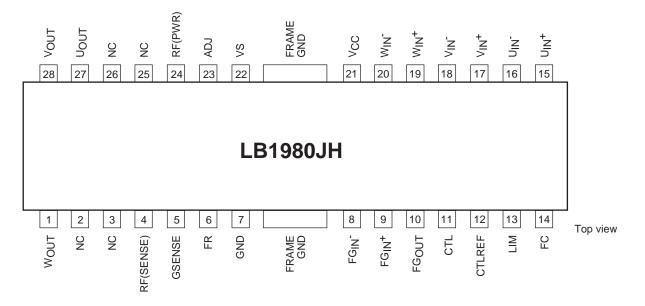
*2. Parameters that are indicated as design target values in the conditions column are not tested.



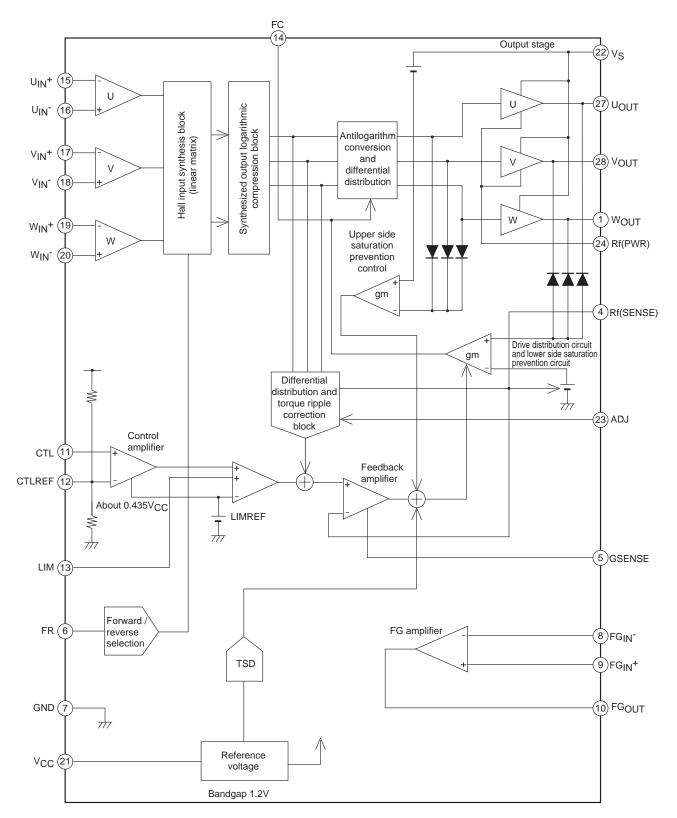
Package Dimensions



Pin Assignment



Block Diagram



Pin F	unction		
Pin No.	Pin Name	Function	Equivalent circuit
27 28 1	U _{OUT} Vout Wout	U phase output, Spark killer diodes are built-in. V phase output, Spark killer diodes are built-in. W phase output, Spark killer diodes are built-in.	
4 5 22 5	Rf (SENSE) Rf (PWR) VS GSENSE	Output current detection. The control block current limiter operates using the resistor Rf connected between these pins and ground. Also, the lower side saturation prevention circuit and the torque ripple correction circuit operate based on the voltages across this resistor. It is especially important to note that, since the saturation prevention level is set using this voltage, the lower side saturation prevention circuit will become less effective in the high current region if the value of Rf is lowered excessively. Also, the PWR and SENSE pins must be connected together. Output block power supply Ground sensing. The influence of the common ground impedance on Rf can be excluded by connecting this pin	Vs 150μA 150μA Lower side saturation prevention circuit input block VCC 30kΩ Rf (PWR) VCC 4 VCC 10μA 10μA 10μA 10μA 10μA 10μA 10μA
6	FR	to nearest ground for the Rf resistor side of the motor ground wiring that includes Rf. (This pin must not be left open.) Forward / reverse selection. The voltage applied to this	
		pin selects the motor direction (forward or reverse). (Vth=2.5V at V _{CC} =5V (typical))	
23	ADJ	Used for external adjustment of the torque ripple correction ratio. Apply a voltage externally with a low-impedance circuit to the ADJ pin to adjust the correction ratio. The correction ratio falls as the applied voltage is increased, and increases as the applied voltage decreases. The torque ripple correction ratio can be modified by factors in the range 0 to 2 times the ratio that applies when his pin is left open. (The pin voltage is set to about V _{CC} / 2 internally, and the input impedance is about 5k Ω .)	$F_{0} = \frac{1}{200 \mu A}$
7	GND	Ground for all circuits other than the output transistors. The lowest potential of the output transistors is that of the Rf pin.	
8	FG _{IN} -	Input used when the FG amplifier is used as an inverting input. A feedback resistor must be connected between FG _{OUT} and this pin.	^V CC4 5μΑ 🔗
9	FG _{IN} +	Non-inverting input used when the FG amplifier is used as a differential input amplifier. No bias is applied internally.	FGIN(-)
10	FG _{OUT}	FG amplifier output. There is an internal resistive load.	V_{CC} V_{CC} V_{CC} $\geq 2k\Omega$ FG_{OUT} \downarrow 300Ω $\geq 10k\Omega$
14	FC	Speed control loop frequency characteristics correction.	

Continued on next page.

Continu	ed from prec	eding page.	
Pin No.	Pin Name	Function	Equivalent circuit
11	CTL	Speed control input. The control implemented is fixed current drive controlled by current feedback from Rf. Gm=0.58 / V (typical) when Rf=0.5W	CTL
12	CTLREF	Control reference voltage. While this pin is set to about $0.43 \times V_{CC}$ internally, this voltage can be modified by applying a voltage from a low-impedance circuit. (The input impedance is about $4.3 \mathrm{k}\Omega$).	$\begin{array}{c} 11 \\ 200\Omega \\ 200\Omega \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\ 10 \\$
13	LIM	Current limiter function control. The output current can be varied linearly by applying a voltage to this pin. The slope is $0.5A / V$ (typical) when Rf= 0.5Ω .	
15	U _{IN} +	U phase Hall element inputs.	(+) input (-) input
16	U _{IN} -	Logic high is defined as states where IN ⁺ >IN ⁻ .	
17	V _{IN} +	V phase Hall element inputs.	
18	V _{IN} -	Logic high is defined as states where IN ⁺ >IN ⁻ .	жарана и соота и Поста и соота и Поста и соота и
19	WIN ⁺	W phase Hall element inputs.	Ý
20	W _{IN} ⁻	Logic high is defined as states where IN ⁺ >IN ⁻ .	7/17
21	VCC	Power supply for all internal blocks other than the output block. This voltage must be stabilized so that noise and ripple do not enter the IC.	

Truth Table and Control Functions

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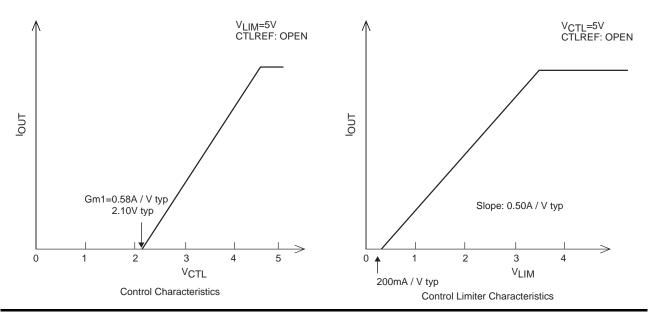
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		Hall input			FR
	Source \rightarrow Sink	U	V	W	FK
1	$Phase\;V\toPhase\;W$	н	н	L	Н
	$Phase\:W\toPhase\:V$				L
2	$Phase\;U\toPhase\;W$	н	L	L	Н
	$Phase\:W\toPhase\:U$				L
3	$Phase\;U\toPhase\;V$	Н	L	Н	Н
	$Phase\;V\toPhase\;U$				L
4	$Phase\:W\toPhase\:V$	L		н	Н
	$Phase\;V\toPhase\;W$		L		L
5	$Phase\:W\toPhase\:U$	L		н	Н
	$Phase\;U\toPhase\;W$		н		L
6	$Phase\;V\toPhase\;U$	L		L	Н
	$Phase\;U\toPhase\;V$		н		L

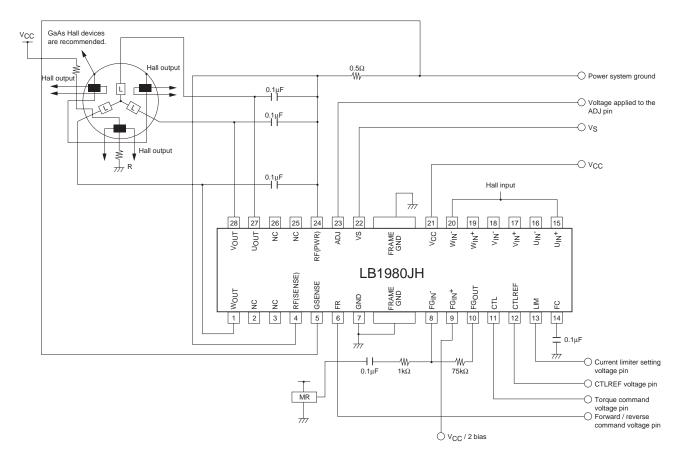
- Note: In the FR column, "H" refers to a voltage of 2.75V or higher, and "L" refers to 2.25V or lower (when VCC=5V.)
- Note: In the Hall input column, "H" refers to the state in the corresponding phase where the +input is at a potential at least 0.01V higher than the -input, and "L" refers to the state where the -input is at a potential at least 0.01V higher than the +input.

Note: Since the drive technique adopted is a 180° technique, phases other than the sink and source phase do not turn off.

Control Function and Current Limiter Function



Application Circuit Example



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