Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	V_{CC} pin	18	V
Output current	I_O max	UL, VL, WL, UH, VH, and WH pins	30	mA
LVS pin applied voltage	LVS max	LVS pin	18	V
Allowable power dissipation 1	Pd max1	Independent IC	0.45	W
Allowable power dissipation 2	Pd max2	Circuit board*	1.05	W
Operating temperature	Topr		–20 to +100	°C
Storage temperature	Tstg		–55 to +150	°C

* When mounted on a 114.3 × 76.1 × 1.6 mm glass epoxy board

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V_{CC}1-1	V_{CC} pin	8 to 17	V
Supply voltage range 1-2	V_{CC}1-2	V_{CC} pin, when V_{CC} is shorted to VREG.	4.5 to 5.5	V
Output current	I_O	UL, VL, WL, UH, VH, and WH pins	25	mA
5 V constant voltage output current	IREG		–30	mA
HP pin applied voltage	VHP		0 to 17	V
HP pin output current	IHP		0 to 15	mA
RD pin applied voltage	VRD		0 to 17	V
RD pin output current	IRD		0 to 15	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics at Ta = 25°C, V_{CC} = 12 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain 1	$I_{CC}1$			12	16	mA
Current drain 2	$I_{CC}2$	Stop mode		2.5	4	mA
5 V Constant Voltage Output (VREG pin)						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC} = 8 to 17 V		40	100	mV
Load regulation	ΔVREG2	I_O = –5 to –20 mA		5	30	mV
Temperature coefficient	ΔVREG3	Design target value*		0		mV/°C
Output Block						
Output voltage 1-1	V_{OUT}1-1	UH, VH, and WH at the low level, I_O = 400 μA		0.2	0.5	V
Output voltage 1-2	V_{OUT}1-2	UH, VH, and WH at the low level, I_O = 10 mA		0.9	1.2	V
Output voltage 2	V_{OUT}2	UH, VH, and WH at the High level, I_O = –20 mA	V_{CC} – 1.1	V_{CC} – 0.9		V
Output voltage 3	V_{OUT}3	UL, VL, and WH at the low level, I_O = 20 mA		0.3		V
Output leakage current	$I_O$leak				10	μA
Hall Amplifier Block						
Input bias current	IHB (HA)		–2	–0.5		μA
Common-mode input voltage range 1	VICM1	When a Hall effect device is used	0.5		V_{CC} – 2.0	V
Common-mode input voltage range 2	VICM2	Single-sided input bias mode (when a Hall IC is used)	0		V_{CC}	V
Hall Input Sensitivity			80			mVp-p
Hysteresis	ΔVIN (HA)		15	24	40	mV
Input voltage low → high	VSLH (HA)		5	12	20	mV
Input voltage high → low	VSHL (HA)		–20	–12	–5	mV
CTL Amplifier						
Input offset voltage	V_{IO} (CTL)		–10		10	mV
Input bias current	I_B (CTL)		–1		1	μA
Common-mode input voltage range	VICM		0		VREG – 1.7	V
High-level output voltage	V_{OH} (CTL)	ITOC = –0.2 mA	VREG – 1.2	VREG – 0.8		V
Low-level output voltage	V_{OL} (CTL)	ITOC = 0.2 mA		0.8	1.05	V
Open-loop gain	G (CTL)	f (CTL) = 1 kHz	45	51		dB
PWM Oscillator (PWM pin)						
High-level output voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL} (PWM)		1.2	1.35	1.5	V
External capacitor charge current	ICHG	VPWM = 2.1 V	–120	–90	–65	μA
Oscillator frequency	f (PWM)	C = 2000 pF		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-p

Note:*Design target value. These items are not tested.

Continued on next page.

Continued from preceding page.

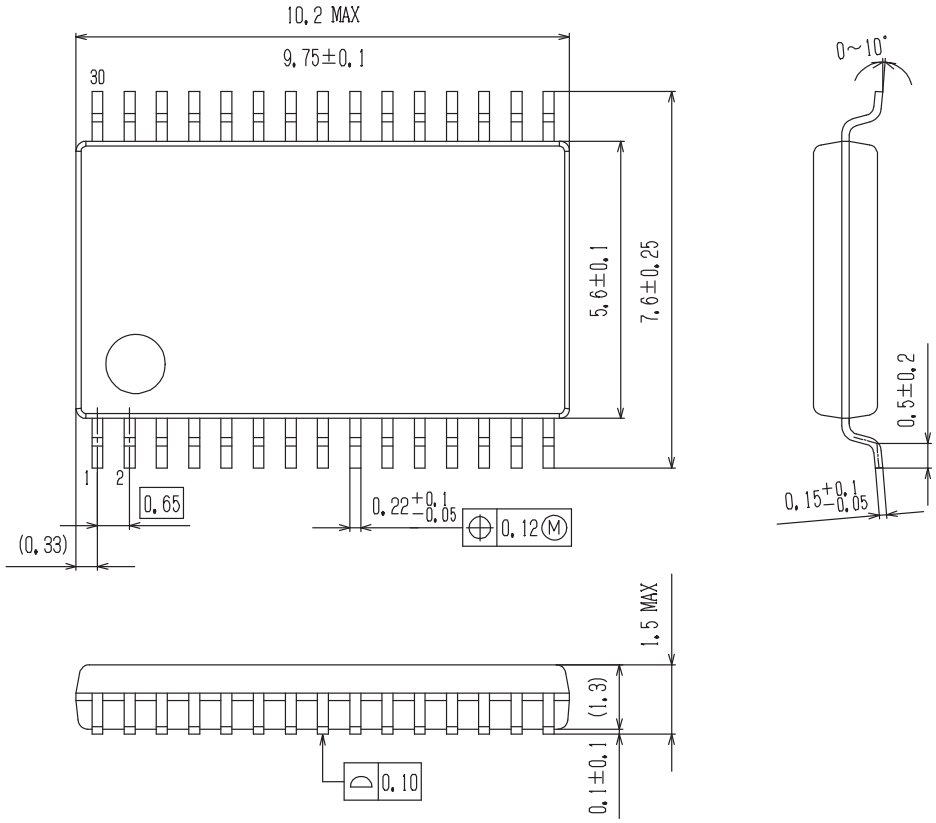
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
TOC pin						
Input voltage 1	VTOC1	Output duty: 100%	2.68	3.0	3.34	V
Input voltage 2	VTOC2	Output duty: 0%	1.2	1.35	1.5	V
Input voltage 1 low	VTOC1L	Design target value*, when VREG = 4.7 V, 100%	2.68	2.82	2.96	V
Input voltage 2 low	VTOC2L	Design target value*, when VREG = 4.7 V, 0%	1.23	1.29	1.34	V
Input voltage 1 high	VTOC1H	Design target value*, when VREG = 5.3 V, 100%	3.02	3.18	3.34	V
Input voltage 2 high	VTOC2H	Design target value*, when VREG = 5.3 V, 0%	1.37	1.44	1.50	
HP Pin						
Output saturation voltage	VHPL	I_O = 10 mA		0.2	0.5	V
Output leakage current	IHPleak	V_O = 18 V			10	μA
CSD Oscillator (CSD pin)						
High-level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low-level output voltage	V_{OL} (CSD)		0.7	1.0	1.3	V
External capacitor charge current	ICHG1	VCSD = 2 V	–3.15	–2.5	–1.85	μA
External capacitor discharge current	ICHG2	VCSD = 2 V	0.1	0.14	0.18	μA
Charge/discharge current ratio	RCSD	(Charge current)/(discharge current)	15	18	21	times
RD Pin						
Low-level output voltage	VRDL	I_O = 10 mA		0.2	0.5	V
Output leakage current	I_L (RD)	V_O = 18 V			10	μA
Current Limiter Circuit (RF pin)						
Limiter voltage	VRF	RF-RFGND	0.225	0.25	0.275	V
Undervoltage Protection Circuit (LVS pin)						
Operating voltage	VSDL		3.5	3.7	3.9	V
Release voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	ΔVSD		0.3	0.45	0.6	V
PWMIN Pin						
Input frequency	f (PI)				50	kHz
High-level input voltage	V_{IH} (PI)		2.0		VREG	V
Low-level input voltage	V_{IL} (PI)		0		1.0	V
Input open voltage	V_{IO} (PI)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (PI)		0.2	0.25	0.4	V
High-level input current	I_{IH} (PI)	VPWMIN = VREG	–10	0	+10	μA
Low-level input current	I_{IL} (PI)	VPWMIN = 0 V	–130	–90		μA
S/S Pin						
High-level input voltage	V_{IH} (SS)		2.0		VREG	V
Low-level input voltage	V_{IL} (SS)		0		1.0	V
Hysteresis	V_{IS} (SS)		0.2	0.25	0.4	V
High-level input current	I_{IH} (SS)	VS/S = VREG	–10	0	+10	μA
Low-level input current	I_{IL} (SS)	VS/S = 0 V	–10	–1		μA
F/R Pin						
High-level input voltage	V_{IH} (FR)		2.0		VREG	V
Low-level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG – 0.5		VREG	V
Hysteresis	V_{IS} (FR)		0.2	0.25	0.4	V
High-level input current	I_{IH} (FR)	VF/R = VREG	–10	0	+10	μA
Low-level input current	I_{IL} (FR)	VF/R = 0 V	–130	–90		μA
N1 Pin						
High-level input voltage	V_{IH} (N1)		2.0		VREG	V
Low-level input voltage	V_{IL} (N1)		0		1.0	V
Input open voltage	V_{IO} (N1)		VREG – 0.5		VREG	V
High-level input current	I_{IH} (N1)	VN1 = VREG	–10	0	+10	μA
Low-level input current	I_{IL} (N1)	VN1 = 0 V	–130	–100		μA
N2 Pin						
High-level input voltage	V_{IH} (N2)		2.0		VREG	V
Low-level input voltage	V_{IL} (N2)		0		1.0	V
Input open voltage	V_{IO} (N2)		VREG – 0.5		VREG	V
High-level input current	I_{IH} (N2)	VN2 = VREG	–10	0	+10	μA
Low-level input current	I_{IL} (N2)	VN2 = 0 V	–130	–100		μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

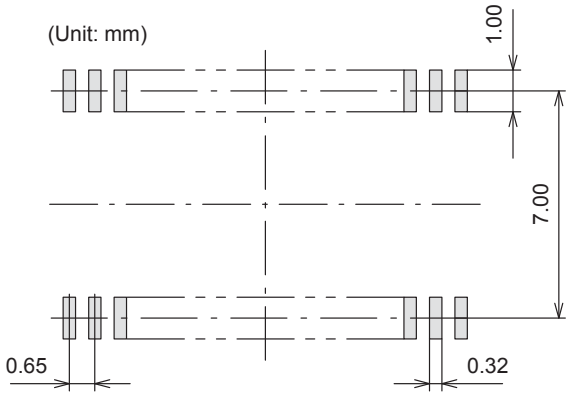
Package Dimensions

unit : mm

SSOP30 (275mil)
CASE 565AT
ISSUE A



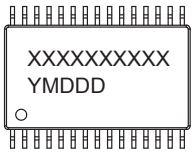
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

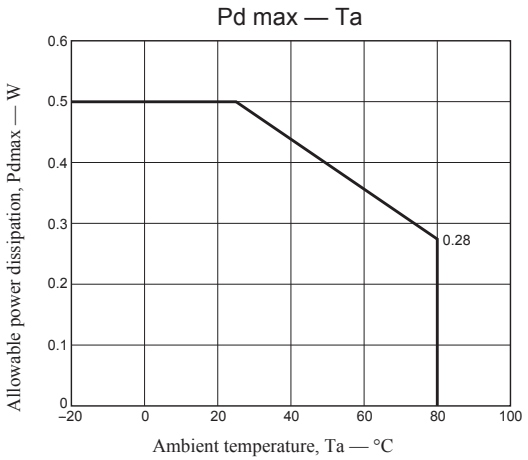
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.



Truth Table

•Three-Phase Logic Truth Table ("IN = 'H'" indicates the state where IN+ > IN–.)

	F/R = L			F/R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	Source	Sink
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

•S/S Pin

Input state	State
H	Stop
L	Start

•PWMIN Pin

Input state	State
High or open	Output off
L	Output on

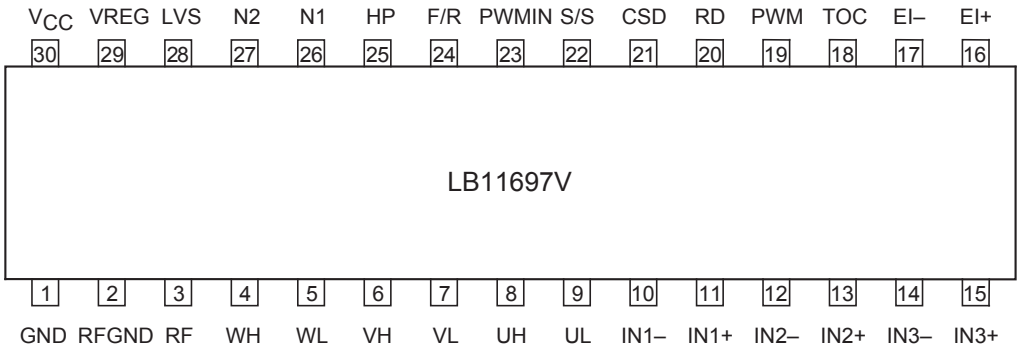
•N1 and N2 Pins

Input state		HP output
N1 pin	N2 pin	
L	L	Single Hall sensor period divided by 2
L	High or open	Single Hall sensor period
High or open	L	Three Hall sensor synthesized period divided by 2
High or open	High or open	Three Hall sensor synthesized period

Since the S/S pin does not have an internal pull-up resistor, an external pull-up resistor or equivalent is required to set the IC to the stop state. If either the S/S or PWMIN pins are not used, the unused pin input must be set to the low-level voltage.

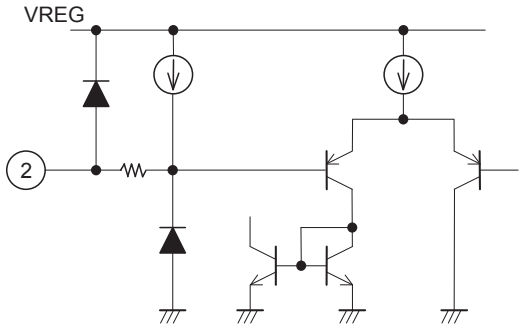
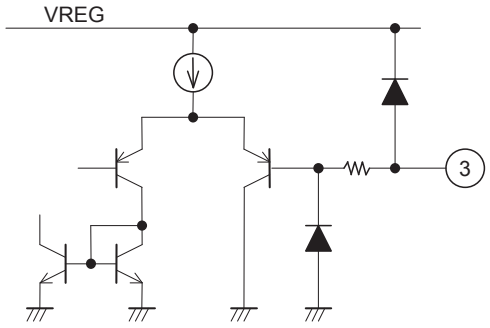
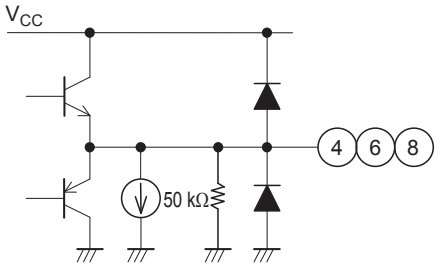
The HP output can be selected (by the N1 and N2 settings) to be one of the following four functions: the IN1 Hall input converted to a pulse output (one-Hall output), the one-Hall output divided by two, the three-phase output synthesized from the Hall inputs (three-Hall synthesized output) or the three-Hall synthesized output divided by two.

Pin Assignment



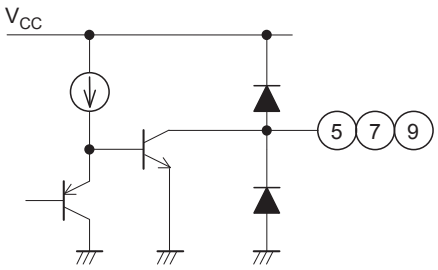
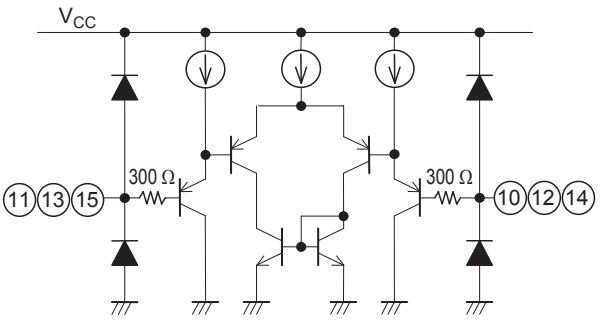
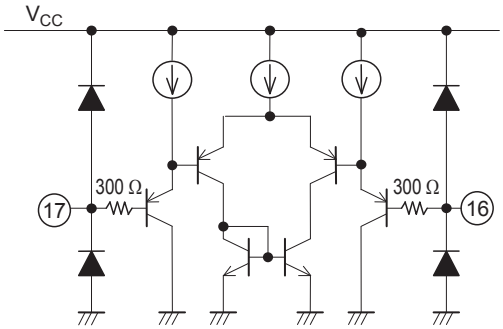
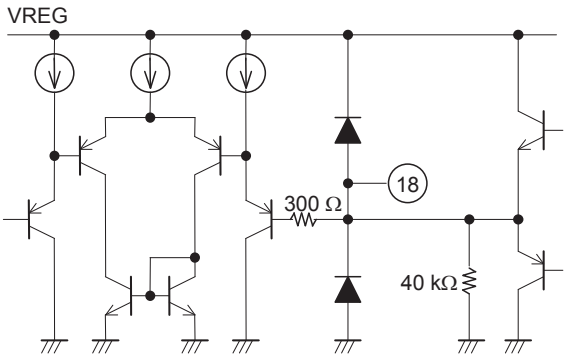
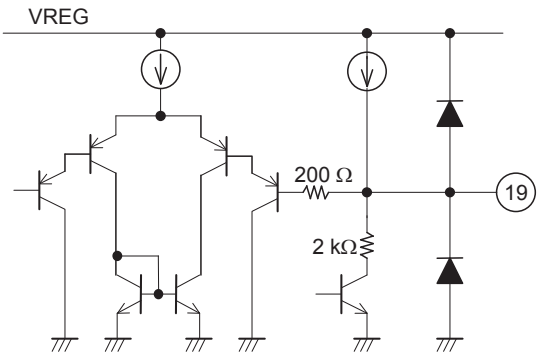
Top view

Pin Functions

Pin No.	Symbol	Pin Description	Equivalent circuit
1	GND	Ground	
2	RF GND	Output current detection reference Connect the ground terminal of the external resistor RF to this pin.	
3	RF	Output current detection Connect a resistor with a small value between this pin and RFGND. This sets the maximum output current I_{OUT} to be 0.25/Rf.	
4 6 8	WH VH UH	Outputs (External transistor drive outputs) These are the PWM outputs used for duty control. These are push-pull outputs.	

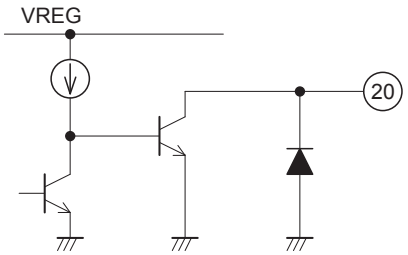
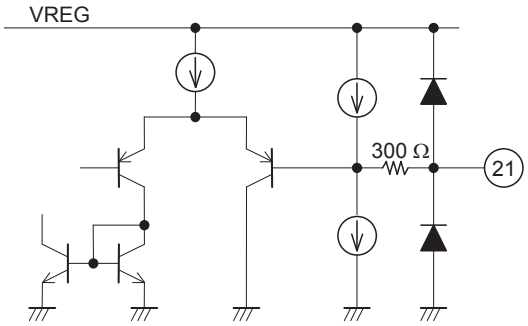
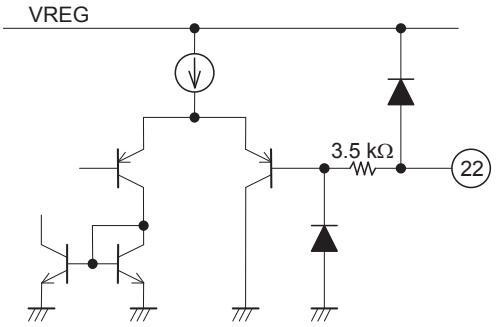
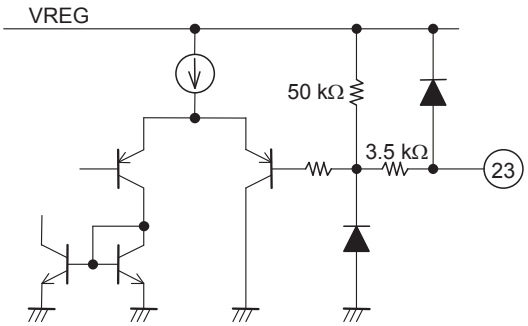
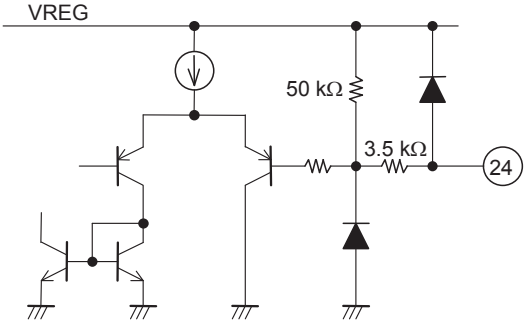
Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Pin Description	Equivalent circuit
5 7 9	WL VL UL	Outputs (External transistor drive outputs) These are open-collector outputs.	
10 11 12 13 14 15	IN1– IN1+ IN2– IN2+ IN3– IN3+	Hall sensor inputs A high-level state is recognized when IN+ > IN–, and a low-level state is recognized under the reverse condition. If noise on the Hall sensor signals becomes a problem, insert capacitors between the IN+ and IN– inputs.	
16 17	EI+ EI–	Control amplifier inputs The PWMIN pin must be held at the low level for control using this pin to function.	
18	TOC	Control amplifier output When the TOC pin voltage rises, the IC changes the UH, VH, and WH output signal PWM duty to increase the torque output.	
19	PWM	Shared function pin: PWM oscillator frequency setting and initial reset pulse generation Insert a capacitor between this pin and ground. A capacitor of 2000 pF sets a frequency of about 22 kHz.	

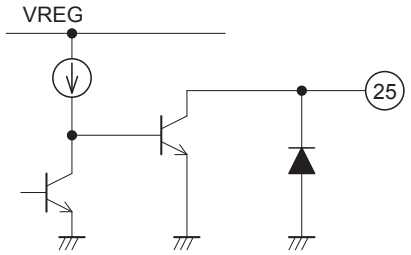
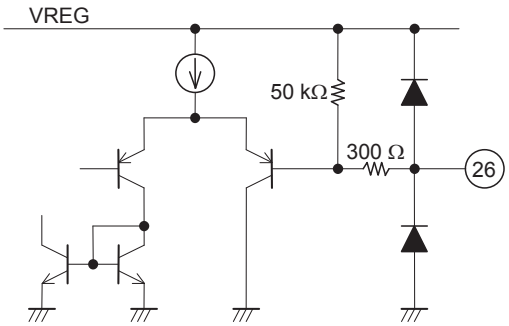
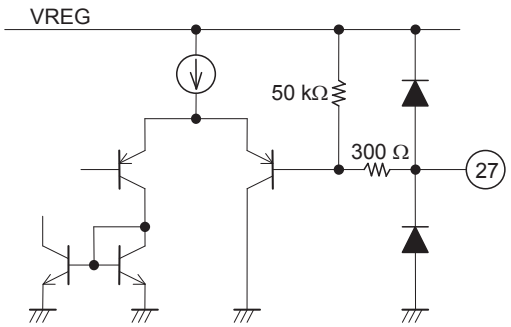
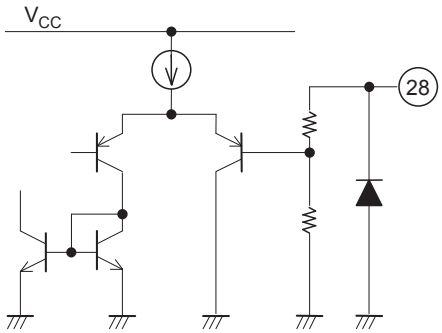
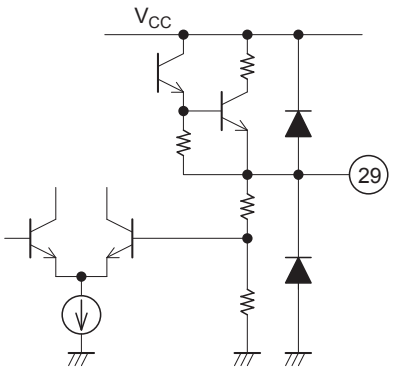
Continued on next page.

Continued from preceding page.

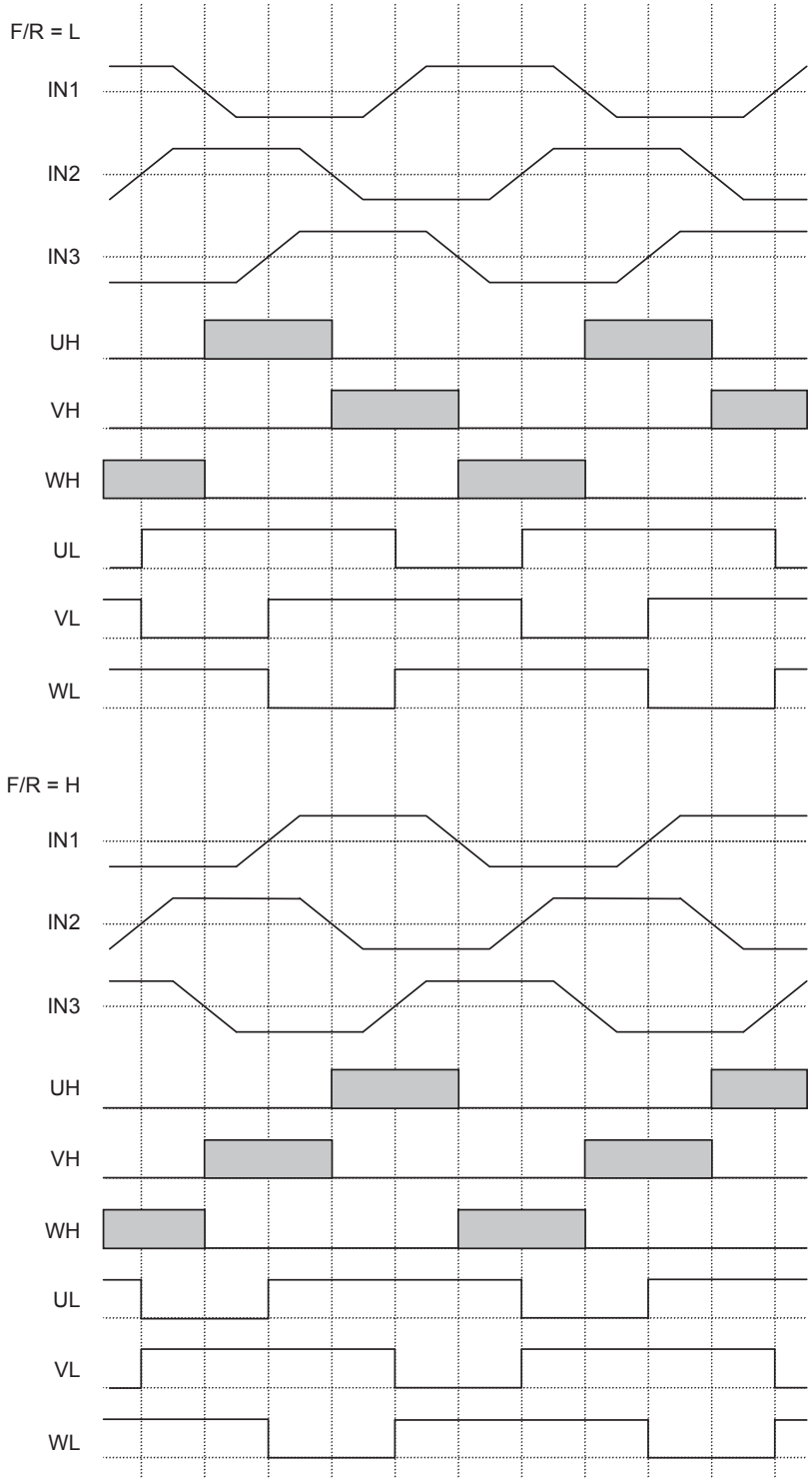
Pin No.	Pin Name	Pin Description	Equivalent circuit
20	RD	Motor constraint detection output This pin output is on when the motor is turning and off when the constraint protection circuit operates.	
21	CSD	Constraint protection circuit operating time setting Insert a capacitor between this pin and ground. This pin must be connected to ground if the constraint protection circuit is not used.	
22	S/S	Start/Stop input A low-level input sets the IC to start mode, and a high-level input sets it to stop mode.	
23	PWM IN	PWM pulse input A low-level input specifies the output drive state, and a high-level or open input specifies the output off state. When this pin is used for control, the TOC pin voltage must be set to a control amplifier input that results in a 100% duty.	
24	F/R	Forward/reverse input	

Continued on next page.

Continued from preceding page.

Pin No.	Pin Name	Pin Description	Equivalent circuit
25	HP	Hall signal output One of four output types is selected by the N1 and N2 pin settings.	
26	N1	Hall signal output (HP signal) type selector	
27	N2	Hall signal output (HP signal) type selector	
28	LVS	Undervoltage protection voltage detection If a 5 V or higher supply voltage is to be detected, set the detection voltage by inserting an appropriate zener diode in series.	
29	VREG	Stabilized power supply output (5 V output) Insert a capacitor (about 0.1 μF) between this pin and ground for stabilization.	
30	V_{CC}	Power supply. Insert a capacitor between this pin and ground for stabilization.	

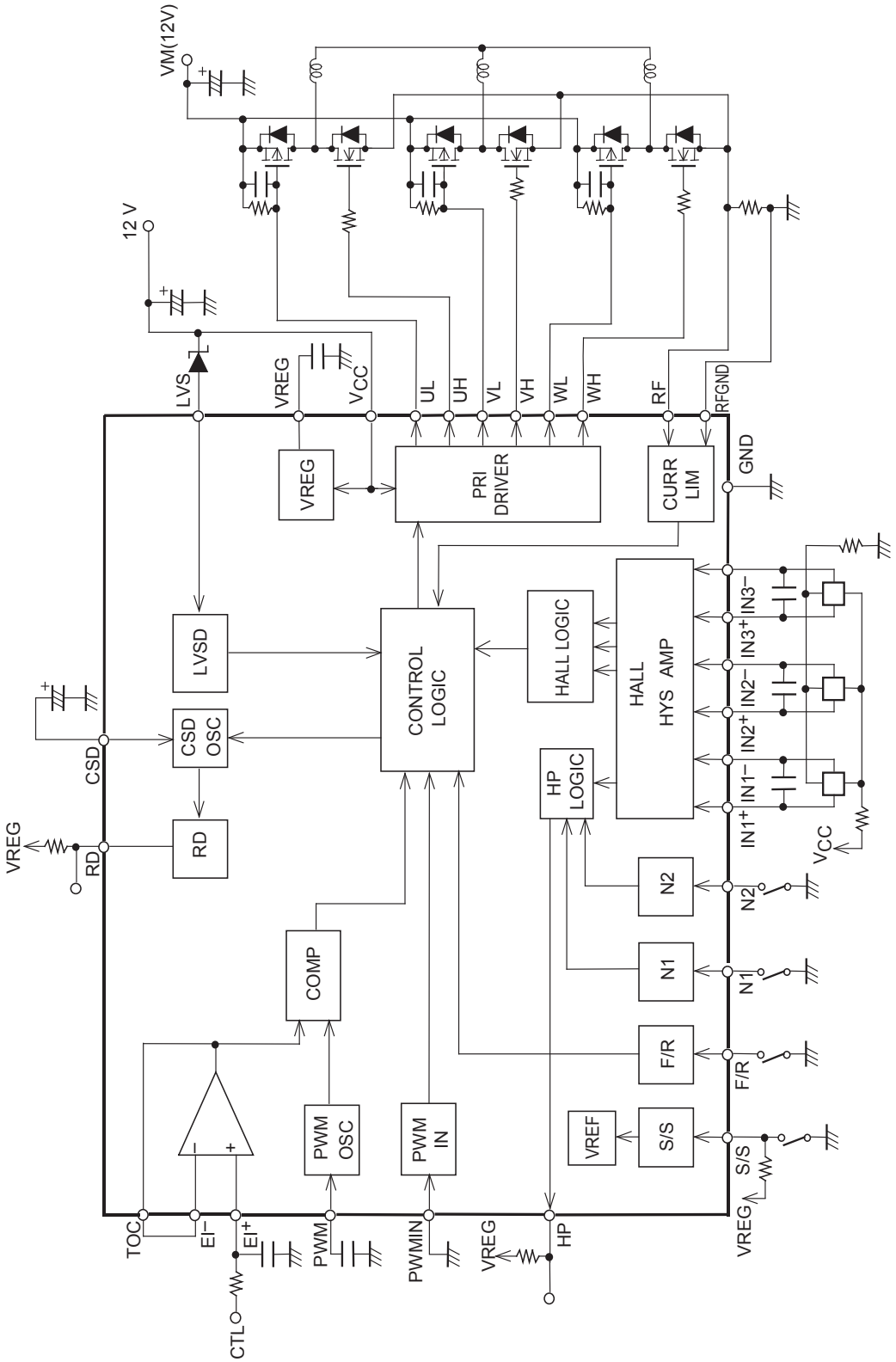
Hall Sensor Signal Input/Output Timing Chart



Areas shown in gray ( ) indicate PWM output.

Application Circuit Examples

MOS transistor drive (low side PWM) using a 12 V power supply



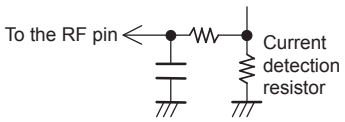
LB11697V Functional Description

1. Output Drive Circuit

The LB11697V adopts direct PWM drive to minimize power loss in the outputs. The output transistors are always saturated when on, and the motor drive power is adjusted by changing the on duty of the output. The output PWM switching is performed on the UH, VH, and WH outputs. The output PWM switching is performed using the UH, VH, and WH outputs, which are external low side transistor drive outputs. Since the reverse recovery time for the diodes connected to the non-PWM side outputs can be a problem, care is required in selecting these diodes. (If diodes with a short reverse recovery time are not used, through currents will flow at the instant the PWM side transistors are turned on.)

2. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation I = VFR/Rf (VRF = 0.25 V typical, Rf: current detection resistor). This circuit suppresses the output current by reducing the output on duty.

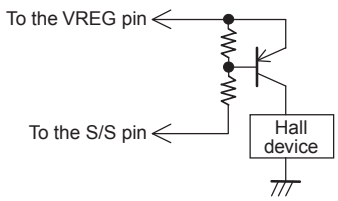


High-precision detection can be implemented by connecting the lines from the RF and RFGND pins close to the two terminal of the current detection resistor Rf.

The current limiter circuit includes an internal filter circuit to prevent incorrect current limiter circuit operation due to detecting the output diode reverse recovery current due to PWM operation. Although there should be no problems with the internal filter circuit in normal applications, applications should add an external filter circuit (such as an RC low-pass filter) if incorrect operation occurs (if the diode reverse recovery current flows for longer than 1 μs).

3. Power Saving Circuit

This IC goes to a low-power mode (power saving state) when set to the stop state with the S/S pin. In the power saving state, the bias currents in most of the circuits are cut off. However, the 5 V regulator output (VREG) is still provided in the power saving state. If it is also necessary to cut the Hall device bias current, this function can be provided by an application that, for example, connects the Hall devices to 5 V through PNP transistors.



4. Notes on the PWM Frequency

The PWM frequency is determined by the capacitor C (F) connected to the PWM pin.

$$f_{PWM} \approx 1/(22500 \times C)$$

If a 2000 pF capacitor is used, the circuit will oscillate at about 22 kHz. If the PWM frequency is too low, switching noise will be audible from the motor, and if it is too high, the output power loss will increase. Thus a frequency in the range 15 to 50 kHz must be used. The capacitor's ground terminal must be placed as close as possible to the IC's ground pin to minimize the influence of output noise and other noise sources.

5. Control Methods

The output duty can be controlled by either of the following methods

• Control based on comparing the TOC pin voltage to the PWM oscillator waveform

The low side output transistor duty is determined according to the result of comparing the TOC pin voltage to the PWM oscillator waveform. When the TOC pin voltage is 1.4 V or lower, the duty will be 0%, and when it is 3.0 V or higher, the duty will be 100%.

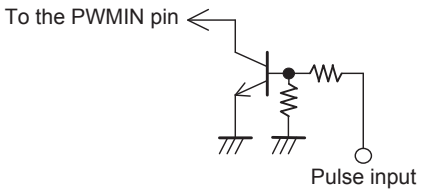
Since the TOC pin is the output of the control amplifier (CTL), a control voltage cannot be directly input to the TOC pin. Normally, the control amplifier is used as a full feedback amplifier (with the EI- pin connected to the TOC pin) and a DC voltage is input to the EI+ pin (the EI+ pin voltage will become equal to the TOC pin voltage). When the EI+ pin voltage becomes higher, the output duty increases. Since the motor will be driven when the EI+ pin is in the open state, a pull-down resistor must be connected to the EI+ pin if the motor should not operate when EI+ is open.

When TOC pin voltage control is used, a low-level input must be applied to the PWMIN pin or that pin connected to ground.

- Pulse Control Using the PWMIN Pin

  A pulse signal can be input to the PWMIN pin, and the output can be controlled based on the duty of that signal. Note that the output is on when a low level is input to the PWMIN pin, and off when a high level is input. When the PWMIN pin is open it goes to the high level and the output is turned off. If inverted input logic is required, this can be implemented with an external transistor (npn).

  When controlling motor operation from the PWMIN pin, the EI– pin must be connected to ground, and the EI+ pin must be connected to the TOC pin.



  Note that since the PWM oscillator is also used as the clock for internal circuits, a capacitor (about 2000 pF) must be connected to the PWM pin even if the PWMIN pin is used for motor control.

6. Hall Input Signals

A signal input with an amplitude in excess of the hysteresis (80 mV maximum) is required for the Hall inputs. Considering the possibility of noise and phase displacement, an even larger amplitude is desirable.

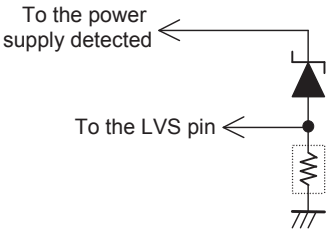
If disruptions to the output waveforms (during phase switching) or to the HP output (Hall signal output) occur due to noise, this must be prevented by inserting capacitors across the inputs. The constraint protection circuit uses the Hall inputs to discriminate the motor constraint state. Although the circuit is designed to tolerate a certain amount of noise, care is required when using the constraint protection circuit.

If all three phases of the Hall input signal system go to the same input state, the outputs are all set to the off state (the UL, VL, WL, UH, VH, and WH outputs all go to the low level).

If the outputs from a Hall IC are used, fixing one side of the inputs (either the + or – side) at a voltage within the common-mode input voltage range allows the other input side to be used as an input over the 0 V to V_{CC} range.

7. Undervoltage Protection Circuit

The undervoltage protection circuit turns one side of the outputs (UH, VH, and WH) off when the LVS pin voltage falls below the minimum operation voltage (see the Electrical Characteristics). To prevent this circuit from repeatedly turning the outputs on and off in the vicinity of the protection operating voltage, this circuit is designed with hysteresis. Thus the output will not recover until the operating voltage rises 0.5 V (typical).



The protection operating voltage detection level is set up for 5 V systems. The detected voltage level can be increased by shifting the voltage by inserting a zener diode in series with the LVS pin to shift the detection level. The LVS influx current during detection is about 75 µA. To increase the diode current to stabilize the zener diode voltage rise, insert a resistor between the LVS pin and ground.

If the LVS pin is left open, the internal pull-down resistor will result in the IC seeing a ground level input, and the output will be turned off. Therefore, a voltage in excess of the LVS circuit clear voltage (about 4.4 V) must be applied to the LVS pin if the application does not use the undervoltage protection circuit. The maximum rating for the LVS pin applied voltage is 18 V.

8. Constraint Protection Circuit

When the motor is physically constrained (held stopped), the CSD pin external capacitor is charged (to about 3.0 V) by a constant current of about 2.25 µA and is then discharged (to about 1.0 V) by a constant current of about 0.15 µA. This process is repeated, generating a sawtooth waveform. The constraint protection circuit turns motor drive on and off repeatedly based on this sawtooth waveform. (The UH, VH, and WH side outputs are turned on and off.) Motor drive is on during the period the CSD pin external capacitor is being charged from about 1.0 V to about 3.0 V, and motor drive is off during the period the CSD pin external capacitor is being discharged from about 3.0 V to about 1.0 V. The IC and the motor are protected by this repeated drive on/off operation when the motor is physically constrained.

The motor drive on and off times are determined by the value of the connected capacitor C (in µF).

TCSD1 (drive on period) ≈ 0.89 × C (seconds)

TCSD2 (drive off period) ≈ 13.3 × C (seconds)

When a 0.47 µF capacitor is connected externally to the CSD pin, this iterated operation will have a drive on period of about 0.4 seconds and a drive off period of about 6.3 seconds.

While the motor is turning, the discharge pulse signal (generated once for each Hall input period) that is created by combining the Hall inputs internally in the IC discharges the CSD pin external capacitor. Since the CSD pin voltage does not rise, the constraint protection circuit does not operate.

When the motor is physically constrained, the Hall inputs do not change and the discharge pulses are not generated. As a result, the CSD pin external capacitor is charged by a constant current of 2.25 μA to about 3.0 V, at which point the constraint protection circuit operates. When the constraint on the motor is released, the constraint protection function is released.
Connect the CSD pin to ground if the constraint protection circuit is not used.

9. Forward/Reverse Direction Switching

This IC is designed so that through currents (due to the output transistor off delay time when switching) do not flow in the output when switching directions when the motor is turning. However, if the direction is switched when the motor is turning, current levels in excess of the current limiter value may flow in the output transistors due to the motor coil resistance and the motor back EMF state when switching. Therefore, designers must consider selecting external output transistors that are not destroyed by those current levels or only switching directions after the speed has fallen below a certain speed.

10. Handling Different Power Supply Types

When this IC is operated from an externally supplied 5 V power supply (4.5 to 5.5 V), short the V_{CC} pin to the VREG pin and connect them to the external power supply.
When this IC is operated from an externally supplied 12 V power supply (8 to 17 V), connect the V_{CC} pin to the power supply. (The VREG pin will generate a 5 V level to function as the control circuit power supply.)

11. Power Supply Stabilization

Since this IC uses a switching drive technique, the power supply line level can be disturbed easily. Therefore capacitors with adequate capacitance to stabilize the power supply line must be inserted between V_{CC} and ground.
If diodes are inserted in the power supply lines to prevent destruction if the power supply is connected with reverse polarity, the power supply lines are even more easily disrupted, and even larger capacitors are required.
If the power supply is turned on and off by a switch, and if there is a significant distance between that switch and the stabilization capacitor, the supply voltage can be disrupted significantly by the line inductance and surge current into the capacitor. As a result, the withstand voltage of the device may be exceeded. In application such as this, the surge current must be suppressed and the voltage rise prevented by not using ceramic capacitors with a low series impedance, and by using electrolytic capacitors instead.

12. VREG Stabilization

To stabilize the VREG voltage, which is the control circuit power supply, a 0.1 μF or larger capacitor must be inserted between the VREG pin and ground. The ground side of this capacitor must connected to the IC ground pin with a line that is as short as possible.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LB11697V-TLM-E	SSOP30 (275mil) (Pb-Free)	1000 / Tape & Reel
LB11697V-W-AH	SOP30 (275mil) (Pb-Free / Halogen Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF