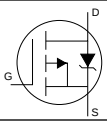


Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.039	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.27	Ω	$V_{GS} = -10V$, $I_D = -1.2A$ ③
		—	—	0.45		$V_{GS} = -4.5V$, $I_D = -0.60A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	0.92	—	—	S	$V_{DS} = -10V$, $I_D = -0.60A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	-1.0	μA	$V_{DS} = -24V$, $V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
Q_g	Total Gate Charge	—	7.5	11	nC	$I_D = -1.2A$
Q_{gs}	Gate-to-Source Charge	—	1.3	1.9		$V_{DS} = -24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	2.5	3.7		$V_{GS} = -10V$, See Fig. 6 and 9 ③
$t_{d(on)}$	Turn-On Delay Time	—	9.7	—		$V_{DD} = -15V$
t_r	Rise Time	—	12	—	ns	$I_D = -1.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	19	—		$R_G = 6.2\Omega$
t_f	Fall Time	—	9.3	—		$R_D = 12\Omega$, See Fig. 10 ③
C_{iss}	Input Capacitance	—	180	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	87	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	42	—		$f = 1.0MHz$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.25	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-9.6		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}$, $I_S = -1.2A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	30	45	ns	$T_J = 25^\circ\text{C}$, $I_F = -1.2A$
Q_{rr}	Reverse Recovery Charge	—	37	55	nC	$di/dt = -100A/\mu s$ ③

Notes:

① Repetitive rating – pulse width limited by max. junction temperature (see fig. 11)

② $I_{SD} \leq -1.2A$, $di/dt \leq -140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

③ Pulse width $\leq 300\mu s$ – duty cycle $\leq 2\%$

④ Surface mounted on FR-4 board, $t \leq 10sec$.

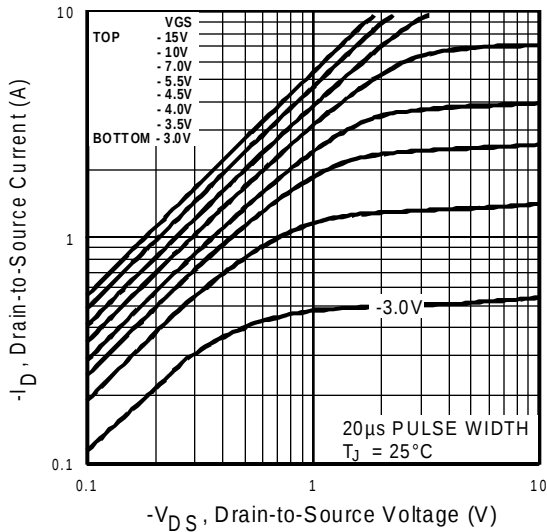


Fig 1. Typical Output Characteristics

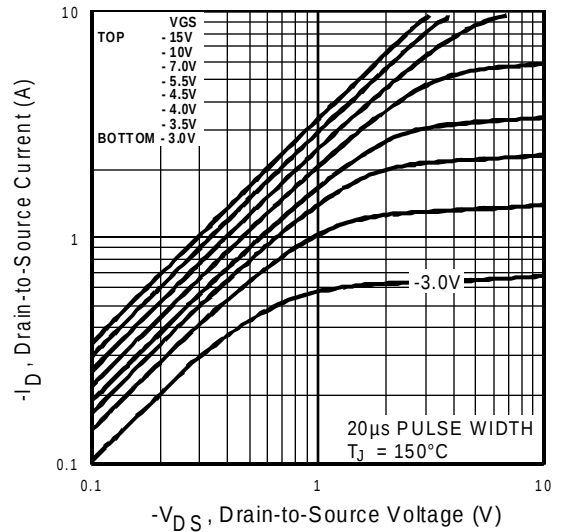


Fig 2. Typical Output Characteristics

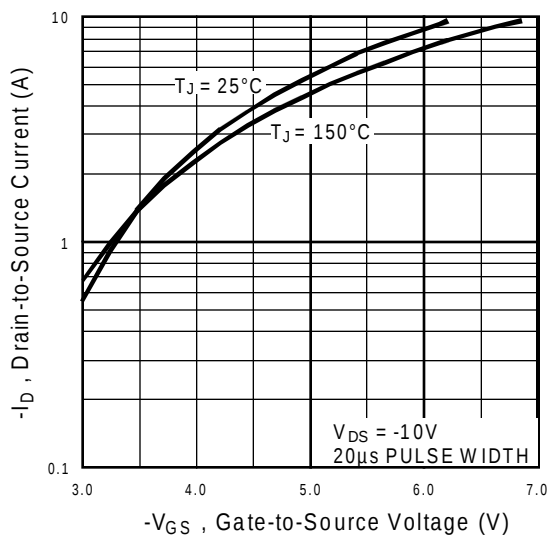


Fig 3. Typical Transfer Characteristics

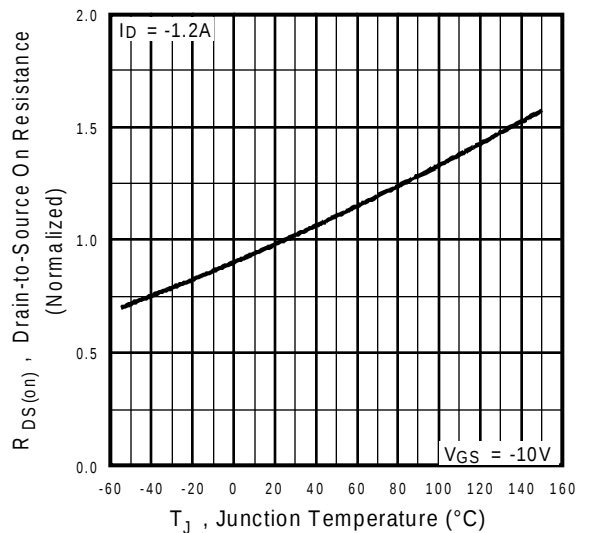


Fig 4. Normalized On-Resistance Vs. Temperature

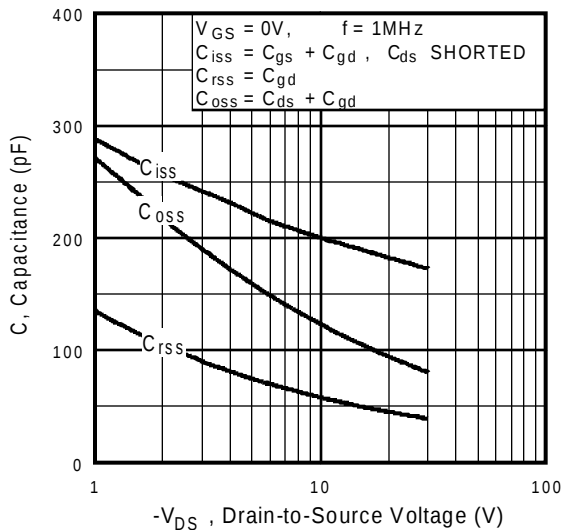


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

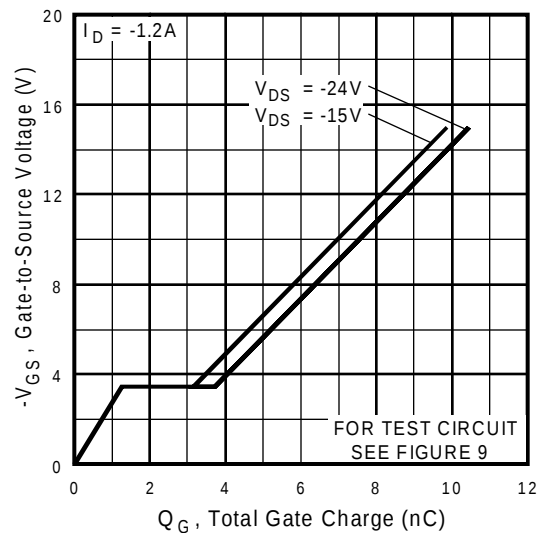


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

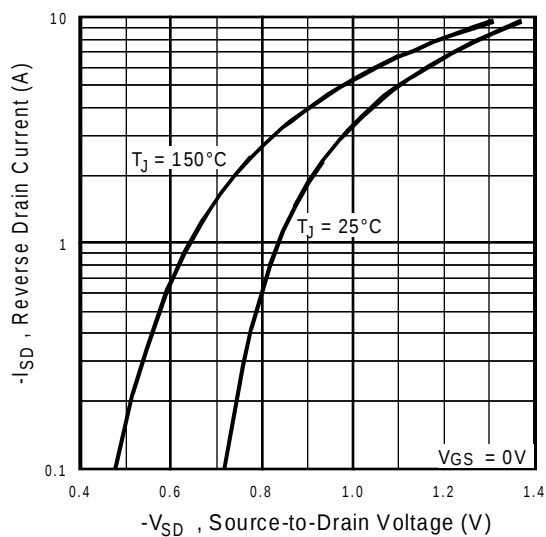


Fig 7. Typical Source-Drain Diode Forward Voltage

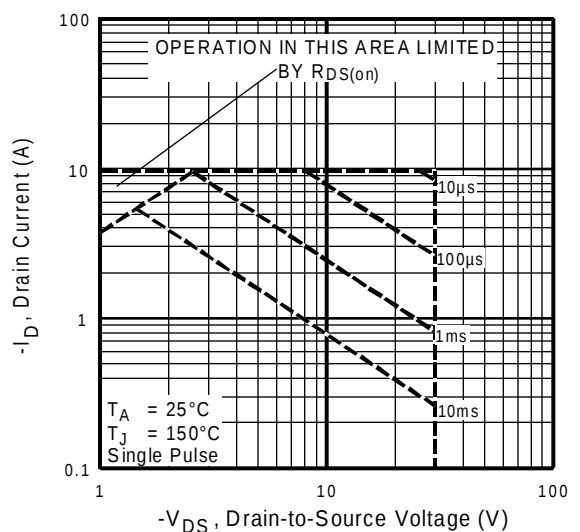


Fig 8. Maximum Safe Operating Area

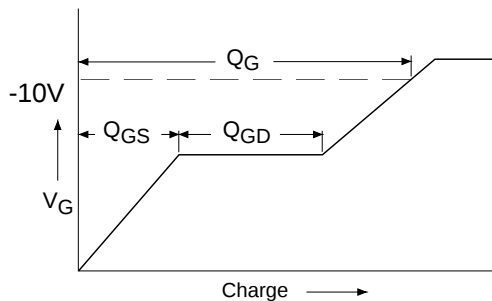


Fig 9a. Basic Gate Charge Waveform

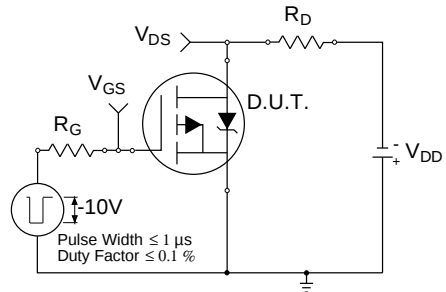


Fig 10a. Switching Time Test Circuit

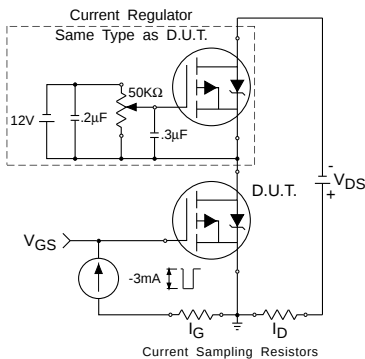


Fig 9b. Gate Charge Test Circuit

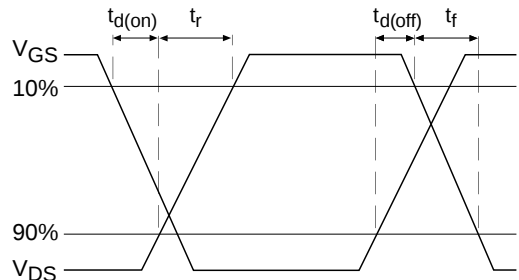


Fig 10b. Switching Time Waveforms

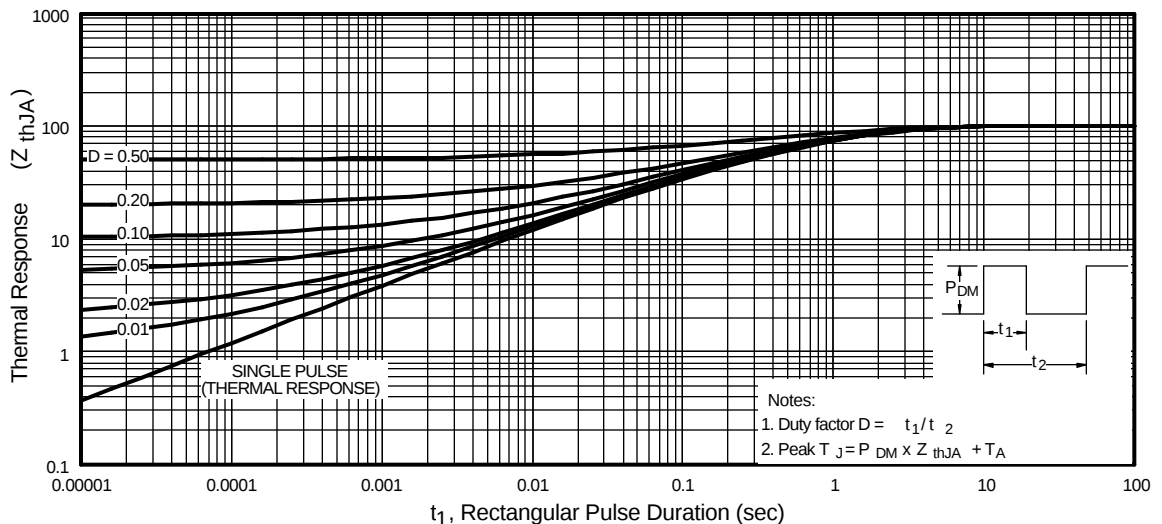


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

The diagram shows a switching circuit for a Device Under Test (D.U.T.). A voltage source V_{GS} is connected to the gate of a MOSFET through a resistor R_G . The MOSFET's source is grounded, and its drain is connected to the D.U.T. The D.U.T. is represented by a circle containing a diode symbol and a switch symbol. The output of the D.U.T. is connected to a load resistor and then to ground. The circuit is labeled with four points of interest: ① at the gate, ② at the drain, ③ at the output, and ④ at the load resistor. A list of circuit layout considerations is provided: Low Stray Inductance, Ground Plane, and Low Leakage Inductance Current Transformer.

Circuit Layout Considerations

- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

① Driver Gate Drive

Period

P.W.

$D = \frac{\text{P.W.}}{\text{Period}}$

$[V_{GS}=10V]$ ***

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current

di/dt

③ D.U.T. V_{DS} Waveform

Re-Applied Voltage

Diode Recovery dv/dt

Body Diode Forward Drop

$[V_{DS}]$

④ Inductor Current

Ripple $\leq 5\%$

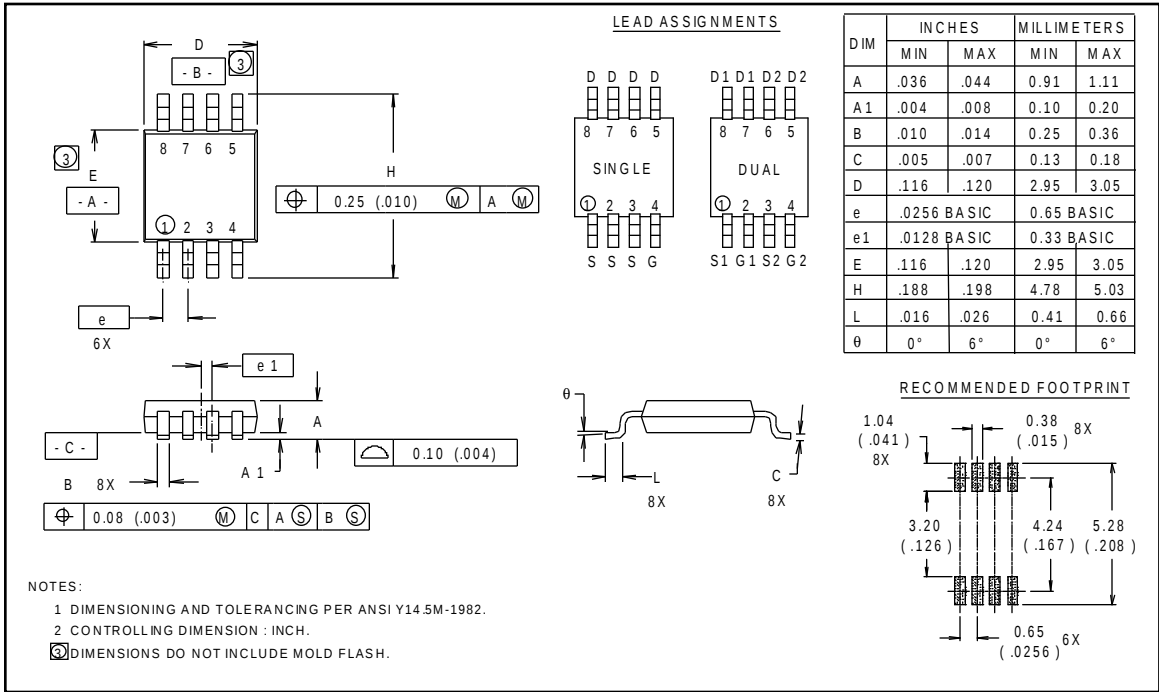
$[I_{SD}]$

Fig 12. For P-Channel HEXFETS

Package Outline

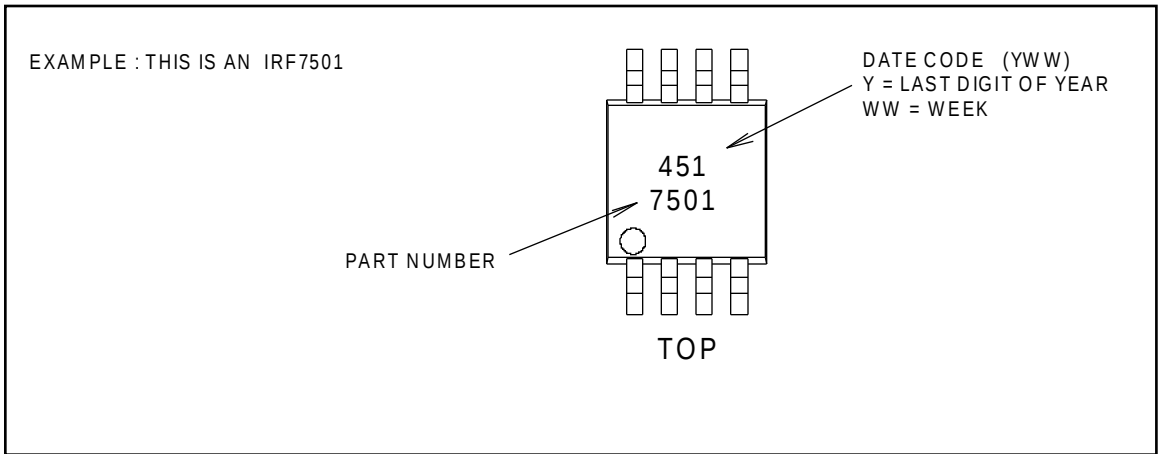
Micro8 Outline

Dimensions are shown in millimeters (inches)



Part Marking Information

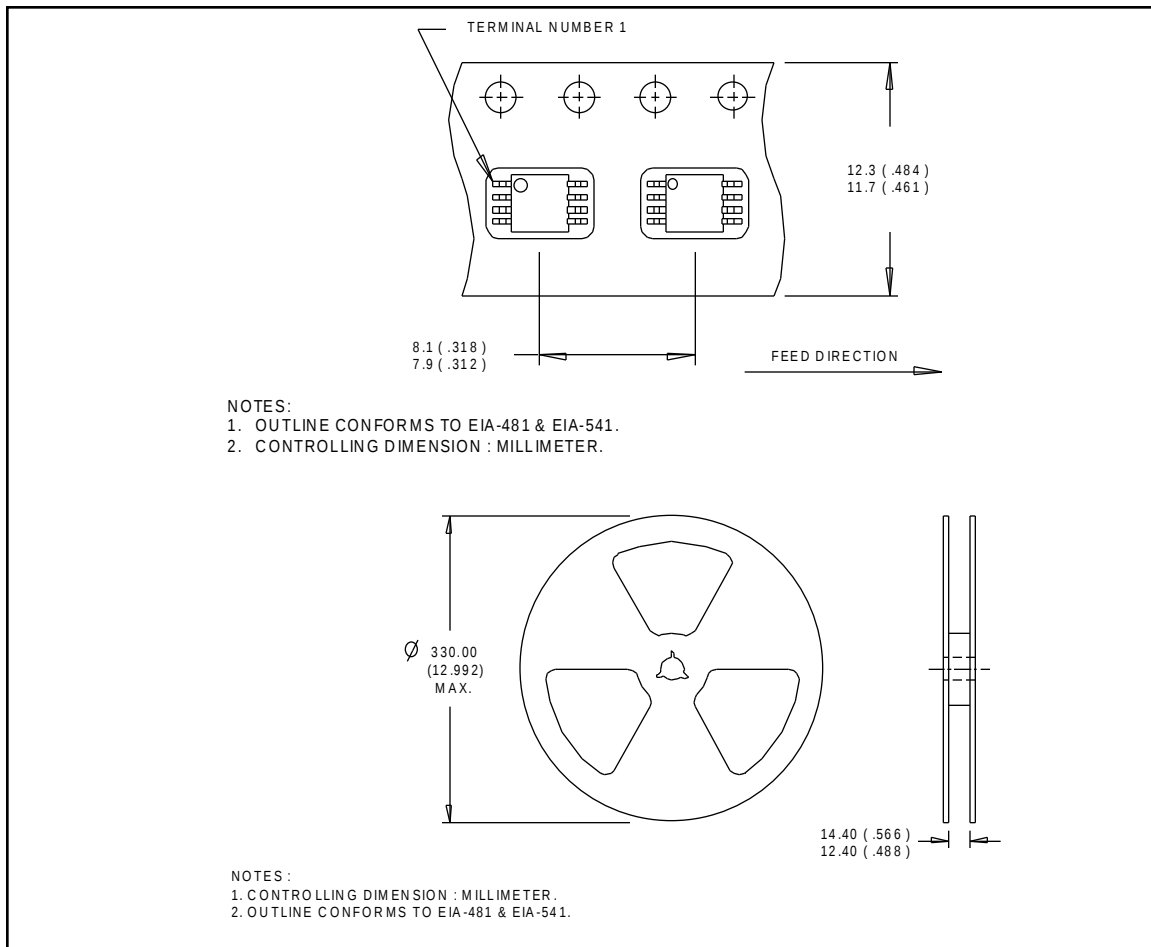
Micro8



Tape & Reel Information

Micro8

Dimensions are shown in millimeters (inches)



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Data and specifications subject to change without notice.

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