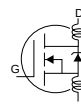
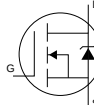


Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.050 0.080	Ω	$V_{GS} = 10V, I_D = 2.4A$ ③ $V_{GS} = 4.5V, I_D = 2.0A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	5.2	—	—	S	$V_{DS} = 15V, I_D = 2.4A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0 25	μA	$V_{DS} = 24V, V_{GS} = 0V$ $V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	25	nC	$I_D = 2.4A$
Q_{gs}	Gate-to-Source Charge	—	—	2.9	nC	$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	7.9	nC	$V_{GS} = 10V$, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time	—	6.8	—	ns	$V_{DD} = 15V$ $I_D = 2.4A$ $R_G = 6.0\Omega$ $R_D = 6.2\Omega$, See Fig. 10 ③
t_r	Rise Time	—	21	—		
$t_{d(off)}$	Turn-Off Delay Time	—	22	—		
t_f	Fall Time	—	7.7	—		
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead tip and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	520	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig. 5
C_{oss}	Output Capacitance	—	180	—		
C_{rss}	Reverse Transfer Capacitance	—	72	—		

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	20		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	$T_J = 25^\circ\text{C}$, $I_S = 1.8A$, $V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	47	71	ns	$T_J = 25^\circ\text{C}$, $I_F = 2.4A$
Q_{rr}	Reverse Recovery Charge	—	56	84	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

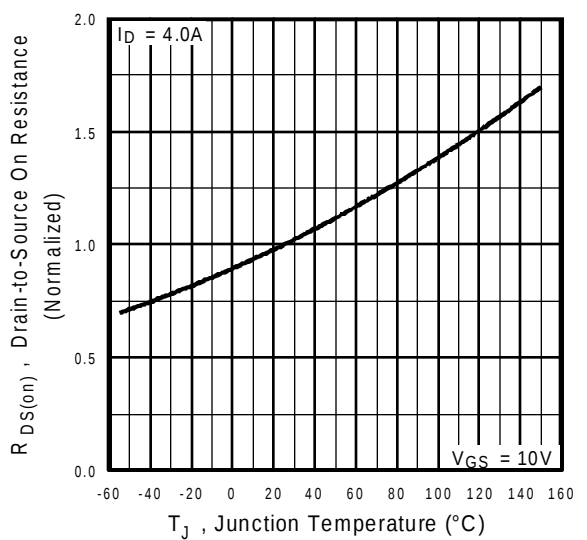
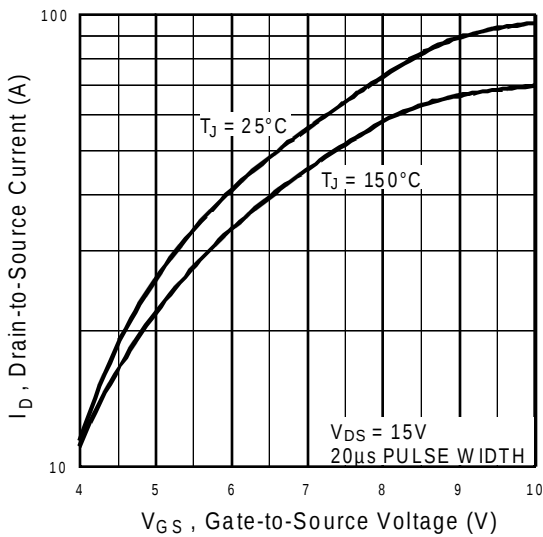
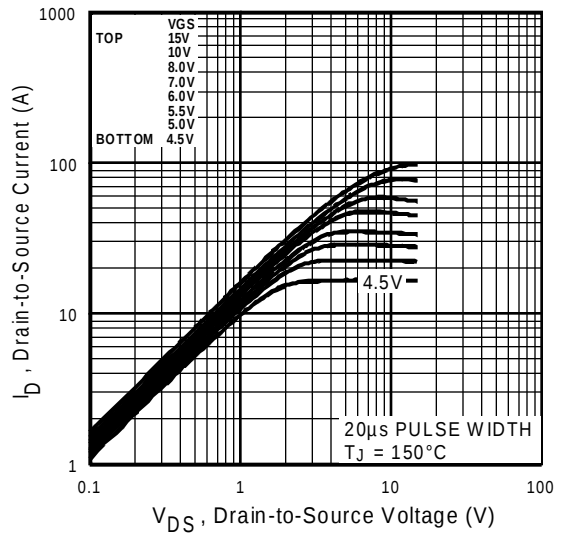
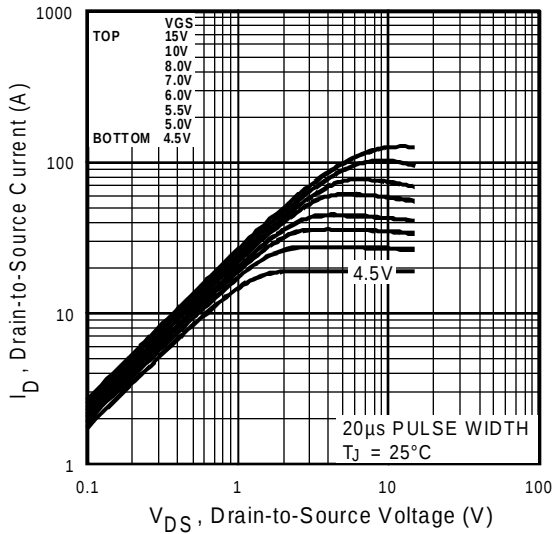
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

② $I_{SD} \leq 2.4A$, $di/dt \leq 73A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$

④ Surface mounted on FR-4 board, $t \leq 10sec$.



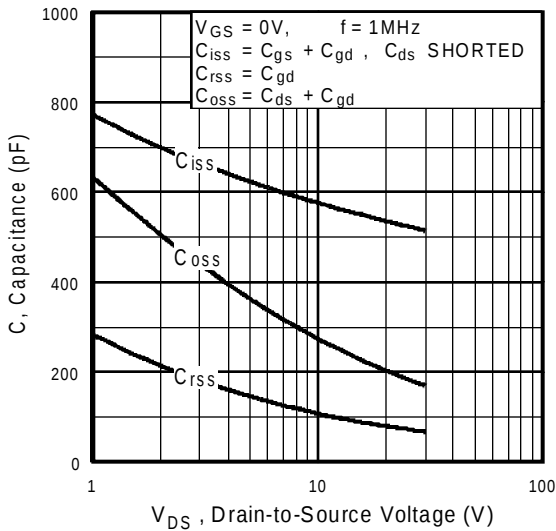


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

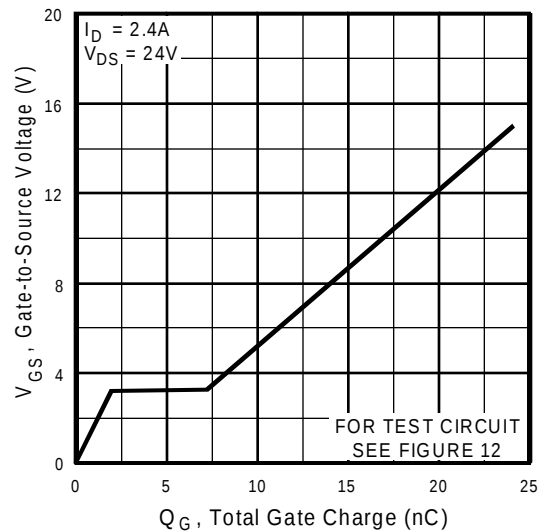


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

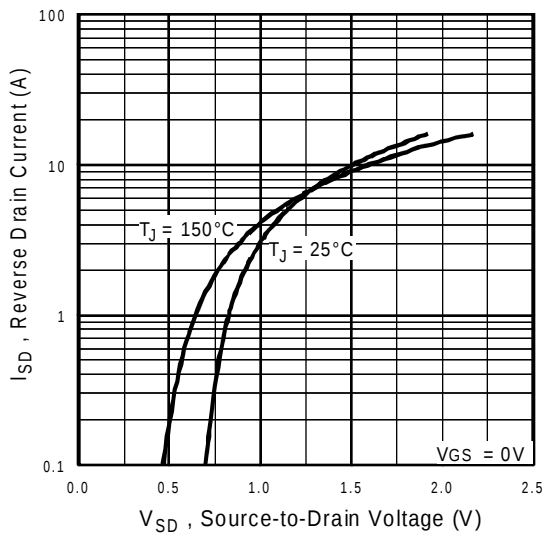


Fig 7. Typical Source-Drain Diode Forward Voltage

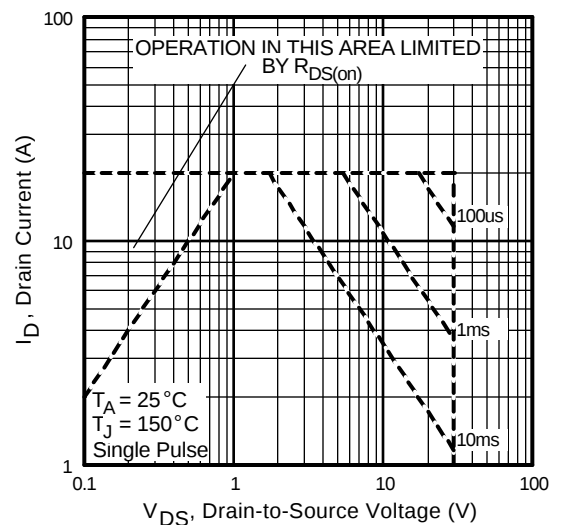


Fig 8. Maximum Safe Operating Area

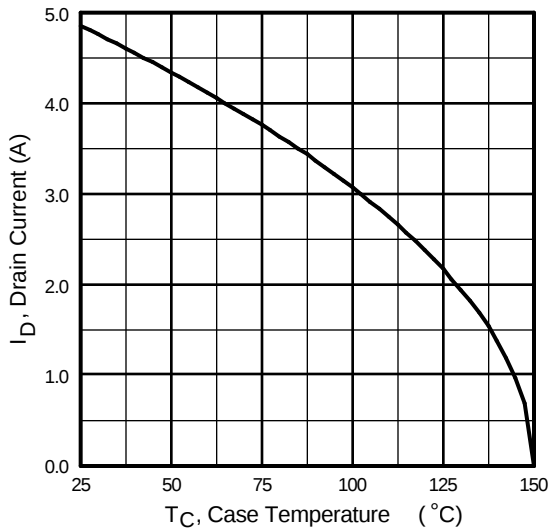


Fig 9. Maximum Drain Current Vs. Ambient Temperature

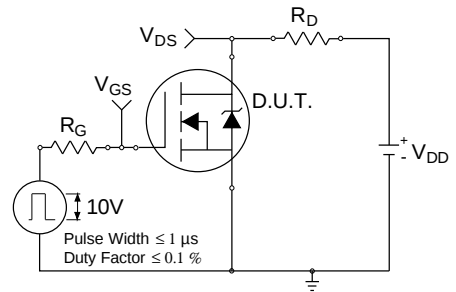


Fig 10a. Switching Time Test Circuit

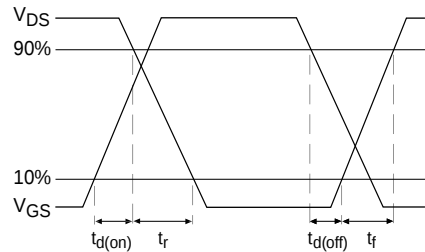


Fig 10b. Switching Time Waveforms

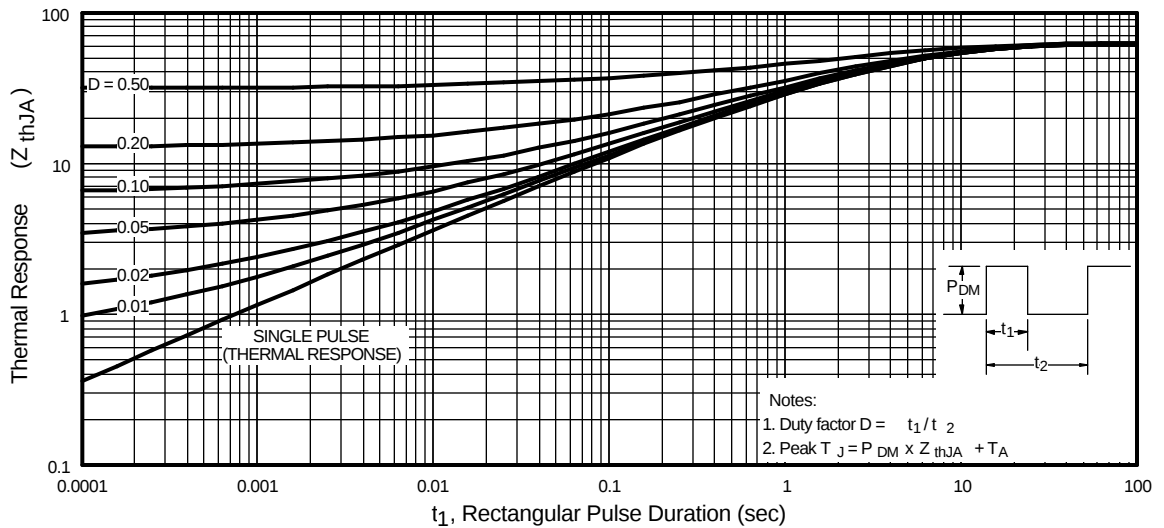


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

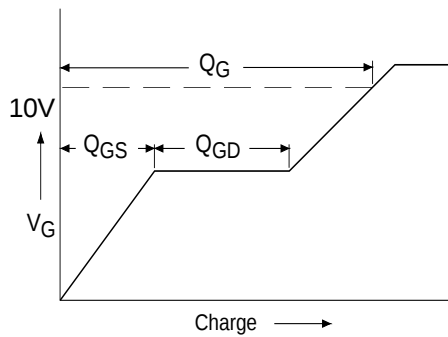


Fig 12a. Basic Gate Charge Waveform

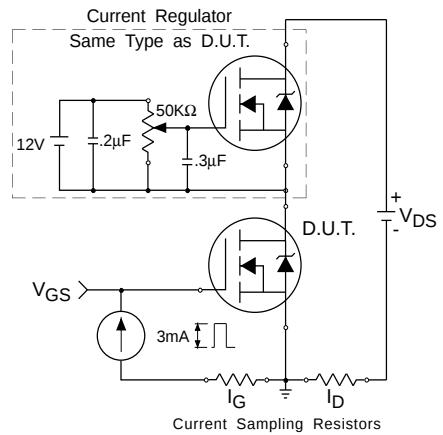
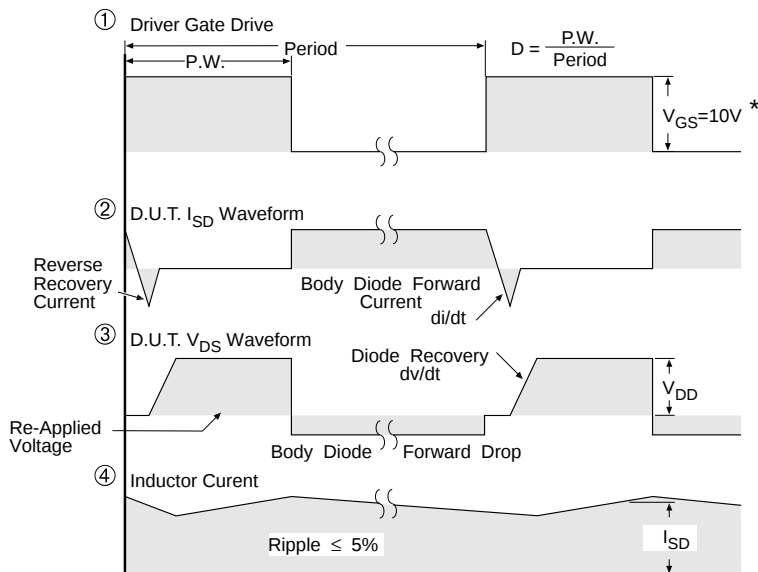
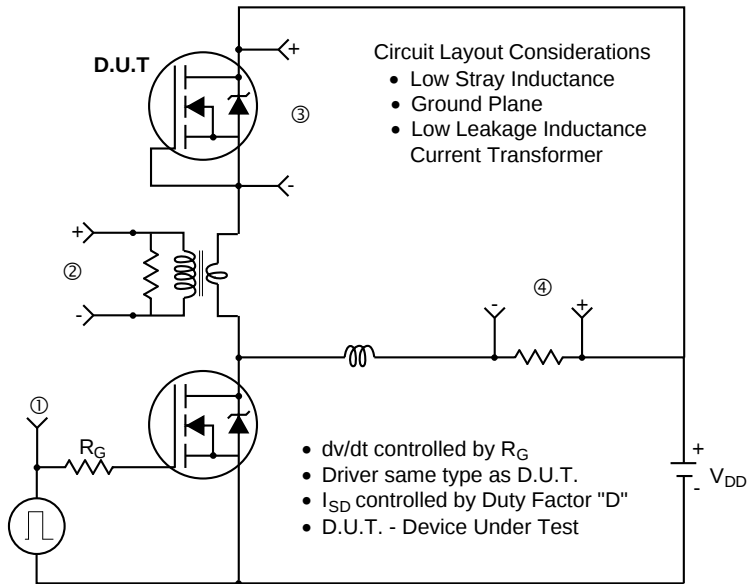


Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

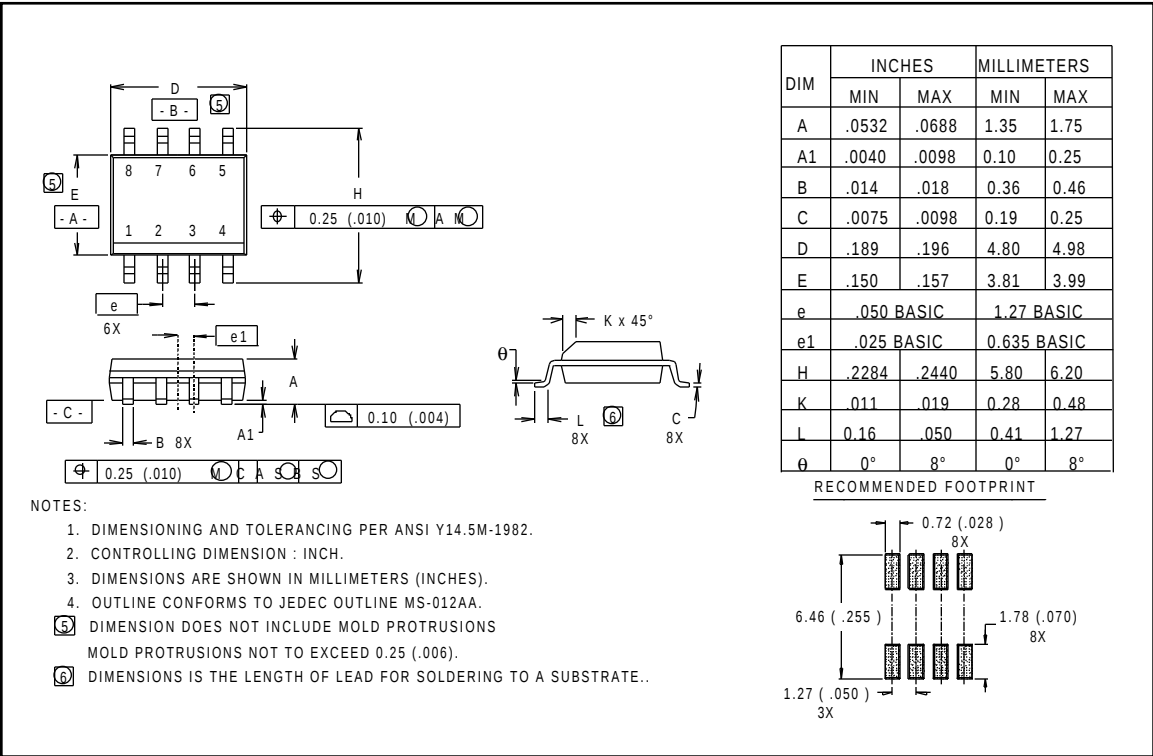


* $V_{GS} = 5V$ for Logic Level Devices

Fig 13.For N-Channel HEXFETS

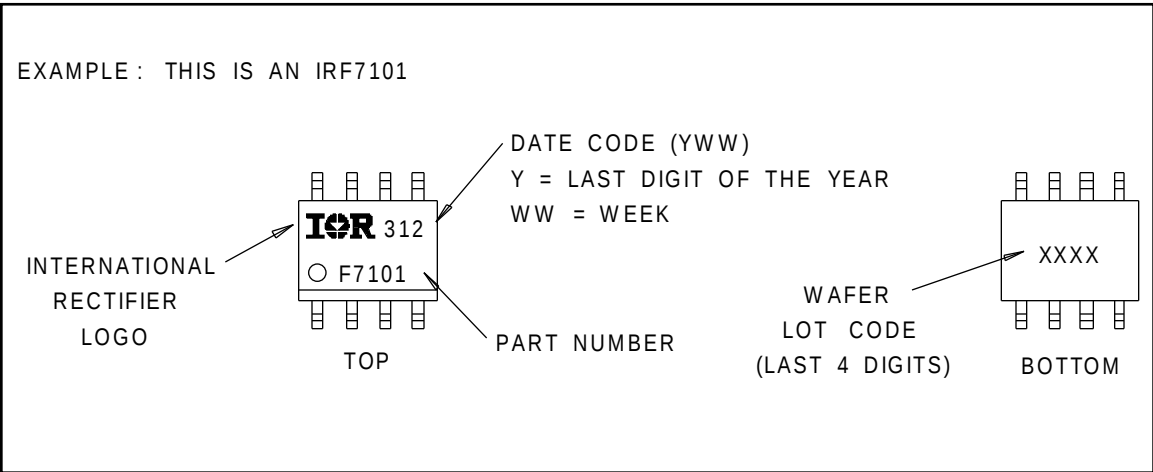
Package Outline

SO8 Outline



Part Marking Information

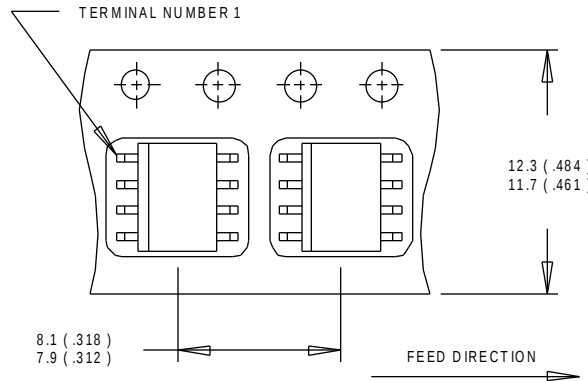
SO8



Tape & Reel Information

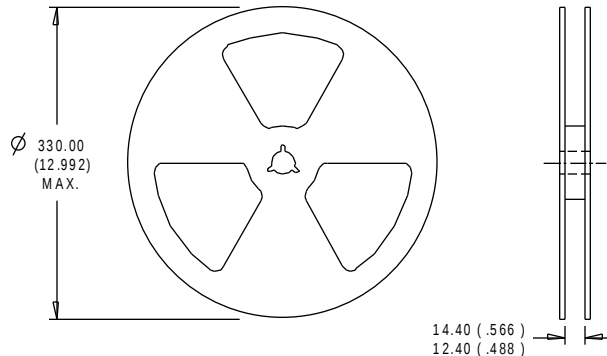
SO8

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

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WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, Tel: (310) 322 3331

EUROPEAN HEADQUARTERS: Hurst Green, Oxted, Surrey RH8 9BB, UK Tel: ++ 44 1883 732020

IR CANADA: 7321 Victoria Park Ave., Suite 201, Markham, Ontario L3R 2Z8, Tel: (905) 475 1897

IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 11 451 0111

IR FAR EAST: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo Japan 171 Tel: 81 3 3983 0086

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Data and specifications subject to change without notice.

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