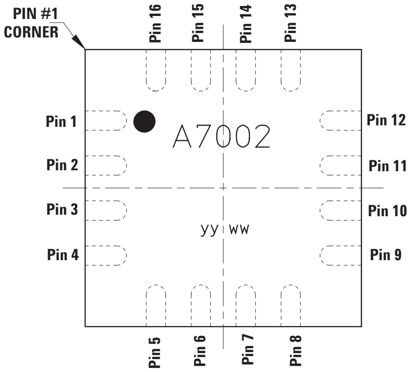


Figure 2. HSDL-7002 Pin Configuration

Order Information

Part Number	Packaging Type	Quantity
HSDL-7002	Tape and Reel	2500

Marking Information

The unit is marked with A7002 and 'yyww' on the chip.

yy = year
ww = work week

I/O Pins Configuration Table

	Name	Type	Function
1	TXD	Digital In	Negative edge triggered input signal that is normally tied to the SOUT signal of the UART (serial data to be transmitted). Data is modulated and output as IR_TXD.
2	RXD	Digital Out	Output signal normally tied to SIN signal of a UART (received serial data). RXD is the demodulated output of IR_RXD.
3	A0	Digital In	Clock Multiplex Signal
4	A1	Digital In	Clock Multiplex Signal
5	A2	Digital In	Clock Multiplex Signal
6	CLK_SEL	Digital In	Used to activate either the internal or external clock. A high on this line activated the external clock (16XCLK) and a low activates the internal clock. When the external clock is activated, the internal oscillator is put in POWERDN mode.
7	GND		Chip Ground
8	NRST	Digital In	Activate low signal used to reset the IrDA® SIR Encode & Decode state machine. This signal can be tied to POR (Power-On-Reset) or Vcc.
9	IR_RXD	Digital In	Input from SIR optoelectronics. Input signal is a 3/16th or 1.63 ms pulse that is demodulated to generate RXD output signal.
10	IR_TXD	Digital Out	This is the modulated TXD signal.
11	PULSEMOD	Digital In (with pull down)	A high level on this input put the chip into the monoshot transmit mode. In this mode, when there is a negative transition on the TXD input, a rising edge on the internal transmit modulation state machine will activate a high pulse on IR_TXD for 6 crystal clock cycles. With a 3.6864 MHz crystal, this corresponds to 1.63 ms. This mode cannot be used in conjunction with the 16XCLK clock. It is meant to be used with the external crystal clock. By default, this input pin is pulled to GND
12	POWERDN	Digital In (with pull down)	A high on this input put only the internal oscillator cell in POWERDN mode. The cell is normally not powered down.
13	OSCOUT	Analog Out	Oscillator Output
14	OSCIN	Analog In	Oscillator Input
15	Vcc		Power
16	16XCLK	Digital In	Positive edge triggered input clock that is set to 16 times the data transmission baud rate. The encode and decode schemes require this signal. The signal is usually tied to a UART's BAUDOUT signal. The 16XCLK may be provided by application circuitry if BAUDOUT is not available. This signal is required when the internal clock is not used.

Note:
There are two methods of putting the internal oscillator cell in POWERDOWN MODE. Whenever the CLK_SEL pin is asserted high (external clock select) the oscillator is automatically put in powerdown mode, or whenever the POWERDN pin asserted high.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_S	-65	+150	°C
Operating Temperature	T_A	-40	+85	°C
Output Current	I_O	-20	15	mA
Power Dissipation [1]	P_{MAX}		0.46	W
Input/Output Voltage [2]	V_I /V_O	-0.5	Vcc+0.5	V
Power Supply Voltage	V_{CC}	-0.5	7.0	V
Electrostatic Protection	V_{ESD}		4000	V

Note: 1. All pins are protected from damage to static discharge by internal diode clamps to Vcc and GND.

Switching Specifications

(Vcc = 2.7 to 5.5 V, T_A = -20 to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Propagation Delay Time [1]	t_{pd}			45	ns	
Output Rise Time [2]	t_{rise}	13 6	22 11	24 12	ns	V_{CC} = 2.7 V, C_L = 50 pF VCC = 5.5 V, C_L = 50 pF
Output Fall Time [3]	t_{fall}	12 5	14 10	16 11	ns	V_{CC} = 2.7 V, C_L = 50 pF V_{CC} = 5.5 V, C_L = 50 pF
Output Capacitance on Output Pads Used for Simulation	C_{OUT}			50	pF	

Notes:
1. Propagation Delay Time in the output buffer is the time taken from the input passing Vcc/2 to the time of the output reaching Vcc/2 with 50 pF as the output load.
2. The Ouput Rise Time is the time taken for the outputs (RXD, IR_TXD) to rise from 10% of the original value to 90% of the final value.
3. The Output Fall Time is the time taken for the outputs (RXD, IR_TXD) to fall from 90% of the original value to 10% of the final value.

Recommended Operating Conditions

(V_{cc} = 2.7 to 5.5 V, T_A = -20 to +85 °C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_{CC}	2.7	5.0	5.5	V	
Input Voltage	V_I	0		V_{CC}	V	
Ambient Temperature	T_A	-20		+85	°C	
High Level Input Voltage	V_{IH}	0.7 V_{CC}		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		0.3 V_{CC}	V	
Output High Voltage	V_{OH}	2.6			V	V_{CC} = 2.7 V I_{OH} = 2 mA
Output Low Voltage	V_{OL}			0.1	V	V_{CC} = 2.7 V I_{OL} = 2 mA
Output High Voltage	V_{OH}	5.1			V	V_{CC} = 5.5 V I_{OH} = 2 mA
Output Low Voltage	V_{OL}			0.1	V	V_{CC} = 2.7 V I_{OL} = 2 mA
Static Power Dissipation	P_{STAT}			0.61	mW	
Dynamic Power Dissipation	P_{DYN}			16.5	mW	
Static Current Consumption	I_{STAT}			50 100	µA	V_{CC} = 2.7 V V_{CC} = 5.5 V
Dynamic Current Consumption	I_{DYN}		1.08 2.45	3 3	mA	V_{CC} = 2.7 V V_{CC} = 5.5 V
Max Clk Frequency (16XCLK) [1]	f16XCLK			2	MHz	
Minimum Pulse Width (IR_TXD) [2]	tmpw	1628			ns	
Pulse Width on Monoshot (IR_TXD and IR_RXD)	tmpw	1628			ns	
Value of Pulldown Resistor used on POW-ERDN & PULSEMOD input pins	RDWN	400 213	460 237	510 260	kW	V_{CC} = 2.7 V V_{CC} = 5.5 V
Trigger Low Level Input Voltage (For NRST input pin)	VIL_TRIG	0.93 2.11	0.96 2.14	0.98 2.15	V	V_{CC} = 2.7 V V_{CC} = 5.5 V
Trigger High Level Input Voltage (For NRST input pin)	VIH_TRIG	1.68 3.22	1.69 3.23	1.70 3.25	V	V_{CC} = 2.7 V V_{CC} = 5.5 V

Notes:

1. IrDA® Parameter. The Max Clk Frequency represents the maximum clock frequency to drive the HSDL-7002's internal state machine. Under normal circumstances, the clock input should not exceed 16*115.2 kbit/s or 1.8432 MHz. This product can operate at higher clock rates, but the above is the recommended rate.
2. The Maximum Pulse Width (t_{mpw}) represents the minimum pulse width of the encoded IR_TXD pulse (and the IR_RXD pulse). As per the IrDA® Physical Layer Specification 1.4, the minimum pulse of the IR_TXD and IR_RXD pulses should be 3*(1/1.8432 MHz) or 1.63 µs.

HSDL-7002 Package Dimensions

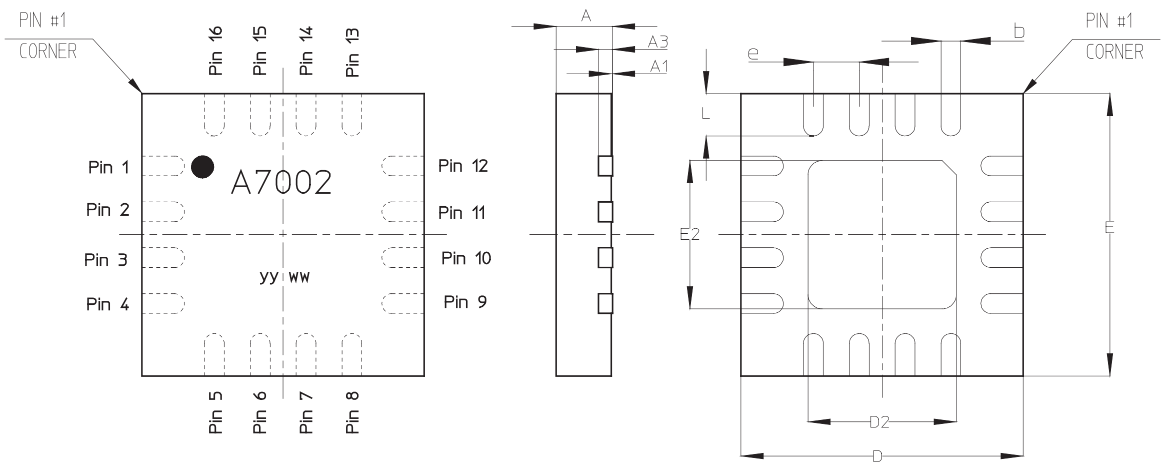


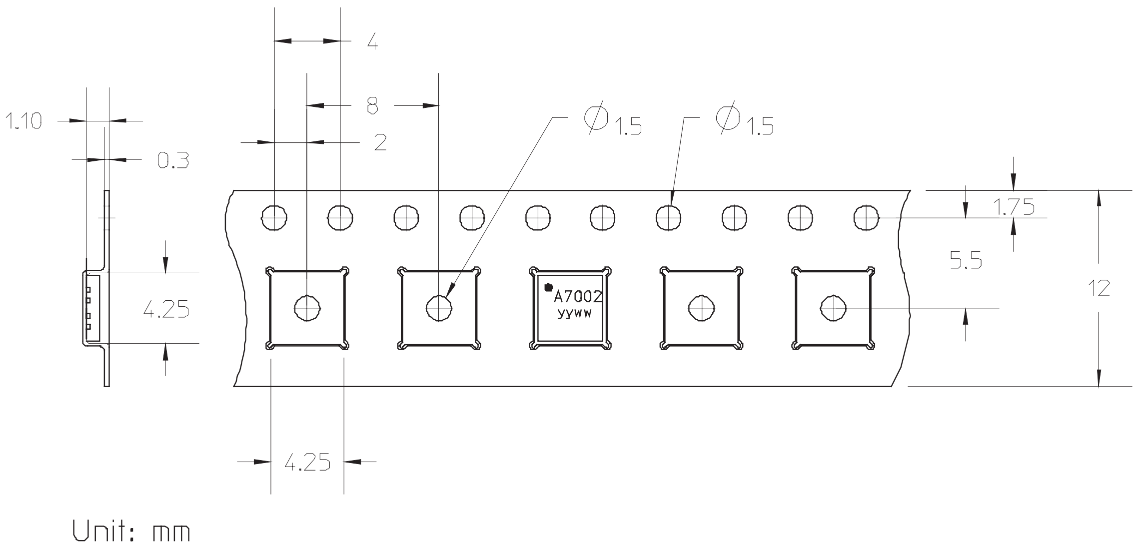
Figure 3. HSDL-7002 Package Dimensions

N	b			D2			E2			e	L			JEDE
	Min.	Nom.	Max.	Min.	Nom.	Max.	Min.	Nom.	Max.		Min.	Nom.	Max.	
16L	0.25	0.28	0.33	2.05	2.10	2.15	2.05	2.10	2.15	0.650 BSC.	0.55	0.60	0.65	MO-220VGGC

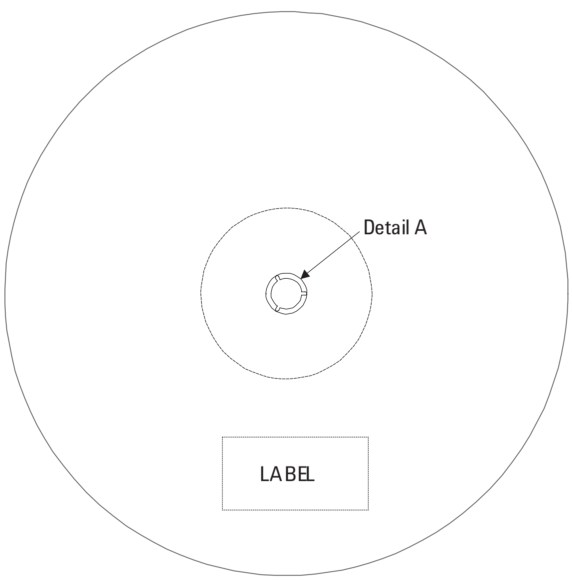
Symbol	Dimension in mm			Dimension in inch		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	-	0.80	0.84	-	0.031	0.033
A1	0.00	0.02	0.04	0.00	0.0008	0.0015
A3	0.20 REF.			0.008 REF.		
D	3.85	4.00	4.15	0.152	0.157	0.163
E	3.85	4.00	4.15	0.152	0.157	0.163
JEDEC	MO-220					

PIN ASSIGNMENT			
PIN 1	/TXD	PIN 9	/IR_RXD
PIN 2	RXD	PIN 10	IR_TXD
PIN 3	A0	PIN 11	PULSEMOD
PIN 4	A1	PIN 12	POWERDN
PIN 5	A2	PIN 13	OSCOUT
PIN 6	CLK_SEL	PIN 14	OSCIN
PIN 7	GND	PIN 15	VCC
PIN 8	/NRST	PIN 16	16XCLK

HSDL-7002 Tape Dimensions

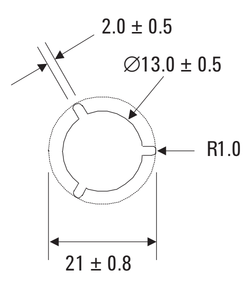


HSDL-7002 Reel Dimensions

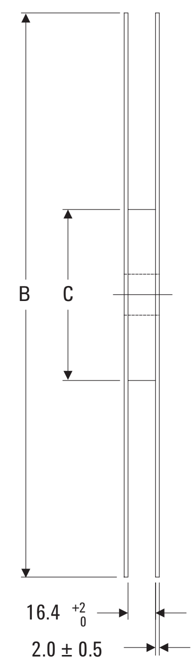


"B"	"C"	Quantity
330	80	2500

Unit: mm



Detail A



HSDL-7002 Moisture Proof Packaging

All HSDL-7002 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC MSL (Moisture Sensetive Level) 3.

Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp	Time
In reels	60 °C	≥ 48hours
In bulk	100 °C	≥ 4hours
	125 °C	≥ 2 hours
	150 °C	≥ 1 hour

Baking should only be done once.

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions. If times longer than three days are needed, the parts must be stored in a dry box.

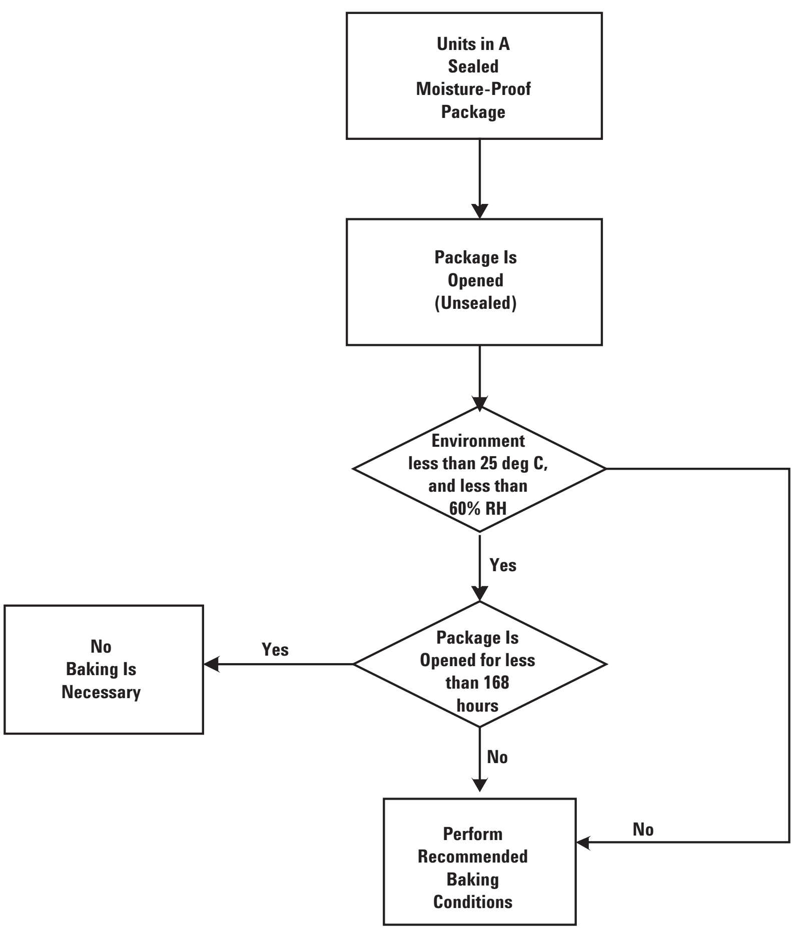
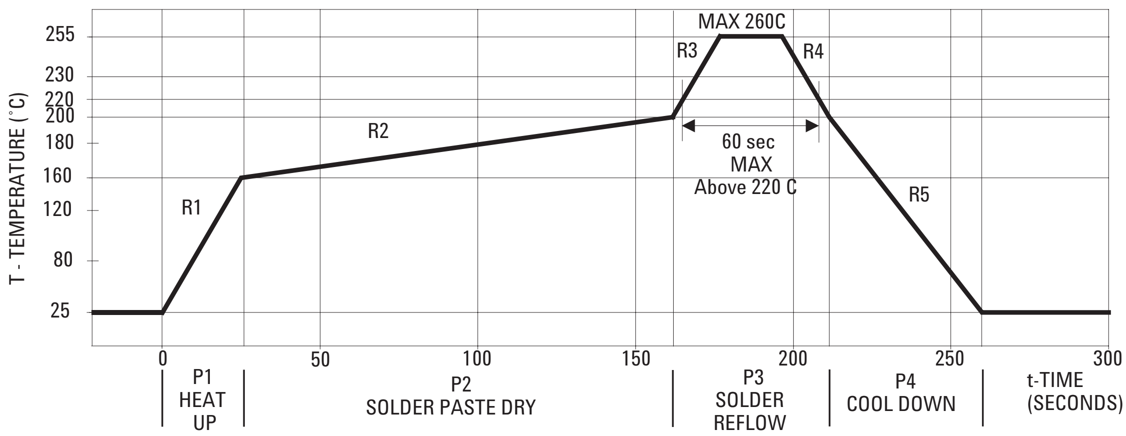


Figure 4. Baking Conditions Chart

Recommended Reflow Profile



Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	4°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3P3, R4	200°C to 255°C (260°C at 10 seconds max) 255°C to 200°C	4°C/s-6°C/s
Cool Down	P4, R5	200°C to 25°C	-6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. TheΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-7002 castellation pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-7002 castellations.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-7002 castellations to change dimensions evenly, putting minimal stresses on the HSDL-7002 endec.

Appendix A: General Application Guide for the HSDL-7002

Application Circuits for HSDL-7002

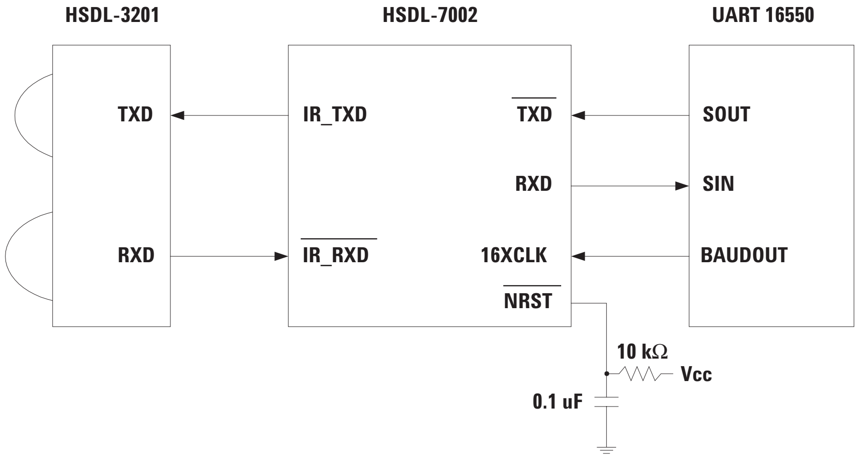


Figure 5. HSDL-7002 Connection between a standard 16550 UART and HSDL-3201

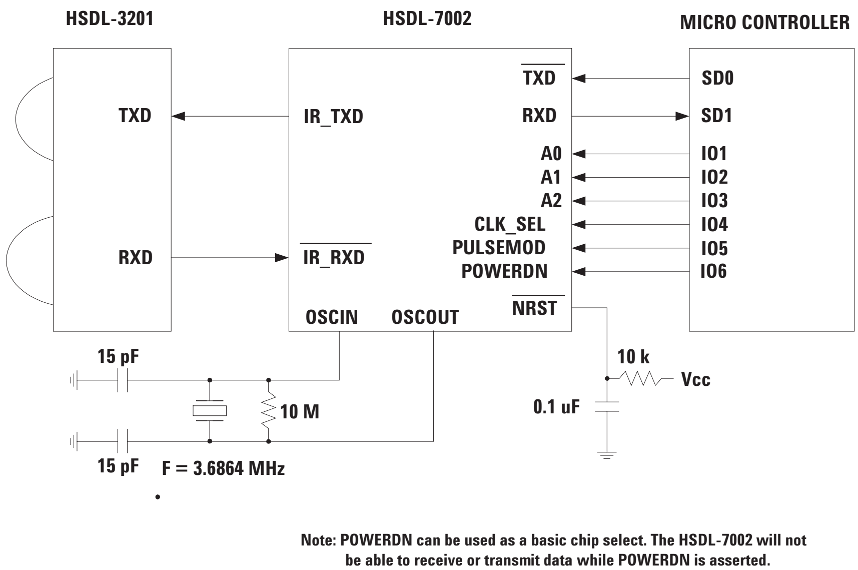


Figure 6. HSDL-7002 Connection between a Microcontroller and HSDL-3201

Selection of Internal Clock Rate from Crystal Oscillator

Selected Clock Rate (bps)	A2	A1	A0	Crystal Freq. Division
115200	0	0	0	Divided by 2
57600	0	0	1	Divided by 4
19200	0	1	0	Divided by 12
9600	0	1	1	Divided by 24
38400	1	0	0	Divided by 6
4800	1	0	1	Divided by 48
2400	1	1	0	Divided by 96

Encoding Scheme

The encoding scheme relies on a clock being present, which is set to 16 times the data transmission baud rate (16XCLK). The encoder sends a pulse for every space or "0" that is sent on the TXD line. On a high to low transition of the TXD line, the generation of the pulse is delayed for 7 clock cycles of the 16XCLK before the pulse is set high for 3 clock cycles (or 3/16th of a bit time) and then subsequently pulled low. This generates a 3/16th bit time pulse centered around the bit of information ("0") that is being transmitted. For consecutive spaces, pulses with a 1 bit time delay are generated in series. If a logic "1" (mark) is sent then the encoder does not generate a pulse.

Decoding Scheme

The IrDA®-SIR decoding modulation method can be thought of as a pulse-stretching scheme. Every high to low transition of the IR_RXD line signifies the arrival of a pulse. This pulse needs to be stretched to accommodate 1 bit time (or 16 16XCLK cycles). Every pulse that is received is translated into a "0" or space on the RXD line equal to 1 bit time.

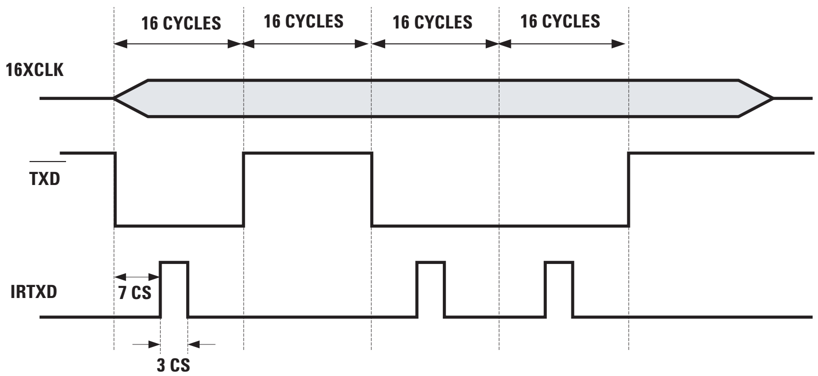


Figure 7. HSDL-7002 Encoding Scheme

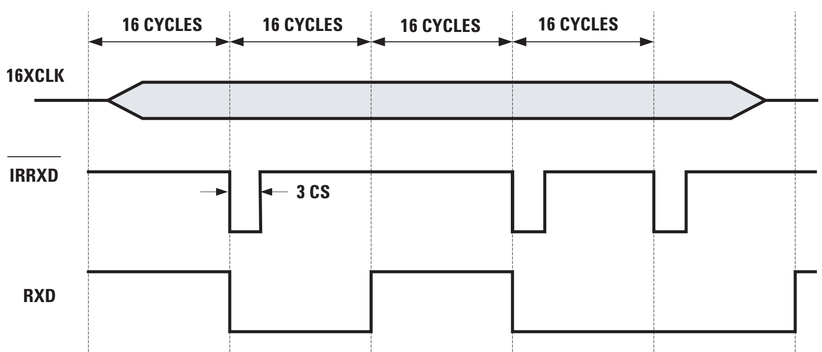
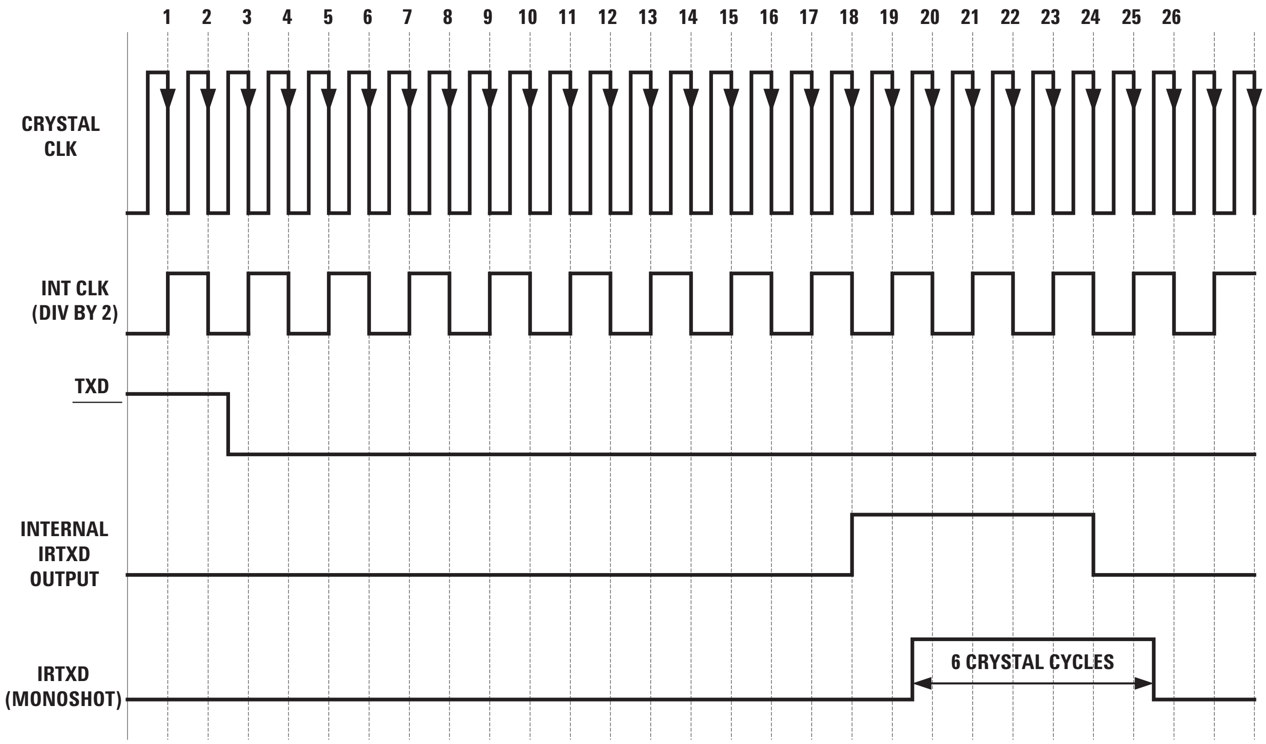


Figure 8. HSDL-7002 Decoding Scheme

Notes:

1. The stretched pulse must be at least ¾ of a bit time in duration to be correctly interpreted by a UART.
2. It is recommended that the TXD remains high when not transmitting. This ensures the LED is off and will not interfere with signal reception.

Monoshot Operation



The figure above illustrates the operation of the monoshot when the internal clock is set to divide by 2 mode, i.e., when A2=0, A1=0, and A0=0. A rising edge on the internal modulation state machine (IR_TXD output), will cause the output on the IR_TXD to go up for 6 crystal clock cycles. With a 3.6864 MHz clock, this corresponds to a pulse of 1.63 µs. The duration of this pulse is independent of the code A2, A1, A0 and is always 6 clock cycles of the crystal, corresponding to the monoshot operation.

For company and product information, please go to our web site: **WWW.liteon.com** or **http://optodatabook.liteon.com/databook/databook.aspx**