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ELECTRICAL SPECIFICATIONS

0.01 GHz TO 3 GHz FREQUENCY RANGE

 T_{A} = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.01		3	GHz	
GAIN		17.5	19.5		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.1	1.6	dB	0.3 GHz to 3 GHz
RETURN LOSS						
Input			15		dB	
Output			24		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	19.0	21.0		dBm	
Saturated Output Power	P _{SAT}		22.5		dBm	
Output Third-Order Intercept	IP3		33		dBm	
SUPPLY CURRENT	I _{DQ}		65	80	mA	Adjust V_{GG1} to achieve $I_{DQ} = 65$ mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

3 GHz TO 8 GHz FREQUENCY RANGE

 T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		3		8	GHz	
GAIN		15.5	18		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.4	1.9	dB	
RETURN LOSS						
Input			10		dB	
Output			16		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	18.0	21.0		dBm	
Saturated Output Power	P _{SAT}		22.5		dBm	
Output Third-Order Intercept	IP3		31.5		dBm	
SUPPLY CURRENT	I _{DQ}		65	80	mA	Adjust V _{GG1} to achieve I _{DQ} = 65 mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

8 GHz TO 10 GHz FREQUENCY RANGE

 T_A = 25°C, V_{DD} = 5 V, and I_{DQ} = 65 mA, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Тур	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		8		10	GHz	
GAIN		13	16		dB	
Gain Variation Over Temperature			0.01		dB/°C	
NOISE FIGURE			1.7	2.2	dB	
RETURN LOSS						
Input			8		dB	
Output			7		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB	17.5	19.5		dBm	
Saturated Output Power	P _{SAT}		21.5		dBm	
Output Third-Order Intercept	IP3		33		dBm	
SUPPLY CURRENT	I _{DQ}		65	80	mA	Adjust V_{GG1} to achieve $I_{DQ} = 65$ mA typical
SUPPLY VOLTAGE	V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

1
o +150°C
o +85°C
C/W
Passed

¹ When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the specification is listed. For the full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

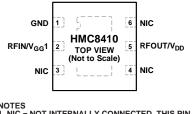
ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

 $^{^{2}}$ See the Ordering Guide section for more information.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. NIC = NOT INTERNALLY CONNECTED. THIS PIN MUST BE CONNECTED TO THE RF/DC GROUND.

20 EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO RF/DC GROUND.

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground. This pin must be connected to the RF/dc ground. See Figure 3 for the interface schematic.
2	RFIN/V _{GG} 1	RF Input (RFIN). This pin is ac-coupled and matched to 50 Ω . See Figure 4 for the interface schematic.
		Gate Bias of the Amplifier ($V_{GG}1$). This pin is ac-coupled and matched to 50 Ω . See Figure 4 for the interface schematic.
3, 4, 6	NIC	Not Internally Connected. This pin must be connected to the RF/dc ground.
5	RFOUT/V _{DD}	RF Output (RFOUT). This pin is ac-coupled and matched to 50 Ω . See Figure 5 for the interface schematic.
		Drain Bias for Amplifier (V_{DD}). This pin is ac-coupled and matched to 50 Ω . See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF/dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

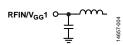


Figure 4. RFIN/V_{GG}1 Interface Schematic



Figure 5. RFOUT/V_{DD} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

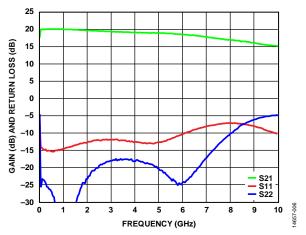


Figure 6. Gain and Return Loss vs. Frequency

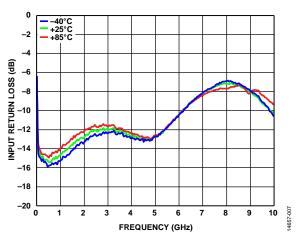


Figure 7. Input Return Loss vs. Frequency for Various Temperatures

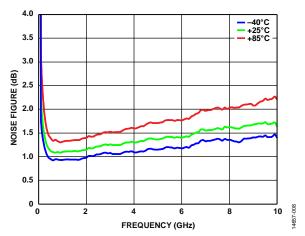


Figure 8. Noise Figure vs. Frequency for Various Temperatures

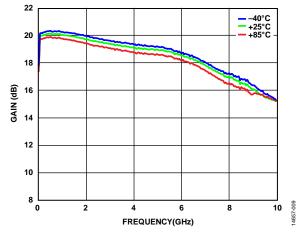


Figure 9. Gain vs. Frequency for Various Temperatures

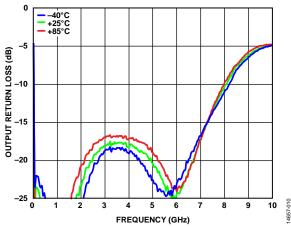


Figure 10. Output Return Loss vs. Frequency for Various Temperatures

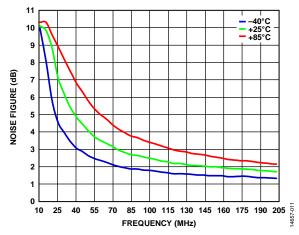


Figure 11. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz

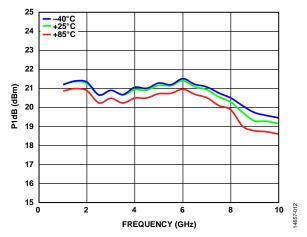


Figure 12. P1dB vs. Frequency for Various Temperatures

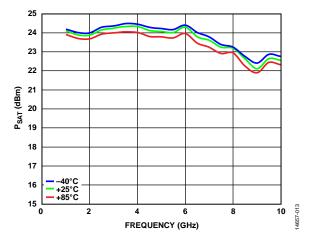


Figure 13. P_{SAT} vs. Frequency for Various Temperatures

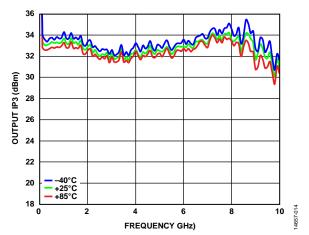


Figure 14. Output IP3 vs. Frequency for Various Temperatures, Output Power (P_{OUT})/Tone = 5 dBm

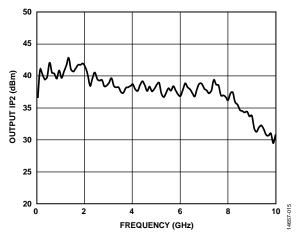


Figure 15. Output IP2 vs. Frequency at Pout/Tone = 5 dBm

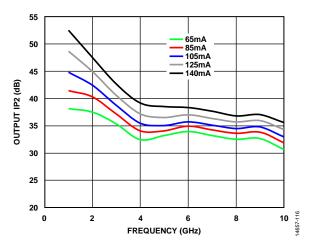


Figure 16. Output IP2 vs. Frequency for Various Supply Currents (IDQ), $P_{OUT}/Tone=5 \ dBm, V_{DD}=5 \ V$

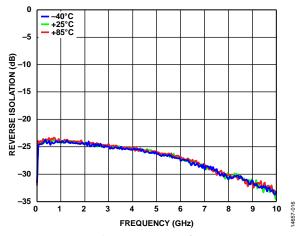


Figure 17. Reverse Isolation vs. Frequency for Various Temperatures

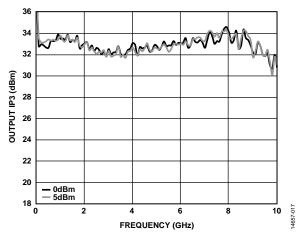


Figure 18. Output IP3 vs. Frequency for Various Pout/Tone

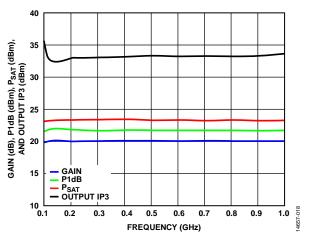


Figure 19. Gain, P1dB, Psat, and Output IP3 vs. Frequency

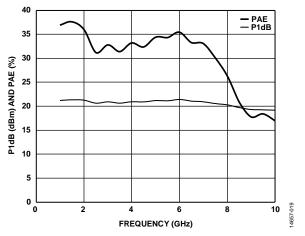


Figure 20. P1dB and Power Added Efficiency (PAE) vs. Frequency

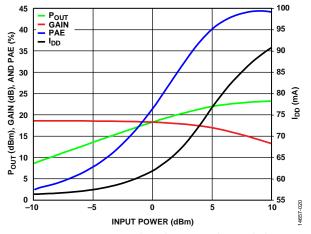


Figure 21. Pout, Gain, PAE, and Supply Current with RF Applied (IDD) vs. Input Power at 5 GHz

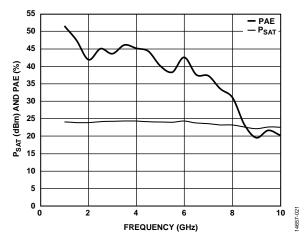


Figure 22. Psat and PAE vs. Frequency

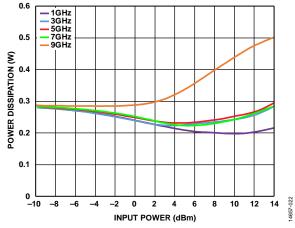


Figure 23. Power Dissipation at 85°C vs. Input Power at Various Frequencies

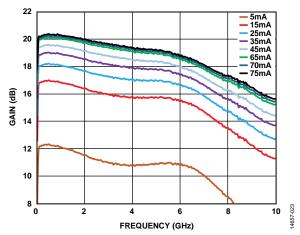


Figure 24. Gain vs. Frequency for Various Supply Currents, $V_{DD} = 5 V$

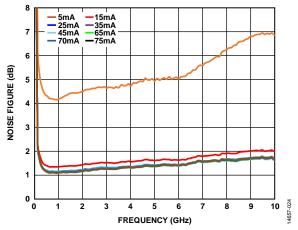


Figure 25. Noise Figure vs. Frequency for Various Supply Currents (I_{DQ}), $V_{DQ} = 5 V$

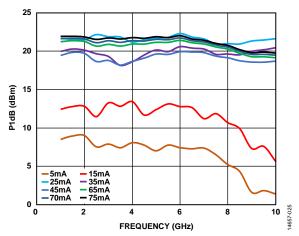


Figure 26. P1dB vs. Frequency for Various Supply Currents (I_{DQ}), $V_{DD} = 5 V$

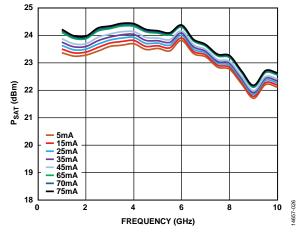


Figure 27. P_{SAT} vs. Frequency for Various Supply Currents (I_{DQ}), $V_{DD} = 5 V$

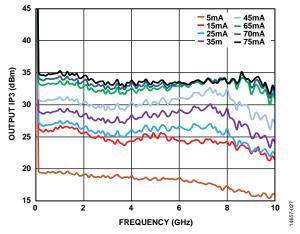


Figure 28. Output IP3 vs. Frequency for Various Supply Currents (I_{DQ}), $P_{OUT}/Tone = 5 dBm$, $V_{DD} = 5 V$

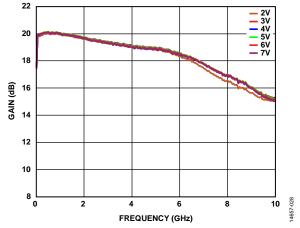


Figure 29. Gain vs. Frequency for Various Supply Voltages, $I_{DQ} = 65 \text{ mA}$

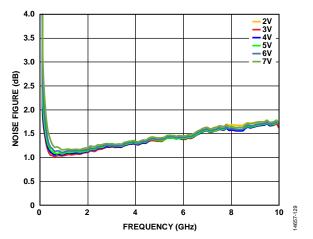


Figure 30. Noise Figure vs. Frequency for Various Supply Voltages, $I_{DQ} = 65 \text{ mA}$

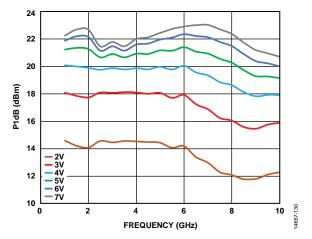


Figure 31. P1dB vs. Frequency for Various Supply Voltages, $I_{DQ} = 65 \text{ mA}$

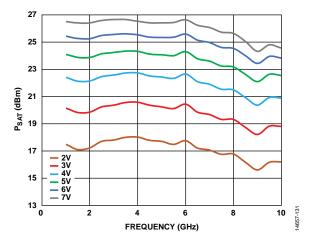


Figure 32. P_{SAT} vs. Frequency for Various Supply Voltages, $I_{DQ} = 65 \text{ mA}$

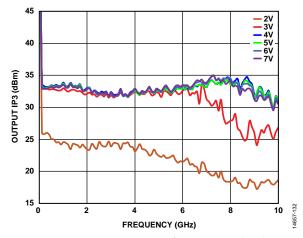


Figure 33. Output IP3 vs. Frequency for Various Supply Voltages, $P_{OUT}/Tone = 5 dBm$

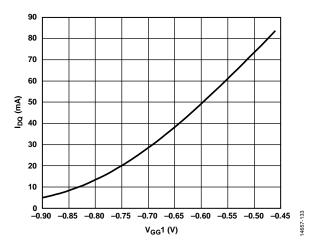


Figure 34. Supply Current (I_{DQ}) vs. V_{GG} 1, V_{DD} = 5 V, Representative of a Typical Device

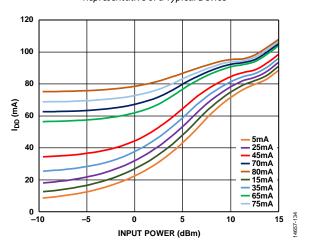


Figure 35. Supply Current with RF Applied (I_{DD}) vs. Input Power for Various Supply Currents (I_{DD}) at 5 GHz, V_{DD} = 5 V

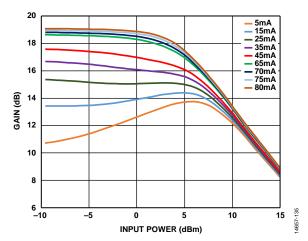


Figure 36. Gain vs. Input Power for Various Supply Currents (IDQ) at 5 GHz, $V_{\rm DD}$ = 5 V

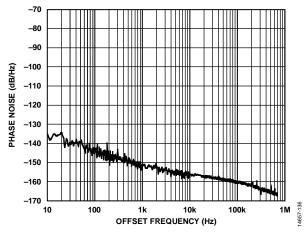


Figure 37. Additive Phase Noise vs. Offset Frequency, RF Frequency = 5 GHz, RF Input Power = 3 dBm (P1dB)

THEORY OF OPERATION

The HMC8410 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic (pHEMT), low noise wideband amplifier.

The HMC8410 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the 0.01 GHz to 10 GHz frequency range. Consequently, it can directly insert into a 50 Ω system with no required impedance matching circuitry, which also means that multiple HMC8410 amplifiers can be cascaded back to back without the need for external matching circuitry.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

Note that it is critical to supply very low inductance ground connections to the ground pins as well as to the backside exposed paddle to ensure stable operation.

To achieve optimal performance from the HMC8410 and prevent damage to the device, do not exceed the absolute maximum ratings.

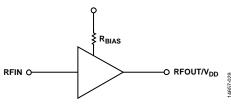


Figure 38. Simplified HMC8410 Architecture

APPLICATIONS INFORMATION

Figure 39 shows the basic connections for operating the HMC8410. AC couple the input and output of the HMC8410 with appropriately sized capacitors. DC block capacitors and RF choke inductors are supplied on the RFIN and RFOUT pins of the HMC8410 evaluation board. See Table 6 for additional information. These dc block capacitors and RF choke inductors form wideband bias tees on the input and output ports to provide both ac coupling and the necessary supply voltages to the RFIN and RFOUT pins. A 5 V dc bias is supplied to the amplifier through the choke inductor connected to the RFOUT pin, and the negative $V_{\rm GG}1$ voltage is supplied to the RFIN pin through the choke inductor.

RECOMMENDED BIAS SEQUENCING

To not damage the amplifier, follow the recommended bias sequencing.

During Power-Up

The recommended bias sequence during power-up for the HMC8410 follows:

- 1. Connect to GND.
- 2. Set $V_{GG}1$ to -2 V.
- 3. Set V_{DD} to 5 V.
- 4. Increase $V_{\rm GG}1$ to achieve a typical supply current ($I_{\rm DQ}$) = 65 mA.
- 5. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down for the HMC8410 follows:

- 1. Turn off the RF signal.
- 2. Decrease $V_{GG}1$ to -2 V to achieve a typical $I_{DQ} = 0$ mA.
- 3. Decrease V_{DD} to 0 V.
- 4. Increase V_{GG}1 to 0 V.

The bias conditions previously listed ($V_{\rm DD}$ = 5 V and $I_{\rm DQ}$ = 65 mA) are the recommended operating points to achieve optimum performance. The data used in this data sheet was taken with the recommended bias conditions. When using the HMC8410 with different bias conditions, different performance than what is shown in the Typical Performance Characteristics section can result.

Figure 19, Figure 31, and Figure 32 show that increasing the voltage from 2 V to 7 V typically increases P1dB and P_{SAT} at the expense of power consumption with minor degradation on noise figure (NF).

TYPICAL APPLICATION CIRCUIT

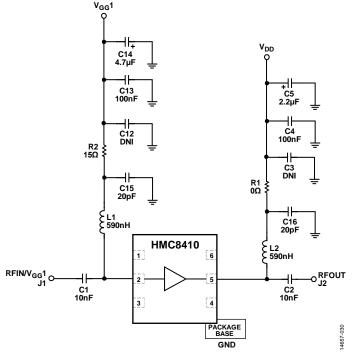


Figure 39. Typical Application Circuit

EVALUATION BOARD

The HMC8410 evaluation board is a 4-layer board fabricated using a Rogers 4350 and the best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance.

The HMC8410 evaluation board and populated components operate over the -40° C to $+85^{\circ}$ C ambient temperature range. For proper bias sequence, see the Applications Information section.

The HMC8410 evaluation board schematic is shown in Figure 41. A fully populated and tested evaluation printed circuit board (PCB) is available from Analog Devices, Inc., upon request (see Figure 40).

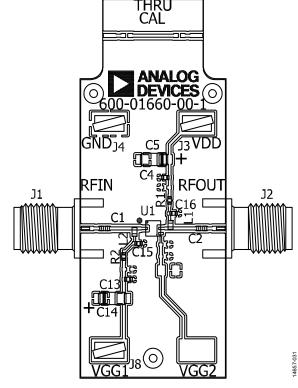


Figure 40. HMC8410 Evaluation PCB

EVALUATION BOARD SCHEMATIC

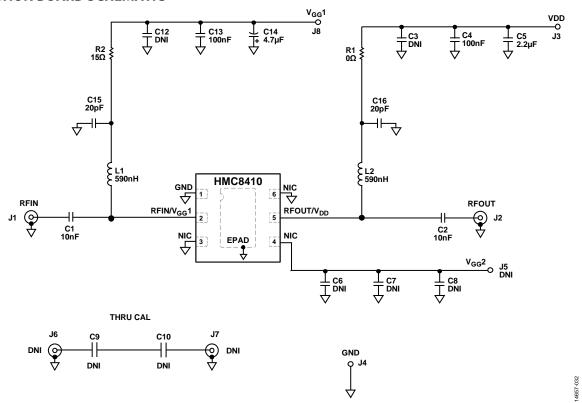


Figure 41. HMC8410 Evaluation Board Schematic

Table 6. Bill of Materials for Evaluation PCB EV1HMC8410LP2F

Table 6. Bill of Materials for Evaluation PCB EV 1HMC8410LP2F						
Item	Description					
J1, J2	PCB mount SMA RF connectors, SRI 21-146-1000-01					
J3, J4, J8	DC bias test points					
C1, C2	Capacitors, broadband, 100 nF and 82 pF, 0502, 160 kHz and 40 GHz; ATC531Z104KT16T					
C3, C6 to C10, C12, J5 to J7	Do not install (DNI)					
C4, C13	Capacitors, ceramic, 100 nF, 0402 package					
C5	Capacitor, tantalum, 2.2 μF, Size A					
C14	Capacitor, tantalum, 4.7 μF, 3216 package					
C15, C16	Capacitors, ceramic, 20 pF, 0402 package					
L1, L2	Inductors, 590 nH, 0402, 5%, ferrite DF, Coilcraft 0402DF-591XJRU					
R1	0 Ω resistor					
R2	15 Ω resistor, 0402 package					
U1	Amplifier, HMC8410					
Heat sink	Heat sink					
PCB	600-01660-00 evaluation PCB; circuit board material: Rogers 4350					

OUTLINE DIMENSIONS

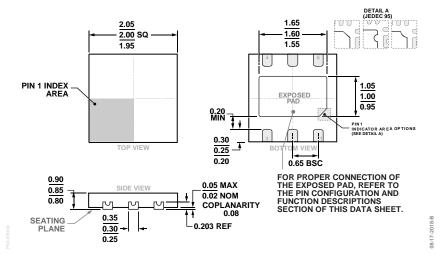


Figure 42. 6-Lead Lead Frame Chip Scale Package [LFCSP] 2 mm × 2 mm Body and 0.85 mm Package Height (CP-6-9) Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	MSL Rating ²	Lead Finish	Package Description	Package Option
HMC8410LP2FE	−40°C to +85°C	MSL3	100% Matte Sn	6-Lead LFCSP	CP-6-9
HMC8410LP2FETR	-40°C to +85°C	MSL3	100% Matte Sn	6-Lead LFCSP	CP-6-9
EV1HMC8410LP2F				Evaluation PCB	

¹ The HMC8410LP2FE and HMC8410LP2FETR are RoHS Compliant Parts.

² See the Absolute Maximum Ratings section for additional information.