Ordering Information

HCPL-3180 is UL Recognized with 3750 Vrms for 1 minute per UL1577.

Part Number	Option RoHS Compliant	Option Non RoHS Compliant	Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-2	Quantity
HCPL-3180	-000E	No option	300 mil DIP-8					50 per tube
	-300E	-300		X	X			50 per tube
	-500E	-500		X	X	X		1000 per reel
	-060E	-060					X	50 per tube
	-360E	-360		X	X	X	X	50 per tube
	-560E	-560		X	X	X	X	1000 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-3180-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval in RoHS compliant.

Example 2:

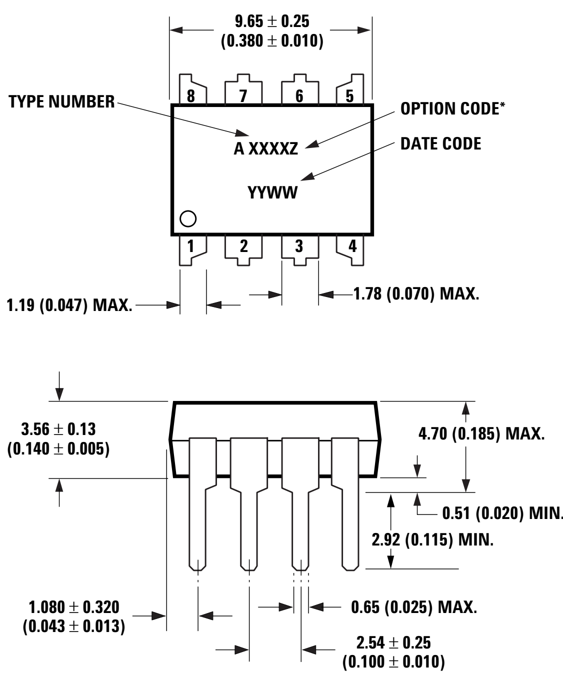
HCPL-3180 to order product of 300 mil DIP package in tube packaging and non RoHS compliant.

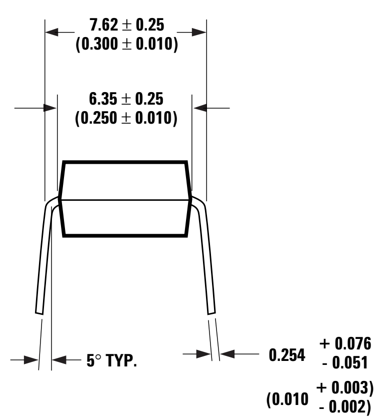
Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

Package Outline Drawings

HCPL-3180 Standard DIP Package



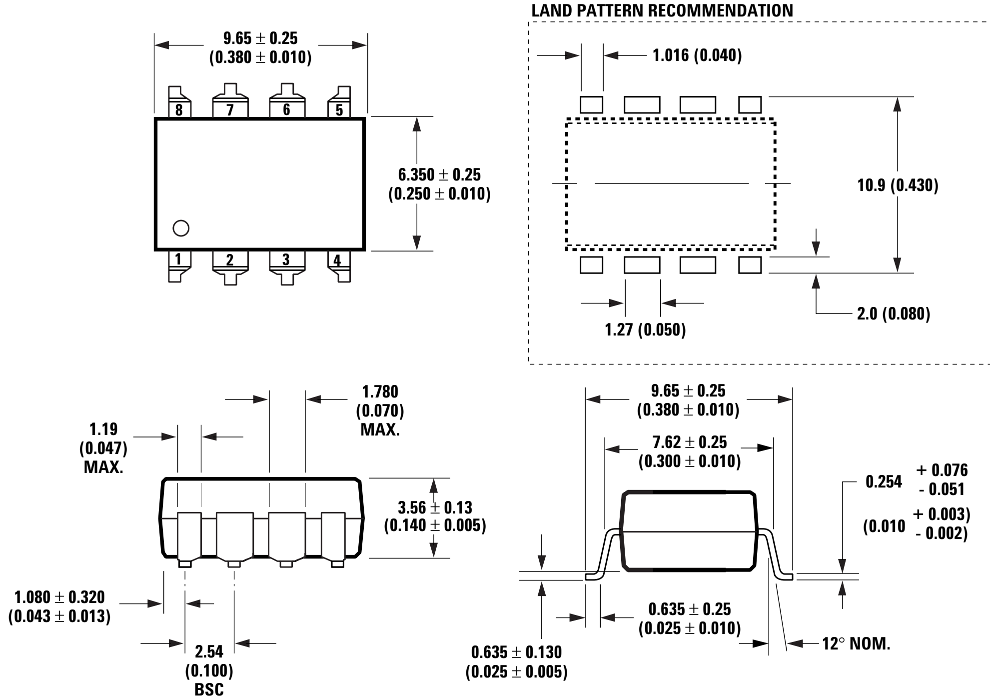


DIMENSIONS IN MILLIMETERS AND (INCHES).

* MARKING CODE LETTER FOR OPTION NUMBERS
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

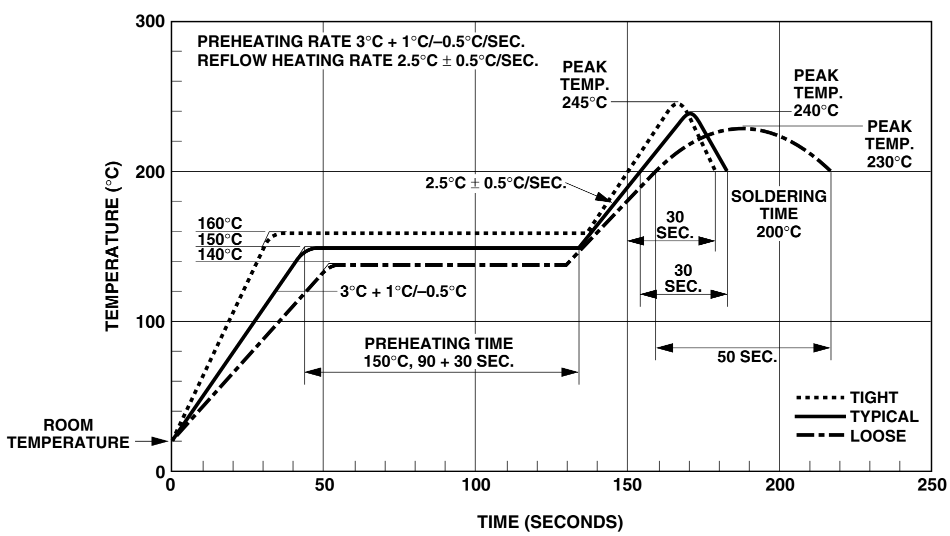
HCPL-3180 Gull Wing Surface Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

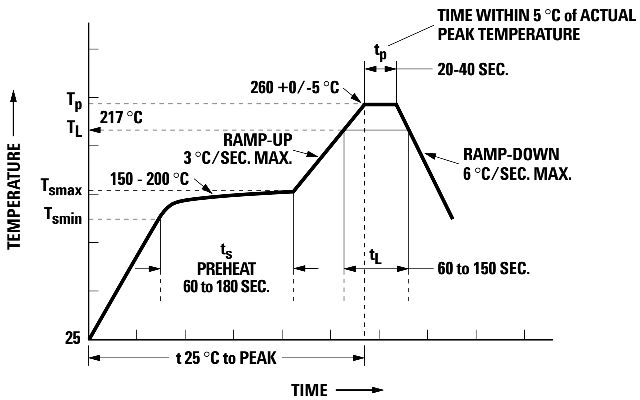
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile



Note: Non-halide flux should be used.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Non-halide flux should be used.

Regulatory Information

The HCPL-3180 has been approved by the following organizations:

IEC/EN/DIN EN 60747-5-2

Approved under: IEC 60747-5-2:1997 + A1:2002
EN 60747-5-2:2001 + A1:2002
DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01
(Option 060 only)

UL

Approval under UL 1577, component recognition program up to V_{ISO} = 3750 Vrms. File E55361.

CSA

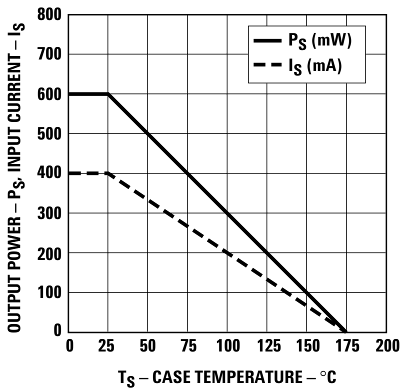
Approval under CSA Component Acceptance Notice #5, File CA 88324.

IEC/EN/DIN EN 60747-5-2 Insulation Characteristics (HCPL-3180 Option 060)

Description	Symbol	HCPL-3180	Unit
Installation classification per DIN EN 0110 1997-04 for rated mains voltage ≤ 150 V_{rms} for rated mains voltage ≤ 300 V_{rms} for rated mains voltage ≤ 600 V_{rms}		 I - IV I - III I-II	
Climatic Classification		55/100/21	
Pollution Degree (DIN EN 0110 1997-04)		2	
Maximum Working Insulation Voltage	V_{IORM}	630	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875=V_{PR}, 100% Production Test with t_m=1 sec, Partial Discharge < 5 pC	V_{PR}	1181	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5=V_{PR}, Type and Sample Test, t_m=60 sec, Partial Discharge < 5 pC	V_{PR}	945	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure. Case Temperature Input Current** Output Power**	 T_S $I_{S,INPUT}$ $P_{S, OUTPUT}$	 175 230 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-2 for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to the following figure for dependence of P_S and I_S on ambient temperature.



Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-3180	Units	Conditions
Minimum External Air Gap (Clearance)	L(101)	7.1	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (Creepage)	L(102)	7.4	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Note: Option 300 – surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	-55	125	°C	
Junction Temperature	T_J	-40	125	°C	
Average Input Current	$I_{F(AVG)}$		25	mA	1
Peak Transient Input Current (<1 µs pulse width, 300 pps)	$I_{F(TRAN)}$		1.0	A	
Reverse Input Voltage	V_R		5	V	
"High" Peak Output Current	$I_{OH(PEAK)}$		2.5	A	2
"Low" Peak Output Current	$I_{OL(PEAK)}$		2.5	A	2
Supply Voltage	V_{CC}-V_{EE}	-0.5	25	V	
Output Voltage	$V_{O(PEAK)}$	0	V_{CC}	V	
Output Power Dissipation	P_O		250	mW	3
Total Power Dissipation	P_T		295	mW	4
Lead Solder Temperature	260°C for 10 sec., 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Power Supply	V_{CC}-V_{EE}	10	20	V	
Input Current (ON)	$I_{F(ON)}$	10	16	mA	
Input Voltage (OFF)	$V_{F(OFF)}$	- 3.6	0.8	V	
Operating Temperature	T_A	-40	100	°C	

Electrical Specifications (DC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}	0.5			A	$V_O = V_{CC}$- 4	2, 3, 17	5
		2.0			A	$V_O = V_{CC}$-10	2, 3, 17	2
Low Level Output Current	I_{OL}	0.5			A	$V_O = V_{EE}$+2.5	5, 6, 18	5
		2.0			A	$V_O = V_{EE}$+10	5, 6, 18	2
High Level Output Voltage	V_{OH}	V_{CC}-4			V	I_O = -100 mA	1, 3, 19	6, 7
Low Level Output Voltage	V_{OL}			0.5	V	I_O = 100 mA	4, 6, 20	
High Level Supply Current	I_{CCH}		3.0	6.0	mA	Output Open I_F = 10 to 16 mA	7, 8	
Low Level Supply Current	I_{CCL}		3.0	6.0	mA	Output Open V_F = 3.0 to 0.8 mA	7, 8	
Threshold Input Current Low to High	I_{FLH}			8.0	mA	I_O = 0 mA,	9, 15, 21	
Threshold Input Voltage High to Low	V_{FHL}	0.8			V	V_O > 5 V		
Input Forward Voltage	V_F	1.2	1.5	1.8	V	I_F = 10 mA	16	
Temperature Coefficient of Input Forward Voltage	$\Delta V_F/\Delta T_A$		–1.6		mV/°C	I_F = 10 mA		
UVLO Threshold	V_{UVLO+}		7.9		V	I_F = 10 mA,		
	V_{UVLO-}		7.4		V	V_O > 5 V	22, 33	
UVLO Hysteresis	$UVLO_{HYST}$		0.5		V			
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 µA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

Switching Specifications (AC)

Over recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}	50	150	200	ns	$I_F = 10$ mA,	10, 11, 12, 13,	14
Propagation Delay Time to Low Output Level	t_{PHL}	50	150	200	ns	$R_g = 10\ \Omega$, f = 250 kHz,	14, 23	
Pulse Width Distortion	PWD		20	65	ns	Duty Cycle = 50%,		10
Propagation Delay Difference Between Any Two Parts or Channels	PDD (t_{PHL}-t_{PLH})	-90		90	ns	$C_g = 10$ nF	34, 35	10
Rise Time	t_r		25		ns	CL = 1 nF,	23	
Fall Time	t_f		25		ns	$R_g = 0\ \Omega$		
UVLO turn On Delay	$t_{UVLO\ ON}$		2.0		µs		22	
UVLO turn Off Delay	$t_{UVLO\ OFF}$		0.3		µs		22	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	10			kV/µs	$T_A = 25°C$, $I_F = 10$ to 16 mA,	24	11, 12
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	10			kV/µs	$V_{CM} = 1.5$ kV, $V_{CC} = 20$ V	24	11, 13

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage	V_{ISO}	3750			Vrms	$T_A = 25°C$, RH < 50%		8,9
Input-Output Resistance	R_{I-O}		$10^{[11]}$		Ω	$V_{I-0} = 500$ V		9
Input-Output Capacitance	C_{I-0}		1		pF	Freq = 1 MHz		

Notes:

1. Derate linearly above +70°C free air temperature at a rate of 0.3 mA/°C.
2. Maximum pulse width = 10 µs, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with IO peak minimum = 2.0 A. See Application section for additional details on limiting IOL peak.
3. Derate linearly above +70°C, free air temperature at the rate of 4.8 mW/°C.
4. Derate linearly above +70°C, free air temperature at the rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed +125°C.
5. Maximum pulse width = 50 µs, maximum duty cycle = 0.5%.
6. In this test, V_{OH} is measured with a dc load current. When driving capacitive load V_{OH} will approach V_{CC} as I_{OH} approaches zero amps.
7. Maximum pulse width = 1 ms, maximum duty cycle = 20%.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage > 4500 V_{rms} for 1 second (leakage detection current limit $I_{I-O} < 5$ µA).
9. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
10. PWD is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
11. Pin 1 and 4 need to be connected to LED common.
12. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse V_{CM} to assure that the output will remain in the high state (i.e. $V_O > 10.0$ V).
13. Common mode transient immunity in a low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e. $V_O < 1.0$ V).
14. t_{PHL} propagation delay is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
15. The difference between t_{PHL} and t_{PLH} between any two HCPL-3180 parts under same test conditions.

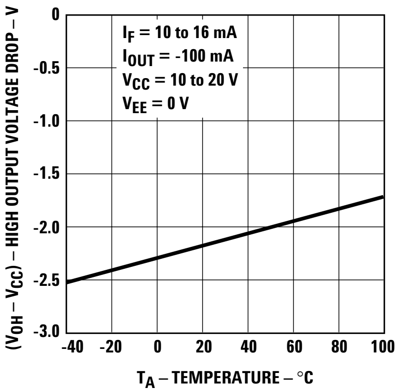


Figure 1. V_{OH} vs. temperature.

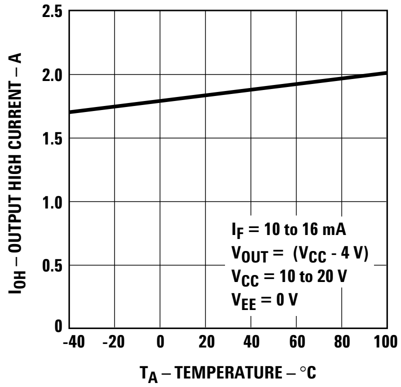


Figure 2. I_{OH} vs. temperature.

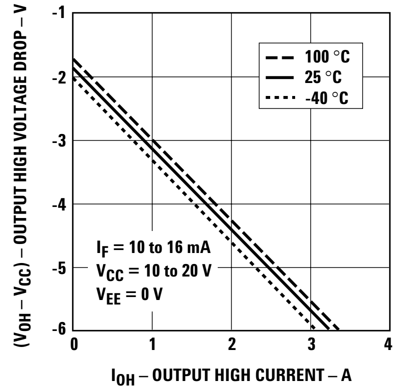


Figure 3. V_{OH} vs. I_{OH}.

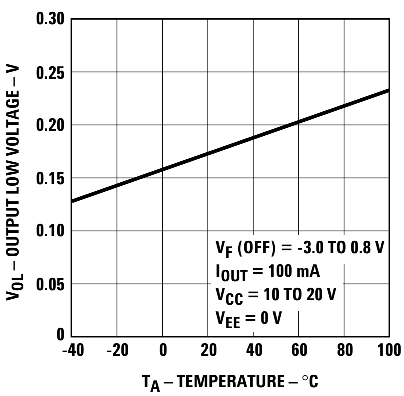


Figure 4. V_{OL} vs. temperature.

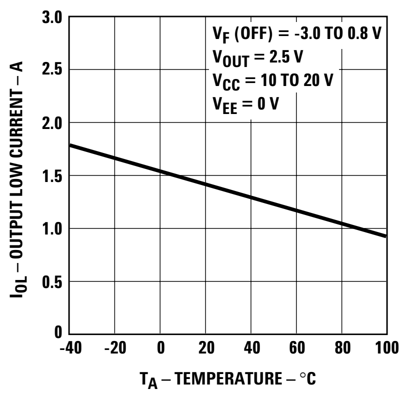


Figure 5. I_{OL} vs. temperature.

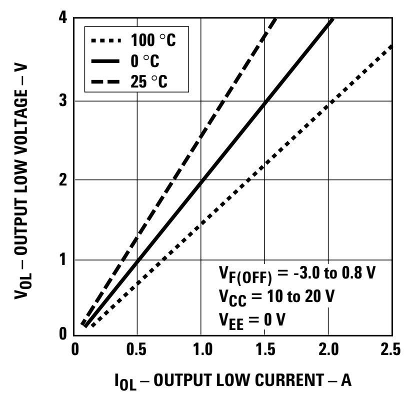


Figure 6. V_{OL} vs. I_{OL}.

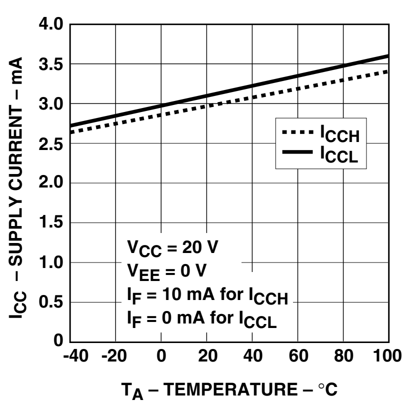


Figure 7. I_{CC} vs. temperature.

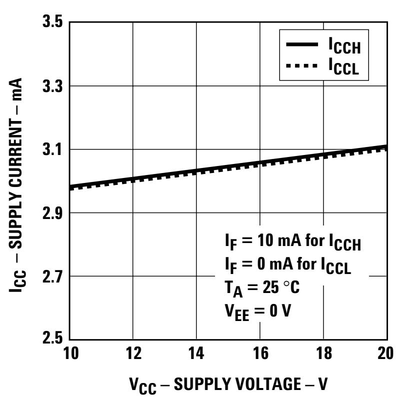


Figure 8. I_{CC} vs. V_{CC}.

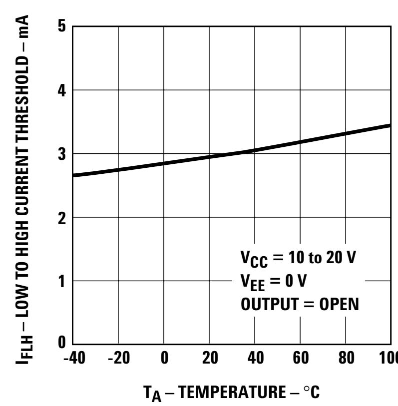


Figure 9. I_{FLH} vs. temperature.

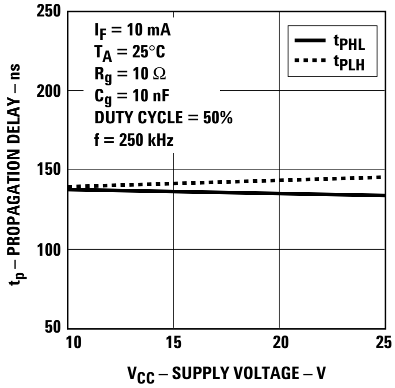


Figure 10. Propagation delay vs. V_{CC}.

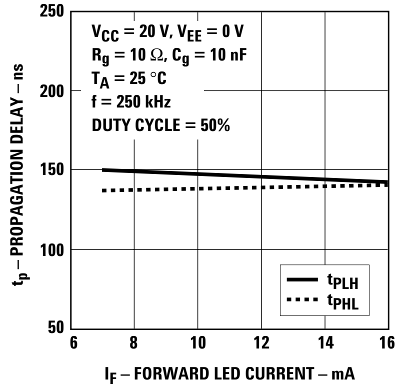


Figure 11. Propagation delay vs. I_F.

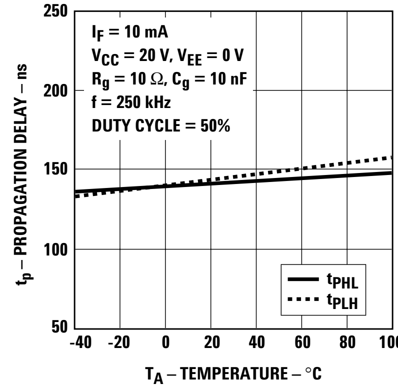


Figure 12. Propagation delay vs. temperature.

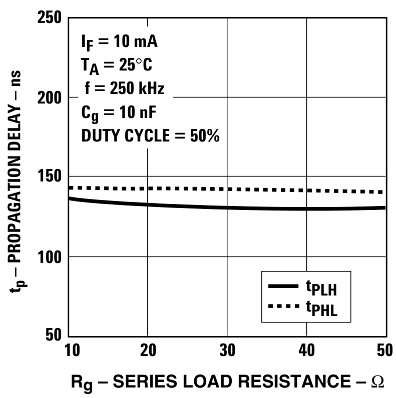


Figure 13. Propagation delay vs. R_g.

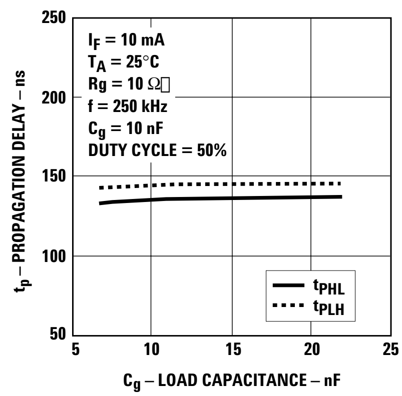


Figure 14. Propagation delay vs. C_g.

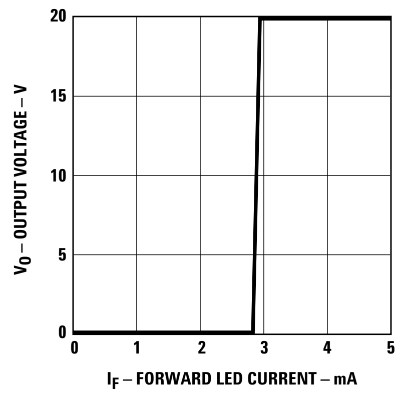


Figure 15. Transfer characteristics.

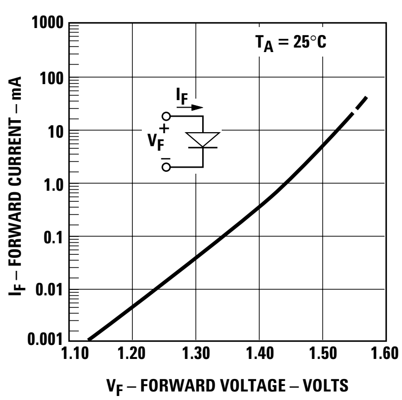


Figure 16. Input current vs. forward voltage.

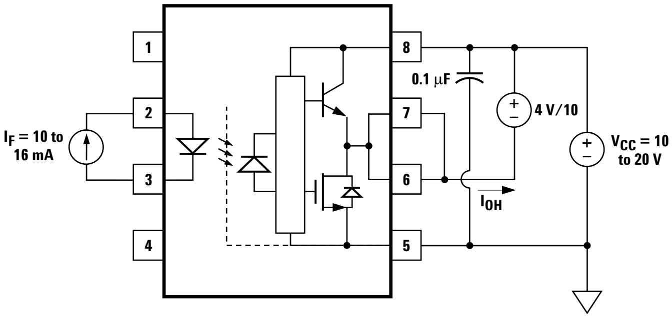


Figure 17. I_{OH} test circuit.

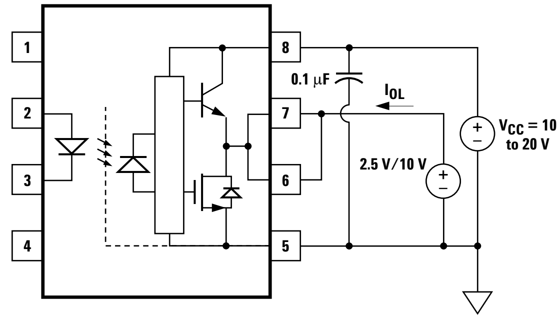


Figure 18. I_{OL} test circuit.

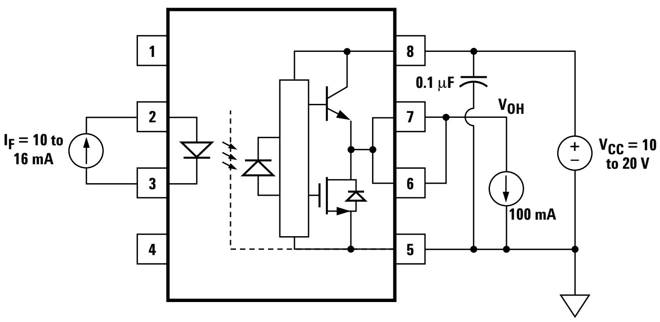


Figure 19. V_{OH} test circuit.

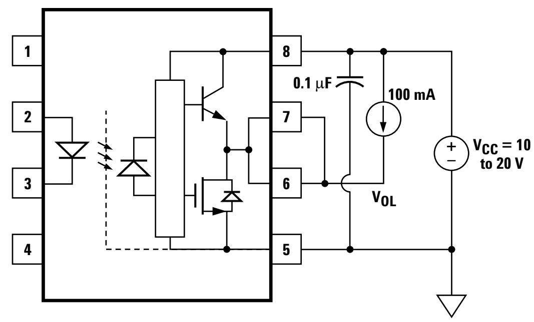


Figure 20. V_{OL} test circuit.

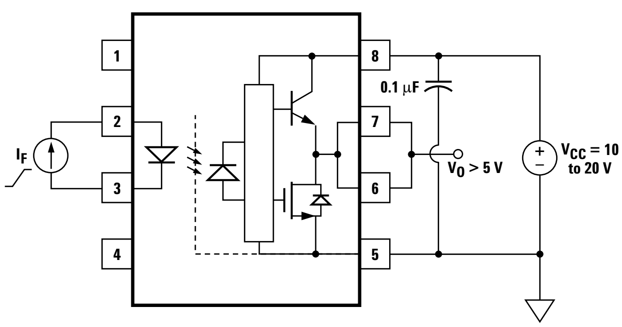


Figure 21. I_{FLH} test circuit.

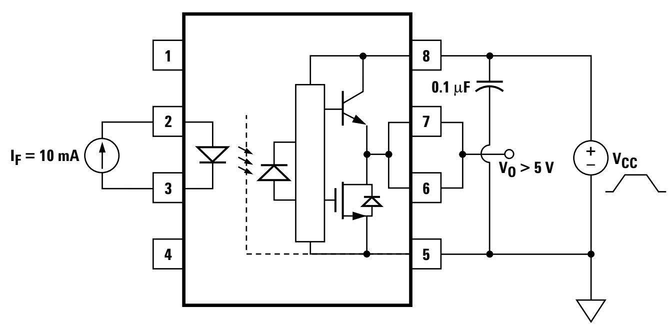


Figure 22. UVLO test circuit.

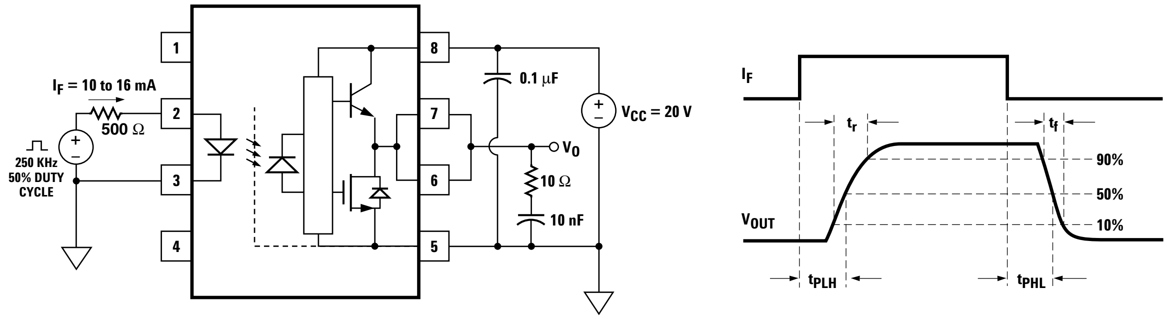


Figure 23. t_{PLH}, t_{PHL}, t_r and t_f test circuit and waveform.

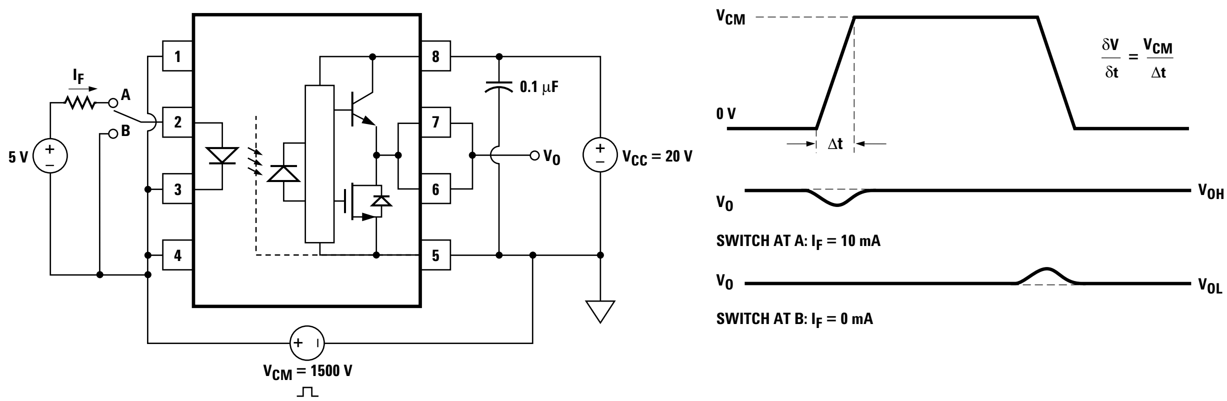


Figure 24. CMR test circuit and waveform.

Applications Information Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3180 has a very low maximum V_{OL} specification of 0.4 V. The HCPL-3180 realizes the very low V_{OL} by using a DMOS transistor with 1 Ω (typical) on resistance in its pull down circuit. When the HCPL-3180 is in the low state, the IGBT gate is shorted to the emitter by R_g + 1 Ω. Minimizing R_g and the lead inductance from the HCPL-3180 to the IGBT gate and emitter (possibly by mounting HCPL-3180 on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in Figure 25. Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3180 input as this can result in unwanted coupling of transient signals into the input of HCPL-3180 and degrade performance.

(If the IGBT drain must be routed near the HCPL-3180 input, then the LED should be reverse biased when in the off state to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3180.)

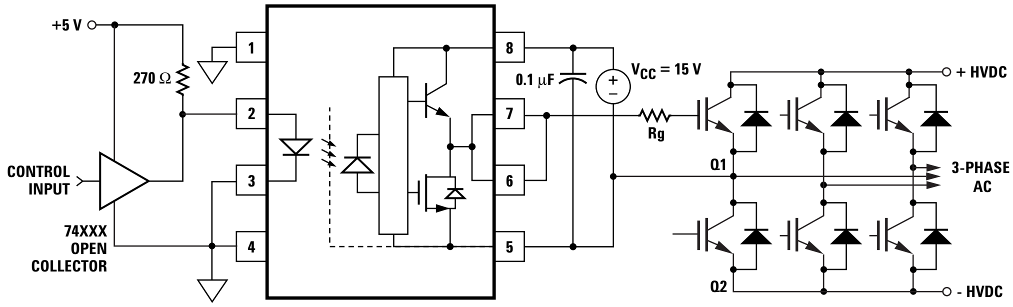


Figure 25. Recommended LED drive and application circuit for HCPL-3180.

Selecting the Gate Resistor (R_g) for HCPL-3180

Step 1: Calculate R_g minimum from the I_{OL} peak specification. The IGBT and R_g in Figure 25 can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3180.

$$R_g \geq \frac{V_{CC} - V_{OL}}{I_{OLPEAK}}$$

$$= \frac{20 - 3}{2}$$

$$= 8.5\ \Omega$$

The V_{OL} value of 3 V in the previous equation is the V_{OL} at the peak current of 2 A. (See Figure 6.)

Step 2: Check the HCPL-3180 power dissipation and increase R_g if necessary. The HCPL-3180 total power dissipation (P_T) is equal to the sum of the emitter power (P_E) and the output power (P_O).

$P_T = P_E + P_O$

$P_E = I_F * V_F *$ Duty Cycle

$P_O = P_{O(BIAS)} + P_{O(SWITCHING)}$

$= I_{CC} * V_{CC} + E_{SW}(R_g;Q_g) * f$

For the circuit in Figure 25 with I_F (worst case) = 16 mA, R_g = 10 Ω, Max Duty Cycle = 80%, Q_g = 100 nC, f = 200 kHz and T_{AMAX} = +75°C:

P_E = 16 mA * 1.8 V * 0.8 = 23 mW

P_O = 4.5 mA * 20 V + 0.85 µ * 200 kHz

= 260 mW ≥ 226 mW ($P_{O(MAX)}$ @ 75°C = 250 mW (5°C * 4.8 mW/°C))

The value of 4.5 mA for I_{CC} in the previous equation was obtained by derating the I_{CC} max of 6 mA to I_{CC} max at +75°C. Since P_O for this case is greater than the $P_{O(MAX)}$, R_g must be increased to reduce the HCPL-3180 power dissipation.

$P_{O(SWITCHING\ MAX)} = P_{O(MAX)} - P_{O(BIAS)}$

= 226 mW – 90 mW

= 136 mW

$$E_{SW(MAX)} = \frac{P_{O(SWITCHING\ MAX)}}{f}$$

$$= \frac{136\ mW}{200\ kHz}$$

= 0.68 µW

For Q_g = 100 nC, a value of E_{sw} = 0.68 µW gives a R_g = 15 Ω.

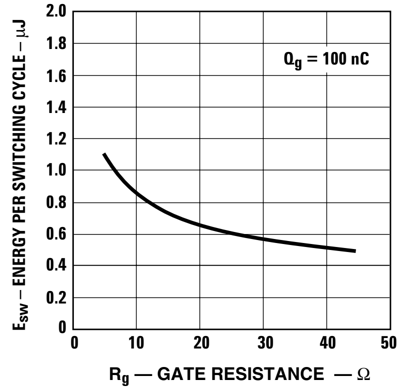


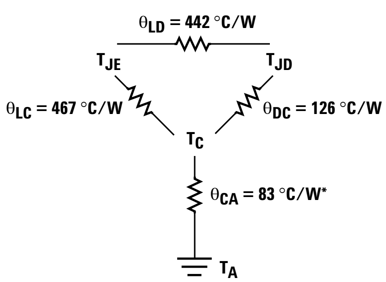
Figure 26. Energy dissipated in the HCPL-3180 and for each IGBT.

Thermal Model
(Discussion applies to HCPL-3180)

The steady state thermal model for the HCPL-3180 is shown in Figure 27. The thermal resistance values given in this model can be used to calculate the temperatures at each node for a given operating condition. As shown by the model, all heat generated flows through θ_{CA} which raises the case temperature TC accordingly. The value of θ_{CA} depends on the conditions of the board design and is, therefore, determined by the designer. The value of θ_{CA} = +83 °C/W was obtained from thermal measurements using a 2.5 x 2.5 inch PC board, with small traces (no ground plane), a single HCPL- 3180 soldered into the center of the board and still air. The absolute maximum power dissipation derating specifications assume a θ_{CA} value of +83 °C/W. From the thermal mode in Figure 27, the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E * (\theta_{LC}//\theta_{LD} + \theta_{DC}) + \theta_{CA}) + P_D * \left[\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right] + T_A$$

$$T_{JD} = P_E * \left[\frac{\theta_{LC} * \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right] + P_D * (\theta_{LC}//\theta_{LD} + \theta_{DC}) + \theta_{CA}) + T_A$$



T_{JE} = LED JUNCTION TEMPERATURE
T_{JD} = DETECTOR IC JUNCTION TEMPERATURE
T_C = CASE TEMPERATURE MEASURED AT THE CENTER OF THE PACKAGE BOTTOM
θ_{LC} = LED-TO-CASE THERMAL RESISTANCE
θ_{LD} = LED-TO-DETECTOR THERMAL RESISTANCE
θ_{DC} = DETECTOR-TO-CASE THERMAL RESISTANCE
θ_{CA} = CASE-TO-AMBIENT THERMAL RESISTANCE

*θ_{CA} WILL DEPEND ON THE BOARD DESIGN AND THE PLACEMENT OF THE PART.

Figure 27. Thermal model.

$$T_{JE} = P_E * (256°C/W + \theta_{CA}) + P_D * (57°C/W + \theta_{CA}) + T_A$$

$$T_{JD} = P_E * (57°C/W + \theta_{CA}) + P_D * (111°C/W + \theta_{CA}) + T_A$$

For example, given P_E = 45 mW,
P_O = 250 mW, T_A = +70 °C and θ_{CA} = +83 °C/W:

$$\begin{aligned} T_{JE} &= P_E * 339°C/W + P_D * 140°C/W + T_A \\ &= 45\ mW * 339°C/W + 250\ mW * 140°C/W + 70°C \\ &= 120°C \end{aligned}$$

$$\begin{aligned} T_{JD} &= P_E * 140°C/W + P_D * 194°C/W + T_A \\ &= 45\ mW * 140°C/W + 250\ mW * 194°C/W + 70°C \\ &= 125°C \end{aligned}$$

T_{JE} and T_{JD} should be limited to +125 °C based on the board layout and part placement (θ_{CA}) specific to the application.

LED Drive Circuit Considerations for Ultra High CMR Performance

Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 28. The HCPL-3180 improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5-8 as shown in Figure 29. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25), can achieve 10 kV/µs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

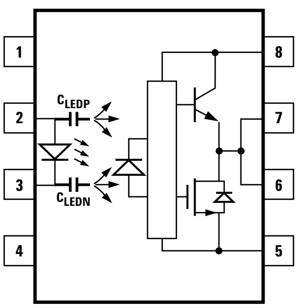


Figure 28. Optocoupler input to output capacitance model for unshielded optocouplers.

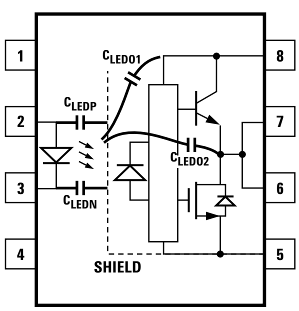


Figure 29. Optocoupler input to output capacitance model for shielded optocouplers.

CMR with the LED On (CMR_H)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by over-driving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I_{FLH} of 8 mA to achieve 10 kV/µs CMR.

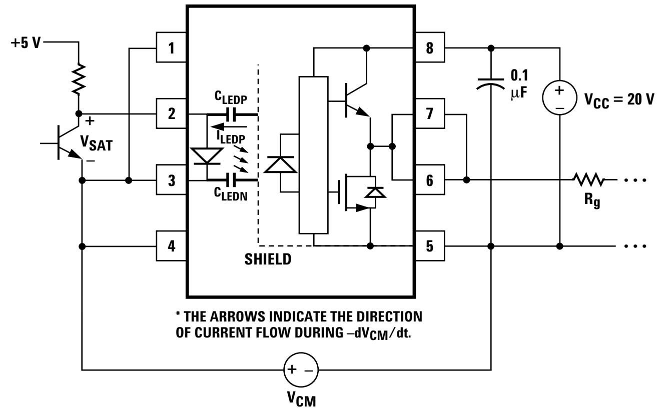


Figure 30. Equivalent circuit for Figure 25 during common mode transient.

CMR with the LED Off (CMR_L)

A high CMR LED drive circuit must keep the LED off ($V_F \leq V_{F(OFF)}$) during common mode transients. For example, during a -dV_{CM}/dt transient in Figure 30, the current flowing through C_{LEDP} also flows through the R_{SAT} and V_{SAT} of the logic gate. As long as the low state voltage developed across the logic gate is less than $V_{F(OFF)}$, the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 31, cannot keep the LED off during a +dV_{CM}/dt transient, since all the current flowing through C_{LEDN} must be supplied by the LED, and it is not recommended for applications requiring ultra high CMR_L performance. Figure 32 is an alternative drive circuit, which like the recommended application circuit (Figure 25), does achieve ultra high CMR performance by shunting the LED in the off state.

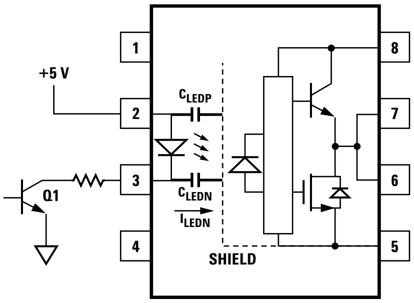


Figure 31. Not recommended open collector drive circuit.

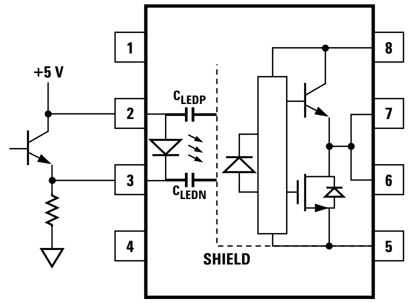


Figure 32. Recommended LED drive circuit for ultra-high CMR.

Under Voltage Lockout Feature

The HCPL-3180 contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions which cause the HCPL-3180 supply voltage (equivalent to the fully charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3180 output is in the high state and the supply voltage drops below the HCPL-3180 V_{UVLO-} threshold (typ 7.5 V) the optocoupler output will go into the low state. When the HCPL-3180 output is in the low state and the supply voltage rises above the HCPL-3180 V_{UVLO+} threshold (typ 8.5 V) the optocoupler output will go into the high state (assume LED is "ON").

IPM Dead Time and Propagation Delay Specifications

The HCPL-3180 includes a Propagation Delay Difference (PDD) specification intended to help designers minimize "dead time" in their power inverter designs. Dead time is the time during which the high and low side power transistors are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high voltage to the low-voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 34. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification, PDD_{MAX}, which is specified to be 90 ns over the operating temperature range of -40 °C to +100 °C.

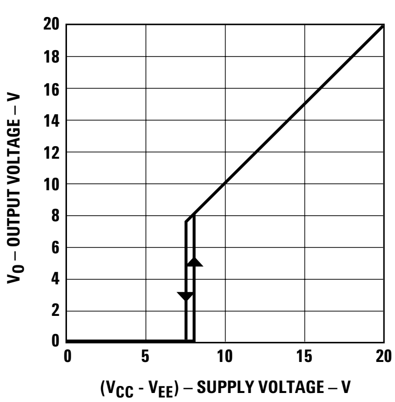


Figure 33. Under voltage lock out.

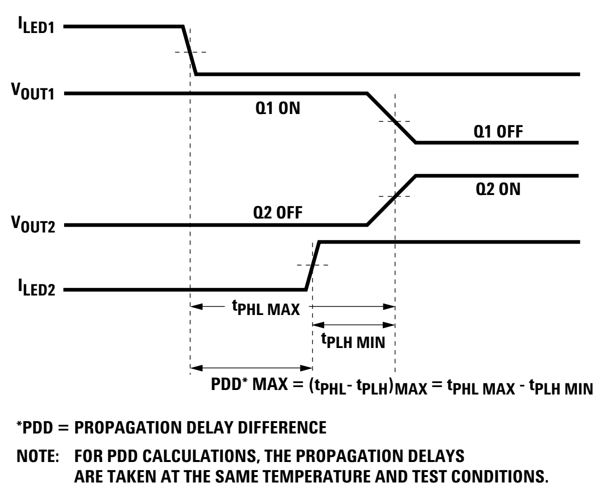


Figure 34. Minimum LED skew for zero dead time.

Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specification as shown in Figure 35. The maximum dead time for the HCPL-3180 is 180 ns (= 90 ns-(- 90 ns)) over the operating temperature range of –40 °C to +100 °C.

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

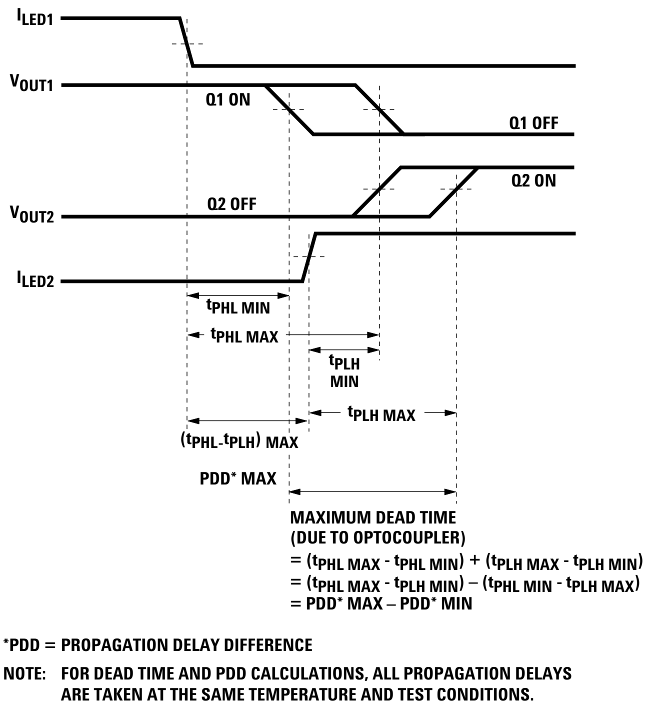


Figure 35. Waveforms for dead time.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV02-0165EN - March 10, 2009