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Contents

| | | |
|---------|--|----|
| 1. | Introduction | 9 |
| 1.1. | flexiFLASH™ Architecture | 10 |
| 1.1.1. | Flexible Logic Architecture | 10 |
| 1.1.2. | Live Update Technology | 10 |
| 1.1.3. | sysDSP™ Block | 10 |
| 1.1.4. | Embedded and Distributed Memory | 10 |
| 1.1.5. | sysCLOCK™ PLLs | 10 |
| 1.1.6. | Flexible I/O Buffer | 10 |
| 1.1.7. | Pre-engineered Source Synchronous Interfaces | 10 |
| 1.1.8. | Density And Package Options | 10 |
| 1.1.9. | Flexible Device Configuration | 10 |
| 1.1.10. | System Level Support | 10 |
| 2. | Architecture | 12 |
| 2.1. | Architecture Overview | 12 |
| 2.2. | PFU Blocks | 13 |
| 2.2.1. | Slice | 14 |
| 2.2.2. | Modes of Operation | 16 |
| 2.3. | Routing | 17 |
| 2.4. | sysCLOCK Phase Locked Loops (PLL) | 17 |
| 2.5. | Clock Dividers | 18 |
| 2.6. | Clock Distribution Network | 19 |
| 2.6.1. | Primary Clock Sources | 19 |
| 2.6.2. | Secondary Clock Sources | 20 |
| 2.6.3. | Edge Clock Sources | 21 |
| 2.6.4. | Primary Clock Routing | 22 |
| 2.6.5. | Dynamic Clock Select (DCS) | 23 |
| 2.6.6. | Secondary Clock/Control Routing | 23 |
| 2.6.7. | Slice Clock Selection | 25 |
| 2.6.8. | Edge Clock Routing | 25 |
| 2.7. | sysMEM Memory | 26 |
| 2.7.1. | sysMEM Memory Block | 26 |
| 2.7.2. | Bus Size Matching | 27 |
| 2.7.3. | FlashBAK EBR Content Storage | 27 |
| 2.7.4. | Memory Cascading | 27 |
| 2.7.5. | Single, Dual and Pseudo-Dual Port Modes | 28 |
| 2.8. | Memory Core Reset | 28 |
| 2.8.1. | EBR Asynchronous Reset | 28 |
| 2.9. | sysDSP™ Block | 29 |
| 2.9.1. | sysDSP Block Approach Compare to General DSP | 29 |
| 2.9.2. | sysDSP Block Capabilities | 30 |
| 2.9.3. | MULT sysDSP Element | 31 |
| 2.9.4. | MAC sysDSP Element | 32 |
| 2.9.5. | MULTADDSUB sysDSP Element | 33 |
| 2.9.6. | MULTADDSUBSUM sysDSP Element | 34 |
| 2.9.7. | Clock, Clock Enable and Reset Resources | 35 |
| 2.9.8. | Signed and Unsigned with Different Widths | 35 |
| 2.9.9. | OVERFLOW Flag from MAC | 35 |
| 2.9.10. | IPexpress™ | 36 |
| 2.10. | Optimized DSP Functions | 36 |
| 2.10.1. | Resources Available in the LatticeXP2 Family | 36 |
| 2.10.2. | LatticeXP2 DSP Performance | 36 |
| 2.11. | Programmable I/O Cells (PIC) | 37 |

| | | |
|---------|--|----|
| 2.12. | PIO..... | 38 |
| 2.12.1. | Input Register Block..... | 39 |
| 2.12.2. | Output Register Block..... | 40 |
| 2.12.3. | Tristate Register Block..... | 42 |
| 2.12.4. | Control Logic Block..... | 42 |
| 2.13. | DDR Memory Support..... | 42 |
| 2.13.1. | DLL Calibrated DQS Delay Block..... | 43 |
| 2.13.2. | Polarity Control Logic..... | 45 |
| 2.13.3. | DQSXFER..... | 45 |
| 2.14. | sysI/O Buffer..... | 46 |
| 2.14.1. | sysI/O Buffer Banks..... | 46 |
| 2.14.2. | Typical sysI/O I/O Behavior During Power-up..... | 47 |
| 2.14.3. | Supported sysI/O Standards..... | 47 |
| 2.14.4. | Hot Socketing..... | 49 |
| 2.15. | IEEE 1149.1-Compliant Boundary Scan Testability..... | 50 |
| 2.16. | flexiFLASH Device Configuration..... | 50 |
| 2.16.1. | Serial TAG Memory..... | 51 |
| 2.16.2. | Live Update Technology..... | 51 |
| 2.16.3. | Soft Error Detect (SED) Support..... | 52 |
| 2.16.4. | On-Chip Oscillator..... | 52 |
| 2.17. | Density Shifting..... | 53 |
| 3. | DC and Switching Characteristics..... | 54 |
| 3.1. | Absolute Maximum Ratings..... | 54 |
| 3.2. | Recommended Operating Conditions..... | 54 |
| 3.3. | On-Chip Flash Memory Specifications..... | 55 |
| 3.4. | Hot Socketing Specifications..... | 55 |
| 3.5. | ESD Performance..... | 55 |
| 3.6. | DC Electrical Characteristics..... | 55 |
| 3.7. | Supply Current (Standby)..... | 56 |
| 3.8. | Initialization Supply Current..... | 57 |
| 3.9. | Programming and Erase Flash Supply Current..... | 58 |
| 3.10. | sysI/O Recommended Operating Conditions..... | 59 |
| 3.11. | sysI/O Single-Ended DC Electrical Characteristics..... | 60 |
| 3.12. | sysI/O Differential Electrical Characteristics..... | 61 |
| 3.12.1. | LVDS 61..... | |
| 3.12.2. | Differential HSTL and SSTL..... | 61 |
| 3.12.3. | LVDS25E..... | 61 |
| 3.12.4. | LVC MOS33D..... | 62 |
| 3.12.5. | BLVDS..... | 62 |
| 3.12.6. | LVPECL..... | 63 |
| 3.12.7. | RS DS 64..... | |
| 3.12.8. | MLVDS..... | 65 |
| 3.13. | Typical Building Block Function Performance..... | 66 |
| 3.13.1. | Pin-to-Pin Performance (LVC MOS25 12 mA Drive)..... | 66 |
| 3.13.2. | Register-to-Register Performance..... | 67 |
| 3.14. | Typical Building Block Function Performance – ZE Devices..... | 68 |
| 3.14.1. | Pin-to-Pin Performance (LVC MOS25 12 mA Drive)..... | 68 |
| 3.14.2. | Register-to-Register Performance..... | 68 |
| 3.15. | Derating Timing Tables..... | 68 |
| 3.16. | LatticeXP2 External Switching Characteristics ¹ | 69 |
| 3.17. | LatticeXP2 Internal Switching Characteristics ¹ | 72 |
| 3.18. | EBR Timing Diagrams..... | 74 |
| 3.19. | LatticeXP2 Family Timing Adders..... | 76 |
| 3.20. | sysCLOCK PLL Timing..... | 79 |

| | | |
|--------|--|----|
| 3.21. | LatticeXP2 sysCONFIG Port Timing Specifications | 80 |
| 3.22. | On-Chip Oscillator and Configuration Master Clock Characteristics | 81 |
| 3.23. | Flash Download Time (from On-Chip Flash to SRAM) | 81 |
| 3.24. | Flash Program Time | 82 |
| 3.25. | Flash Erase Time | 82 |
| 3.26. | FlashBAK Time (from EBR to Flash)..... | 83 |
| 3.27. | JTAG Port Timing Specifications..... | 83 |
| 3.28. | Switching Test Conditions | 84 |
| 4. | Pinout Information | 86 |
| 4.1. | Signal Descriptions..... | 86 |
| 4.2. | PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin | 88 |
| 4.3. | Pin Information Summary..... | 89 |
| 4.4. | Logic Signal Connections..... | 91 |
| 4.5. | Thermal Management | 91 |
| 4.6. | For Further Information..... | 91 |
| 5. | Ordering Information | 92 |
| 5.1. | Part Number Description | 92 |
| 5.2. | Ordering Information..... | 92 |
| 5.2.1. | Lead-Free Packaging | 93 |
| 5.2.2. | Conventional Packaging | 95 |
| 6. | Supplemental Information | 97 |
| | Technical Support Assistance | 98 |
| | Revision History | 99 |

Figures

| | |
|---|----|
| Figure 2.1. Simplified Block Diagram, LatticeXP2-17 Device (Top Level) | 13 |
| Figure 2.2. PFU Diagram | 14 |
| Figure 2.3. Slice Diagram | 15 |
| Figure 2.4. General Purpose PLL (GPLL) Diagram | 18 |
| Figure 2.5. Clock Divider Connections | 19 |
| Figure 2.6. Primary Clock Sources for XP2-17 | 20 |
| Figure 2.7. Secondary Clock Sources | 21 |
| Figure 2.8. Edge Clock Sources | 22 |
| Figure 2.9. Per Quadrant Primary Clock Selection | 23 |
| Figure 2.10. DCS Waveforms | 23 |
| Figure 2.11. Secondary Clock Regions XP2-40 | 24 |
| Figure 2.12. Secondary Clock Selection | 24 |
| Figure 2.13. Slice0 through Slice2 Clock Selection | 25 |
| Figure 2.14. Slice0 through Slice2 Control Selection | 25 |
| Figure 2.15. Edge Clock Mux Connections | 26 |
| Figure 2.16. FlashBAK Technology | 27 |
| Figure 2.17. Memory Core Reset | 28 |
| Figure 2.18. EBR Asynchronous Reset (Including GSR) Timing Diagram | 29 |
| Figure 2.19. Comparison of General DSP and LatticeXP2 Approaches | 30 |
| Figure 2.20. MULT sysDSP Element | 31 |
| Figure 2.21. MAC sysDSP | 32 |
| Figure 2.22. MULTADDSUB | 33 |
| Figure 2.23. MULTADDSUBSUM | 34 |
| Figure 2.24. Accumulator Overflow/Underflow | 35 |
| Figure 2.25. PIC Diagram..... | 37 |
| Figure 2.26. Input Register Block | 40 |
| Figure 2.27. Output and Tristate Block | 41 |
| Figure 2.28. DQS Input Routing (Left and Right)..... | 42 |
| Figure 2.29. DQS Input Routing (Top and Bottom) | 43 |
| Figure 2.30. Edge Clock, DLL Calibration and DQS Local Bus Distribution | 44 |
| Figure 2.31. DQS Local Bus | 45 |
| Figure 2.32. LatticeXP2 Banks | 46 |
| Figure 2.33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices | 50 |
| Figure 2.34. Serial TAG Memory Diagram | 51 |
| Figure 3.1. LVDS25E Output Termination Example | 61 |
| Figure 3.2. BLVDS Multi-point Output Example..... | 62 |
| Figure 3.3. Differential LVPECL | 63 |
| Figure 3.4. RSDS (Reduced Swing Differential Standard)..... | 64 |
| Figure 3.5. MLVDS (Reduced Swing Differential Standard) | 65 |
| Figure 3.6. Read/Write Mode (Normal)..... | 74 |
| Figure 3.7. Read/Write Mode with Input and Output Registers | 75 |
| Figure 3.8. Write Through (SP Read/Write on Port A, Input Registers Only) | 75 |
| Figure 3.9. Master SPI Configuration Waveforms | 81 |
| Figure 3.10. JTAG Port Timing Waveforms | 84 |
| Figure 3.11. Output Test Load, LVTTTL and LVCMOS Standards | 84 |
| Figure 5.1. LatticeXP2 Part Number Description | 92 |

Tables

| | |
|--|----|
| Table 1.1. LatticeXP2 Family Selection Guide | 11 |
| Table 2.1. Resources and Modes Available per Slice | 14 |
| Table 2.2. Slice Signal Descriptions | 16 |
| Table 2.3. Number of Slices Required For Implementing Distributed RAM | 17 |
| Table 2.4. GPLL Block Signal Descriptions | 18 |
| Table 2.5. sysMEM Block Configurations | 27 |
| Table 2.6. Maximum Number of Elements in a Block | 30 |
| Table 2.7. Sign Extension Example | 35 |
| Table 2.8. Maximum Number of DSP Blocks in the LatticeXP2 Family | 36 |
| Table 2.9. Embedded SRAM/TAG Memory in the LatticeXP2 Family | 36 |
| Table 2.10. DSP Performance | 36 |
| Table 2.11. PIO Signal List | 38 |
| Table 2.12. Supported Input Standards | 48 |
| Table 2.13. Supported Output Standards | 49 |
| Table 2.14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode | 52 |
| Table 3.1. Absolute Maximum Ratings ^{1, 2, 3} | 54 |
| Table 3.2. Recommended Operating Conditions | 54 |
| Table 3.3. On-Chip Flash Memory Specifications | 55 |
| Table 3.4. Hot Socketing Specifications | 55 |
| Table 3.5. DC Electrical Characteristics | 55 |
| Table 3.6. Supply Current (Standby) ^{1, 2, 3, 4} | 56 |
| Table 3.7. Initialization Supply Current ^{1, 2, 3, 4, 5} | 57 |
| Table 3.8. Programming and Erase Flash Supply Current ^{1, 2, 3, 4, 5} | 58 |
| Table 3.9. sysI/O Recommended Operating Conditions | 59 |
| Table 3.10. sysI/O Single-Ended DC Electrical Characteristics | 60 |
| Table 3.11. LVDS | 61 |
| Table 3.12. LVDS25E DC Conditions | 62 |
| Table 3.13. BLVDS DC Conditions | 63 |
| Table 3.14. LVPECL DC Conditions | 64 |
| Table 3.15. RSDS DC Conditions | 65 |
| Table 3.16. MLVDS DC Conditions | 66 |
| Table 3.17. Pin-to-Pin Performance (LVCMOS25 12 mA Drive) | 66 |
| Table 3.18. Register-to-Register Performance | 67 |
| Table 3.19. Pin-to-Pin Performance (LVCMOS25 12 mA Drive) | 68 |
| Table 3.20. Register-to-Register Performance | 68 |
| Table 3.21. LatticeXP2 External Switching Characteristics | 69 |
| Table 3.22. LatticeXP2 Family Timing Adders ^{1, 2, 3, 4} | 76 |
| Table 3.23. sysCLOCK PLL Timing | 79 |
| Table 3.24. LatticeXP2 sysCONFIG Port Timing Specifications | 80 |
| Table 3.25. On-Chip Oscillator and Configuration Master Clock Characteristics | 81 |
| Table 3.26. Flash Download Time (from On-Chip Flash to SRAM) | 81 |
| Table 3.27. Flash Program Time | 82 |
| Table 3.28. Flash Erase Time | 82 |
| Table 3.29. FlashBAK Time (from EBR to Flash) | 83 |
| Table 3.30. FlashBAK Time (from EBR to Flash) | 83 |
| Table 3.31. Test Fixture Required Components, Non-Terminated Interfaces | 85 |
| Table 4.1. Signal Descriptions | 86 |
| Table 4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin | 88 |
| Table 4.3. Pin Information Summary | 89 |

Table 5.1. Lead-Free Packaging.....93

Table 5.2. Lead-Free Packaging.....94

Table 5.3. Conventional Packaging (Commercial).....95

Table 5.4. Conventional Packaging (Industrial).....96

1. Introduction

LatticeXP2™ devices combine a Look-up Table (LUT) based FPGA fabric with non-volatile Flash cells in an architecture referred to as flexiFLASH.

The flexiFLASH approach provides benefits including instant-on, infinite reconfigurability, on chip storage with FlashBAK embedded block memory and Serial TAG memory and design security. The parts also support Live Update technology with TransFR, 128-bit AES Encryption and Dual-boot technologies.

The LatticeXP2 FPGA fabric was optimized for the new technology from the outset with high performance and low cost in mind. LatticeXP2 devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support and enhanced sysDSP blocks.

Lattice Diamond® design software allows large and complex designs to be efficiently implemented using the LatticeXP2 family of FPGA devices. Synthesis library support for LatticeXP2 is available for popular logic synthesis tools. The Diamond software uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeXP2 device. The Diamond tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-designed Intellectual Property (IP) LatticeCORE™ modules for the LatticeXP2 family. By using these IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. flexiFLASH™ Architecture

1.1.1. Flexible Logic Architecture

- Instant-on
- Infinitely reconfigurable
- Single chip
- FlashBAK™ technology
- Serial TAG memory
- Design security

1.1.2. Live Update Technology

- TransFR™ technology
- Secure updates with 128 bit AES encryption
- Dual-boot with external SPI

1.1.3. sysDSP™ Block

- Three to eight blocks for high performance Multiply and Accumulate
- 12 to 32 18x18 multipliers
- Each block supports one 36x36 multiplier or four 18x18 or eight 9x9 multipliers

1.1.4. Embedded and Distributed Memory

- Up to 885 Kbits sysMEM™ EBR
- Up to 83 Kbits Distributed RAM

1.1.5. sysCLOCK™ PLLs

- Up to four analog PLLs per device
- Clock multiply, divide and phase shifting

1.1.6. Flexible I/O Buffer

- sysI/O™ buffer supports:
 - LVCMOS 33/25/18/15/12; LVTTTL
 - SSTL 33/25/18 class I, II
 - HSTL15 class I; HSTL18 class I, II
 - PCI
 - LVDS, Bus-LVDS, MLVDS, LVPECL, RSDS

1.1.7. Pre-engineered Source Synchronous Interfaces

- DDR / DDR2 interfaces up to 200 MHz
- 7:1 LVDS interfaces support display applications
- XGMII

1.1.8. Density And Package Options

- 5k to 40k LUT4s, 86 to 540 I/O
- csBGA, TQFP, PQFP, ftBGA and fpBGA packages
- Density migration supported

1.1.9. Flexible Device Configuration

- SPI (master and slave) Boot Flash Interface
- Dual Boot Image supported
- Soft Error Detect (SED) macro embedded

1.1.10. System Level Support

- IEEE 1149.1 and IEEE 1532 Compliant
- On-chip oscillator for initialization and general use
- Devices operate with 1.2 V power supply

Table 1.1. LatticeXP2 Family Selection Guide

| Device | XP2-5 | XP2-8 | XP2-17 | XP2-30 | XP2-40 |
|--------------------------------------|-------|-------|--------|--------|--------|
| LUTs (K) | 5 | 8 | 17 | 29 | 40 |
| Distributed RAM (KBits) | 10 | 18 | 35 | 56 | 83 |
| EBR SRAM (KBits) | 166 | 221 | 276 | 387 | 885 |
| EBR SRAM Blocks | 9 | 12 | 15 | 21 | 48 |
| sysDSP Blocks | 3 | 4 | 5 | 7 | 8 |
| 18 x 18 Multipliers | 12 | 16 | 20 | 28 | 32 |
| VCC Voltage | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| GPLL | 2 | 2 | 4 | 4 | 4 |
| Max Available I/O | 172 | 201 | 358 | 472 | 540 |
| Packages and I/O Combinations | | | | | |
| 132-Ball csBGA (8 x 8 mm) | 86 | 86 | | | |
| 144-Pin TQFP (20 x 20 mm) | 100 | 100 | | | |
| 208-Pin PQFP (28 x 28 mm) | 146 | 146 | 146 | | |
| 256-Ball ftBGA (17 x 17 mm) | 172 | 201 | 201 | 201 | |
| 484-Ball fpBGA (23 x 23 mm) | | | 358 | 363 | 363 |
| 672-Ball fpBGA (27 x 27 mm) | | | | 472 | 540 |

2. Architecture

2.1. Architecture Overview

Each LatticeXP2 device contains an array of logic blocks surrounded by Programmable I/O Cells (PIC). Interspersed between the rows of logic blocks are rows of sysMEM™ Embedded Block RAM (EBR) and a row of sysDSP™ Digital Signal Processing blocks as shown in [Figure 2.1](#).

On the left and right sides of the Programmable Functional Unit (PFU) array, there are Non-volatile Memory Blocks. In configuration mode the nonvolatile memory is programmed via the IEEE 1149.1 TAP port or the sysCONFIG™ peripheral port. On power up, the configuration data is transferred from the Non-volatile Memory Blocks to the configuration SRAM. With this technology, expensive external configuration memory is not required, and designs are secured from unauthorized read-back. This transfer of data from non-volatile memory to configuration SRAM via wide busses happens in microseconds, providing an “instant-on” capability that allows easy interfacing in many applications. LatticeXP2 devices can also transfer data from the sysMEM EBR blocks to the Non-volatile Memory Blocks at user request.

There are two kinds of logic blocks, the PFU and the PFU without RAM (PFF). The PFU contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFF block contains building blocks for logic, arithmetic and ROM functions. Both PFU and PFF blocks are optimized for flexibility allowing complex designs to be implemented quickly and efficiently. Logic Blocks are arranged in a two-dimensional array. Only one type of block is used per row.

LatticeXP2 devices contain one or more rows of sysMEM EBR blocks. sysMEM EBRs are large dedicated 18 Kbit memory blocks. Each sysMEM block can be configured in a variety of depths and widths of RAM or ROM. In addition, LatticeXP2 devices contain up to two rows of DSP Blocks. Each DSP block has multipliers and adder/accumulators, which are the building blocks for complex signal processing capabilities.

Each PIC block encompasses two PIOs (PIO pairs) with their respective sysI/O buffers. The sysI/O buffers of the LatticeXP2 devices are arranged into eight banks, allowing the implementation of a wide variety of I/O standards. PIO pairs on the left and right edges of the device can be configured as LVDS transmit/receive pairs. The PIC logic also includes pre-engineered support to aid in the implementation of high speed source synchronous standards such as 7:1 LVDS interfaces, found in many display applications, and memory interfaces including DDR and DDR2.

The LatticeXP2 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration setting, allowing device entering to a known state for predictable system function.

Other blocks provided include PLLs and configuration functions. The LatticeXP2 architecture provides up to four General Purpose PLLs (GPLL) per device. The GPLL blocks are located in the corners of the device.

The configuration block that supports features such as configuration bit-stream de-encryption, transparent updates and dual boot support is located between banks two and three. Every device in the LatticeXP2 family supports a sysCONFIG port, muxed with bank seven I/O, which supports serial device configuration. A JTAG port is provided between banks two and three.

This family also provides an on-chip oscillator. LatticeXP2 devices use 1.2 V as their core voltage.

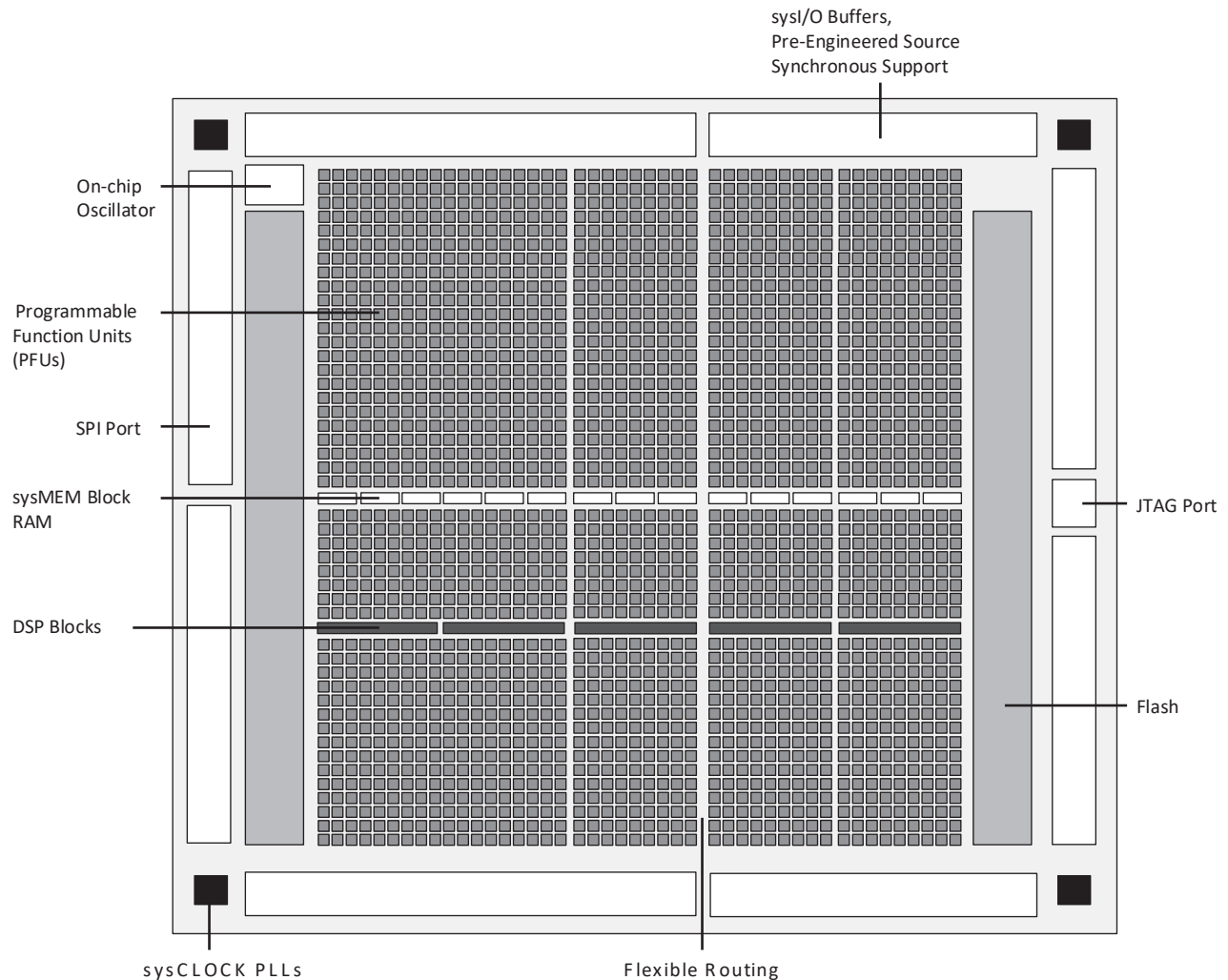


Figure 2.1. Simplified Block Diagram, LatticeXP2-17 Device (Top Level)

2.2. PFU Blocks

The core of the LatticeXP2 device is made up of logic blocks in two forms, PFUs and PFFs. PFUs can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. PFF blocks can be programmed to perform logic, arithmetic and ROM functions. Except where necessary, the remainder of this data sheet uses the term PFU to refer to both PFU and PFF blocks.

Each PFU block consists of four interconnected slices, numbered Slice 0 through Slice 3, as shown in [Figure 2.2](#). All the interconnections to and from PFU blocks are from routing. There are 50 inputs and 23 outputs associated with each PFU block.

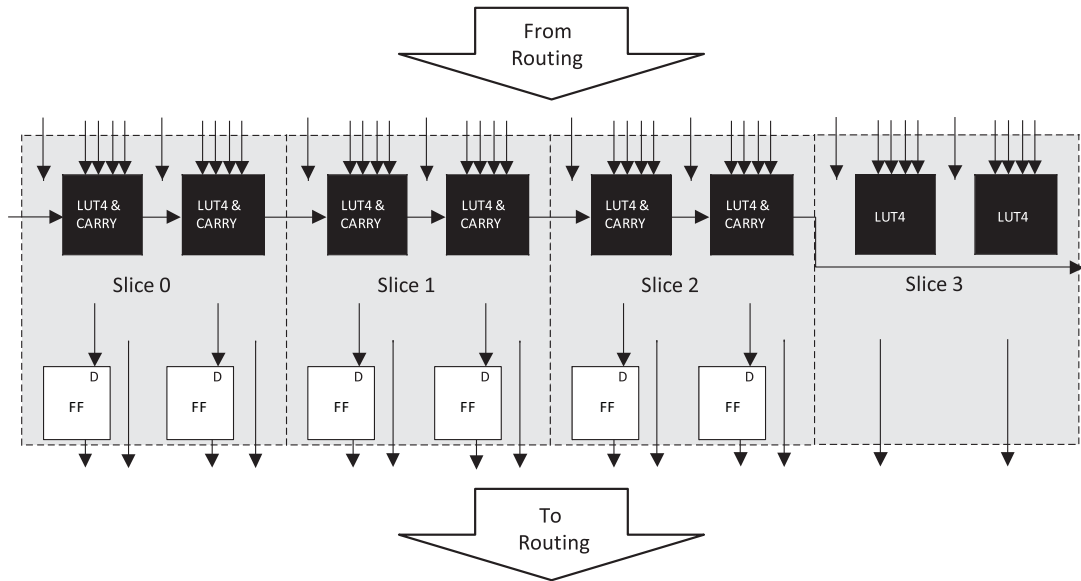


Figure 2.2. PFU Diagram

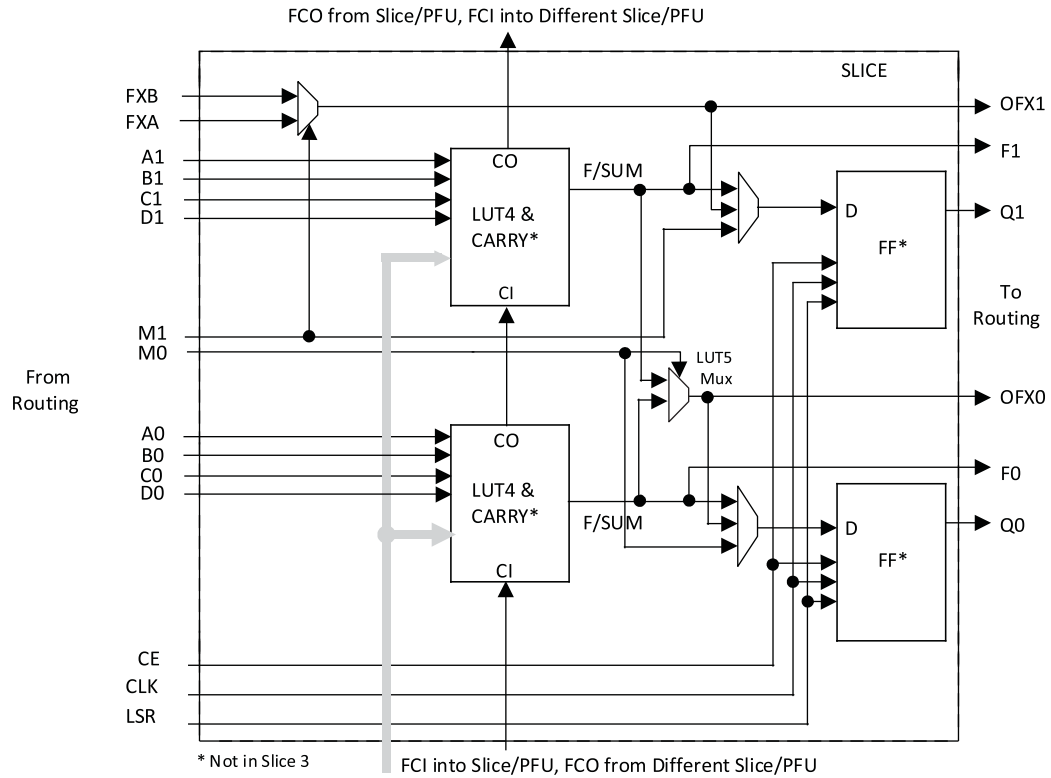
2.2.1. Slice

Slice 0 through Slice 2 contain two 4-input combinatorial Look-Up Tables (LUT4), which feed two registers. Slice 3 contains two LUT4s and no registers. For PFUs, Slice 0 and Slice 2 can also be configured as distributed memory, a capability not available in PFF blocks. Table 2.1 shows the capability of the slices in both PFF and PFU blocks along with the operation modes they enable. In addition, each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 2.3 shows an overview of the internal logic of the slice. The registers in the slice can be configured as positive/ negative edge triggered or level sensitive clocks.

Table 2.1. Resources and Modes Available per Slice

| Slice | PFU BLock | | PFF Block | |
|---------|-------------------------|-------------------------|-------------------------|--------------------|
| | Resources | Modes | Resources | Modes |
| Slice 0 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 1 | 2 LUT4s and 2 Registers | Logic, Ripple, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 2 | 2 LUT4s and 2 Registers | Logic, Ripple, RAM, ROM | 2 LUT4s and 2 Registers | Logic, Ripple, ROM |
| Slice 3 | 2 LUT4s | Logic, ROM | 2 LUT4s | Logic, ROM |

Slice 0 through Slice 2 have 14 input signals: 13 signals from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six to routing and one to carry-chain (to the adjacent PFU). Slice 3 has 13 input signals from routing and four signals to routing. Table 2.2 lists the signals associated with Slice 0 to Slice 2.



For Slices 0 and 2, memory control signals are generated from Slice 1 as follows:

WCK is CLK

WRE is from LSR

DI[3:2] for Slice 2 and DI[1:0] for Slice 0 data

WAD [A:D] is a 4 bit address from slice 1 LUT input

Figure 2.3. Slice Diagram

Table 2.2. Slice Signal Descriptions

| Function | Type | Signal Names | Description |
|----------|--------------------|----------------|--|
| Input | Data signal | A0, B0, C0, D0 | Inputs to LUT4 |
| Input | Data signal | A1, B1, C1, D1 | Inputs to LUT4 |
| Input | Multi-purpose | M0 | Multipurpose Input |
| Input | Multi-purpose | M1 | Multipurpose Input |
| Input | Control signal | CE | Clock Enable |
| Input | Control signal | LSR | Local Set/Reset |
| Input | Control signal | CLK | System Clock |
| Input | Inter-PFU signal | FCI | Fast Carry-In ¹ |
| Input | Inter-slice signal | FXA | Intermediate signal to generate LUT6 and LUT7 |
| Input | Inter-slice signal | FXB | Intermediate signal to generate LUT6 and LUT7 |
| Output | Data signals | F0, F1 | LUT4 output register bypass signals |
| Output | Data signals | Q0, Q1 | Register outputs |
| Output | Data signals | OFX0 | Output of a LUT5 MUX |
| Output | Data signals | OFX1 | Output of a LUT6, LUT7, LUT8 ² MUX depending on the slice |
| Output | Inter-PFU signal | FCO | Slice 2 of each PFU is the fast carry chain output ¹ |

Notes:

1. See [Figure 2.3](#) for connection details.
2. Requires two PFUs.

2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

Logic Mode

In this mode, the LUTs in each slice are configured as LUT4s. A LUT4 has 16 possible input combinations. Four input logic functions are generated by programming the LUT4. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger LUTs such as LUT6, LUT7 and LUT8, can be constructed by concatenating two or more slices. Note that a LUT8 requires more than four slices.

Ripple Mode

Ripple mode allows efficient implementation of small arithmetic functions. In ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/Down counter with async clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
- A greater-than-or-equal-to B
- A not-equal-to B
- A less-than-or-equal-to B

Two carry signals, FCI and FCO, are generated per slice in this mode, allowing fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In this mode, a 16x4-bit distributed Single Port RAM (SPR) can be constructed using each LUT block in Slice 0 and Slice 2 as a 16x1-bit memory. Slice 1 is used to provide memory address and control signals. A 16x2-bit Pseudo Dual Port RAM (PDPR) memory is created by using one slice as the read-write port and the other companion slice as the read-only port.

The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. [Table 2.3](#) shows the number of slices required to implement different distributed RAM primitives. For more information on using RAM in LatticeXP2 devices, see [LatticeXP2 Memory Usage Guide \(TN1137\)](#).

Table 2.3. Number of Slices Required For Implementing Distributed RAM

| | SPR 16x4 | PDPR 16x4 |
|------------------|----------|-----------|
| Number of Slices | 3 | 3 |

Note: SPR = Single Port RAM, PDPR = Pseudo Dual Port RAM

ROM Mode

ROM mode uses the LUT logic; hence, Slices 0 through 3 can be used in the ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

2.3. Routing

There are many resources provided in the LatticeXP2 devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments. The inter-PFU connections are made with x1 (spans two PFU), x2 (spans three PFU) or x6 (spans seven PFU) connections. The x1 and x2 connections provide fast and efficient connections in horizontal and vertical directions. The x2 and x6 resources are buffered to allow both short and long connections routing between PFUs.

The LatticeXP2 family has an enhanced routing architecture to produce a compact design. The Diamond design tool takes the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.4. sysCLOCK Phase Locked Loops (PLL)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The LatticeXP2 family supports between two and four full featured General Purpose PLLs (GPLL). The architecture of the GPLL is shown in [Figure 2.4](#).

CLKI, the PLL reference frequency, is provided either from the pin or from routing; it feeds into the Input Clock Divider block. CLKFB, the feedback signal, is generated from CLKOP (the primary clock output) or from a user clock pin/logic. CLKFB feeds into the Feedback Divider and is used to multiply the reference frequency.

Both the input path and feedback signals enter the Voltage Controlled Oscillator (VCO) block. The phase and frequency of the VCO are determined from the input path and feedback signals. A LOCK signal is generated by the VCO to indicate that the VCO is locked with the input clock signal.

The output of the VCO feeds into the CLKOP Divider, a post-scalar divider. The duty cycle of the CLKOP Divider output can be fine tuned using the Duty Trim block, which creates the CLKOP signal. By allowing the VCO to operate at higher frequencies than CLKOP, the frequency range of the GPLL is expanded. The output of the CLKOP Divider is passed through the CLKOK Divider, a secondary clock divider, to generate lower frequencies for the CLKOK output. For applications that require even lower frequencies, the CLKOP signal is passed through a divide-by-three divider to produce the CLKOK2 output. The CLKOK2 output is provided for applications that use source synchronous logic. The Phase/Duty Cycle/Duty Trim block is used to adjust the phase and duty cycle of the CLKOP Divider output to generate the CLKOS signal. The phase/duty cycle setting can be pre-programmed or dynamically adjusted.

The clock outputs from the GPLL; CLKOP, CLKOK, CLKOK2 and CLKOS, are fed to the clock distribution network.

For further information on the GPLL, see [LatticeXP2 sysCLOCK PLL Design and Usage Guide \(TN1126\)](#).

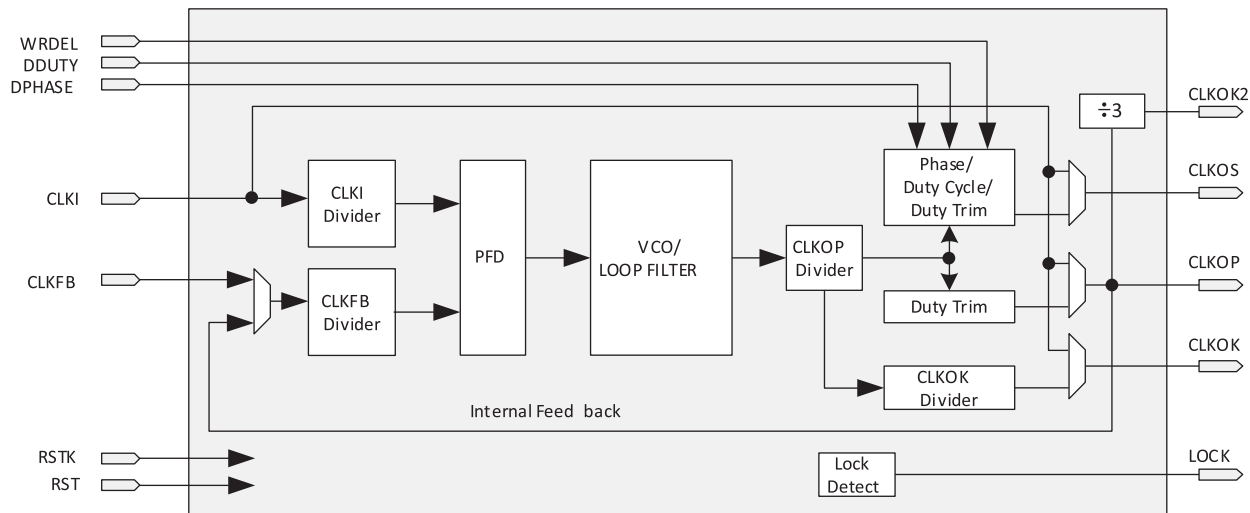


Figure 2.4. General Purpose PLL (GPLL) Diagram

Table 2.4 provides a description of the signals in the GPLL blocks.

Table 2.4. GPLL Block Signal Descriptions

| Signal | I/O | Description |
|--------------|-----|--|
| CLKI | I | Clock input from external pin or routing |
| CLKFB | I | PLL feedback input from CLKOP (PLL internal), from clock net (CLKOP) or from a user clock (PIN or logic) |
| RST | I | "1" to reset PLL counters, VCO, charge pumps and M-dividers |
| RSTK | I | "1" to reset K-divider |
| DPHASE [3:0] | I | DPA Phase Adjust input |
| DDUTY [3:0] | I | DPA Duty Cycle Select input |
| WRDEL | I | DPA Fine Delay Adjust input |
| CLKOS | O | PLL output clock to clock tree (phase shifted/duty cycle changed) |
| CLKOP | O | PLL output clock to clock tree (no phase shift) |
| CLKOK | O | PLL output to clock tree through secondary clock divider |
| CLKOK2 | O | PLL output to clock tree (CLKOP divided by 3) |
| LOCK | O | "1" indicates PLL LOCK to CLKI |

2.5. Clock Dividers

LatticeXP2 devices have two clock dividers, one on the left side and one on the right side of the device. These are intended to generate a slower-speed system clock from a high-speed edge clock. The block operates in a $\div 2$, $\div 4$ or $\div 8$ mode and maintains a known phase relationship between the divided down clock and the high-speed clock based on the release of its reset signal. The clock dividers can be fed from the CLKOP output from the GPLLs or from the Edge Clocks (ECLK). The clock divider outputs serve as primary clock sources and feed into the clock distribution network. The Reset (RST) control signal resets the input and forces all outputs to low. The RELEASE signal releases outputs to the input clock. For further information on clock dividers, see [LatticeXP2 sysCLOCK PLL Design and Usage Guide \(TN1126\)](#). [Figure 2.5](#) shows the clock divider connections.

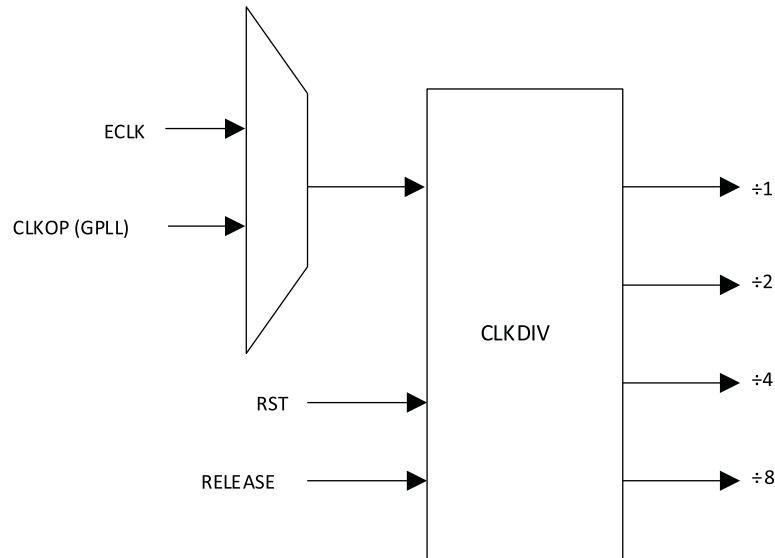


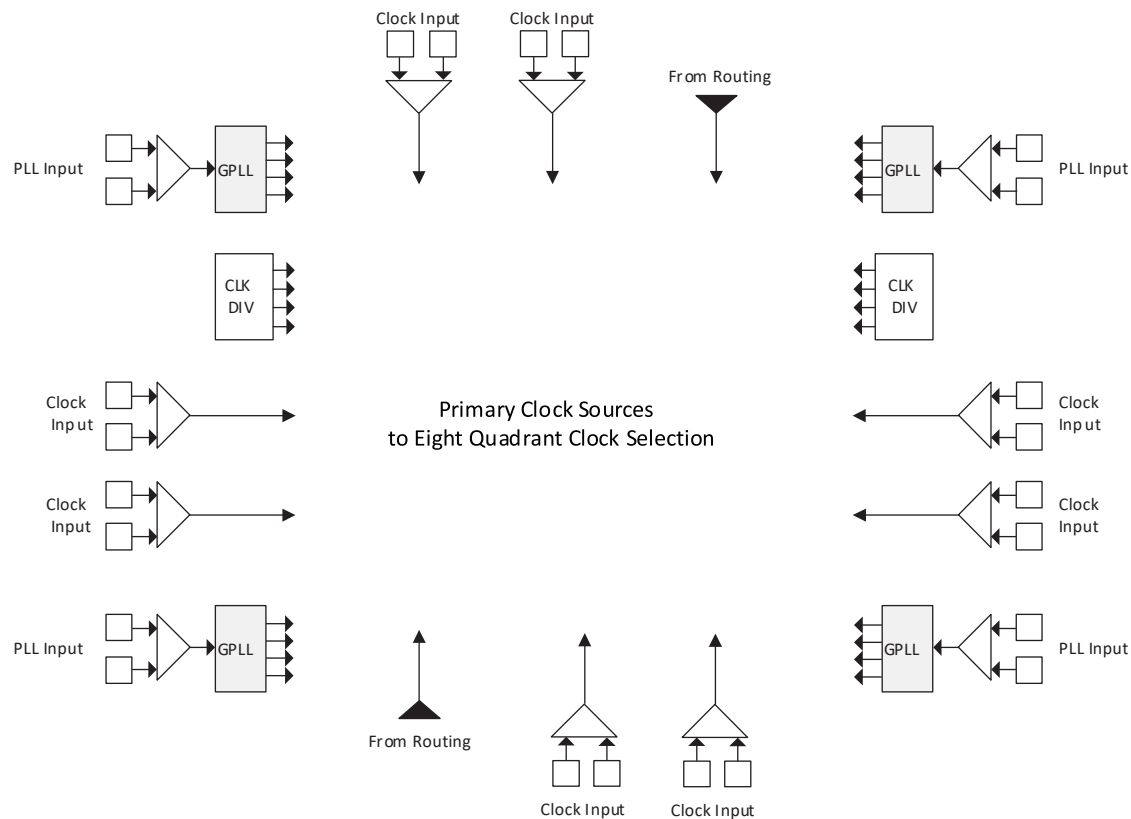
Figure 2.5. Clock Divider Connections

2.6. Clock Distribution Network

LatticeXP2 devices have eight quadrant-based primary clocks and between six and eight flexible region-based secondary clocks/control signals. Two high performance edge clocks are available on each edge of the device to support high speed interfaces. The clock inputs are selected from external I/O, the sysCLOCK PLLs, or routing. Clock inputs are fed throughout the chip via the primary, secondary and edge clock networks.

2.6.1. Primary Clock Sources

LatticeXP2 devices derive primary clocks from four sources: PLL outputs, CLKDIV outputs, dedicated clock inputs and routing. LatticeXP2 devices have two to four sysCLOCK PLLs, located in the four corners of the device. There are eight dedicated clock inputs, two on each side of the device. [Figure 2.6](#) shows the primary clock sources.



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

Figure 2.6. Primary Clock Sources for XP2-17

2.6.2. Secondary Clock Sources

LatticeXP2 devices derive secondary clocks (SC0 through SC7) from eight dedicated clock input pads and the rest from routing. [Figure 2.7](#) shows the secondary clock sources.

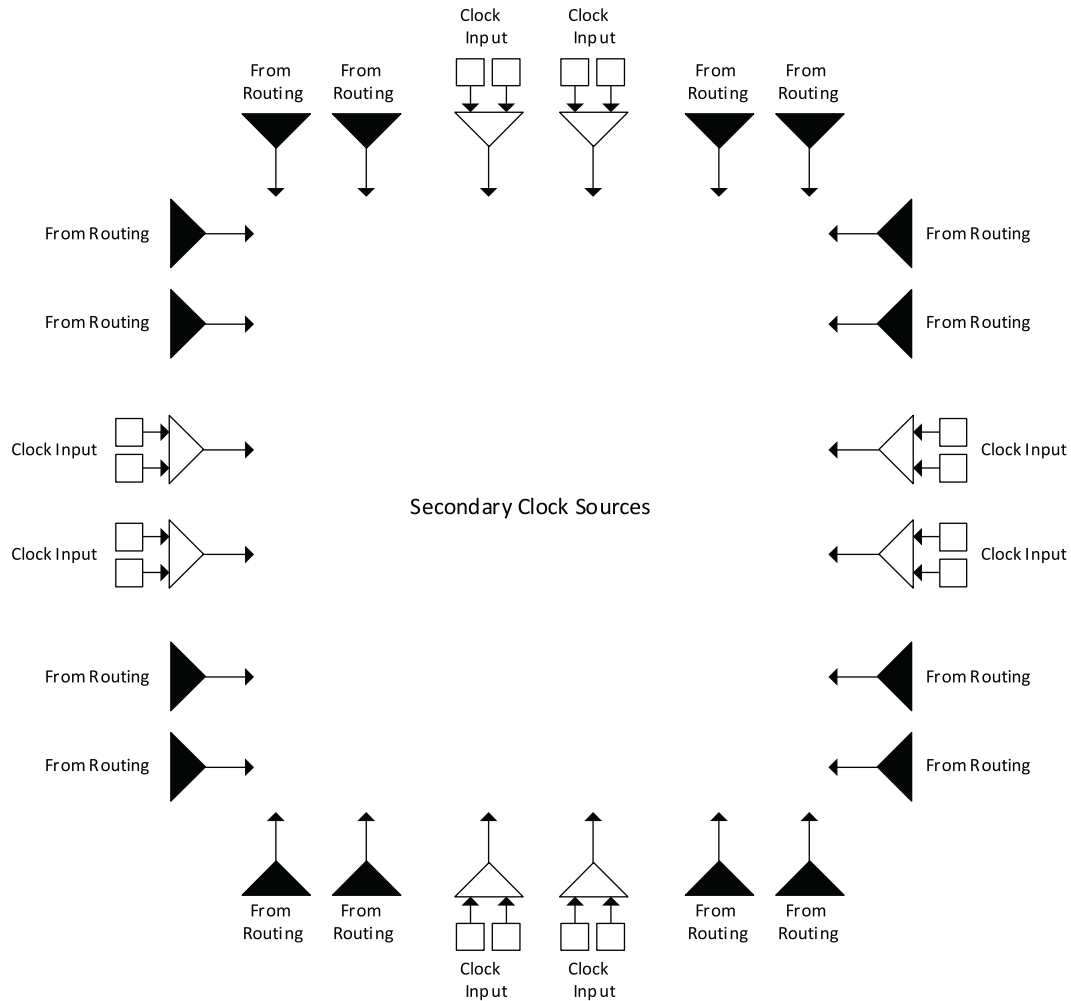
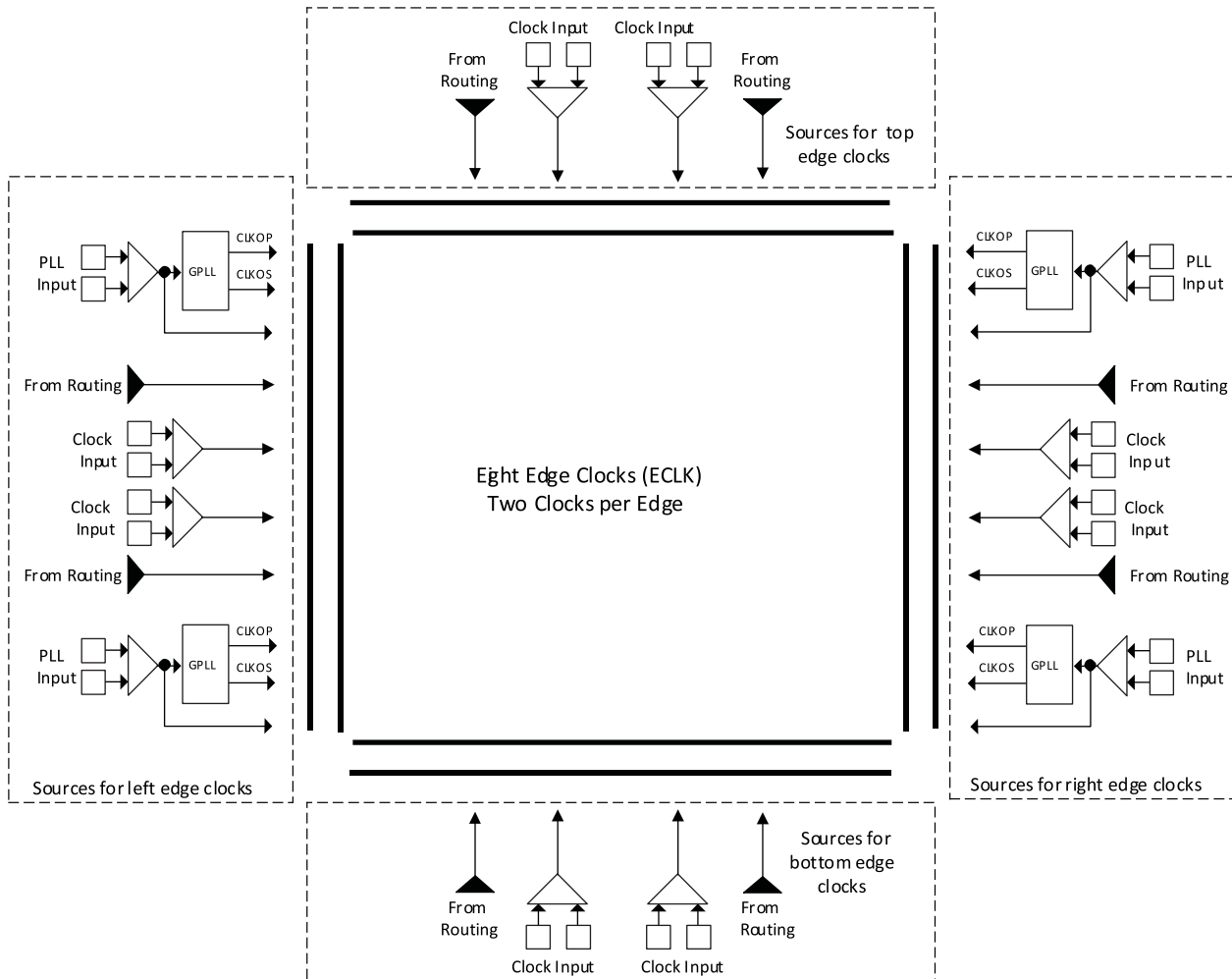


Figure 2.7. Secondary Clock Sources

2.6.3. Edge Clock Sources

Edge clock resources can be driven from a variety of sources at the same edge. Edge clock resources can be driven from adjacent edge clock PIOs, primary clock PIOs, PLLs and clock dividers as shown in [Figure 2.8](#).



Note: This diagram shows sources for the XP2-17 device. Smaller LatticeXP2 devices have two GPLLs.

Figure 2.8. Edge Clock Sources

2.6.4. Primary Clock Routing

The clock routing structure in LatticeXP2 devices consists of a network of eight primary clock lines (CLK0 through CLK7) per quadrant. The primary clocks of each quadrant are generated from muxes located in the center of the device. All the clock sources are connected to these muxes. [Figure 2.9](#) shows the clock routing for one quadrant. Each quadrant mux is identical. If desired, any clock can be routed globally.

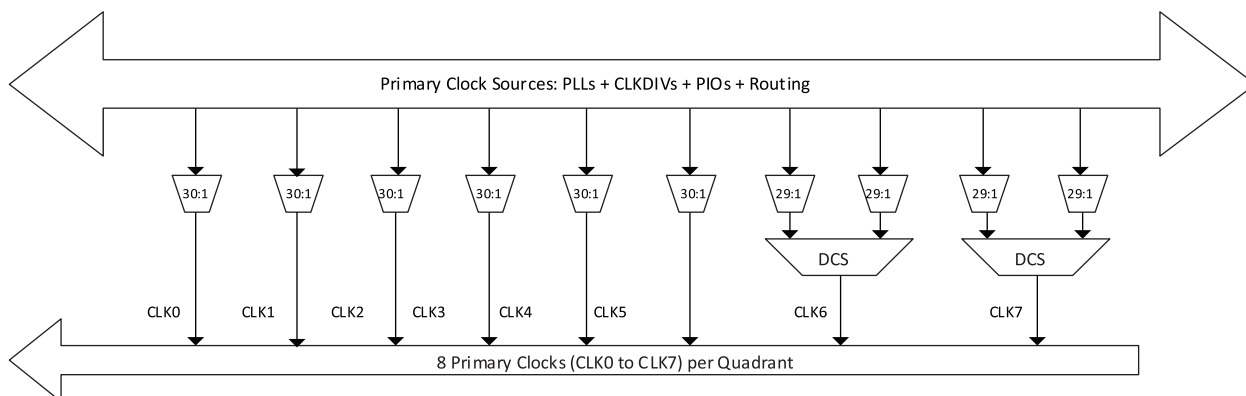


Figure 2.9. Per Quadrant Primary Clock Selection

2.6.5. Dynamic Clock Select (DCS)

The DCS is a smart multiplexer function available in the primary clock routing. It switches between two independent input clock sources without any glitches or runt pulses. This is achieved irrespective of when the select signal is toggled. There are two DCS blocks per quadrant; in total, eight DCS blocks per device. The inputs to the DCS block come from the center muxes. The output of the DCS is connected to primary clocks CLK6 and CLK7 (see [Figure 2.9](#)).

[Figure 2.10](#) shows the timing waveforms of the default DCS operating mode. The DCS block can be programmed to other modes. For more information on the DCS, see [LatticeXP2 sysCLOCK PLL Design and Usage Guide \(TN1126\)](#).

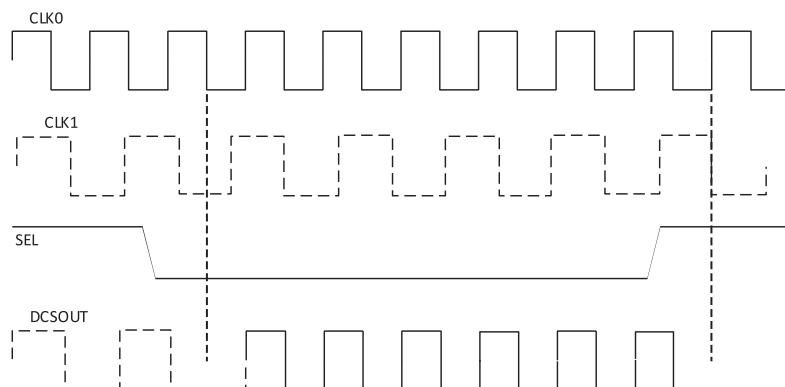


Figure 2.10. DCS Waveforms

2.6.6. Secondary Clock/Control Routing

Secondary clocks in the LatticeXP2 devices are region-based resources. The benefit of region-based resources is the relatively low injection delay and skew within the region, as compared to primary clocks. EBR rows, DSP rows and a special vertical routing channel bound the secondary clock regions. This special vertical routing channel aligns with either the left edge of the center DSP block in the DSP row or the center of the DSP row. [Figure 2.11](#) shows this special vertical routing channel and the eight secondary clock regions for the LatticeXP2-40.

LatticeXP2-30 and smaller devices have six secondary clock regions. All devices in the LatticeXP2 family have four secondary clocks (SC0 to SC3) which are distributed to every region.

The secondary clock muxes are located in the center of the device. [Figure 2.12](#) shows the mux structure of the secondary clock routing. Secondary clocks SC0 to SC3 are used for clock and control and SC4 to SC7 are used for high fan-out signals.

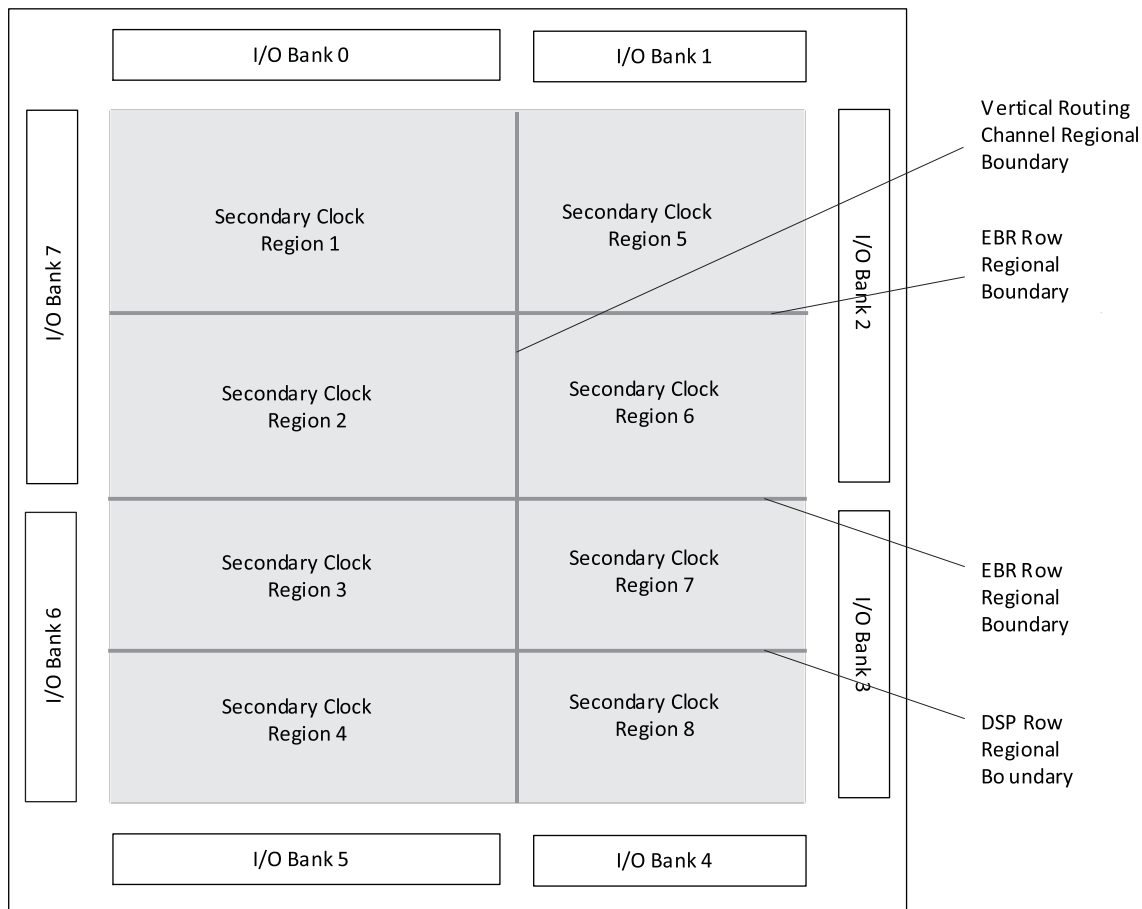


Figure 2.11. Secondary Clock Regions XP2-40

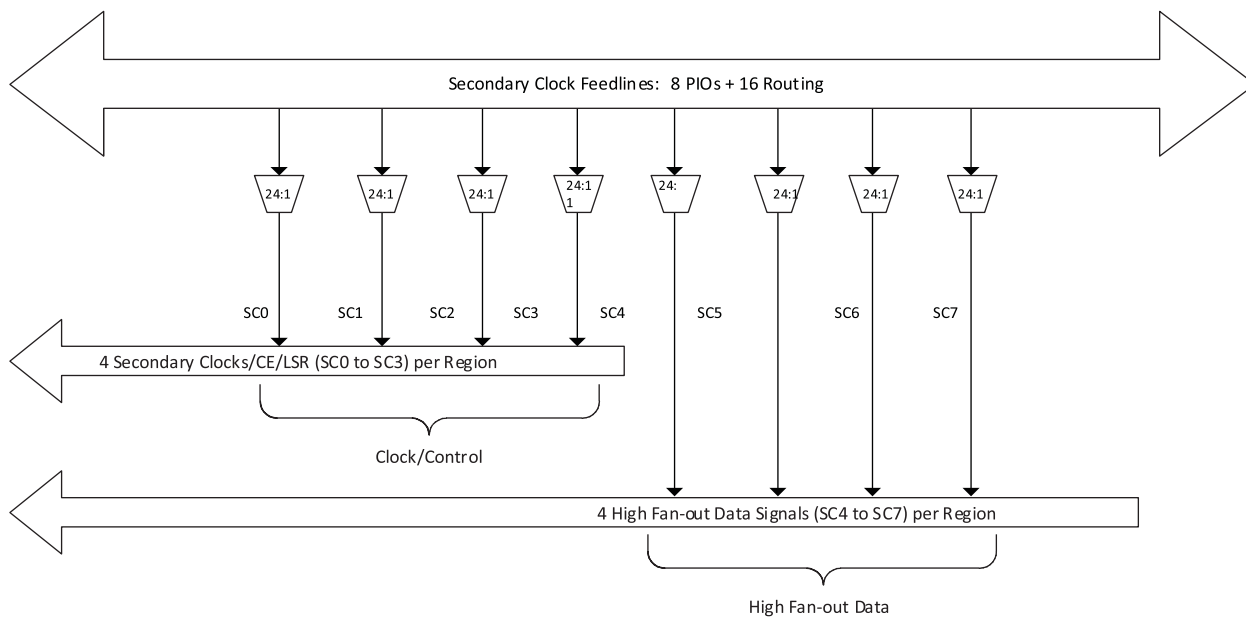


Figure 2.12. Secondary Clock Selection

2.6.7. Slice Clock Selection

Figure 2.13 shows the clock selections and Figure 2.14 shows the control selections for Slice0 through Slice2. All the primary clocks and the four secondary clocks are routed to this clock selection mux. Other signals, via routing, can be used as clock inputs to the slices. Slice controls are generated from the secondary clocks or other signals connected via routing.

If none of the signals are selected for both clock and control, then the default value of the mux output is 1. Slice 3 does not have any registers; therefore it does not have the clock or control muxes.

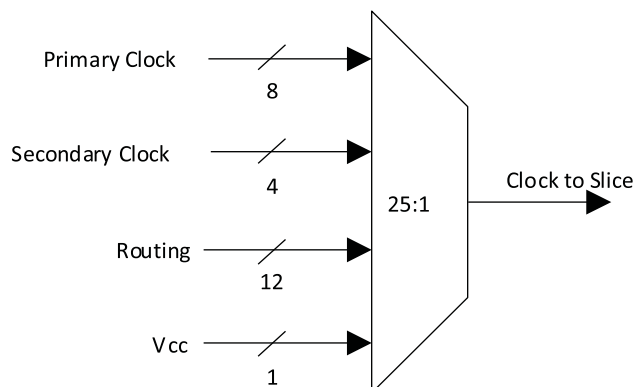


Figure 2.13. Slice0 through Slice2 Clock Selection

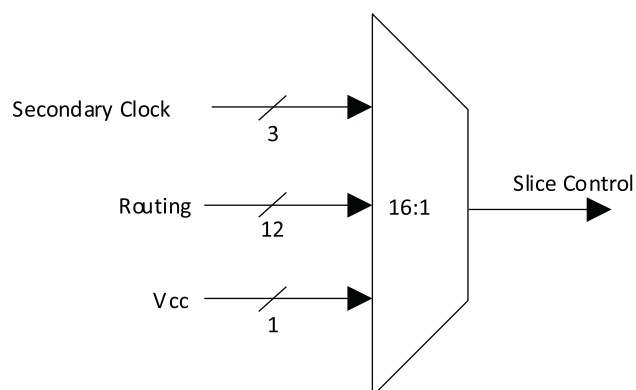


Figure 2.14. Slice0 through Slice2 Control Selection

2.6.8. Edge Clock Routing

LatticeXP2 devices have eight high-speed edge clocks that are intended for use with the PIOs in the implementation of high-speed interfaces. Each device has two edge clocks per edge. Figure 2.15 shows the selection muxes for these clocks.

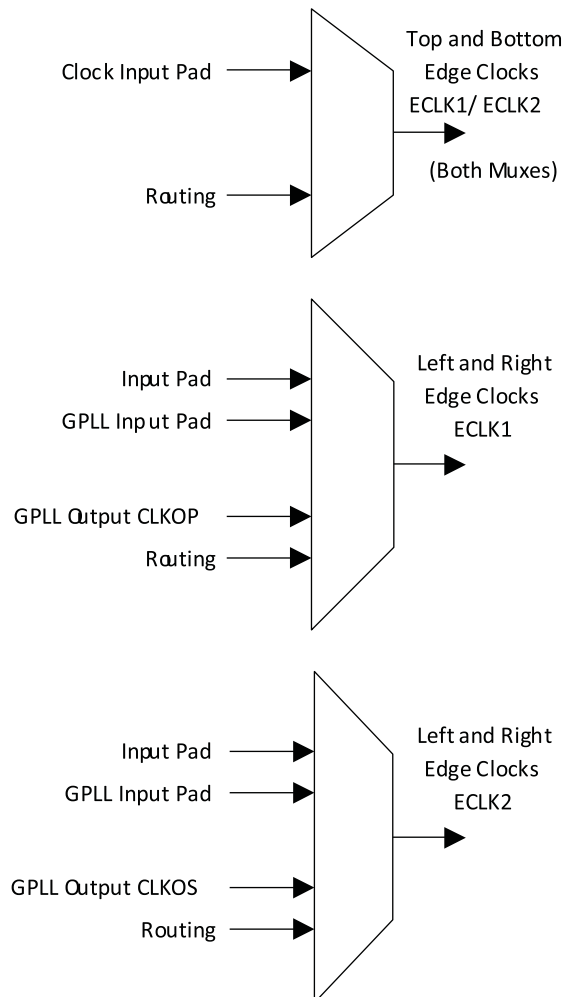


Figure 2.15. Edge Clock Mux Connections

2.7. sysMEM Memory

LatticeXP2 devices contains a number of sysMEM Embedded Block RAM (EBR). The EBR consists of 18 Kbit RAM with dedicated input and output registers.

2.7.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as shown in [Table 2.5](#). FIFOs can be implemented in sysMEM EBR blocks by using support logic with PFUs. The EBR block supports an optional parity bit for each data byte to facilitate parity checking. EBR blocks provide byte-enable support for configurations with 18-bit and 36-bit data widths.

Table 2.5. sysMEM Block Configurations

| Memory Mode | Configurations |
|------------------|---|
| Single Port | 16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36 |
| True Dual Port | 16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 |
| Pseudo Dual Port | 16,384 x 1 8,192 x 2 4,096 x 4 2,048 x 9 1,024 x 18 512 x 36 |

2.7.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.7.3. FlashBAK EBR Content Storage

All the EBR memory in the LatticeXP2 is shadowed by Flash memory. Optionally, initialization values for the memory blocks can be defined using the Lattice Diamond design tools. The initialization values are loaded into the Flash memory during device programming and into the SRAM at power up or whenever the device is reconfigured. This feature is ideal for the storage of a variety of information such as look-up tables and microprocessor code. It is also possible to write the current contents of the EBR memory back to Flash memory. This capability is useful for the storage of data such as error codes and calibration information. For additional information on the FlashBAK capability see [LatticeXP2 Memory Usage Guide \(TN1137\)](#).

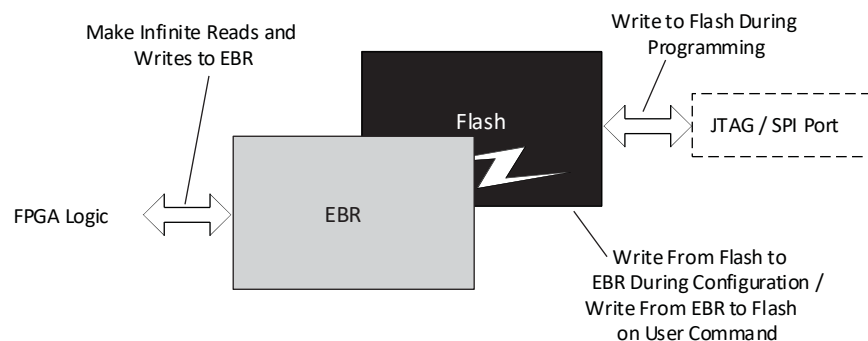


Figure 2.16. FlashBAK Technology

2.7.4. Memory Cascading

Larger and deeper blocks of RAMs can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.7.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

EBR memory supports two forms of write behavior for single port or dual port operation:

1. Normal – Data on the output appears only during a read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
2. Write Through – A copy of the input data appears at the output of the same port during a write cycle. This mode is supported for all data widths.

2.8. Memory Core Reset

The memory array in the EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B respectively. GSRN, the global reset signal, resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.17.

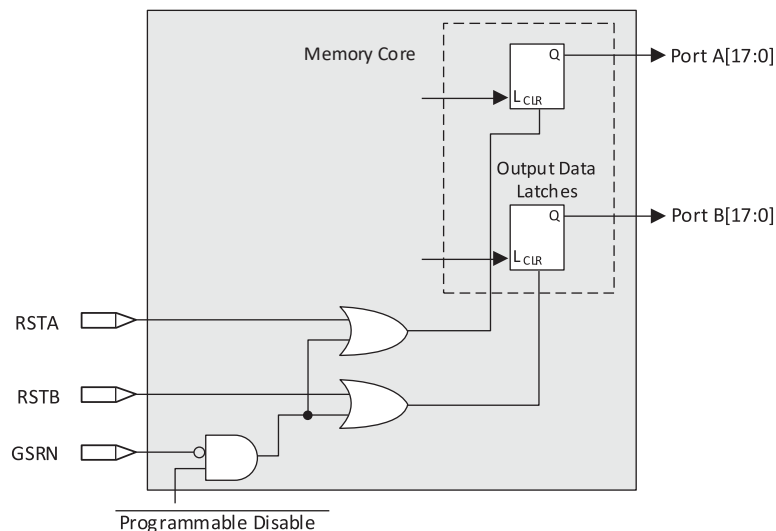


Figure 2.17. Memory Core Reset

For further information on the sysMEM EBR block, see [LatticeXP2 Memory Usage Guide \(TN1137\)](#).

2.8.1. EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the low-to-high transition of the reset signal, as shown in Figure 2.18. The GSR input to the EBR is always asynchronous.

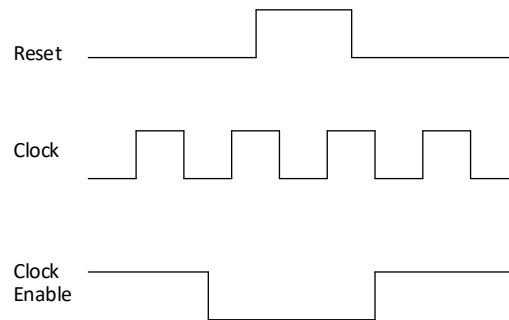


Figure 2.18. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device Wake Up must occur before the release of the device I/O becoming active.

These instructions apply to all EBR RAM and ROM implementations.

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.9. sysDSP™ Block

The LatticeXP2 family provides a sysDSP block making it ideally suited for low cost, high performance Digital Signal Processing (DSP) applications. Typical functions used in these applications include Bit Correlators, Fast Fourier Transform (FFT) functions, Finite Impulse Response (FIR) Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. These complex signal processing functions use similar building blocks such as multiply-adders and multiply-accumulators.

2.9.1. sysDSP Block Approach Compare to General DSP

Conventional general-purpose DSP chips typically contain one to four (Multiply and Accumulate) MAC units with fixed data-width multipliers; this leads to limited parallelism and limited throughput. Their throughput is increased by higher clock speeds. The LatticeXP2 family, on the other hand, has many DSP blocks that support different datawidths. This allows the designer to use highly parallel implementations of DSP functions. The designer can optimize the DSP performance vs. area by choosing appropriate levels of parallelism. [Figure 2.19](#) compares the fully serial and the mixed parallel and serial implementations.

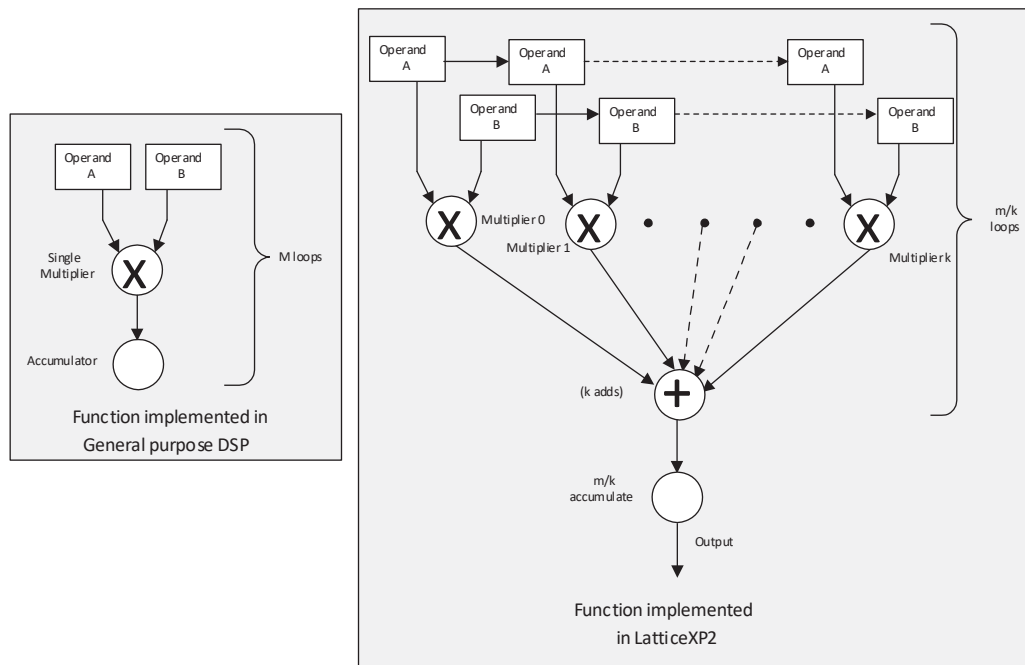


Figure 2.19. Comparison of General DSP and LatticeXP2 Approaches

2.9.2. sysDSP Block Capabilities

The sysDSP block in the LatticeXP2 family supports four functional elements in three 9, 18 and 36 data path widths. You select a function element for a DSP block and then selects the width and type (signed/unsigned) of its operands. The operands in the LatticeXP2 family sysDSP Blocks can be either signed or unsigned but not mixed within a function element. Similarly, the operand widths cannot be mixed within a block. DSP elements can be concatenated.

The resources in each sysDSP block can be configured to support the following four elements:

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Accumulate)

The number of elements available in each block depends on the width selected from the three available options: x9, x18, and x36. A number of these elements are concatenated for highly parallel implementations of DSP functions. Table 2.6 shows the capabilities of the block.

Table 2.6. Maximum Number of Elements in a Block

| Width of Multiply | x9 | x18 | x36 |
|-------------------|----|-----|-----|
| MULT | 8 | 4 | 1 |
| MAC | 2 | 2 | — |
| MULTADDSUB | 4 | 2 | — |
| MULTADDSUBSUM | 2 | 1 | — |

Some options are available in four elements. The input register in all the elements can be directly loaded or can be loaded as shift register from previous operand registers. By selecting 'dynamic operation' the following operations are possible:

- In the 'Signed/Unsigned' options the operands can be switched between signed and unsigned on every cycle.
- In the 'Add/Sub' option the Accumulator can be switched between addition and subtraction on every cycle.
- The loading of operands can switch between parallel and serial operations.

2.9.3. MULT sysDSP Element

This multiplier element implements a multiply with no addition or accumulator nodes. The two operands, A and B, are multiplied and the result is available at the output. You can enable the input/output and pipeline registers. Figure 2.20 shows the MULT sysDSP element.

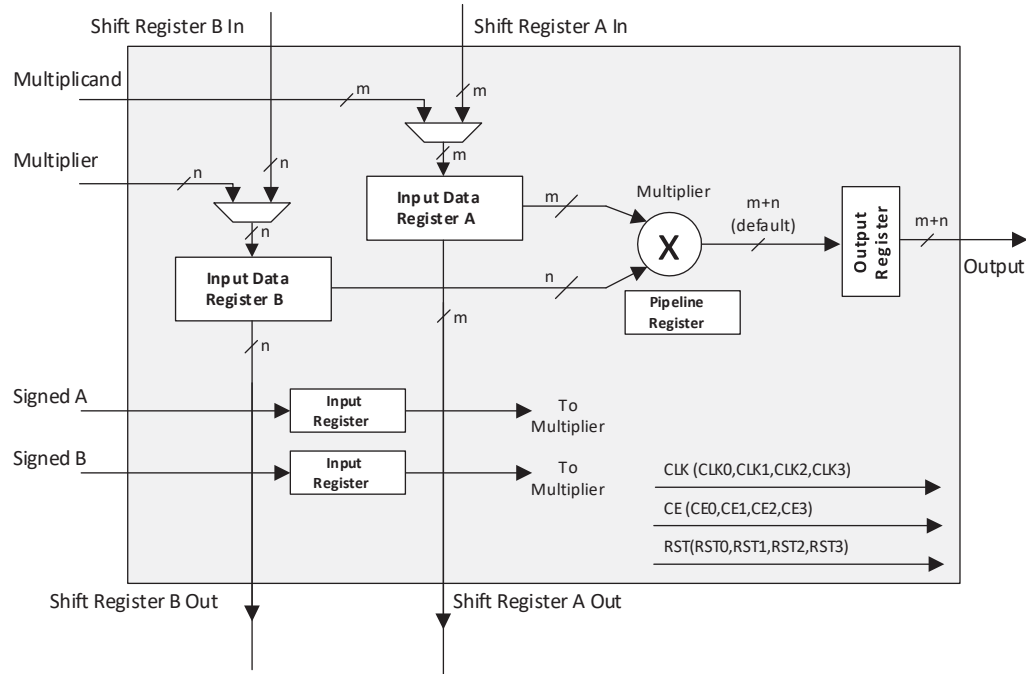


Figure 2.20. MULT sysDSP Element

2.9.4. MAC sysDSP Element

In this case, the two operands, A and B, are multiplied and the result is added with the previous accumulated value. This accumulated value is available at the output. You can enable the input and pipeline registers but the output register is always enabled. The output register is used to store the accumulated value. The Accumulators in the DSP blocks in LatticeXP2 family can be initialized dynamically. A registered overflow signal is also available. The overflow conditions are provided later in this document. [Figure 2.21](#) shows the MAC sysDSP element.

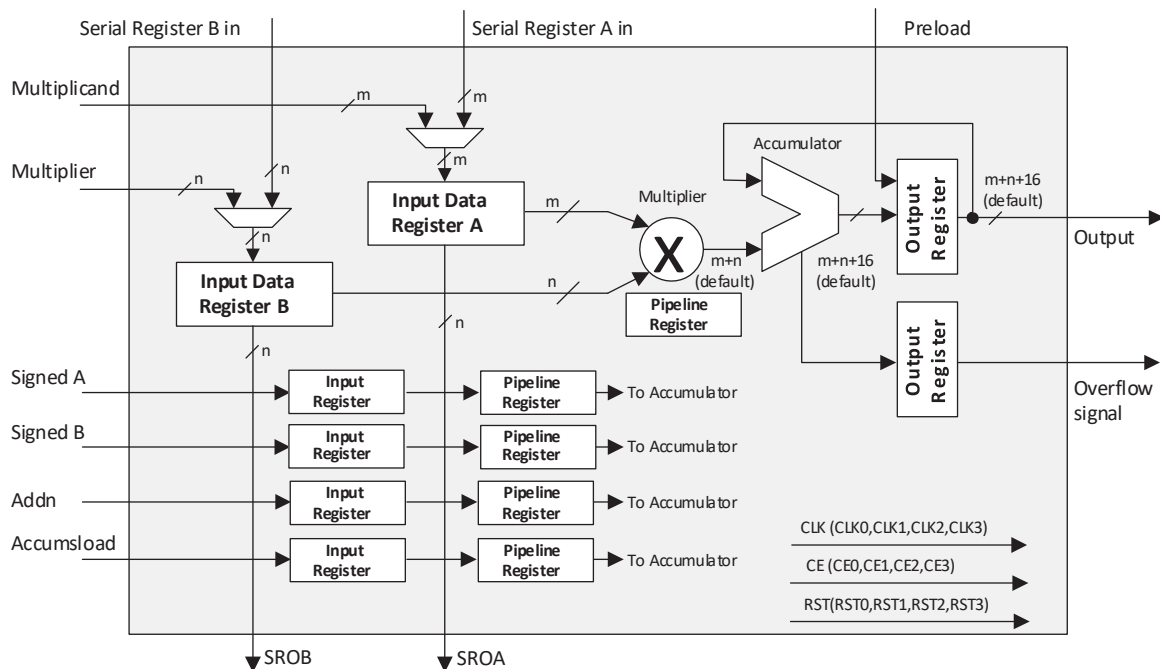


Figure 2.21. MAC sysDSP

2.9.5. MULTADDSUB sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. You can enable the input, output and pipeline registers. Figure 2.22 shows the MULTADDSUB sysDSP element.

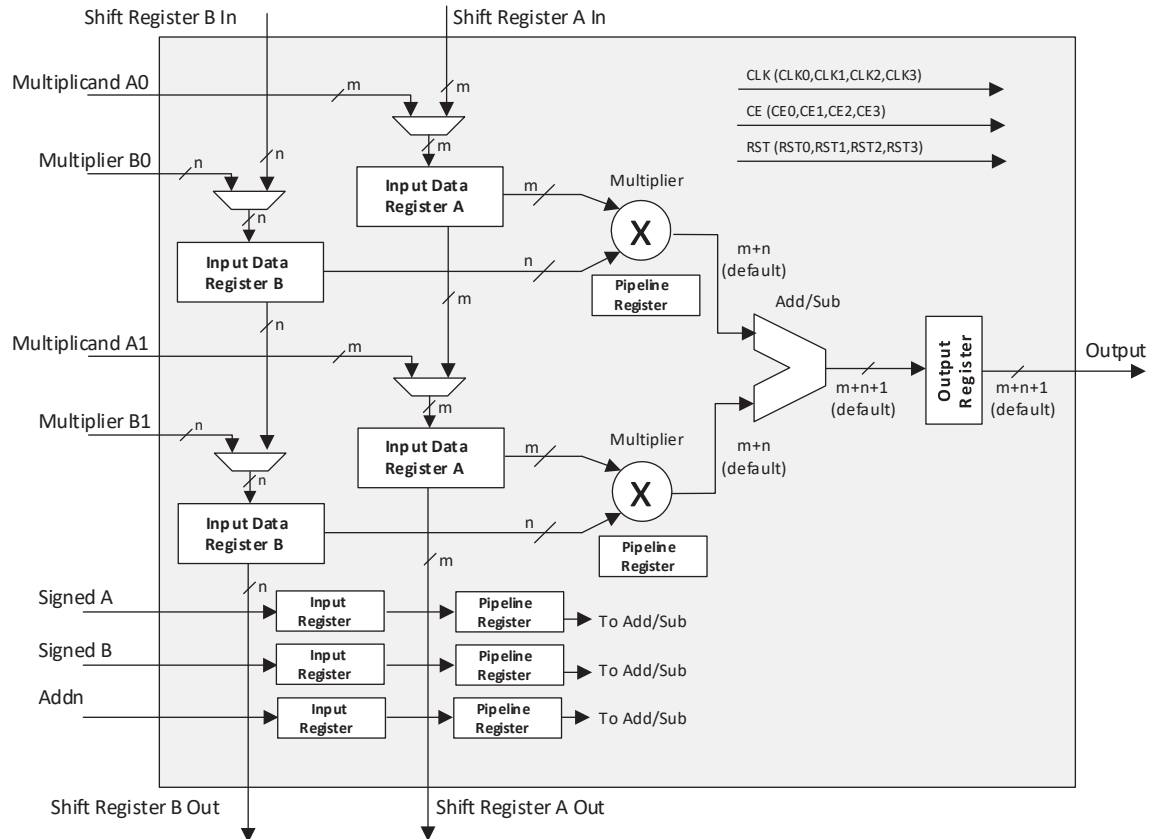


Figure 2.22. MULTADDSUB

2.9.6. MULTADDSUBSUM sysDSP Element

In this case, the operands A0 and B0 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A1 and B1. Additionally the operands A2 and B2 are multiplied and the result is added/subtracted with the result of the multiplier operation of operands A3 and B3. The result of both addition/subtraction are added in a summation block. You can enable the input, output and pipeline registers. Figure 2.23 shows the MULTADDSUBSUM sysDSP element.

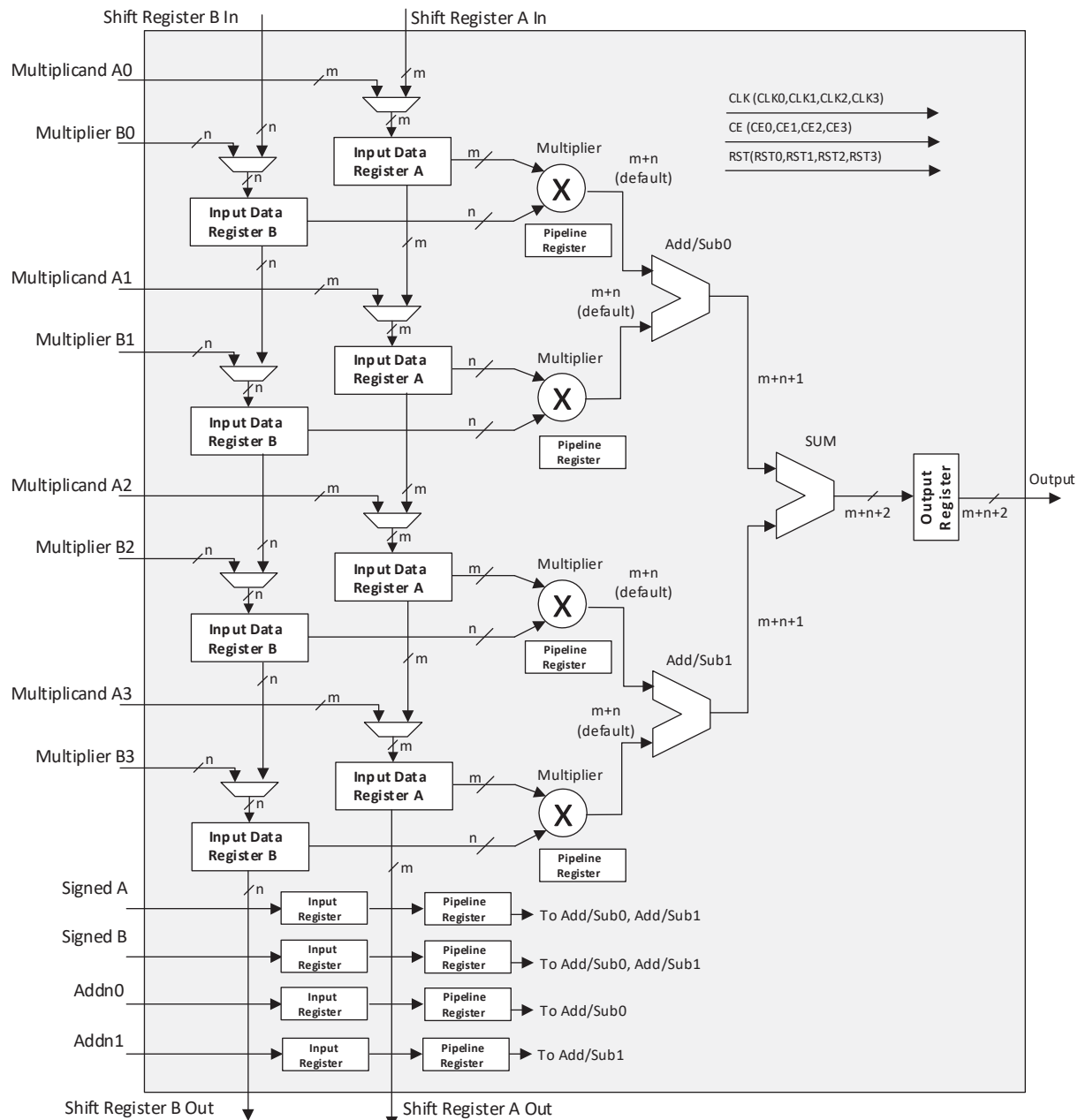


Figure 2.23. MULTADDSUBSUM

2.9.7. Clock, Clock Enable and Reset Resources

Global Clock, Clock Enable (CE) and Reset (RST) signals from routing are available to every DSP block. From four clock sources (CLK0, CLK1, CLK2, CLK3) one clock is selected for each input register, pipeline register and output register. Similarly, CE and RST are selected from their four respective sources (CE0, CE1, CE2, CE3 and RST0, RST1, RST2, RST3) at each input register, pipeline register and output register.

2.9.8. Signed and Unsigned with Different Widths

The DSP block supports other widths, in addition to x9, x18 and x36 widths, of signed and unsigned multipliers. For unsigned operands, unused upper data bits should be filled to create a valid x9, x18 or x36 operand. For signed two's complement operands, sign extension of the most significant bit should be performed until x9, x18 or x36 width is reached. Table 2.7 provides an example of this.

Table 2.7. Sign Extension Example

| Number | Unsigned | Unsigned 9-bit | Unsigned 18-bit | Signed | Two's Complement Signed 9 Bits | Two's Complement Signed 18 Bits |
|--------|----------|----------------|--------------------|--------|--------------------------------|---------------------------------|
| +5 | 0101 | 000000101 | 000000000000000101 | 0101 | 000000101 | 000000000000000101 |
| -6 | N/A | N/A | N/A | 1010 | 11111010 | 111111111111111010 |

2.9.9. OVERFLOW Flag from MAC

The sysDSP block provides an overflow output to indicate that the accumulator has overflowed. "Roll-over" occurs and an overflow signal is indicated when any of the following is true: two unsigned numbers are added and the result is a smaller number than the accumulator, two positive numbers are added with a negative sum or two negative numbers are added with a positive sum. Note that when overflow occurs the overflow flag is present for only one cycle. By counting these overflow pulses in FPGA logic, larger accumulators can be constructed. The conditions for the overflow signal for signed and unsigned operands are listed in Figure 2.24.

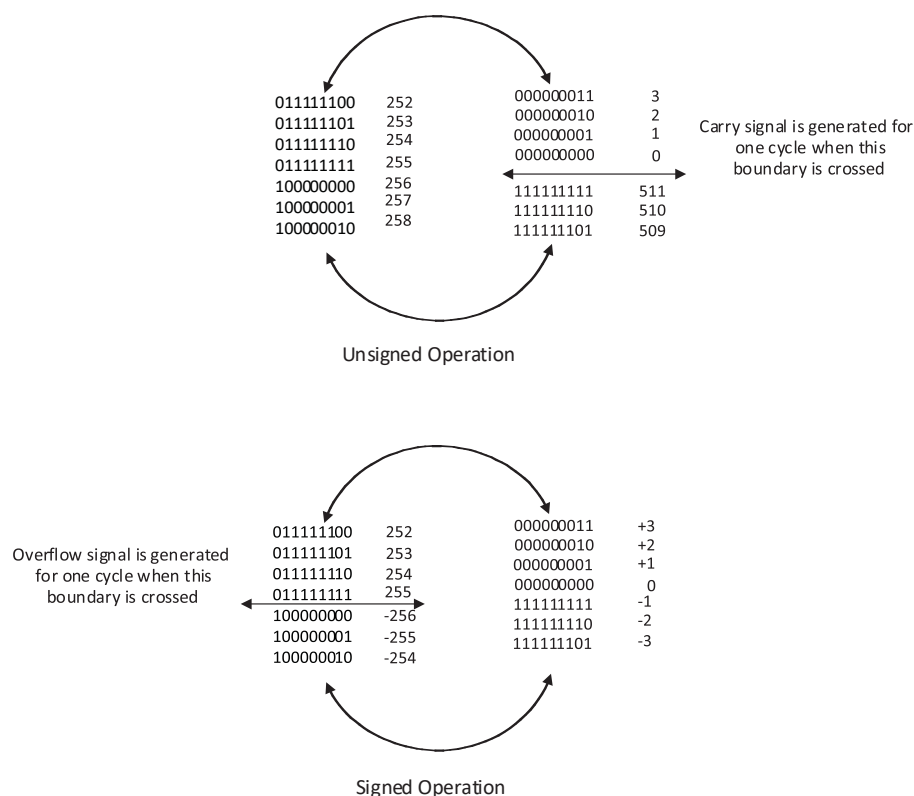


Figure 2.24. Accumulator Overflow/Underflow

2.9.10. IPexpress™

You can access the sysDSP block via the Lattice IPexpress tool, which provides the option to configure each DSP module (or group of modules), or by direct HDL instantiation. In addition, Lattice has partnered with The MathWorks® to support instantiation in the Simulink® tool, a graphical simulation environment. Simulink works with Diamond to dramatically shorten the DSP design cycle in Lattice FPGAs.

2.10. Optimized DSP Functions

Lattice provides a library of optimized DSP IP functions. Some of the IP cores planned for the LatticeXP2 DSP include the Bit Correlator, FFT functions, FIR Filter, Reed-Solomon Encoder/Decoder, Turbo Encoder/Decoder and Convolutional Encoder/Decoder. Contact Lattice to obtain the latest list of available DSP IP cores.

2.10.1. Resources Available in the LatticeXP2 Family

Table 2.8 shows the maximum number of multipliers for each member of the LatticeXP2 family. Table 2.9 shows the maximum available EBR RAM Blocks and Serial TAG Memory bits in each LatticeXP2 device. EBR blocks, together with Distributed RAM can be used to store variables locally for fast DSP operations.

Table 2.8. Maximum Number of DSP Blocks in the LatticeXP2 Family

| Device | DSP Block | 9x9 Multiplier | 18x18 Multiplier | 36x36 Multiplier |
|--------|-----------|----------------|------------------|------------------|
| XP2-5 | 3 | 24 | 12 | 3 |
| XP2-8 | 4 | 32 | 16 | 4 |
| XP2-17 | 5 | 40 | 20 | 5 |
| XP2-30 | 7 | 56 | 28 | 7 |
| XP2-40 | 8 | 64 | 32 | 8 |

Table 2.9. Embedded SRAM/TAG Memory in the LatticeXP2 Family

| Device | EBR SRAM Block | Total EBR SRAM (Kbits) | TAG Memory (Bits) |
|--------|----------------|------------------------|-------------------|
| XP2-5 | 9 | 166 | 632 |
| XP2-8 | 12 | 221 | 768 |
| XP2-17 | 15 | 276 | 2184 |
| XP2-30 | 21 | 387 | 2640 |
| XP2-40 | 48 | 885 | 3384 |

2.10.2. LatticeXP2 DSP Performance

Table 2.10 lists the maximum performance in Millions of MAC (MMAC) operations per second for each member of the LatticeXP2 family.

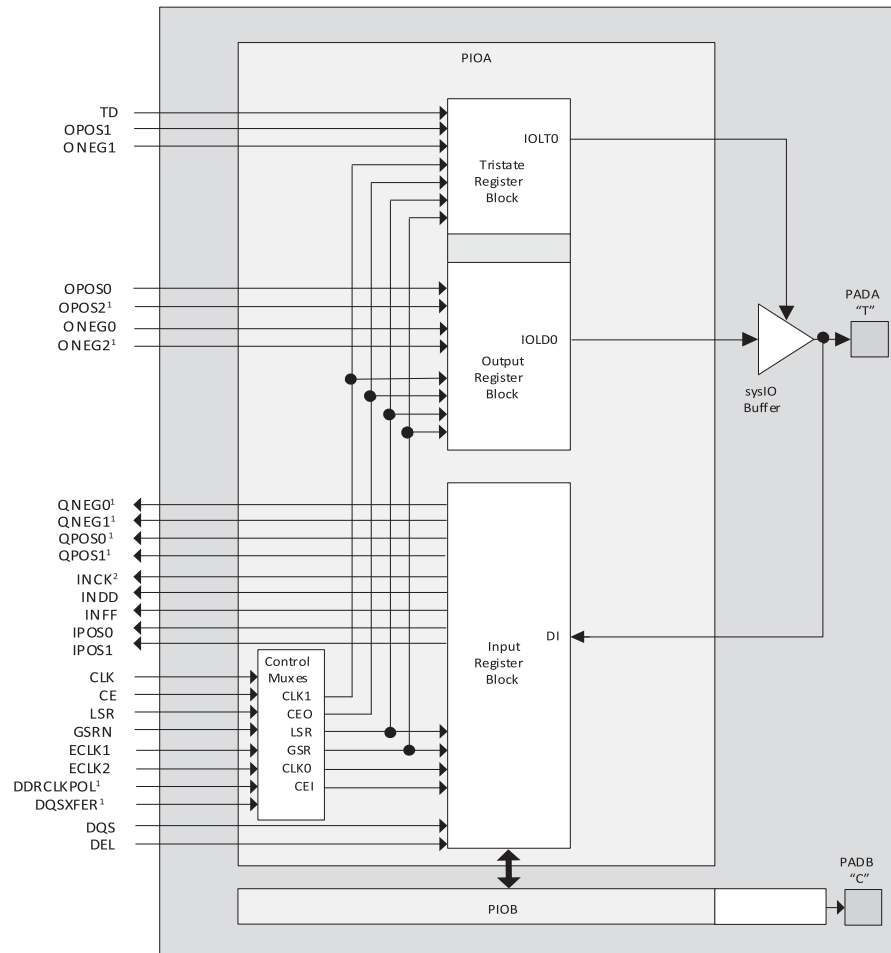
Table 2.10. DSP Performance

| Device | DSP Block | DSP Performance MMAC |
|--------|-----------|----------------------|
| XP2-5 | 3 | 3,900 |
| XP2-8 | 4 | 5,200 |
| XP2-17 | 5 | 6,500 |
| XP2-30 | 7 | 9,100 |
| XP2-40 | 8 | 10,400 |

For further information on the sysDSP block, see [LatticeXP2 sysDSP Usage Guide \(TN1140\)](#).

2.11. Programmable I/O Cells (PIC)

Each PIC contains two PIOs connected to their respective sysI/O buffers as shown in Figure 2.25. The PIO Block supplies the output data (DO) and the tri-state control signal (TO) to the sysI/O buffer and receives input from the buffer. Table 2.11 provides the PIO signal list.



1. Signals are available on left/right/bottom edges only.
2. Selected blocks.

Figure 2.25. PIC Diagram

Two adjacent PIOs can be joined to provide a differential I/O pair (labeled as “T” and “C”) as shown in [Figure 2.25](#). The PAD Labels “T” and “C” distinguish the two PIOs. Approximately 50% of the PIO pairs on the left and right edges of the device can be configured as true LVDS outputs. All I/O pairs can operate as inputs.

Table 2.11. PIO Signal List

| Name | Type | Description |
|-------------------------------|---------------------------------|---|
| CE | Control from the core | Clock enables for input and output block flip-flops |
| CLK | Control from the core | System clocks for input and output blocks |
| ECLK1, ECLK2 | Control from the core | Fast edge clocks |
| LSR | Control from the core | Local Set/Reset |
| GSRN | Control from routing | Global Set/Reset (active low) |
| INCK ² | Input to the core | Input to Primary Clock Network or PLL reference inputs |
| DQS | Input to PIO | DQS signal from logic (routing) to PIO |
| INDD | Input to the core | Unregistered data input to core |
| INFF | Input to the core | Registered input on positive edge of the clock (CLK0) |
| IPOS0, IPOS1 | Input to the core | Double data rate registered inputs to the core |
| QPOS01, QPOS1 ¹ | Input to the core | Gearbox pipelined inputs to the core |
| QNEG01, QNEG1 ¹ | Input to the core | Gearbox pipelined inputs to the core |
| OPOS0, ONEG0, OPOS2, ONEG2 | Output data from the core | Output signals from the core for SDR and DDR operation |
| OPOS1 ONEG1 | Tristate control from the core | Signals to Tristate Register block for DDR operation |
| DEL[3:0] | Control from the core | Dynamic input delay control bits |
| TD | Tristate control from the core | Tristate signal from the core used in SDR operation |
| DDRCLKPOL | Control from clock polarity bus | Controls the polarity of the clock (CLK0) that feed the DDR input block |
| DQSXFER | Control from core | Controls signal to the Output block |

Notes:

1. Signals available on left/right/bottom only.
2. Selected I/O.

2.12. PIO

The PIO contains four blocks: an input register block, output register block, tristate register block and a control logic block. These blocks contain registers for operating in a variety of modes along with necessary clock and selection logic.

2.12.1. Input Register Block

The input register blocks for PIOs contain delay elements and registers that can be used to condition high-speed interface signals, such as DDR memory interfaces and source synchronous interfaces, before they are passed to the device core. [Figure 2.6](#) shows the diagram of the input register block.

Input signals are fed from the sysI/O buffer to the input register block (as signal DI). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), a clock (INCK) and, in selected blocks, the input to the DQS delay block. If an input delay is desired, designers can select either a fixed delay or a dynamic delay DEL[3:0]. The delay, if selected, reduces input register hold time requirements when using a global clock.

The input block allows three modes of operation. In the Single Data Rate (SDR) mode, the data is registered, by one of the registers in the SDR Sync register block, with the system clock. In DDR mode two registers are used to sample the data on the positive and negative edges of the DQS signal which creates two data streams, D0 and D2. D0 and D2 are synchronized with the system clock before entering the core. Further information on this topic can be found in the DDR Memory Support section of this data sheet.

By combining input blocks of the complementary PIOs and sharing registers from output blocks, a gearbox function can be implemented, that takes a double data rate signal applied to PIOA and converts it as four data streams, IPOS0A, IPOS1A, IPOS0B and IPOS1B. [Figure 2.6](#) shows the diagram using this gearbox function. For more information on this topic, see [LatticeXP2 High Speed I/O Interface \(TN1138\)](#).

The signal DDRCLKPOL controls the polarity of the clock used in the synchronization registers. It ensures adequate timing when data is transferred from the DQS to system clock domain. For further discussion on this topic, see the DDR Memory section of this data sheet.

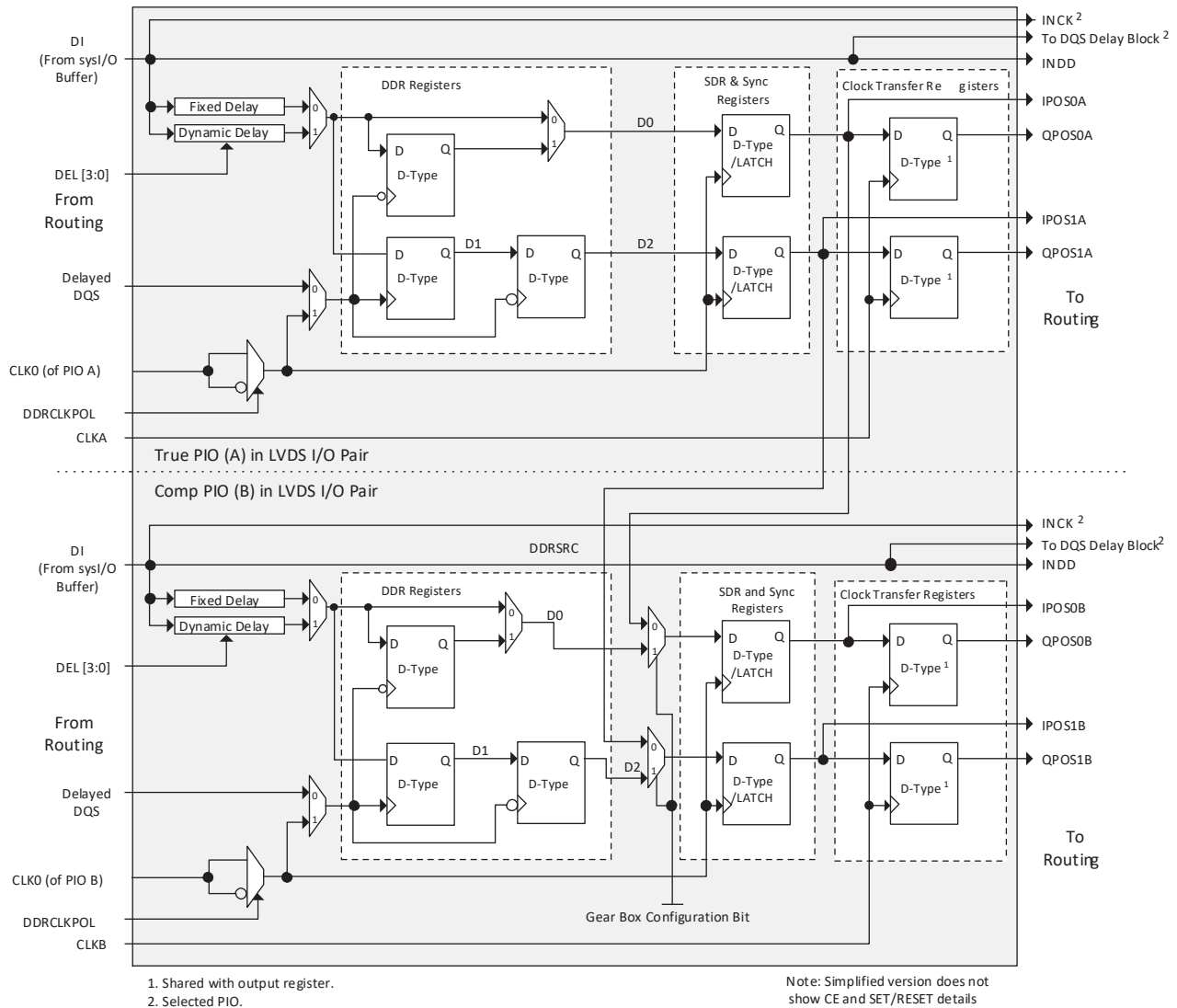


Figure 2.26. Input Register Block

2.12.2. Output Register Block

The output register block provides the ability to register signals from the core of the device before they are passed to the sysI/O buffers. The blocks on the PIOs on the left, right and bottom contain registers for SDR operation that are combined with an additional latch for DDR operation. [Figure 2.27](#) shows the diagram of the Output Register Block for PIOs.

In SDR mode, ONEG0 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as a D-type or latch. In DDR mode, ONEG0 and OPOS0 are fed into registers on the positive edge of the clock. At the next clock cycle the registered OPOS0 is latched. A multiplexer running off the same clock cycle selects the correct register to feed the output (D0).

By combining output blocks of the complementary PIOs and sharing some registers from input blocks, a gearbox function can be implemented, to take four data streams ONEG0A, ONEG1A, ONEG1B and ONEG1B. [Figure 2.27](#) shows the diagram using this gearbox function. For more information on this topic, see [LatticeXP2 High Speed I/O Interface \(TN1138\)](#).

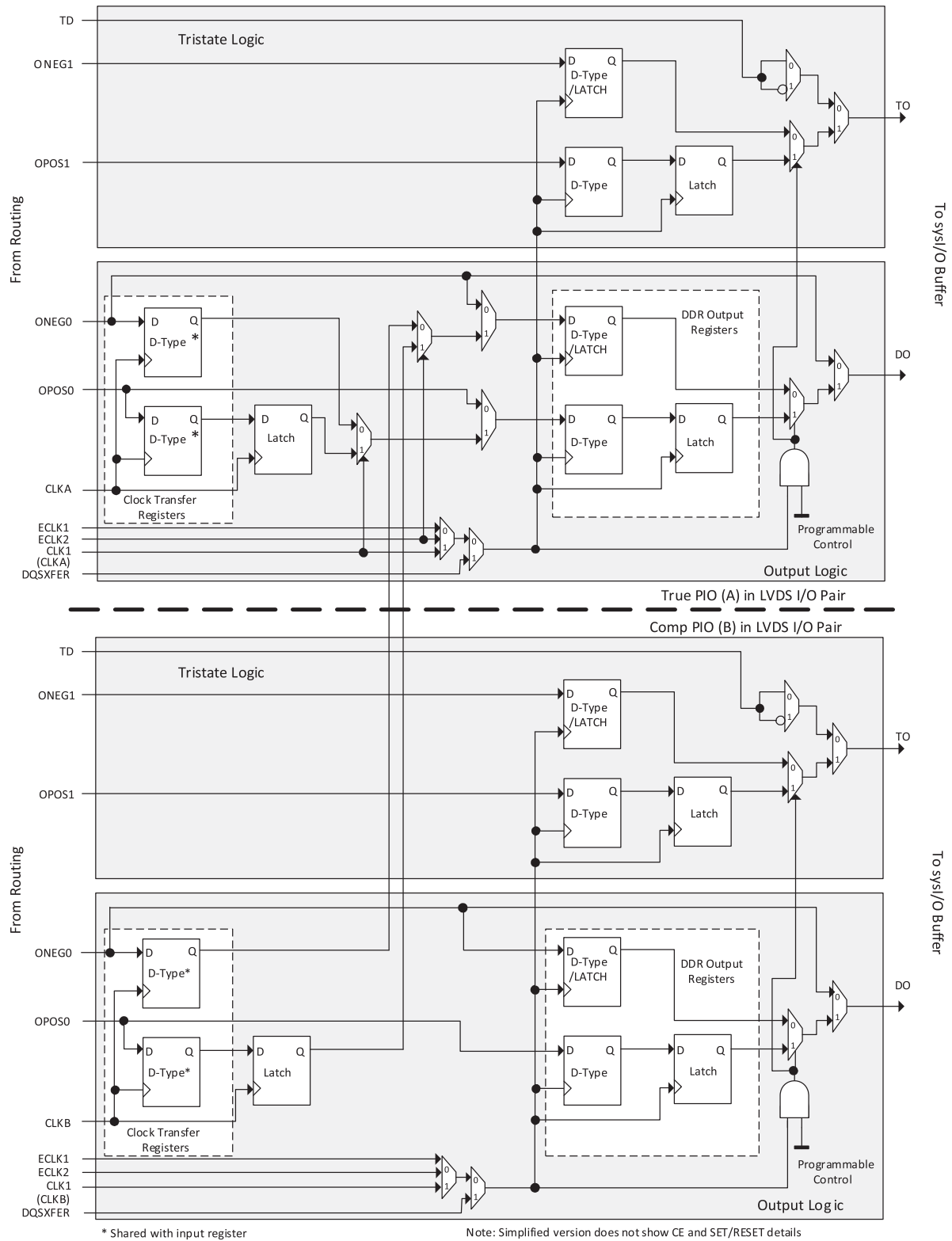


Figure 2.27. Output and Tristate Block

2.12.3. Tristate Register Block

The tristate register block provides the ability to register tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation and an additional latch for DDR operation. [Figure 2.27](#) shows the Tristate Register Block with the Output Block.

In SDR mode, ONEG1 feeds one of the flip-flops that then feeds the output. The flip-flop can be configured as Dtype or latch. In DDR mode, ONEG1 and OPOS1 are fed into registers on the positive edge of the clock. Then in the next clock the registered OPOS1 is latched. A multiplexer running off the same clock cycle selects the correct register for feeding to the output (D0).

2.12.4. Control Logic Block

The control logic block allows the selection and modification of control signals for use in the PIO block. A clock signal is selected from general purpose routing, ECLK1, ECLK2 or a DQS signal (from the programmable DQS pin) and is provided to the input register block. The clock can optionally be inverted.

2.13. DDR Memory Support

PICs have additional circuitry to allow implementation of high speed source synchronous and DDR memory interfaces. PICs have registered elements that support DDR memory interfaces. Interfaces on the left and right edges are designed for DDR memories that support 16 bits of data, whereas interfaces on the top and bottom are designed for memories that support 18 bits of data. One of every 16 PIOs on the left and right and one of every 18 PIOs on the top and bottom contain delay elements to facilitate the generation of DQS signals. The DQS signals feed the DQS buses which span the set of 16 or 18 PIOs. [Figure 2.28](#) and [Figure 2.29](#) show the DQS pin assignments in each set of PIOs.

The exact DQS pins are shown in a dual function in the Logic Signal Connections table in this data sheet. Additional detail is provided in the Signal Descriptions table. The DQS signal from the bus is used to strobe the DDR data from the memory into input register blocks. For additional information on using DDR memory support see [LatticeXP2 High Speed I/O Interface \(TN1138\)](#).

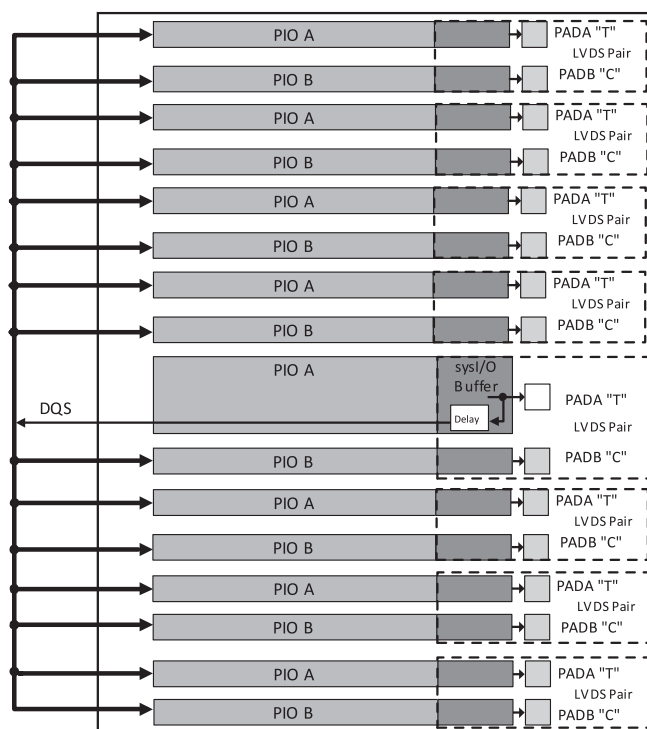


Figure 2.28. DQS Input Routing (Left and Right)

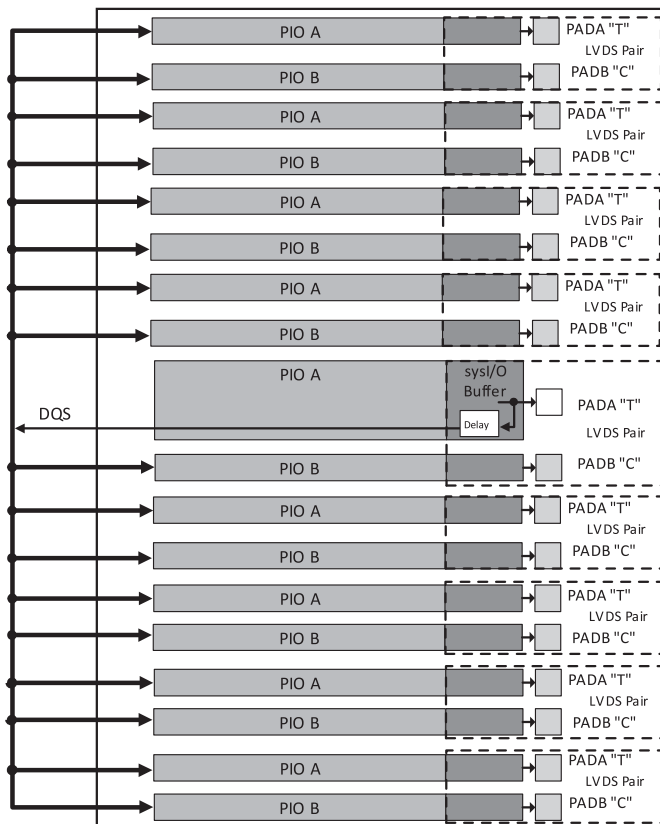


Figure 2.29. DQS Input Routing (Top and Bottom)

2.13.1. DLL Calibrated DQS Delay Block

Source synchronous interfaces generally require the input clock to be adjusted in order to correctly capture data at the input register. For most interfaces a PLL is used for this adjustment. However, in DDR memories the clock, referred to as DQS, is not free-running, and this approach cannot be used. The DQS Delay block provides the required clock alignment for DDR memory interfaces.

The DQS signal (selected PIOs only, as shown in Figure 2.30) feeds from the PAD through a DQS delay element to a dedicated DQS routing resource. The DQS signal also feeds polarity control logic which controls the polarity of the clock to the sync registers in the input register blocks. Figure 2.30 and Figure 2.31 show how the DQS transition signals are routed to the PIOs.

The temperature, voltage and process variations of the DQS delay block are compensated by a set of 6-bit bus calibration signals from two dedicated DLLs (DDR_DLL) on opposite sides of the device. Each DLL compensates DQS delays in its half of the device as shown in Figure 2.30. The DLL loop is compensated for temperature, voltage and process variations by the system clock and feedback loop.

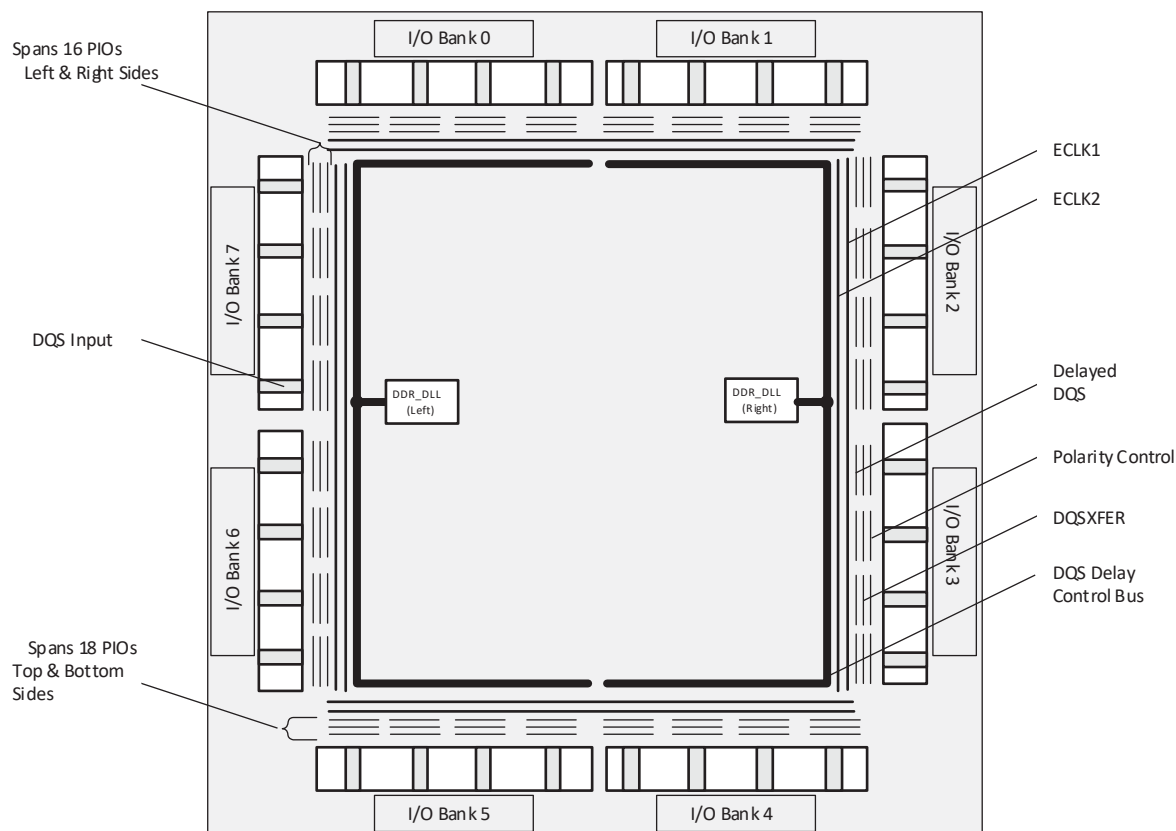


Figure 2.30. Edge Clock, DLL Calibration and DQS Local Bus Distribution

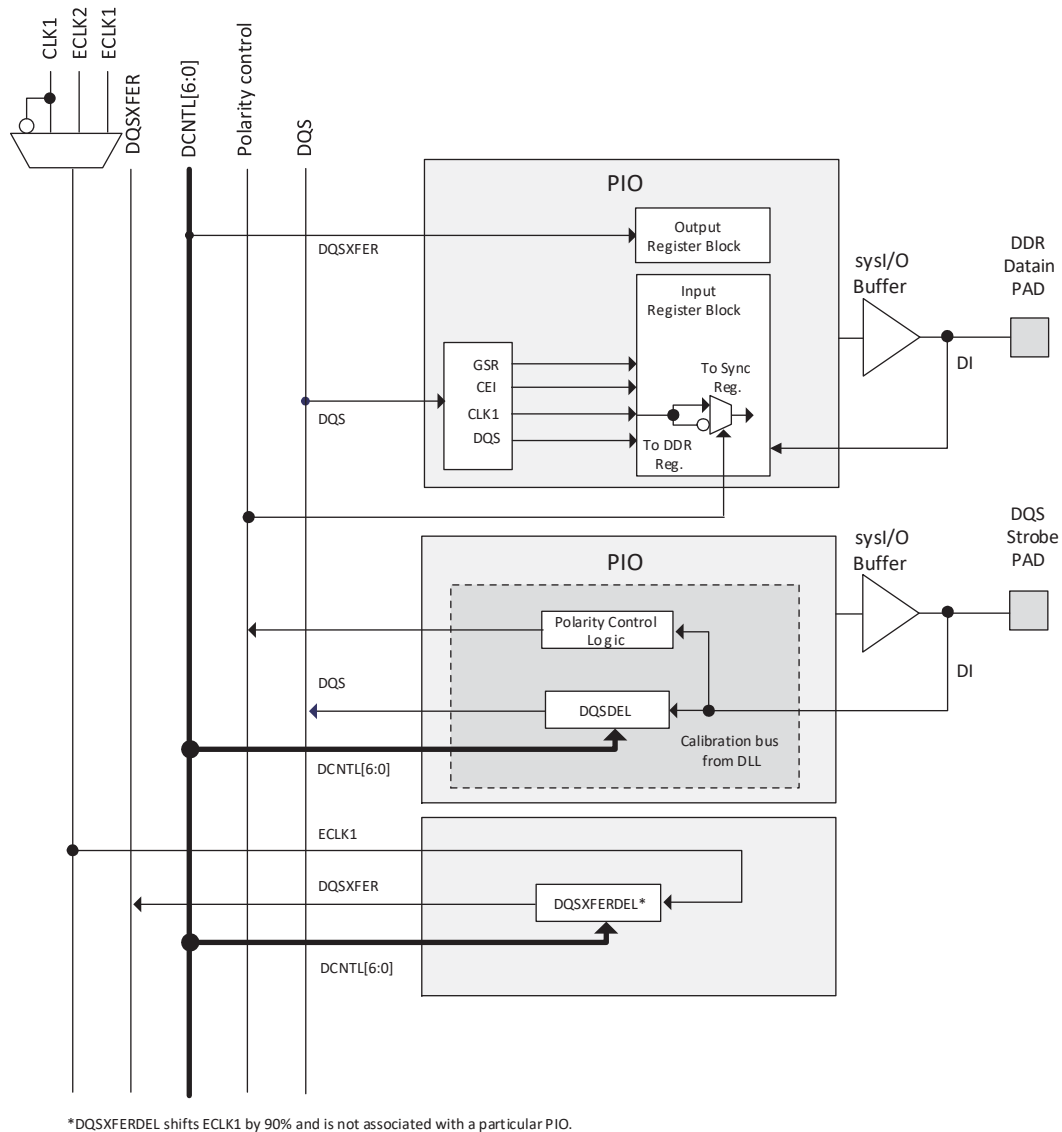


Figure 2.31. DQS Local Bus

2.13.2. Polarity Control Logic

In a typical DDR memory interface design, the phase relationship between the incoming delayed DQS strobe and the internal system clock (during the READ cycle) is unknown. The LatticeXP2 family contains dedicated circuits to transfer data between these domains. To prevent set-up and hold violations, at the domain transfer between DQS (delayed) and the system clock, a clock polarity selector is used. This changes the edge on which the data is registered in the synchronizing registers in the input register block and requires evaluation at the start of each READ cycle for the correct clock polarity.

Prior to the READ operation in DDR memories, DQS is in tristate (pulled by termination). The DDR memory device drives DQS low at the start of the preamble state. A dedicated circuit detects this transition. This signal is used to control the polarity of the clock to the synchronizing registers.

2.13.3. DQSXFER

LatticeXP2 devices provide a DQSXFER signal to the output buffer to assist it in data transfer to DDR memories that require DQS strobe be shifted 90°. This shifted DQS strobe is generated by the DQSDEL block. The DQSXFER signal runs the span of the data bus.

2.14. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement the wide variety of standards that are found in today's systems including LVCMOS, SSTL, HSTL, LVDS and LVPECL.

2.14.1. sysI/O Buffer Banks

LatticeXP2 devices have eight sysI/O buffer banks for user I/O arranged two per side. Each bank is capable of supporting multiple I/O standards. Each sysI/O bank has its own I/O supply voltage (V_{CCIO}). In addition, each bank has voltage references, V_{REF1} and V_{REF2} , that allow it to be completely independent from the others. Figure 2.32 shows the eight banks and their associated supplies.

In LatticeXP2 devices, single-ended output buffers and ratioed input buffers (LVTTTL, LVCMOS and PCI) are powered using V_{CCIO} . LVTTTL, LVCMOS33, LVCMOS25 and LVCMOS12 can also be set as fixed threshold inputs independent of V_{CCIO} .

Each bank can support up to two separate V_{REF} voltages, V_{REF1} and V_{REF2} , that set the threshold for the referenced input buffers. Some dedicated I/O pins in a bank can be configured to be a reference voltage supply pin. Each I/O is individually configurable based on the bank's supply and reference voltages.

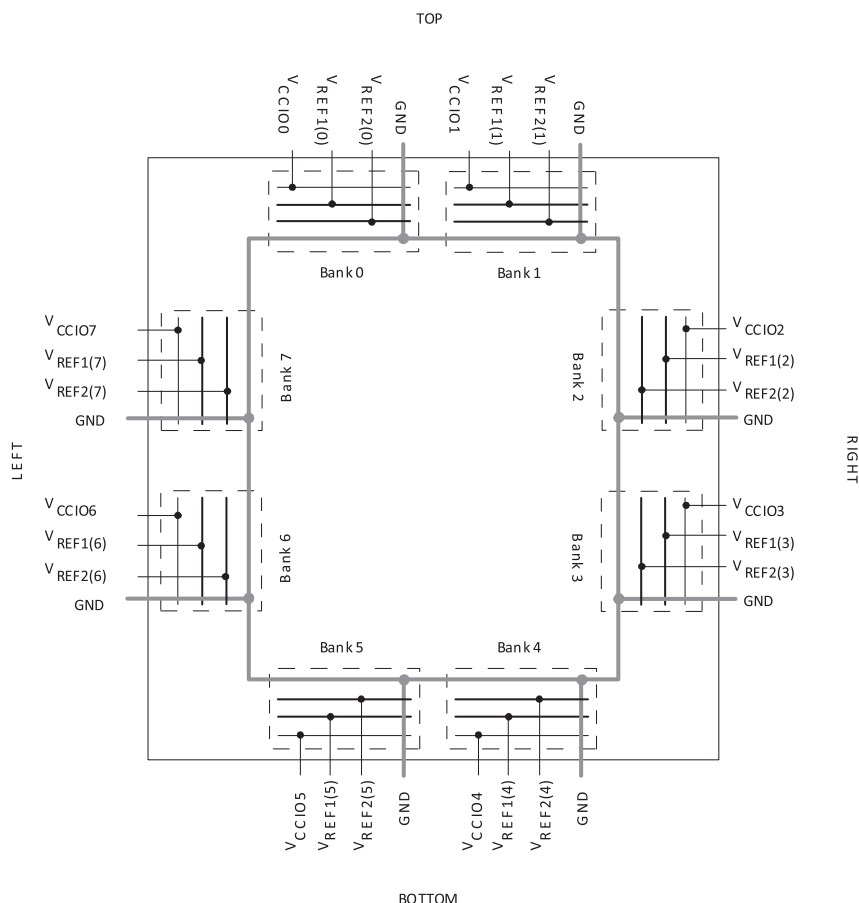


Figure 2.32. LatticeXP2 Banks

LatticeXP2 devices contain two types of sysI/O buffer pairs.

1. Top and Bottom (Banks 0, 1, 4 and 5) sysI/O Buffer Pairs (Single-Ended Outputs Only)

The sysI/O buffer pairs in the top banks of the device consist of two single-ended output drivers and two sets of single-ended input buffers (both ratioed and referenced). One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential input buffer and the comp (complementary) pad is associated with the negative side of the differential input buffer.

Only the I/O on the top and bottom banks have programmable PCI clamps.

2. Left and Right (Banks 2, 3, 6 and 7) sysI/O Buffer Pairs (50% Differential and 100% Single-Ended Outputs)

The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers, two sets of single-ended input buffers (both ratioed and referenced) and one differential output driver. One of the referenced input buffers can also be configured as a differential input.

The two pads in the pair are described as “true” and “comp”, where the true pad is associated with the positive side of the differential I/O, and the comp pad is associated with the negative side of the differential I/O.

LVDS differential output drivers are available on 50% of the buffer pairs on the left and right banks.

2.14.2. Typical sysI/O I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} , V_{CCCONF} (V_{CCIO7}) and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated, the FPGA core logic becomes active. It is your responsibility to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. During power up and before the FPGA core logic becomes active, all user I/O are high-impedance with weak pull-up. Refer to [LatticeXP2 sysI/O Usage Guide \(TN1136\)](#) for additional information.

The V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas the V_{CCIO} supplies power to the I/O buffers. In order to simplify system design while providing consistent and predictable I/O behavior, it is recommended that the I/O buffers be powered-up prior to the FPGA core fabric. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.

2.14.3. Supported sysI/O Standards

The LatticeXP2 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS, LVTTTL and other standards. The buffers support the LVTTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V standards. In the LVCMOS and LVTTTL modes, the buffer has individual configuration options for drive strength, bus maintenance (weak pull-up, weak pull-down, or a bus-keeper latch) and open drain. Other single-ended standards supported include SSTL and HSTL. Differential standards supported include LVDS, MLVDS, BLVDS, LVPECL, RSDS, differential SSTL and differential HSTL. [Table 2.12](#) and [Table 2.13](#) show the I/O standards (together with their supply and reference voltages) supported by LatticeXP2 devices. For further information on utilizing the sysI/O buffer to support a variety of standards, see [LatticeXP2 sysI/O Usage Guide \(TN1136\)](#).

Table 2.12. Supported Input Standards

| Input Standard | VREF (Nom.) | VCCIO* (Nom.) |
|----------------------------------|-------------|---------------|
| Single Ended Interfaces | | |
| LVTTTL | — | — |
| LVC MOS33 | — | — |
| LVC MOS25 | — | — |
| LVC MOS18 | — | 1.8 |
| LVC MOS15 | — | 1.5 |
| LVC MOS12 | — | — |
| PCI33 | — | — |
| HSTL18 Class I, II | 0.9 | — |
| HSTL15 Class I | 0.75 | — |
| SSTL33 Class I, II | 1.5 | — |
| SSTL25 Class I, II | 1.25 | — |
| SSTL18 Class I, II | 0.9 | — |
| Differential Interfaces | | |
| Differential SSTL18 Class I, II | — | — |
| Differential SSTL25 Class I, II | — | — |
| Differential SSTL33 Class I, II | — | — |
| Differential HSTL15 Class I | — | — |
| Differential HSTL18 Class I, II | — | — |
| LVDS, MLVDS, LVPECL, BLVDS, RSDS | — | — |

***Note:** When not specified, VCCIO can be set anywhere in the valid operating range (page 54).

Table 2.13. Supported Output Standards

| Output Standard | Drive | VCCIO (Nom.) |
|----------------------------------|---------------------------------|--------------|
| Single-ended Interfaces | | |
| LVTTL | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | 3.3 |
| LVC MOS33 | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | 3.3 |
| LVC MOS25 | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | 2.5 |
| LVC MOS18 | 4 mA, 8 mA, 12 mA, 16 mA | 1.8 |
| LVC MOS15 | 4 mA, 8 mA | 1.5 |
| LVC MOS12 | 2 mA, 6 mA | 1.2 |
| LVC MOS33, Open Drain | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | — |
| LVC MOS25, Open Drain | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | — |
| LVC MOS18, Open Drain | 4 mA, 8 mA, 12 mA, 16 mA | — |
| LVC MOS15, Open Drain | 4 mA, 8 mA | — |
| LVC MOS12, Open Drain | 2 mA, 6 mA | — |
| PCI33 | N/A | 3.3 |
| HSTL18 Class I, II | N/A | 1.8 |
| HSTL15 Class I | N/A | 1.5 |
| SSTL33 Class I, II | N/A | 3.3 |
| SSTL25 Class I, II | N/A | 2.5 |
| SSTL18 Class I, II | N/A | 1.8 |
| Differential Interfaces | | |
| Differential SSTL33, Class I, II | N/A | 3.3 |
| Differential SSTL25, Class I, II | N/A | 2.5 |
| Differential SSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL18, Class I, II | N/A | 1.8 |
| Differential HSTL15, Class I | N/A | 1.5 |
| LVDS ^{1, 2} | N/A | 2.5 |
| MLVDS ¹ | N/A | 2.5 |
| BLVDS ¹ | N/A | 2.5 |
| LVPECL ¹ | N/A | 3.3 |
| RSDS ¹ | N/A | 2.5 |
| LVC MOS33D ¹ | 4 mA, 8 mA, 12 mA, 16 mA, 20 mA | 3.3 |

Notes:

1. Emulated with external resistors.
2. On the left and right edges, LVDS outputs are supported with a dedicated differential output driver on 50% of the I/O. This solution does not require external resistors at the driver.

2.14.4. Hot Socketing

LatticeXP2 devices have been carefully designed to ensure predictable behavior during power-up and powerdown. Power supplies can be sequenced in any order. During power-up and power-down sequences, the I/O remain in tri-state until the power supply voltage is high enough to ensure reliable operation. In addition, leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the LatticeXP2 ideal for many multiple power supply and hot-swap applications.

2.15. IEEE 1149.1-Compliant Boundary Scan Testability

All LatticeXP2 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant Test Access Port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port has its own supply voltage V_{CC} and can operate with LVCMOS3.3, 2.5, 1.8, 1.5 and 1.2 standards. For more information, see [LatticeXP2 sysCONFIG Usage Guide \(TN1141\)](#).

2.16. flexiFLASH Device Configuration

The LatticeXP2 devices combine Flash and SRAM on a single chip to provide users with flexibility in device programming and configuration. [Figure 2.33](#) provides an overview of the arrangement of Flash and SRAM configuration cells within the device. The remainder of this section provides an overview of these capabilities. See [LatticeXP2 sysCONFIG Usage Guide \(TN1141\)](#) for a more detailed description.

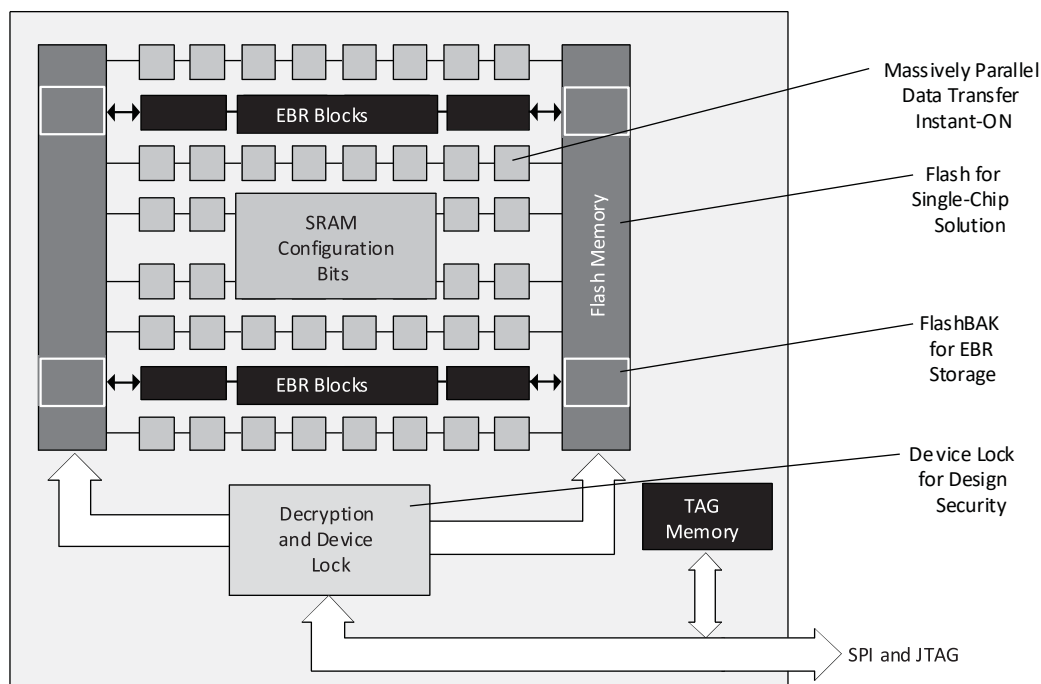


Figure 2.33. Overview of Flash and SRAM Configuration Cells Within LatticeXP2 Devices

At power-up, or on user command, data is transferred from the on-chip Flash memory to the SRAM configuration cells that control the operation of the device. This is done with massively parallel buses enabling the parts to operate within microseconds of the power supplies reaching valid levels; this capability is referred to as Instant-On.

The on-chip Flash enables a single-chip solution eliminating the need for external boot memory. This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports. The JTAG port is IEEE 1149.1 and IEEE 1532 compliant.

As described in the EBR section of the data sheet, the FlashBAK capability of the parts enables the contents of the EBR blocks to be written back into the Flash storage area without erasing or reprogramming other aspects of the device configuration. Serial TAG memory is also available to allow the storage of small amounts of data such as calibration coefficients and error codes.

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM only FPGAs. This is further enhanced by device locking. The device can be in one of three modes:

1. Unlocked
2. Key Locked – Presenting the key through the programming interface allows the device to be unlocked.
3. Permanently Locked – The device is permanently locked.

To further complement the security of the device a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash portion of the device.

2.16.1. Serial TAG Memory

LatticeXP2 devices offer 0.6 to 3.3kbits of Flash memory in the form of Serial TAG memory. The TAG memory is an area of the on-chip Flash that can be used for non-volatile storage including electronic ID codes, version codes, date stamps, asset IDs and calibration settings. A block diagram of the TAG memory is shown in Figure 2.34. The TAG memory is accessed in the same way as external SPI Flash and it can be read or programmed either through JTAG, an external Slave SPI Port, or directly from FPGA logic. To read the TAG memory, a start address is specified and the entire TAG memory contents are read sequentially in a first-in-first-out manner. The TAG memory is independent of the Flash used for device configuration and given its use for general-purpose storage functions is always accessible regardless of the device security settings. For more information, see [LatticeXP2 Memory Usage Guide \(FPGA-UG-02080\)](#) and [LatticeXP2 sysCONFIG Usage Guide \(TN1141\)](#).

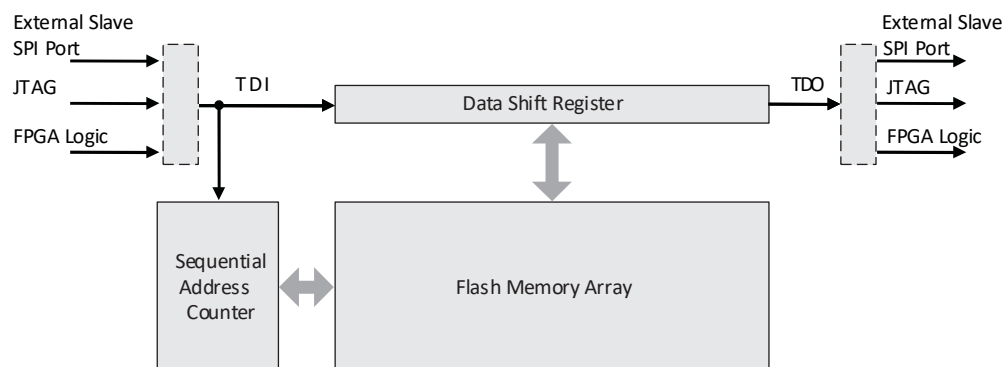


Figure 2.34. Serial TAG Memory Diagram

2.16.2. Live Update Technology

Many applications require field updates of the FPGA. LatticeXP2 devices provide three features that enable this configuration to be done in a secure and failsafe manner while minimizing impact on system operation.

1. Decryption Support

LatticeXP2 devices provide on-chip, non-volatile key storage to support decryption of a 128-bit AES encrypted bitstream, securing designs and deterring design piracy.

2. TransFR (Transparent Field Reconfiguration)

TransFR I/O (TFR) is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a single ispVM command. TransFR I/O allows I/O states to be frozen during device configuration. This allows the device to be field updated with a minimum of system disruption and downtime. For more information, see [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#).

3. Dual Boot Image Support

Dual boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the LatticeXP2 can be re-booted from this new configuration file. If there is a problem such as corrupt data during download or incorrect version number with this new boot image, the LatticeXP2 device can revert back to the original backup configuration and try again. This all can be done without power cycling the system. For more information, see [LatticeXP2 Dual Boot Feature \(TN1220\)](#).

For more information on device configuration, see [LatticeXP2 sysCONFIG Usage Guide \(TN1141\)](#).

2.16.3. Soft Error Detect (SED) Support

LatticeXP2 devices have dedicated logic to perform Cyclic Redundancy Code (CRC) checks. During configuration, the configuration data bitstream can be checked with the CRC logic block. In addition, LatticeXP2 devices can be programmed for checking soft errors in SRAM. SED can be run on a programmed device when the user logic is not active. In the event a soft error occurs, the device can be programmed to either reload from a known good boot image (from internal Flash or external SPI memory) or generate an error signal.

For further information on SED support, see [LatticeXP2 Soft Error Detection \(SED\) Usage Guide \(TN1130\)](#).

2.16.4. On-Chip Oscillator

Every LatticeXP2 device has an internal CMOS oscillator that is used to derive a Master Clock (CCLK) for configuration. The oscillator and CCLK run continuously and are available to user logic after configuration is complete. The available CCLK frequencies are listed in [Table 2.14](#). When a different CCLK frequency is selected during the design process, the following sequence takes place:

1. Device powers up with the default CCLK frequency.
2. During configuration, users select a different CCLK frequency.
3. CCLK frequency changes to the selected frequency after clock configuration bits are received.

This internal CMOS oscillator is available to you by routing it as an input clock to the clock tree. For further information on the use of this oscillator for configuration or user mode, see [LatticeXP2 sysCLOCK PLL Design and Usage Guide \(TN1126\)](#).

Table 2.14. Selectable CCLKs and Oscillator Frequencies During Configuration and User Mode

| CCLK/Oscillator (MHz) |
|-----------------------|
| 2.51 |
| 3.12 |
| 4.3 |
| 5.4 |
| 6.9 |
| 8.1 |
| 9.2 |
| 10 |
| 13 |
| 15 |
| 20 |
| 26 |
| 32 |
| 40 |
| 54 |
| 803 |
| 1633 |

Notes:

1. Software default oscillator frequency.
2. Software default CCLK frequency.
3. Frequency not valid for CCLK.

2.17. Density Shifting

The LatticeXP2 family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likely success in each case.

3. DC and Switching Characteristics

3.1. Absolute Maximum Ratings

Table 3.1. Absolute Maximum Ratings^{1, 2, 3}

| Parameter | Min | Max | Unit |
|--|------|------|------|
| Supply Voltage V_{CC} | -0.5 | 1.32 | V |
| Supply Voltage V_{CCAUX} | -0.5 | 3.75 | V |
| Supply Voltage V_{CCJ} | -0.5 | 3.75 | V |
| Supply Voltage V_{CCPLL}^4 | -0.5 | 3.75 | V |
| Output Supply Voltage V_{CCIO} | -0.5 | 3.75 | V |
| Input or I/O Tristate Voltage Applied ⁵ | -0.5 | 3.75 | V |
| Storage Temperature (Ambient) | -65 | 150 | °C |
| Junction Temperature Under Bias (T_j) | +125 | | °C |

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
5. Overshoot and undershoot of -2V to ($V_{IHMAX} + 2$) volts is permitted for a duration of <20 ns.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions

| Symbol | Parameter | Min. | Max. | Units |
|----------------------|---|-------|-------|-------|
| V_{CC} | Core Supply Voltage | 1.14 | 1.26 | V |
| $V_{CCAUX}^{4, 5}$ | Auxiliary Supply Voltage | 3.135 | 3.465 | V |
| V_{CCPLL}^1 | PLL Supply Voltage | 3.135 | 3.465 | V |
| $V_{CCIO}^{2, 3, 4}$ | I/O Driver Supply Voltage | 1.14 | 3.465 | V |
| V_{CCJ}^2 | Supply Voltage for IEEE 1149.1 Test Access Port | 1.14 | 3.465 | V |
| t_{JCOM} | Junction Temperature, Commercial Operation | 0 | 85 | °C |
| t_{JIND} | Junction Temperature, Industrial Operation | -40 | 100 | °C |

Notes:

1. V_{CCPLL} only available on csBGA, PQFP and TQFP packages.
2. If V_{CCIO} or V_{CCJ} is set to 1.2 V, they must be connected to the same power supply as V_{CC} . If V_{CCIO} or V_{CCJ} is set to 3.3 V, they must be connected to the same power supply as V_{CCAUX} .
3. See recommended voltages by I/O standard in subsequent table.
4. To ensure proper I/O behavior, V_{CCIO} must be turned off at the same time or earlier than V_{CCAUX} .
5. In fpBGA and ftBGA packages, the PLLs are connected to, and powered from, the auxiliary power supply.

3.3. On-Chip Flash Memory Specifications

Table 3.3. On-Chip Flash Memory Specifications

| Symbol | Parameter | Max. | Units |
|----------------------|---|---------|--------|
| N _{PROGCYC} | Flash Programming Cycles per t _{RETENTION} * | 10,000 | Cycles |
| | Flash Functional Programming Cycles | 100,000 | |

*Note: The minimum data retention, t_{RETENTION}, is 20 years.

3.4. Hot Socketing Specifications

Table 3.4. Hot Socketing Specifications

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------|------------------------------|--|------|------|------|-------|
| IDK | Input or I/O Leakage Current | $0 \leq V_{IN} \leq V_{IH} \text{ (MAX.)}$ | — | — | +/-1 | mA |

Notes:

- Insensitive to sequence of V_{CC}, V_{CCAUX} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC}, V_{CCAUX} and V_{CCIO}.
- $0 \leq V_{CC} \leq V_{CC} \text{ (MAX.)}$, $0 \leq V_{CCIO} \leq V_{CCIO} \text{ (MAX.)}$ or $0 \leq V_{CCAUX} \leq V_{CCAUX} \text{ (MAX.)}$.
- I_{DK} is additive to I_{PU}, I_{PD} or I_{BH}.
- LVCMOS and LVTTTL only.

3.5. ESD Performance

Refer to the [LatticeXP2 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

3.6. DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.5. DC Electrical Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--|----------------------------------|--|-----------------------|------|-----------------------|-------|
| I _{IL} , I _{IH} ¹ | Input or I/O Low Leakage | $0 \leq V_{IN} \leq V_{CCIO}$ | — | — | 10 | μA |
| | | $V_{CCIO} \leq V_{IN} \leq V_{IH} \text{ (MAX.)}$ | — | — | 150 | μA |
| I _{PU} | I/O Active Pull-up Current | $0 \leq V_{IN} \leq 0.7 V_{CCIO}$ | -30 | — | -150 | μA |
| I _{PD} | I/O Active Pull-down Current | $V_{IL} \text{ (MAX.)} \leq V_{IN} \leq V_{CCIO}$ | 30 | — | 210 | μA |
| I _{BHLS} | Bus Hold Low Sustaining Current | $V_{IN} = V_{IL} \text{ (MAX.)}$ | 30 | — | — | μA |
| I _{BHHS} | Bus Hold High Sustaining Current | $V_{IN} = 0.7 V_{CCIO}$ | -30 | — | — | μA |
| I _{BHLO} | Bus Hold Low Overdrive Current | $0 \leq V_{IN} \leq V_{CCIO}$ | — | — | 210 | μA |
| I _{BHHO} | Bus Hold High Overdrive Current | $0 \leq V_{IN} \leq V_{CCIO}$ | — | — | -150 | μA |
| V _{BHT} | Bus Hold Trip Points | | V _{IL} (MAX) | — | V _{IH} (MIN) | V |
| C1 | I/O Capacitance ² | V _{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V _{CC} = 1.2 V, V _{IO} = 0 to V _{IH} (MAX) | — | 8 | — | pf |
| C2 | Dedicated Input Capacitance | V _{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, V _{CC} = 1.2 V, V _{IO} = 0 to V _{IH} (MAX) | — | 6 | — | pf |

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. TA 25°C, f = 1.0 MHz.

3.7. Supply Current (Standby)

Table 3.6. Supply Current (Standby)^{1, 2, 3, 4}

| Symbol | Parameter | Device | Typical ⁵ | Units |
|-------------|---|--------|----------------------|-------|
| I_{CC} | Core Power Supply Current | XP2-5 | 14 | mA |
| | | XP2-8 | 18 | mA |
| | | XP2-17 | 24 | mA |
| | | XP2-30 | 35 | mA |
| | | XP2-40 | 45 | mA |
| I_{CCAUX} | Auxiliary Power Supply Current ⁶ | XP2-5 | 15 | mA |
| | | XP2-8 | 15 | mA |
| | | XP2-17 | 15 | mA |
| | | XP2-30 | 16 | mA |
| | | XP2-40 | 16 | mA |
| I_{CCPLL} | PLL Power Supply Current (per PLL) | — | 0.1 | mA |
| I_{CCIO} | Bank Power Supply Current (per bank) | — | 2 | mA |
| I_{CCJ} | V_{CCJ} Power Supply Current | — | 0.25 | mA |

Notes:

- For further information on supply current, see [Power Estimation and Management for LatticeXP2 Devices \(TN1139\)](#).
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 MHz.
- Pattern represents a “blank” configuration data file. A “blank” pattern configures the part to the following conditions:
 - All outputs are tri-stated, all inputs are held at either V_{CCIO} , or GND.
 - All clock inputs are at 0 MHz.
 - $T_J = 25^\circ\text{C}$, all power supplies at nominal voltages.
 - No pull-ups on I/O.
- $T_J = 25^\circ\text{C}$, power supplies at nominal voltage.
- In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL} . For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

3.8. Initialization Supply Current

Over Recommended Operating Conditions

Table 3.7. Initialization Supply Current^{1, 2, 3, 4, 5}

| Symbol | Parameter | Device | Typical (25°C, Max. Supply) ⁶ | Units |
|--------------------|---|--------|--|-------|
| I _{CC} | Core Power Supply Current | XP2-5 | 20 | mA |
| | | XP2-8 | 21 | mA |
| | | XP2-17 | 44 | mA |
| | | XP2-30 | 58 | mA |
| | | XP2-40 | 62 | mA |
| I _{CCAUX} | Auxiliary Power Supply Current ⁷ | XP2-5 | 67 | mA |
| | | XP2-8 | 74 | mA |
| | | XP2-17 | 112 | mA |
| | | XP2-30 | 124 | mA |
| | | XP2-40 | 130 | mA |
| I _{CCPLL} | PLL Power Supply Current (per PLL) | — | 1.8 | mA |
| I _{CCIO} | Bank Power Supply Current (per Bank) | — | 6.4 | mA |
| I _{CCJ} | VCCJ Power Supply Current | — | 1.2 | mA |

Notes:

- For further information on supply current, see [Power Estimation and Management for LatticeXP2 Devices \(TN1139\)](#).
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 MHz.
- Does not include additional current from bypass or decoupling capacitor across the supply.
- A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
- T_J = 25°C, power supplies at nominal voltage.
- In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.

3.9. Programming and Erase Flash Supply Current

Over Recommended Operating Conditions

Table 3.8. Programming and Erase Flash Supply Current^{1, 2, 3, 4, 5}

| Symbol | Parameter | Device | Typical (25°C, Max. Supply) ⁶ | Units |
|--------------------|--|--------|---|-------|
| I _{CC} | Core Power Supply Current | XP2-5 | 17 | mA |
| | | XP2-8 | 21 | mA |
| | | XP2-17 | 28 | mA |
| | | XP2-30 | 36 | mA |
| | | XP2-40 | 50 | mA |
| I _{CCAUX} | Auxiliary Power Supply Current ⁷ | XP2-5 | 64 | mA |
| | | XP2-8 | 66 | mA |
| | | XP2-17 | 83 | mA |
| | | XP2-30 | 87 | mA |
| | | XP2-40 | 88 | mA |
| I _{CCPLL} | PLL Power Supply Current (per PLL) | — | 0.1 | mA |
| I _{CCIO} | Bank Power Supply Current (per Bank) | — | 5 | mA |
| I _{CCJ} | V _{CCJ} Power Supply Current ⁸ | — | 14 | mA |

Notes:

- For further information on supply current, see [Power Estimation and Management for LatticeXP2 Devices \(TN1139\)](#).
- Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
- Frequency 0 MHz (excludes dynamic power from FPGA operation).
- A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.
- Bypass or decoupling capacitor across the supply.
- T_J = 25°C, power supplies at nominal voltage.
- In fpBGA and ftBGA packages the PLLs are connected to and powered from the auxiliary power supply. For these packages, the actual auxiliary supply current is the sum of I_{CCAUX} and I_{CCPLL}. For csBGA, PQFP and TQFP packages the PLLs are powered independent of the auxiliary power supply.
- When programming via JTAG.

3.10. sysl/O Recommended Operating Conditions

Over Recommended Operating Conditions

Table 3.9. sysl/O Recommended Operating Conditions

| Standard | V _{CCIO} | | | V _{REF} (V) | | |
|---|-------------------|------|-------|----------------------|------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| LVC MOS33 ² | 3.135 | 3.3 | 3.465 | — | — | — |
| LVC MOS25 ² | 2.375 | 2.5 | 2.625 | — | — | — |
| LVC MOS18 | 1.71 | 1.8 | 1.89 | — | — | — |
| LVC MOS15 | 1.425 | 1.5 | 1.575 | — | — | — |
| LVC MOS12 ² | 1.14 | 1.2 | 1.26 | — | — | — |
| LVTTL33 ² | 3.135 | 3.3 | 3.465 | — | — | — |
| PCI33 | 3.135 | 3.3 | 3.465 | — | — | — |
| SSTL18_I ² , SSTL18_II ² | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 |
| SSTL25_I ² , SSTL25_II ² | 2.375 | 2.5 | 2.625 | 1.15 | 1.25 | 1.35 |
| SSTL33_I ² , SSTL33_II ² | 3.135 | 3.3 | 3.465 | 1.3 | 1.5 | 1.7 |
| HSTL15_I ² | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 |
| HSTL18_I ² , HSTL18_II ² | 1.71 | 1.8 | 1.89 | 0.816 | 0.9 | 1.08 |
| LVDS25 ² | 2.375 | 2.5 | 2.625 | — | — | — |
| MLVDS25 ¹ | 2.375 | 2.5 | 2.625 | — | — | — |
| LVPECL33 ^{1, 2} | 3.135 | 3.3 | 3.465 | — | — | — |
| BLVDS25 ^{1, 2} | 2.375 | 2.5 | 2.625 | — | — | — |
| RSDS ^{1, 2} | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL18D_I ² , SSTL18D_II ² | 1.71 | 1.8 | 1.89 | — | — | — |
| SSTL25D_I ² , SSTL25D_II ² | 2.375 | 2.5 | 2.625 | — | — | — |
| SSTL33D_I ² , SSTL33D_II ² | 3.135 | 3.3 | 3.465 | — | — | — |
| HSTL15D_I ² | 1.425 | 1.5 | 1.575 | — | — | — |
| HSTL18D_I ² , HSTL18D_II ² | 1.71 | 1.8 | 1.89 | — | — | — |

Notes:

1. Inputs on chip. Outputs are implemented with the addition of external resistors.
2. Input on this standard does not depend on the value of V_{CCIO}.

3.11. sysI/O Single-Ended DC Electrical Characteristics

Over Recommended Operating Conditions

Table 3.10. sysI/O Single-Ended DC Electrical Characteristics

| Input/Output Standard | V _{IL} | | V _{IH} | | V _{OL} | V _{OH} | I _{OL} * (mA) | I _{OH} * (mA) |
|-----------------------|-----------------|--------------------------|--------------------------|----------|-----------------------|--------------------------|------------------------|------------------------|
| | Min. (V) | Max. (V) | Min. (V) | Max. (V) | Max. (V) | Min. (V) | | |
| LVCMOS33 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| LVTTTL33 | -0.3 | 0.8 | 2.0 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| LVCMOS25 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 20, 16, 12, 8, 4 | -20, -16, -12, -8, -4 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| LVCMOS18 | -0.3 | 0.35 V _{CCIO} | 0.65 V _{CCIO} | 3.6 | 0.4 | V _{CCIO} - 0.4 | 16, 12, 8, 4 | -16, -12, -8, -4 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| LVCMOS15 | -0.3 | 0.35 V _{CCIO} | 0.65 V _{CCIO} | 3.6 | 0.4 | V _{CCIO} - 0.4 | 8, 4 | -8, -4 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| LVCMOS12 | -0.3 | 0.35 V _{CC} | 0.65 V _{CC} | 3.6 | 0.4 | V _{CCIO} - 0.4 | 6, 2 | -6, -2 |
| | | | | | 0.2 | V _{CCIO} - 0.2 | 0.1 | -0.1 |
| PCI33 | -0.3 | 0.3 V _{CCIO} | 0.5 V _{CCIO} | 3.6 | 0.1 V _{CCIO} | 0.9 V _{CCIO} | 1.5 | -0.5 |
| SSTL33_I | -0.3 | V _{REF} - 0.2 | V _{REF} + 0.2 | 3.6 | 0.7 | V _{CCIO} - 1.1 | 8 | -8 |
| SSTL33_II | -0.3 | V _{REF} - 0.2 | V _{REF} + 0.2 | 3.6 | 0.5 | V _{CCIO} - 0.9 | 16 | -16 |
| SSTL25_I | -0.3 | V _{REF} - 0.18 | V _{REF} + 0.18 | 3.6 | 0.54 | V _{CCIO} - 0.62 | 7.6 | -7.6 |
| | | | | | | | 12 | -12 |
| SSTL25_II | -0.3 | V _{REF} - 0.18 | V _{REF} + 0.18 | 3.6 | 0.35 | V _{CCIO} - 0.43 | 15.2 | -15.2 |
| | | | | | | | 20 | -20 |
| SSTL18_I | -0.3 | V _{REF} - 0.125 | V _{REF} + 0.125 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 6.7 | -6.7 |
| SSTL18_II | -0.3 | V _{REF} - 0.125 | V _{REF} + 0.125 | 3.6 | 0.28 | V _{CCIO} - 0.28 | 8 | -8 |
| | | | | | | | 11 | -11 |
| HSTL15_I | -0.3 | V _{REF} - 0.1 | V _{REF} + 0.1 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 4 | -4 |
| | | | | | | | 8 | -8 |
| HSTL18_I | -0.3 | V _{REF} - 0.1 | V _{REF} + 0.1 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 8 | -8 |
| | | | | | | | 12 | -12 |
| HSTL18_II | -0.3 | V _{REF} - 0.1 | V _{REF} + 0.1 | 3.6 | 0.4 | V _{CCIO} - 0.4 | 16 | -16 |

***Note:** The average DC current drawn by I/O between GND connections, or between the last GND in an I/O bank and the end of an I/O bank, as shown in the logic signal connections table shall not exceed n * 8 mA, where n is the number of I/O between bank GND connections or between the last GND in a bank and the end of a bank.

3.12. sysI/O Differential Electrical Characteristics

3.12.1. LVDS

Over Recommended Operating Conditions

Table 3.11. LVDS

| Parameter | Description | Test Conditions | Min. | Typ. | Max. | Units |
|--------------------|--|---|---------|------|-------|---------|
| V_{INP}, V_{INM} | Input Voltage | — | 0 | — | 2.4 | V |
| V_{CM} | Input Common Mode Voltage | Half the Sum of the Two Inputs | 0.05 | — | 2.35 | V |
| V_{THD} | Differential Input Threshold | Difference Between the Two Inputs | +/- 100 | — | — | mV |
| I_{IN} | Input Current | Power On or Power Off | — | — | +/-10 | μ A |
| V_{OH} | Output High Voltage for V_{OP} or V_{OM} | $R_T = 100 \text{ Ohm}$ | — | 1.38 | 1.60 | V |
| V_{OL} | Output Low Voltage for V_{OP} or V_{OM} | $R_T = 100 \text{ Ohm}$ | 0.9V | 1.03 | — | V |
| V_{OD} | Output Voltage Differential | $(V_{OP} - V_{OM}), R_T = 100 \Omega$ | 250 | 350 | 450 | mV |
| ΔV_{OD} | Change in V_{OD} Between High and Low | — | — | — | 50 | mV |
| V_{OS} | Output Voltage Offset | $(V_{OP} + V_{OM})/2, R_T = 100 \Omega$ | 1.125 | 1.20 | 1.375 | V |
| ΔV_{OS} | Change in V_{OS} Between H and L | — | — | — | 50 | mV |
| I_{SA} | Output Short Circuit Current | $V_{OD} = 0 \text{ V}$ Driver Outputs Shorted to Ground | — | — | 24 | mA |
| I_{SAB} | Output Short Circuit Current | $V_{OD} = 0 \text{ V}$ Driver Outputs Shorted to Each Other | — | — | 12 | mA |

3.12.2. Differential HSTL and SSTL

Differential HSTL and SSTL outputs are implemented as a pair of complementary single-ended outputs. All allowable single-ended output classes (class I and class II) are supported in this mode.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces, see details in additional technical notes listed at the end of this data sheet.

3.12.3. LVDS25E

The top and bottom sides of LatticeXP2 devices support LVDS outputs via emulated complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The scheme shown in [Figure 3.1](#) is one possible solution for point-to-point signals.

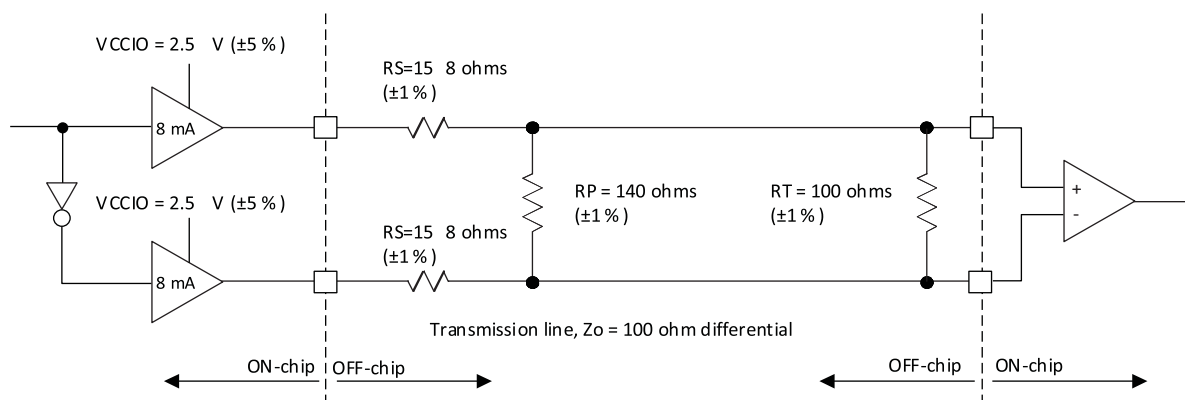


Figure 3.1. LVDS25E Output Termination Example

Table 3.12. LVDS25E DC Conditions

| Parameter | Description | Typical | Units |
|------------|--|---------|----------|
| V_{CCIO} | Output Driver Supply (+/-5%) | 2.50 | V |
| Z_{OUT} | Driver Impedance | 20 | Ω |
| R_S | Driver Series Resistor (+/-1%) | 158 | Ω |
| R_P | Driver Parallel Resistor (+/-1%) | 140 | Ω |
| R_T | Receiver Termination (+/-1%) | 100 | Ω |
| V_{OH} | Output High Voltage (after R_P) | 1.43 | V |
| V_{OL} | Output Low Voltage (after R_P) | 1.07 | V |
| V_{OD} | Output Differential Voltage (After R_P) | 0.35 | V |
| V_{CM} | Output Common Mode Voltage | 1.25 | V |
| Z_{BACK} | Back Impedance | 100.5 | Ω |
| I_{DC} | DC Output Current | 6.03 | mA |

3.12.4. LVCMOS33D

All I/O banks support emulated differential I/O using the LVCMOS33D I/O type. This option, along with the external resistor network, provides the system designer the flexibility to place differential outputs on an I/O bank with 3.3 V V_{CCIO} . The default drive current for LVCMOS33D output is 12 mA with the option to change the device strength to 4 mA, 8 mA, 16 mA or 20 mA. Follow the LVCMOS33 specifications for the DC characteristics of the LVCMOS33D.

3.12.5. BLVDS

The LatticeXP2 devices support the BLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel external resistor across the driver outputs. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

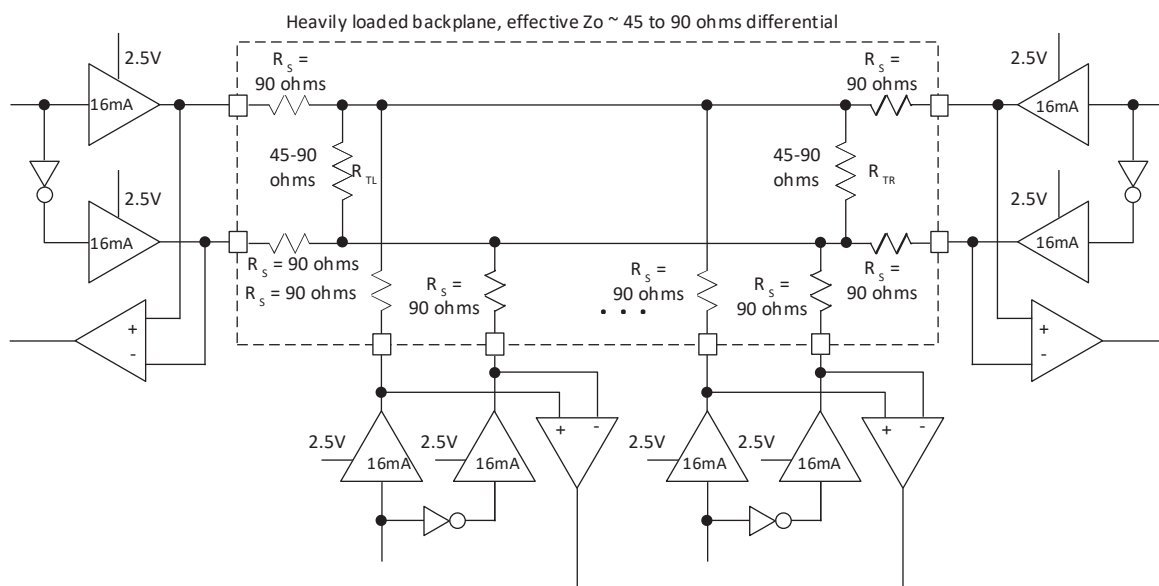


Figure 3.2. BLVDS Multi-point Output Example

Table 3.13. BLVDS DC Conditions

Over Recommended Operating Conditions

| Parameter | Description | Typical | | Units |
|-------------------|--|-----------------------|-----------------------|-------|
| | | Z _o = 45 Ω | Z _o = 90 Ω | |
| V _{CCIO} | Output Driver Supply (+/- 5%) | 2.50 | 2.50 | V |
| Z _{OUT} | Driver Impedance | 10.00 | 10.00 | Ω |
| R _S | Driver Series Resistor (+/- 1%) | 90.00 | 90.00 | Ω |
| R _{TL} | Driver Parallel Resistor (+/- 1%) | 45.00 | 90.00 | Ω |
| R _{TR} | Receiver Termination (+/- 1%) | 45.00 | 90.00 | Ω |
| V _{OH} | Output High Voltage (After R _{TL}) | 1.38 | 1.48 | V |
| V _{OL} | Output Low Voltage (After R _{TL}) | 1.12 | 1.02 | V |
| V _{OD} | Output Differential Voltage (After R _{TL}) | 0.25 | 0.46 | V |
| V _{CM} | Output Common Mode Voltage | 1.25 | 1.25 | V |
| I _{DC} | DC Output Current | 11.24 | 10.20 | mA |

Note: For input buffer, see LVDS table.

3.12.6. LVPECL

The LatticeXP2 devices support the differential LVPECL standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.3 is one possible solution for point-to-point signals.

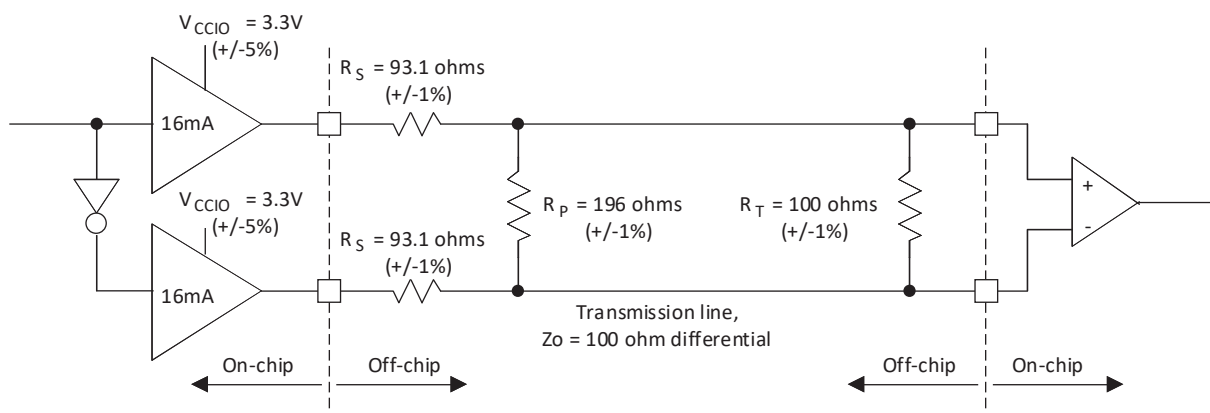


Figure 3.3. Differential LVPECL

Table 3.14. LVPECL DC Conditions

Over Recommended Operating Conditions

| Parameter | Description | Typical | Units |
|------------|--|---------|----------|
| V_{CCIO} | Output Driver Supply (+/-5%) | 3.30 | V |
| Z_{OUT} | Driver Impedance | 10 | Ω |
| R_S | Driver Series Resistor (+/-1%) | 93 | Ω |
| R_P | Driver Parallel Resistor (+/-1%) | 196 | Ω |
| R_T | Receiver Termination (+/-1%) | 100 | Ω |
| V_{OH} | Output High Voltage (After R_P) | 2.05 | V |
| V_{OL} | Output Low Voltage (After R_P) | 1.25 | V |
| V_{OD} | Output Differential Voltage (After R_P) | 0.80 | V |
| V_{CM} | Output Common Mode Voltage | 1.65 | V |
| Z_{BACK} | Back Impedance | 100.5 | Ω |
| I_{DC} | DC Output Current | 12.11 | mA |

Note: For input buffer, see LVDS table.

3.12.7. RSDS

The LatticeXP2 devices support differential RSDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The RSDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.5 is one possible solution for RSDS standard implementation. Resistor values in Figure 3.5 are industry standard values for 1% resistors.

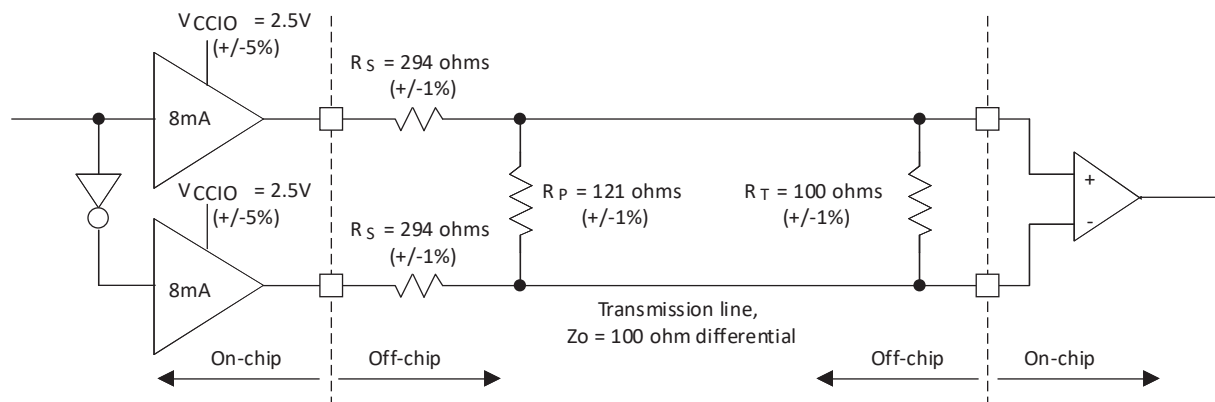


Figure 3.4. RSDS (Reduced Swing Differential Standard)

Table 3.15. RSDS DC Conditions

Over Recommended Operating Conditions

| Parameter | Description | Typical | Units |
|------------|--|---------|----------|
| V_{CCIO} | Output Driver Supply (+/-5%) | 2.50 | V |
| Z_{OUT} | Driver Impedance | 20 | Ω |
| R_S | Driver Series Resistor (+/-1%) | 294 | Ω |
| R_P | Driver Parallel Resistor (+/-1%) | 121 | Ω |
| R_T | Receiver Termination (+/-1%) | 100 | Ω |
| V_{OH} | Output High Voltage (After R_P) | 1.35 | V |
| V_{OL} | Output Low Voltage (After R_P) | 1.15 | V |
| V_{OD} | Output Differential Voltage (After R_P) | 0.20 | V |
| V_{CM} | Output Common Mode Voltage | 1.25 | V |
| Z_{BACK} | Back Impedance | 101.5 | Ω |
| I_{DC} | DC Output Current | 3.66 | mA |

Note: For input buffer, see LVDS table.

3.12.8. MLVDS

The LatticeXP2 devices support the differential MLVDS standard. This standard is emulated using complementary LVCMOS outputs in conjunction with a parallel resistor across the driver outputs. The MLVDS input standard is supported by the LVDS differential input buffer. The scheme shown in Figure 3.5 is one possible solution for MLVDS standard implementation. Resistor values in Figure 3.5 are industry standard values for 1% resistors.

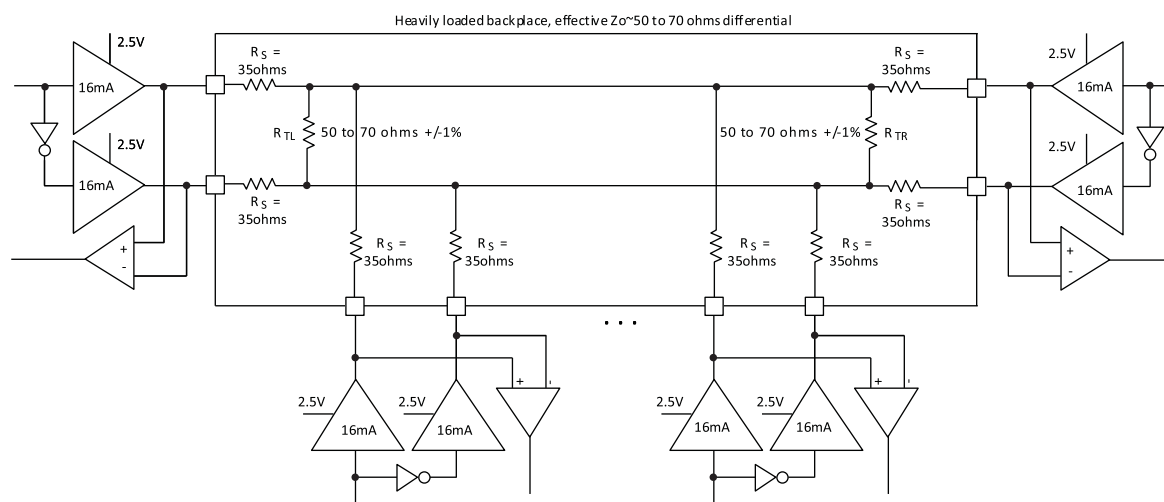


Figure 3.5. MLVDS (Reduced Swing Differential Standard)

Table 3.16. MLVDS DC Conditions

| Parameter | Description | Typical | | Units |
|-------------------|--|----------------|----------------|----------|
| | | Zo=50 Ω | Zo=70 Ω | |
| V _{CCIO} | Output Driver Supply (+/-5%) | 2.50 | 2.50 | V |
| Z _{OUT} | Driver Impedance | 10.00 | 10.00 | Ω |
| R _S | Driver Series Resistor (+/-1%) | 35.00 | 35.00 | Ω |
| R _{TL} | Driver Parallel Resistor (+/-1%) | 50.00 | 70.00 | Ω |
| R _{TR} | Receiver Termination (+/-1%) | 50.00 | 70.00 | Ω |
| V _{OH} | Output High Voltage (After R _{TL}) | 1.52 | 1.60 | V |
| V _{OL} | Output Low Voltage (After R _{TL}) | 0.98 | 0.90 | V |
| V _{OD} | Output Differential Voltage (After R _{TL}) | 0.54 | 0.70 | V |
| V _{CM} | Output Common Mode Voltage | 1.25 | 1.25 | V |
| I _{DC} | DC Output Current | 21.74 | 20.00 | mA |

Note: For input buffer, see LVDS table.

For further information on LVPECL, RSDS, MLVDS, BLVDS and other differential interfaces. see details of additional technical information at the end of this data sheet.

3.13. Typical Building Block Function Performance

3.13.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.17. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | -7 Timing | Units |
|------------------------|-----------|-------|
| Basic Functions | | |
| 16-bit Decoder | 4.4 | ns |
| 32-bit Decoder | 5.2 | ns |
| 64-bit Decoder | 5.6 | ns |
| 4:1 MUX | 3.7 | ns |
| 8:1 MUX | 3.9 | ns |
| 16:1 MUX | 4.3 | ns |
| 32:1 MUX | 4.5 | ns |

3.13.2. Register-to-Register Performance

Table 3.18. Register-to-Register Performance

| Function | -7 Timing | Units |
|--|-----------|-------|
| Basic Functions | | |
| 16-bit Decoder | 521 | MHz |
| 32-bit Decoder | 537 | MHz |
| 64-bit Decoder | 484 | MHz |
| 4:1 MUX | 744 | MHz |
| 8:1 MUX | 678 | MHz |
| 16:1 MUX | 616 | MHz |
| 32:1 MUX | 529 | MHz |
| 8-bit Adder | 570 | MHz |
| 16-bit Adder | 507 | MHz |
| 64-bit Adder | 293 | MHz |
| 16-bit Counter | 541 | MHz |
| 32-bit Counter | 440 | MHz |
| 64-bit Counter | 321 | MHz |
| 64-bit Accumulator | 261 | MHz |
| Embedded Memory Functions | | |
| 512x36 Single Port RAM, EBR Output Registers | 315 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, EBR Output Registers) | 315 | MHz |
| 1024x18 True-Dual Port RAM (Write Through or Normal, PLC Output Registers) | 231 | MHz |
| Distributed Memory Functions | | |
| 16x4 Pseudo-Dual Port RAM (One PFU) | 760 | MHz |
| 32x2 Pseudo-Dual Port RAM | 455 | MHz |
| 64x1 Pseudo-Dual Port RAM | 351 | MHz |
| DSP Functions | | |
| 18x18 Multiplier (All Registers) | 342 | MHz |
| 9x9 Multiplier (All Registers) | 342 | MHz |
| 36x36 Multiply (All Registers) | 330 | MHz |
| 18x18 Multiply/Accumulate (Input and Output Registers) | 218 | MHz |
| 18x18 Multiply-Add/Sub-Sum (All Registers) | 292 | MHz |
| DSP IP Functions | | |
| 16-Tap Fully-Parallel FIR Filter | 198 | MHz |
| 1024-pt FFT | 221 | MHz |
| 8X8 Matrix Multiplication | 196 | MHz |

Note: These timing numbers were generated using the ispLEVER design tool. Exact performance may vary with device, design and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

3.14. Typical Building Block Function Performance – ZE Devices

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.19. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

| Function | –6 Timing | Units |
|------------------------|-----------|-------|
| Basic Functions | | |
| 16-bit decoder | 8.9 | ns |
| 4:1 MUX | 7.5 | ns |
| 16:1 MUX | 8.3 | ns |

3.14.2. Register-to-Register Performance

Table 3.20. Register-to-Register Performance

| Function | –6 Timing | Units |
|--|-----------|-------|
| Basic Functions | | |
| 16:1 MUX | 412 | MHz |
| 16-bit adder | 297 | MHz |
| 16-bit counter | 324 | MHz |
| 64-bit counter | 161 | MHz |
| Embedded Memory Functions | | |
| 1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers) | 183 | MHz |
| Distributed Memory Functions | | |
| 16x4 Pseudo-Dual Port RAM (one PFU) | 500 | MHz |

Note: The above timing numbers are generated using the Diamond design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.

3.15. Derating Timing Tables

Logic timing provided in the following sections of this data sheet and the Diamond design tools are worst case numbers in the operating range. Actual delays at nominal temperature and voltage for best case process, can be much better than the values given in the tables. The Diamond design tool can provide logic timing numbers at a particular temperature and voltage.

3.16. LatticeXP2 External Switching Characteristics¹

Over Recommended Operating Conditions

Table 3.21. LatticeXP2 External Switching Characteristics

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|---|--|--------|------|------|------|------|------|------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| General I/O Pin Parameters (using Primary Clock without PLL) ¹ | | | | | | | | | |
| t _{CO} | Clock to Output - PIO Output Register | XP2-5 | — | 3.80 | — | 4.20 | — | 4.60 | ns |
| | | XP2-8 | — | 3.80 | — | 4.20 | — | 4.60 | ns |
| | | XP2-17 | — | 3.80 | — | 4.20 | — | 4.60 | ns |
| | | XP2-30 | — | 4.00 | — | 4.40 | — | 4.90 | ns |
| | | XP2-40 | — | 4.00 | — | 4.40 | — | 4.90 | ns |
| t _{SU} | Clock to Data Setup - PIO Input Register | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| t _H | Clock to Data Hold - PIO Input Register | XP2-5 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-8 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-17 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-30 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-40 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| t _{SU_DEL} | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-8 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-17 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-30 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| | | XP2-40 | 1.40 | — | 1.70 | — | 1.90 | — | ns |
| t _{H_DEL} | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| f _{MAX_IO} | Clock Frequency of I/O and PFU Register | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| General I/O Pin Parameters (using Edge Clock without PLL) ¹ | | | | | | | | | |
| t _{COE} | Clock to Output - PIO Output Register | XP2-5 | — | 3.20 | — | 3.60 | — | 3.90 | ns |
| | | XP2-8 | — | 3.20 | — | 3.60 | — | 3.90 | ns |
| | | XP2-17 | — | 3.20 | — | 3.60 | — | 3.90 | ns |
| | | XP2-30 | — | 3.20 | — | 3.60 | — | 3.90 | ns |
| | | XP2-40 | — | 3.20 | — | 3.60 | — | 3.90 | ns |
| t _{SUE} | Clock to Data Setup - PIO Input Register | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |

| Parameter | Description | Device | −7 | | −6 | | −5 | | Units |
|--|--|--------|------|------|------|------|------|------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{HE} | Clock to Data Hold - PIO Input Register | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| t _{SU_DELE} | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-8 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-17 | 1.00 | — | 1.30 | — | 1.60 | — | ns |
| | | XP2-30 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| | | XP2-40 | 1.20 | — | 1.60 | — | 1.90 | — | ns |
| t _{H_DELE} | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| f _{MAX_IOE} | Clock Frequency of I/O and PFU Register | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| General I/O Pin Parameters (using Primary Clock with PLL) ¹ | | | | | | | | | |
| t _{COPLL} | Clock to Output - PIO Output Register | XP2-5 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-8 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-17 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-30 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| | | XP2-40 | — | 3.00 | — | 3.30 | — | 3.70 | ns |
| t _{SUPLL} | Clock to Data Setup - PIO Input Register | XP2-5 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-8 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-17 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| t _{HPLL} | Clock to Data Hold - PIO Input Register | XP2-5 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-8 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-17 | 0.90 | — | 1.10 | — | 1.30 | — | ns |
| | | XP2-30 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| | | XP2-40 | 1.00 | — | 1.20 | — | 1.40 | — | ns |
| t _{SU_DEPLL} | Clock to Data Setup - PIO Input Register with Data Input Delay | XP2-5 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-8 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-17 | 1.90 | — | 2.10 | — | 2.30 | — | ns |
| | | XP2-30 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| | | XP2-40 | 2.00 | — | 2.20 | — | 2.40 | — | ns |
| t _{H_DEPLL} | Clock to Data Hold - PIO Input Register with Input Data Delay | XP2-5 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-8 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-17 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-30 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| | | XP2-40 | 0.00 | — | 0.00 | — | 0.00 | — | ns |
| DDR2 and DDR23 I/O Pin Parameters | | | | | | | | | |
| t _{DVADQ} | Data Valid After DQS (DDR Read) | XP2 | — | 0.29 | — | 0.29 | — | 0.29 | UI |

| Parameter | Description | Device | -7 | | -6 | | -5 | | Units |
|-------------------------------------|--|--------|------|------|------|------|------|------|-------|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t_{DVEDQ} | Data Hold After DQS (DDR Read) | XP2 | 0.71 | — | 0.71 | — | 0.71 | — | UI |
| t_{DQVBS} | Data Valid Before DQS | XP2 | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| t_{DQVAS} | Data Valid After DQS | XP2 | 0.25 | — | 0.25 | — | 0.25 | — | UI |
| f_{MAX_DDR} | DDR Clock Frequency | XP2 | 95 | 200 | 95 | 166 | 95 | 133 | MHz |
| f_{MAX_DDR2} | DDR Clock Frequency | XP2 | 133 | 200 | 133 | 200 | 133 | 166 | MHz |
| Primary Clock | | | | | | | | | |
| f_{MAX_PRI} | Frequency for Primary Clock Tree | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| t_{W_PRI} | Clock Pulse Width for Primary Clock | XP2 | 1 | — | 1 | — | 1 | — | ns |
| t_{SKEW_PRI} | Primary Clock Skew Within a Bank | XP2 | — | 160 | — | 160 | — | 160 | ps |
| Edge Clock (ECLK1 and ECLK2) | | | | | | | | | |
| f_{MAX_ECLK} | Frequency for Edge Clock | XP2 | — | 420 | — | 357 | — | 311 | MHz |
| t_{W_ECLK} | Clock Pulse Width for Edge Clock | XP2 | 1 | — | 1 | — | 1 | — | ns |
| t_{SKEW_ECLK} | Edge Clock Skew Within an Edge of the Device | XP2 | — | 130 | — | 130 | — | 130 | ps |

Notes:

- General timing numbers based on LVCMOS 2.5, 12 mA, 0pf load.
- DDR timing numbers based on SSTL25.
- DDR2 timing numbers based on SSTL18.

3.17. LatticeXP2 Internal Switching Characteristics¹

Over Recommended Operating Conditions

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|----------------------------------|---|--------|-------|--------|-------|--------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| PFU/PFF Logic Mode Timing | | | | | | | | |
| tLUT4_PFU | LUT4 delay (A to D inputs to F output) | — | 0.216 | — | 0.238 | — | 0.260 | ns |
| tLUT6_PFU | LUT6 delay (A to D inputs to OFX output) | — | 0.304 | — | 0.399 | — | 0.494 | ns |
| tLSR_PFU | Set/Reset to output of PFU (Asyn-chronous) | — | 0.720 | — | 0.769 | — | 0.818 | ns |
| tSUM_PFU | Clock to Mux (M0,M1) Input Setup Time | 0.154 | — | 0.151 | — | 0.148 | — | ns |
| tHM_PFU | Clock to Mux (M0,M1) Input Hold Time | -0.061 | — | -0.057 | — | -0.053 | — | ns |
| tSUD_PFU | Clock to D input setup time | 0.061 | — | 0.077 | — | 0.093 | — | ns |
| tHD_PFU | Clock to D input hold time | 0.002 | — | 0.003 | — | 0.003 | — | ns |
| tCK2Q_PFU | Clock to Q delay, (D-type Register Configuration) | — | 0.342 | — | 0.363 | — | 0.383 | ns |
| tRSTREC_PFU | Asynchronous reset recovery time for PFU Logic | — | 0.520 | — | 0.634 | — | 0.748 | ns |
| tRST_PFU | Asynchronous reset time for PFU Logic | — | 0.720 | — | 0.769 | — | 0.818 | ns |
| PFU Dual Port Memory Mode Timing | | | | | | | | |
| tCORAM_PFU | Clock to Output (F Port) | — | 1.082 | — | 1.267 | — | 1.452 | ns |
| tSUDATA_PFU | Data Setup Time | -0.206 | — | -0.240 | — | -0.274 | — | ns |
| tHDATA_PFU | Data Hold Time | 0.239 | — | 0.275 | — | 0.312 | — | ns |
| tSUADDR_PFU | Address Setup Time | -0.294 | — | -0.333 | — | -0.371 | — | ns |
| tHADDR_PFU | Address Hold Time | 0.295 | — | 0.333 | — | 0.371 | — | ns |
| tSUWREN_PFU | Write/Read Enable Setup Time | -0.146 | — | -0.169 | — | -0.193 | — | ns |
| tHWREN_PFU | Write/Read Enable Hold Time | 0.158 | — | 0.182 | — | 0.207 | — | ns |
| PIO Input/Output Buffer Timing | | | | | | | | |
| tIN_PIO | Input Buffer Delay (LVCMOS25) | — | 0.858 | — | 0.766 | — | 0.674 | ns |
| tOUT_PIO | Output Buffer Delay (LVCMOS25) | — | 1.561 | — | 1.403 | — | 1.246 | ns |
| IOLOGIC Input/Output Timing | | | | | | | | |
| tSUI_PIO | Input Register Setup Time (Data Before Clock) | 0.583 | — | 0.893 | — | 1.201 | — | ns |
| tHI_PIO | Input Register Hold Time (Data after Clock) | 0.062 | — | 0.322 | — | 0.482 | — | ns |
| tCOO_PIO | Output Register Clock to Output Delay | — | 0.608 | — | 0.661 | — | 0.715 | ns |
| tSUCE_PIO | Input Register Clock Enable Setup Time | 0.032 | — | 0.037 | — | 0.041 | — | ns |
| tHCE_PIO | Input Register Clock Enable Hold Time | -0.022 | — | -0.025 | — | -0.028 | — | ns |
| tSULSR_PIO | Set/Reset Setup Time | 0.184 | — | 0.201 | — | 0.217 | — | ns |
| tHLRS_PIO | Set/Reset Hold Time | -0.080 | — | -0.086 | — | -0.093 | — | ns |
| tRSTREC_PIO | Asynchronous reset recovery time for IO Logic | 0.228 | — | 0.247 | — | 0.266 | — | ns |
| tRST_PIO | Asynchronous reset time for PFU Logic | — | 0.386 | — | 0.419 | — | 0.452 | ns |

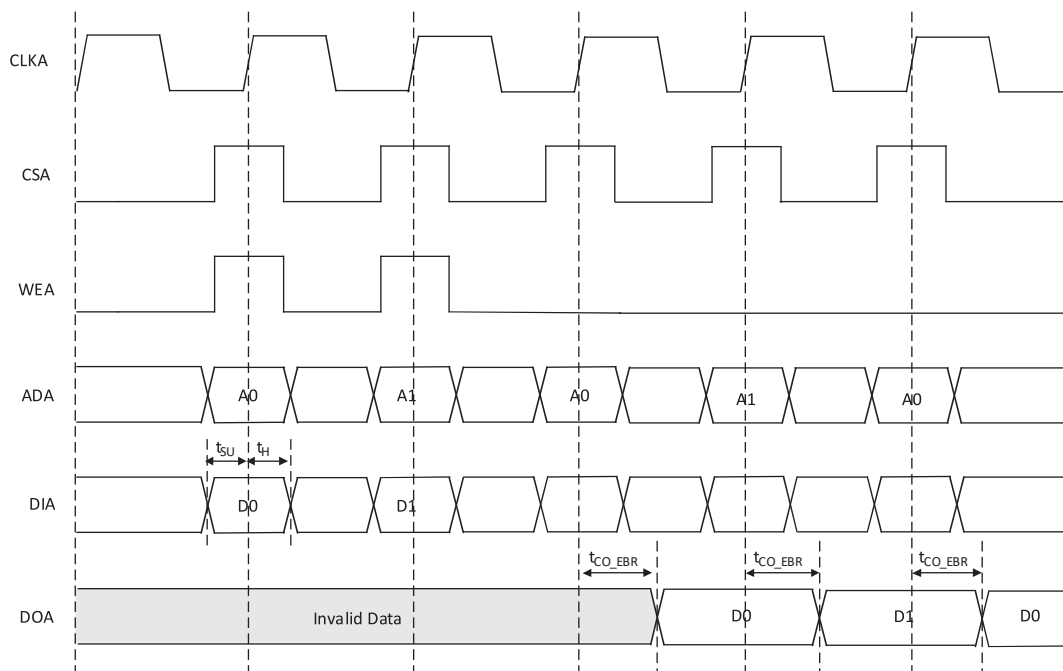
| Parameter | Description | -7 | | -6 | | -5 | | Units |
|-----------------------------------|--|--------|-------|--------|-------|--------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{DEL} | Dynamic Delay Step Size | 0.035 | 0.035 | 0.035 | 0.035 | 0.035 | 0.035 | ns |
| EBR Timing | | | | | | | | |
| t _{CO_EBR} | Clock (Read) to Output from Address or Data | — | 2.774 | — | 3.142 | — | 3.510 | ns |
| t _{COO_EBR} | Clock (Write) to Output from EBR Output Register | — | 0.360 | — | 0.408 | — | 0.456 | ns |
| t _{SUDATA_EBR} | Setup Data to EBR Memory (Write Clk) | -0.167 | — | -0.198 | — | -0.229 | — | ns |
| t _{HDATA_EBR} | Hold Data to EBR Memory (Write Clk) | 0.194 | — | 0.231 | — | 0.267 | — | ns |
| t _{SUADDR_EBR} | Setup Address to EBR Memory (Write Clk) | -0.117 | — | -0.137 | — | -0.157 | — | ns |
| t _{HADDR_EBR} | Hold Address to EBR Memory (Write Clk) | 0.157 | — | 0.182 | — | 0.207 | — | ns |
| t _{SUWREN_EBR} | Setup Write/Read Enable to EBR Memory (Write/Read Clk) | -0.135 | — | -0.159 | — | -0.182 | — | ns |
| t _{HWREN_EBR} | Hold Write/Read Enable to EBR Memory (Write/Read Clk) | 0.158 | — | 0.186 | — | 0.214 | — | ns |
| t _{SUCE_EBR} | Clock Enable Setup Time to EBR Output Register (Read Clk) | 0.144 | — | 0.160 | — | 0.176 | — | ns |
| t _{HCE_EBR} | Clock Enable Hold Time to EBR Output Register (Read Clk) | -0.097 | — | -0.113 | — | -0.129 | — | ns |
| t _{RSTO_EBR} | Reset To Output Delay Time from EBR Output Register (Asynchronous) | — | 1.156 | — | 1.341 | — | 1.526 | ns |
| t _{SUBE_EBR} | Byte Enable Set-Up Time to EBR Output Register | -0.117 | — | -0.137 | — | -0.157 | — | ns |
| t _{HBE_EBR} | Byte Enable Hold Time to EBR Output Register Dynamic Delay on Each PIO | 0.157 | — | 0.182 | — | 0.207 | — | ns |
| t _{RSTREC_EBR} | Asynchronous reset recovery time for EBR | 0.233 | — | 0.291 | — | 0.347 | — | ns |
| t _{RST_EBR} | Asynchronous reset time for EBR | — | 1.156 | — | 1.341 | — | 1.526 | ns |
| PLL Parameters | | | | | | | | |
| t _{RSTKREC_PLL} | After RSTK De-assert, Recovery Time Before Next Clock Edge Can Toggle K-divider Counter | 1.000 | — | 1.000 | — | 1.000 | — | ns |
| t _{RSTREC_PLL} | After RST De-assert, Recovery Time Before Next Clock Edge Can Toggle M-divider Counter (Applies to M-Divider Portion of RST Only2) | 1.000 | — | 1.000 | — | 1.000 | — | ns |
| DSP Block Timing | | | | | | | | |
| t _{SUI_DSP} | Input Register Setup Time | 0.135 | — | 0.151 | — | 0.166 | — | ns |
| t _{HI_DSP} | Input Register Hold Time | 0.021 | — | -0.006 | — | -0.031 | — | ns |
| t _{SUP_DSP} | Pipeline Register Setup Time | 2.505 | — | 2.784 | — | 3.064 | — | ns |
| t _{HP_DSP} | Pipeline Register Hold Time | -0.787 | — | -0.890 | — | -0.994 | — | ns |
| t _{SUO_DSP} | Output Register Setup Time | 4.896 | — | 5.413 | — | 5.931 | — | ns |
| t _{HO_DSP} | Output Register Hold Time | -1.439 | — | -1.604 | — | -1.770 | — | ns |
| t _{COI_DSP} ³ | Input Register Clock to Output Time | — | 4.513 | — | 4.947 | — | 5.382 | ns |

| Parameter | Description | -7 | | -6 | | -5 | | Units |
|------------------|--|--------|-------|--------|-------|--------|-------|-------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{COP_DSP}^3$ | Pipeline Register Clock to Output Time | — | 2.153 | — | 2.272 | — | 2.391 | ns |
| $t_{COO_DSP}^3$ | Output Register Clock to Output Time | — | 0.569 | — | 0.600 | — | 0.631 | ns |
| $t_{SUADSUB}$ | AdSub Input Register Setup Time | -0.270 | — | -0.298 | — | -0.327 | — | ns |
| t_{HADSUB} | AdSub Input Register Hold Time | 0.306 | — | 0.338 | — | 0.371 | — | ns |

Notes:

1. Internal parameters are characterized, but not tested on every device.
2. RST resets VCO and all counters in PLL.
3. These parameters include the Adder Subtractor block in the path.

3.18. EBR Timing Diagrams



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock

Figure 3.6. Read/Write Mode (Normal)

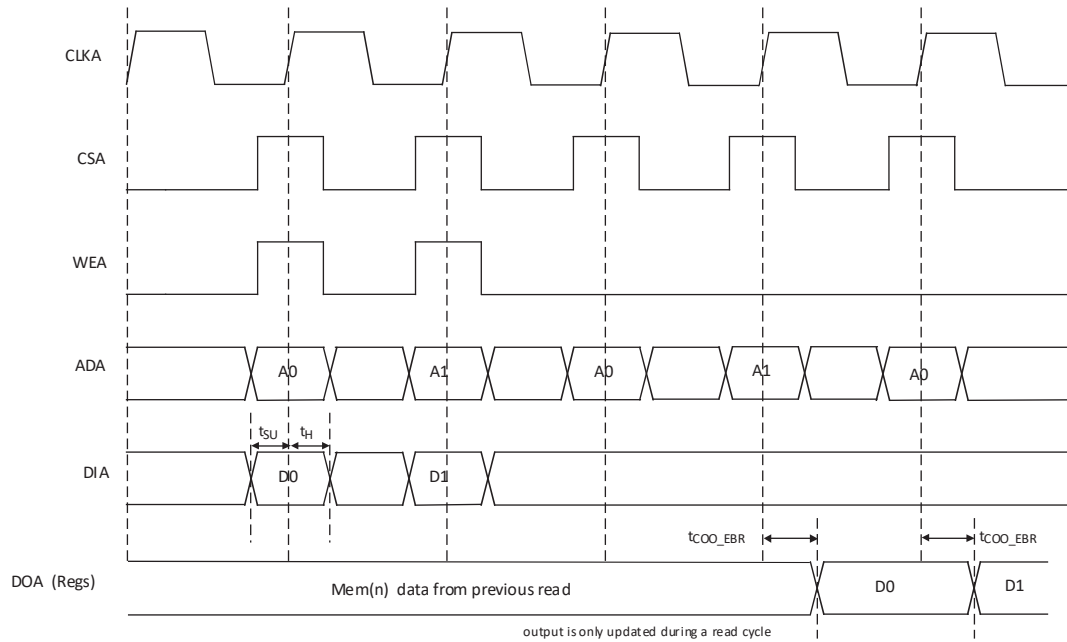
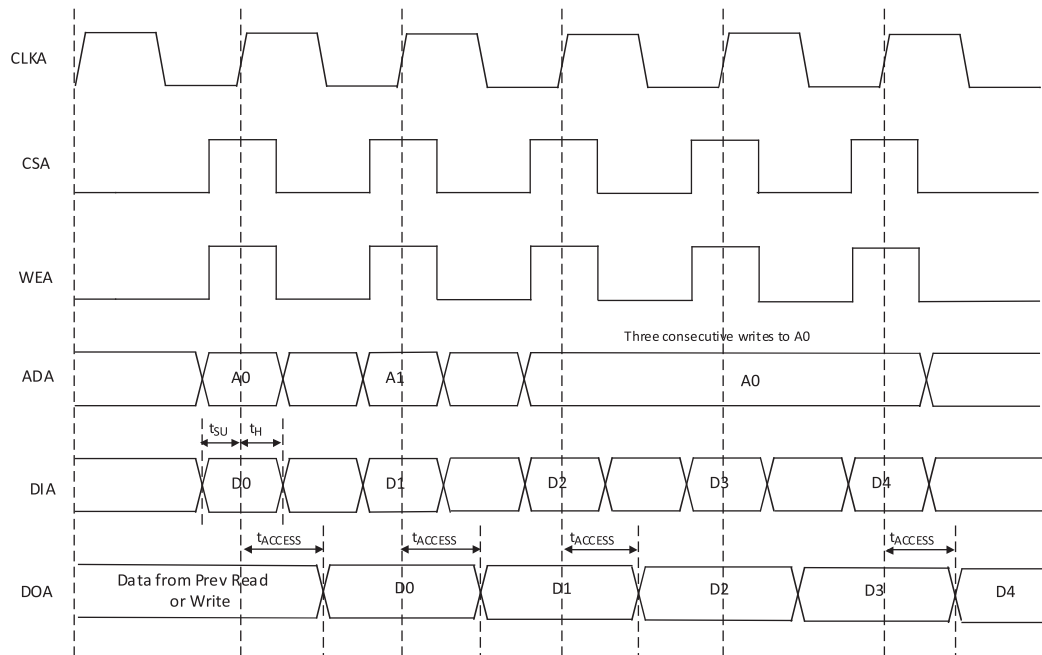


Figure 3.7. Read/Write Mode with Input and Output Registers



Note: Input data and address are registered at the positive edge of the clock and output data appears after the positive edge of the clock.

Figure 3.8. Write Through (SP Read/Write on Port A, Input Registers Only)

3.19. LatticeXP2 Family Timing Adders

Over Recommended Operating Conditions

Table 3.22. LatticeXP2 Family Timing Adders^{1, 2, 3, 4}

| Buffer Type | Description | –7 | –6 | –5 | Units |
|-------------------------|---|-------|-------|-------|-------|
| Input Adjusters | | | | | |
| LVDS25 | LVDS | –0.26 | –0.11 | 0.04 | ns |
| BLVDS25 | BLVDS | –0.26 | –0.11 | 0.04 | ns |
| MLVDS | LVDS | –0.26 | –0.11 | 0.04 | ns |
| RSDS | RSDS | –0.26 | –0.11 | 0.04 | ns |
| LVPECL33 | LVPECL | –0.26 | –0.11 | 0.04 | ns |
| HSTL18_I | HSTL_18 class I | –0.23 | –0.08 | 0.07 | ns |
| HSTL18_II | HSTL_18 class II | –0.23 | –0.08 | 0.07 | ns |
| HSTL18D_I | Differential HSTL 18 class I | –0.28 | –0.13 | 0.02 | ns |
| HSTL18D_II | Differential HSTL 18 class II | –0.28 | –0.13 | 0.02 | ns |
| HSTL15_I | HSTL_15 class I | –0.23 | –0.09 | 0.06 | ns |
| HSTL15D_I | Differential HSTL 15 class I | –0.28 | –0.13 | 0.01 | ns |
| SSTL33_I | SSTL_3 class I | –0.20 | –0.04 | 0.12 | ns |
| SSTL33_II | SSTL_3 class II | –0.20 | –0.04 | 0.12 | ns |
| SSTL33D_I | Differential SSTL_3 class I | –0.27 | –0.11 | 0.04 | ns |
| SSTL33D_II | Differential SSTL_3 class II | –0.27 | –0.11 | 0.04 | ns |
| SSTL25_I | SSTL_2 class I | –0.21 | –0.06 | 0.10 | ns |
| SSTL25_II | SSTL_2 class II | –0.21 | –0.06 | 0.10 | ns |
| SSTL25D_I | Differential SSTL_2 class I | –0.27 | –0.12 | 0.03 | ns |
| SSTL25D_II | Differential SSTL_2 class II | –0.27 | –0.12 | 0.03 | ns |
| SSTL18_I | SSTL_18 class I | –0.23 | –0.08 | 0.07 | ns |
| SSTL18_II | SSTL_18 class II | –0.23 | –0.08 | 0.07 | ns |
| SSTL18D_I | Differential SSTL_18 class I | –0.28 | –0.13 | 0.02 | ns |
| SSTL18D_II | Differential SSTL_18 class II | –0.28 | –0.13 | 0.02 | ns |
| LVTTL33 | LVTTL | –0.09 | 0.05 | 0.18 | ns |
| LVC MOS33 | LVC MOS 3.3 | –0.09 | 0.05 | 0.18 | ns |
| LVC MOS25 | LVC MOS 2.5 | 0.00 | 0.00 | 0.00 | ns |
| LVC MOS18 | LVC MOS 1.8 | –0.23 | –0.07 | 0.09 | ns |
| LVC MOS15 | LVC MOS 1.5 | –0.20 | –0.02 | 0.16 | ns |
| LVC MOS12 | LVC MOS 1.2 | –0.35 | –0.20 | –0.04 | ns |
| PCI33 | 3.3V PCI | –0.09 | 0.05 | 0.18 | ns |
| Output Adjusters | | | | | |
| LVDS25E | LVDS 2.5 E ⁵ | –0.25 | 0.02 | 0.30 | ns |
| LVDS25 | LVDS 2.5 | –0.25 | 0.02 | 0.30 | ns |
| BLVDS25 | BLVDS 2.5 | –0.28 | 0.00 | 0.28 | ns |
| MLVDS | MLVDS 2.5 ⁵ | –0.28 | 0.00 | 0.28 | ns |
| RSDS | RSDS 2.5 ⁵ | –0.25 | 0.02 | 0.30 | ns |
| LVPECL33 | LVPECL 3.3 ⁵ | –0.37 | –0.10 | 0.18 | ns |
| HSTL18_I | HSTL_18 class I 8 mA drive | –0.17 | 0.13 | 0.43 | ns |
| HSTL18_II | HSTL_18 class II | –0.29 | 0.00 | 0.29 | ns |
| HSTL18D_I | Differential HSTL 18 class I 8 mA drive | –0.17 | 0.13 | 0.43 | ns |
| HSTL18D_II | Differential HSTL 18 class II | –0.29 | 0.00 | 0.29 | ns |

| Buffer Type | Description | -7 | -6 | -5 | Units |
|-----------------|---|-------|-------|-------|-------|
| HSTL15_I | HSTL_15 class I 4 mA drive | 0.32 | 0.69 | 1.06 | ns |
| HSTL15D_I | Differential HSTL 15 class I 4 mA drive | 0.32 | 0.69 | 1.06 | ns |
| SSTL33_I | SSTL_3 class I | -0.25 | 0.05 | 0.35 | ns |
| SSTL33_II | SSTL_3 class II | -0.31 | -0.02 | 0.27 | ns |
| SSTL33D_I | Differential SSTL_3 class I | -0.25 | 0.05 | 0.35 | ns |
| SSTL33D_II | Differential SSTL_3 class II | -0.31 | -0.02 | 0.27 | ns |
| SSTL25_I | SSTL_2 class I 8 mA drive | -0.25 | 0.02 | 0.30 | ns |
| SSTL25_II | SSTL_2 class II 16 mA drive | -0.28 | 0.00 | 0.28 | ns |
| SSTL25D_I | Differential SSTL_2 class I 8 mA drive | -0.25 | 0.02 | 0.30 | ns |
| SSTL25D_II | Differential SSTL_2 class II 16 mA drive | -0.28 | 0.00 | 0.28 | ns |
| SSTL18_I | SSTL_1.8 class I | -0.17 | 0.13 | 0.43 | ns |
| SSTL18_II | SSTL_1.8 class II 8 mA drive | -0.18 | 0.12 | 0.42 | ns |
| SSTL18D_I | Differential SSTL_1.8 class I | -0.17 | 0.13 | 0.43 | ns |
| SSTL18D_II | Differential SSTL_1.8 class II 8 mA drive | -0.18 | 0.12 | 0.42 | ns |
| LVTTTL33_4 mA | LVTTTL 4 mA drive | -0.37 | -0.05 | 0.26 | ns |
| LVTTTL33_8 mA | LVTTTL 8 mA drive | -0.45 | -0.18 | 0.10 | ns |
| LVTTTL33_12 mA | LVTTTL 12 mA drive | -0.52 | -0.24 | 0.04 | ns |
| LVTTTL33_16 mA | LVTTTL 16 mA drive | -0.43 | -0.14 | 0.14 | ns |
| LVTTTL33_20 mA | LVTTTL 20 mA drive | -0.46 | -0.18 | 0.09 | ns |
| LVC MOS33_4 mA | LVC MOS 3.3 4 mA drive, fast slew rate | -0.37 | -0.05 | 0.26 | ns |
| LVC MOS33_8 mA | LVC MOS 3.3 8 mA drive, fast slew rate | -0.45 | -0.18 | 0.10 | ns |
| LVC MOS33_12 mA | LVC MOS 3.3 12 mA drive, fast slew rate | -0.52 | -0.24 | 0.04 | ns |
| LVC MOS33_16 mA | LVC MOS 3.3 16 mA drive, fast slew rate | -0.43 | -0.14 | 0.14 | ns |
| LVC MOS33_20 mA | LVC MOS 3.3 20 mA drive, fast slew rate | -0.46 | -0.18 | 0.09 | ns |
| LVC MOS25_4 mA | LVC MOS 2.5 4 mA drive, fast slew rate | -0.42 | -0.15 | 0.13 | ns |
| LVC MOS25_8 mA | LVC MOS 2.5 8 mA drive, fast slew rate | -0.48 | -0.21 | 0.05 | ns |
| LVC MOS25_12 mA | LVC MOS 2.5 12 mA drive, fast slew rate | 0.00 | 0.00 | 0.00 | ns |
| LVC MOS25_16 mA | LVC MOS 2.5 16 mA drive, fast slew rate | -0.45 | -0.18 | 0.08 | ns |
| LVC MOS25_20 mA | LVC MOS 2.5 20 mA drive, fast slew rate | -0.49 | -0.22 | 0.04 | ns |
| LVC MOS18_4 mA | LVC MOS 1.8 4 mA drive, fast slew rate | -0.46 | -0.18 | 0.10 | ns |
| LVC MOS18_8 mA | LVC MOS 1.8 8 mA drive, fast slew rate | -0.52 | -0.25 | 0.02 | ns |
| LVC MOS18_12 mA | LVC MOS 1.8 12 mA drive, fast slew rate | -0.56 | -0.30 | -0.03 | ns |
| LVC MOS18_16 mA | LVC MOS 1.8 16 mA drive, fast slew rate | -0.50 | -0.24 | 0.03 | ns |
| LVC MOS15_4 mA | LVC MOS 1.5 4 mA drive, fast slew rate | -0.45 | -0.17 | 0.11 | ns |
| LVC MOS15_8 mA | LVC MOS 1.5 8 mA drive, fast slew rate | -0.53 | -0.26 | 0.00 | ns |
| LVC MOS12_2 mA | LVC MOS 1.2 2 mA drive, fast slew rate | -0.46 | -0.19 | 0.08 | ns |
| LVC MOS12_6 mA | LVC MOS 1.2 6 mA drive, fast slew rate | -0.55 | -0.29 | -0.02 | ns |
| LVC MOS33_4 mA | LVC MOS 3.3 4 mA drive, slow slew rate | 0.98 | 1.41 | 1.84 | ns |
| LVC MOS33_8 mA | LVC MOS 3.3 8 mA drive, slow slew rate | 0.74 | 1.16 | 1.58 | ns |
| LVC MOS33_12 mA | LVC MOS 3.3 12 mA drive, slow slew rate | 0.56 | 0.97 | 1.38 | ns |
| LVC MOS33_16 mA | LVC MOS 3.3 16 mA drive, slow slew rate | 0.77 | 1.19 | 1.61 | ns |
| LVC MOS33_20 mA | LVC MOS 3.3 20 mA drive, slow slew rate | 0.57 | 0.98 | 1.40 | ns |
| LVC MOS25_4 mA | LVC MOS 2.5 4 mA drive, slow slew rate | 1.05 | 1.43 | 1.81 | ns |
| LVC MOS25_8 mA | LVC MOS 2.5 8 mA drive, slow slew rate | 0.78 | 1.15 | 1.52 | ns |
| LVC MOS25_12 mA | LVC MOS 2.5 12 mA drive, slow slew rate | 0.59 | 0.96 | 1.33 | ns |
| LVC MOS25_16 mA | LVC MOS 2.5 16 mA drive, slow slew rate | 0.81 | 1.18 | 1.55 | ns |

| Buffer Type | Description | –7 | –6 | –5 | Units |
|-----------------|---|-------|-------|-------|-------|
| LVC MOS25_20 mA | LVC MOS 2.5 20 mA drive, slow slew rate | 0.61 | 0.98 | 1.35 | ns |
| LVC MOS18_4 mA | LVC MOS 1.8 4 mA drive, slow slew rate | 1.01 | 1.38 | 1.75 | ns |
| LVC MOS18_8 mA | LVC MOS 1.8 8 mA drive, slow slew rate | 0.72 | 1.08 | 1.45 | ns |
| LVC MOS18_12 mA | LVC MOS 1.8 12 mA drive, slow slew rate | 0.53 | 0.90 | 1.26 | ns |
| LVC MOS18_16 mA | LVC MOS 1.8 16 mA drive, slow slew rate | 0.74 | 1.11 | 1.48 | ns |
| LVC MOS15_4 mA | LVC MOS 1.5 4 mA drive, slow slew rate | 0.96 | 1.33 | 1.71 | ns |
| LVC MOS15_8 mA | LVC MOS 1.5 8 mA drive, slow slew rate | –0.53 | –0.26 | 0.00 | ns |
| LVC MOS12_2 mA | LVC MOS 1.2 2 mA drive, slow slew rate | 0.90 | 1.27 | 1.65 | ns |
| LVC MOS12_6 mA | LVC MOS 1.2 6 mA drive, slow slew rate | –0.55 | –0.29 | –0.02 | ns |
| PCI33 | 3.3 V PCI | –0.29 | –0.01 | 0.26 | ns |

Notes:

1. Timing Adders are characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. The base parameters used with these timing adders to calculate timing are listed in the LatticeXP2 Internal Switching Characteristics table under PIO Input/Output Timing.
5. These timing adders are measured with the recommended resistor values.

3.20. sysCLOCK PLL Timing

Over Recommended Operating Conditions

Table 3.23. sysCLOCK PLL Timing

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---------------------------|---------------------------------------|--|-------|------|-------|-------|
| f_{IN} | Input Clock Frequency (CLKI, CLKFB) | | 10 | — | 435 | MHz |
| f_{OUT} | Output Clock Frequency (CLKOP, CLKOS) | | 10 | — | 435 | MHz |
| f_{OUT2} | K-Divider Output Frequency | CLKOK | 0.078 | — | 217.5 | MHz |
| | | CLKOK2 | 3.3 | — | 145 | MHz |
| f_{VCO} | PLL VCO Frequency | | 435 | — | 870 | MHz |
| f_{PFD} | Phase Detector Input Frequency | | 10 | — | 435 | MHz |
| AC Characteristics | | | | | | |
| t_{DT} | Output Clock Duty Cycle | Default duty cycle selected ³ | 45 | 50 | 55 | % |
| t_{CPA} | Coarse Phase Adjust | | –5 | 0 | 5 | % |
| t_{PH}^4 | Output Phase Accuracy | | –5 | 0 | 5 | % |
| t_{OPJIT}^1 | Output Clock Period Jitter | $f_{OUT} > 400$ MHz | — | — | ±50 | ps |
| | | 100 MHz < f_{OUT} < 400 MHz | — | — | ±125 | ps |
| | | $f_{OUT} < 100$ MHz | — | — | 0.025 | UIPP |
| t_{SK} | Input Clock to Output Clock Skew | N/M = integer | — | — | ±240 | ps |
| t_{OPW} | Output Clock Pulse Width | At 90% or 10% | 1 | — | — | ns |
| t_{LOCK}^2 | PLL Lock-in Time | 25 to 435 MHz | — | — | 50 | μs |
| | | 10 to 25 MHz | — | — | 100 | μs |
| t_{IPJIT} | Input Clock Period Jitter | | — | — | ±200 | ps |
| t_{FBKDLY} | External Feedback Delay | | — | — | 10 | ns |
| t_{HI} | Input Clock High Time | 90% to 90% | 0.5 | — | — | ns |
| t_{LO} | Input Clock Low Time | 10% to 10% | 0.5 | — | — | ns |
| t_{RSTKW} | Reset Signal Pulse Width (RSTK) | | 10 | — | — | ns |
| t_{RSTW} | Reset Signal Pulse Width (RST) | | 500 | — | — | ns |

Notes:

1. Jitter sample is taken over 10,000 samples of the primary PLL output with clean reference clock.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Using LVDS output buffers.
4. Relative to CLKOP.

3.21. LatticeXP2 sysCONFIG Port Timing Specifications

Over Recommended Operating Conditions

Table 3.24. LatticeXP2 sysCONFIG Port Timing Specifications

| Parameter | Description | Min | Max | Units |
|--|--|------|----------|---------|
| sysCONFIG POR, Initialization and Wake Up | | | | |
| t_{ICFG} | Minimum Vcc to INITN High | — | 50 | ms |
| t_{VMC} | Time from t_{ICFG} to valid Master CCLK | — | 2 | μ s |
| t_{PRGMRJ} | PROGRAMN Pin Pulse Rejection | — | 12 | ns |
| t_{PRGM} | PROGRAMN Low Time to Start Configuration | 50 | — | ns |
| t_{DINIT}^* | PROGRAMN High to INITN High Delay | — | 1 | ms |
| $t_{DPPINIT}$ | Delay Time from PROGRAMN Low to INITN Low | — | 50 | ns |
| $t_{DPPDONE}$ | Delay Time from PROGRAMN Low to DONE Low | — | 50 | ns |
| t_{IODISS} | User I/O Disable from PROGRAMN Low | — | 35 | ns |
| t_{IOENSS} | User I/O Enabled Time from CCLK Edge During Wake-up Sequence | — | 25 | ns |
| t_{MWC} | Additional Wake Master Clock Signals after DONE Pin High | 0 | — | Cycles |
| sysCONFIG SPI Port (Master) | | | | |
| t_{CFGX} | INITN High to CCLK Low | — | 1 | μ s |
| t_{CSSPI} | INITN High to CSSPIN Low | — | 2 | μ s |
| t_{CSCCLK} | CCLK Low before CSSPIN Low | 0 | — | ns |
| t_{SOCDO} | CCLK Low to Output Valid | — | 15 | ns |
| t_{CSPID} | CSSPIN[0:1] Low to First CCLK Edge Setup Time | 2cyc | 600+6cyc | ns |
| f_{MAXSPI} | Max CCLK Frequency | — | 20 | MHz |
| t_{SUSPI} | SOSPI Data Setup Time Before CCLK | 7 | — | ns |
| t_{HSPI} | SOSPI Data Hold Time After CCLK | 10 | — | ns |
| sysCONFIG SPI Port (Slave) | | | | |
| $f_{MAXSPIS}$ | Slave CCLK Frequency | — | 25 | MHz |
| t_{RF} | Rise and Fall Time | 50 | — | mV/ns |
| t_{STCO} | Falling Edge of CCLK to SOSPI Active | — | 20 | ns |
| t_{STOZ} | Falling Edge of CCLK to SOSPI Disable | — | 20 | ns |
| t_{STSU} | Data Setup Time (SISPI) | 8 | — | ns |
| t_{STH} | Data Hold Time (SISPI) | 10 | — | ns |
| t_{STCKH} | CCLK Clock Pulse Width, High | 0.02 | 200 | μ s |
| t_{STCKL} | CCLK Clock Pulse Width, Low | 0.02 | 200 | μ s |
| t_{STVO} | Falling Edge of CCLK to Valid SOSPI Output | — | 20 | ns |
| t_{SCS} | CSSPISN High Time | 25 | — | ns |
| t_{SCSS} | CSSPISN Setup Time | 25 | — | ns |
| t_{SCSH} | CSSPISN Hold Time | 25 | — | ns |

***Note:** Re-toggling the PROGRAMN pin is not permitted until the INITN pin is high. Avoid consecutive toggling of PROGRAMN.

3.22. On-Chip Oscillator and Configuration Master Clock Characteristics

Over Recommended Operating Conditions

Table 3.25. On-Chip Oscillator and Configuration Master Clock Characteristics

| Parameter | Min. | Max. | Units |
|------------------------|---------------------|---------------------|-------|
| Master Clock Frequency | Selected value -30% | Selected value +30% | MHz |
| Duty Cycle | 40 | 60 | % |

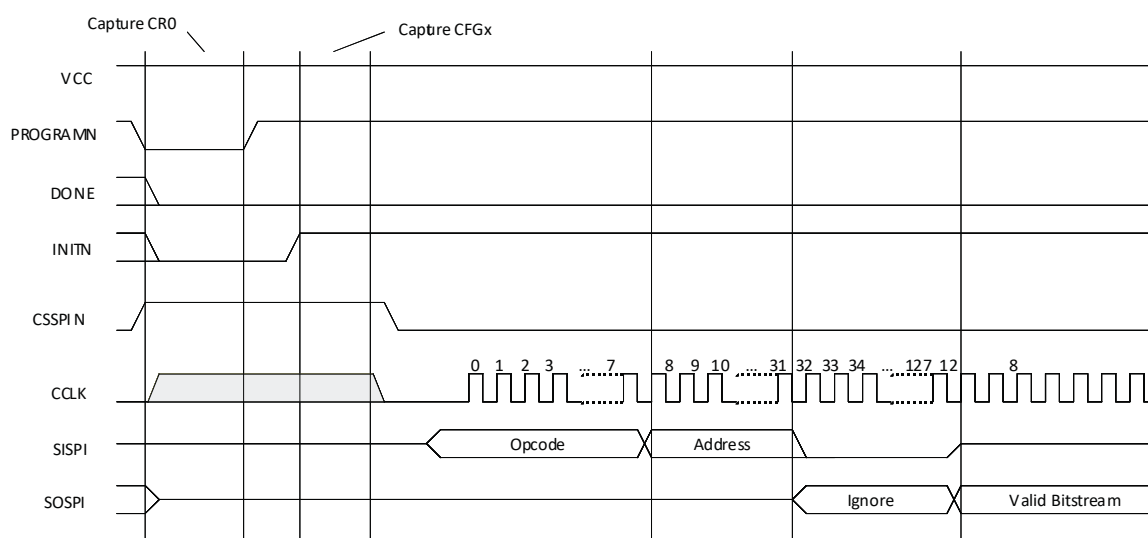


Figure 3.9. Master SPI Configuration Waveforms

3.23. Flash Download Time (from On-Chip Flash to SRAM)

Over Recommended Operating Conditions

Table 3.26. Flash Download Time (from On-Chip Flash to SRAM)

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|----------------------|---|--------|------|------|------|-------|
| t_{REFRESH} | PROGRAMN Low-to-High. Transition to Done High. | XP2-5 | — | 1.8 | 2.1 | ms |
| | | XP2-8 | — | 1.9 | 2.3 | ms |
| | | XP2-17 | — | 1.7 | 2.0 | ms |
| | | XP2-30 | — | 2.0 | 2.1 | ms |
| | | XP2-40 | — | 2.0 | 2.3 | ms |
| | Power-up refresh when PROGRAMN is pulled up to V_{CC} ($V_{CC}=V_{CC \text{ Min}}$) | XP2-5 | — | 1.8 | 2.1 | ms |
| | | XP2-8 | — | 1.9 | 2.3 | ms |
| | | XP2-17 | — | 1.7 | 2.0 | ms |
| | | XP2-30 | — | 2.0 | 2.1 | ms |
| | | XP2-40 | — | 2.0 | 2.3 | ms |

3.24. Flash Program Time

Over Recommended Operating Conditions

Table 3.27. Flash Program Time

| Device | Flash Density | | Program Time | Units |
|--------|---------------|------------|--------------|-------|
| | | | Typ. | |
| XP2-5 | 1.2 M | TAG | 1.0 | ms |
| | | Main Array | 1.1 | s |
| XP2-8 | 2.0 M | TAG | 1.0 | ms |
| | | Main Array | 1.4 | s |
| XP2-17 | 3.6 M | TAG | 1.0 | ms |
| | | Main Array | 1.8 | s |
| XP2-30 | 6.0 M | TAG | 2.0 | ms |
| | | Main Array | 3.0 | s |
| XP2-40 | 8.0 M | TAG | 2.0 | ms |
| | | Main Array | 4.0 | s |

3.25. Flash Erase Time

Over Recommended Operating Conditions

Table 3.28. Flash Erase Time

| Device | Flash Density | | Erase Time | Units |
|--------|---------------|------------|------------|-------|
| | | | Typ. | |
| XP2-5 | 1.2 M | TAG | 1.0 | s |
| | | Main Array | 3.0 | s |
| XP2-8 | 2.0 M | TAG | 1.0 | s |
| | | Main Array | 4.0 | s |
| XP2-17 | 3.6 M | TAG | 1.0 | s |
| | | Main Array | 5.0 | s |
| XP2-30 | 6.0 M | TAG | 2.0 | s |
| | | Main Array | 7.0 | s |
| XP2-40 | 8.0 M | TAG | 2.0 | s |
| | | Main Array | 9.0 | s |

3.26. FlashBAK Time (from EBR to Flash)

Over Recommended Operating Conditions

Table 3.29. FlashBAK Time (from EBR to Flash)

| Device | EBR Density (Bits) | Time (Typ.) | Units |
|--------|--------------------|-------------|-------|
| XP2-5 | 166K | 1.5 | s |
| XP2-8 | 221K | 1.5 | s |
| XP2-17 | 276K | 1.5 | s |
| XP2-30 | 387K | 2.0 | s |
| XP2-40 | 885K | 3.0 | s |

3.27. JTAG Port Timing Specifications

Over Recommended Operating Conditions

Table 3.30. FlashBAK Time (from EBR to Flash)

| Symbol | Parameter | Min. | Max. | Units |
|----------------------|--|------|------|-------|
| f _{MAX} | TCK Clock Frequency | — | 25 | MHz |
| t _{BTCP} | TCK [BSCAN] clock pulse width | 40 | — | ns |
| t _{BTCPH} | TCK [BSCAN] clock pulse width high | 20 | — | ns |
| t _{BTCPL} | TCK [BSCAN] clock pulse width low | 20 | — | ns |
| t _{BTS} | TCK [BSCAN] setup time | 8 | — | ns |
| t _{BTH} | TCK [BSCAN] hold time | 10 | — | ns |
| t _{BTRF} | TCK [BSCAN] rise/fall time | 50 | — | mV/ns |
| t _{BTCO} | TAP controller falling edge of clock to valid output | — | 10 | ns |
| t _{BTCODIS} | TAP controller falling edge of clock to valid disable | — | 10 | ns |
| t _{BTCOEN} | TAP controller falling edge of clock to valid enable | — | 10 | ns |
| t _{BTCRS} | BSCAN test capture register setup time | 8 | — | ns |
| t _{BTCRH} | BSCAN test capture register hold time | 25 | — | ns |
| t _{BUTCO} | BSCAN test update register, falling edge of clock to valid output | — | 25 | ns |
| t _{BTUODIS} | BSCAN test update register, falling edge of clock to valid disable | — | 25 | ns |
| t _{BTUPOEN} | BSCAN test update register, falling edge of clock to valid enable | — | 25 | ns |



Figure 3.11 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.31.



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Table 3.31. Test Fixture Required Components, Non-Terminated Interfaces

| Test Condition | R1 | R2 | CL | Timing Ref. | VT |
|---|--------------|--------------|------|---------------------------|------------|
| LVTTTL and other LVCMOS settings (L -> H, H -> L) | ∞ | ∞ | 0 pF | LVCMOS 3.3 = 1.5 V | — |
| | | | | LVCMOS 2.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.8 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.5 = $V_{CCIO}/2$ | — |
| | | | | LVCMOS 1.2 = $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> H) | ∞ | 1 M Ω | | $V_{CCIO}/2$ | — |
| LVCMOS 2.5 I/O (Z -> L) | 1 M Ω | ∞ | | $V_{CCIO}/2$ | V_{CCIO} |
| LVCMOS 2.5 I/O (H -> Z) | ∞ | 100 | | $V_{OH} - 0.10$ | — |
| LVCMOS 2.5 I/O (L -> Z) | 100 | ∞ | | $V_{OL} + 0.10$ | V_{CCIO} |

Note: Output test conditions for all other interfaces are determined by the respective standards.

4. Pinout Information

4.1. Signal Descriptions

Table 4.1. Signal Descriptions

| Signal Name | I/O | Description |
|---|-----|--|
| General Purpose | | |
| P[Edge] [Row/Column Number*]_[A/B] | I/O | <p>[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top).</p> <p>[Row/Column Number] indicates the PFU row or the column of the device on which the PIC exists. When Edge is T (Top) or B (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number.</p> <p>[A/B] indicates the PIO within the PIC to which the pad is connected. Some of these user-programmable pins are shared with special function pins. These pins, when not used as special purpose pins, can be programmed as I/O for user logic. During configuration the user-programmable I/O are tri-stated with an internal pull-up resistor enabled. If any pin is not used (or not bonded to a package pin), it is also tri-stated with an internal pull-up resistor enabled after configuration.</p> |
| GSRN | I | Global RESET signal (active low). Any I/O pin can be GSRN. |
| NC | — | No connect. |
| GND | — | Ground. Dedicated pins. |
| V _{CC} | — | Power supply pins for core logic. Dedicated pins. |
| V _{CCAUX} | — | Auxiliary power supply pin. This dedicated pin powers all the differential and referenced input buffers. |
| V _{CCPLL} | — | PLL supply pins. csBGA, PQFP and TQFP packages only. |
| V _{CCIOx} | — | Dedicated power supply pins for I/O bank x. |
| V _{REF1_x} , V _{REF2_x} | — | Reference supply pins for I/O bank x. Pre-determined pins in each bank are assigned as V _{REF} inputs. When not used, they may be used as I/O pins. |
| PLL and Clock Functions (Used as user programmable I/O pins when not in use for PLL or clock pins) | | |
| [LOC][num]_V _{CCPLL} | — | Power supply pin for PLL: LLC, LRC, URC, ULC, num = row from center. |
| [LOC][num]_GPLL[T, C]_IN_A | I | General Purpose PLL (GPLL) input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| [LOC][num]_GPLL[T, C]_FB_A | I | Optional feedback GPLL input pads: LLC, LRC, URC, ULC, num = row from center, T = true and C = complement, index A,B,C...at each side. |
| PCLK[T, C]_[n:0]_[3:0] | I | Primary Clock pads, T = true and C = complement, n per side, indexed by bank and 0,1,2,3 within bank. |
| [LOC]DQS[num] | I | DQS input pads: T (Top), R (Right), B (Bottom), L (Left), DQS, num = ball function number. Any pad can be configured to be output. |
| Test and Programming (Dedicated Pins) | | |
| TMS | I | Test Mode Select input, used to control the 1149.1 state machine. Pull-up is enabled during configuration. |
| TCK | I | Test Clock input pin, used to clock the 1149.1 state machine. No pull-up enabled. |
| TDI | I | Test Data in pin. Used to load data into device using 1149.1 state machine. After power-up, this TAP port can be activated for configuration by sending appropriate command. (Note: once a configuration port is selected it is locked. Another configuration port cannot be selected until the power-up sequence). Pull-up is enabled during configuration. |

| Signal Name | I/O | Description |
|---|-----|---|
| TDO | O | Output pin. Test Data Out pin used to shift data out of a device using 1149.1. |
| VCCJ | — | Power supply pin for JTAG Test Access Port. |
| Configuration Pads (Used during sysCONFIG) | | |
| CFG[1:0] | I | Mode pins used to specify configuration mode values latched on rising edge of INITN. During configuration, an internal pull-up is enabled. |
| INITN ¹ | I/O | Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. |
| PROGRAMN | I | Initiates configuration sequence when asserted low. This pin always has an active pull-up. |
| DONE | I/O | Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. |
| CCLK | I/O | Configuration Clock for configuring an FPGA in sysCONFIG mode. |
| SISPI ² | I/O | Input data pin in slave SPI mode and Output data pin in Master SPI mode. |
| SOSPI ² | I/O | Output data pin in slave SPI mode and Input data pin in Master SPI mode. |
| CSSPIN ² | O | Chip select for external SPI Flash memory in Master SPI mode. This pin has a weak internal pull-up. |
| CSSPISN | I | Chip select in Slave SPI mode. This pin has a weak internal pull-up. |
| TOE | I | Test Output Enable tristates all I/O pins when driven low. This pin has a weak internal pull-up, but when not used an external pull-up to V _{CC} is recommended. |

Notes:

1. If not actively driven, the internal pull-up may not be sufficient. An external pull-up resistor of 4.7k to 10k Ω is recommended.
2. When using the device in Master SPI mode, it must be mutually exclusive from JTAG operations (i.e. TCK tied to GND) or the JTAG TCK must be free-running when used in a system JTAG test environment. If Master SPI mode is used in conjunction with a JTAG download cable, the device power cycle is required after the cable is unplugged.

4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

Table 4.2. PICs and DDR Data (DQ) Pins Associated with the DDR Strobe (DQS) Pin

| PICs Associated with DQS Strobe | PIO Within PIC | DDR Strobe (DQS) and Data (DQ) Pins |
|---|----------------|-------------------------------------|
| For Left and Right Edges of the Device | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| For Top and Bottom Edges of the Device | | |
| P[Edge] [n-4] | A | DQ |
| | B | DQ |
| P[Edge] [n-3] | A | DQ |
| | B | DQ |
| P[Edge] [n-2] | A | DQ |
| | B | DQ |
| P[Edge] [n-1] | A | DQ |
| | B | DQ |
| P[Edge] [n] | A | [Edge]DQSn |
| | B | DQ |
| P[Edge] [n+1] | A | DQ |
| | B | DQ |
| P[Edge] [n+2] | A | DQ |
| | B | DQ |
| P[Edge] [n+3] | A | DQ |
| | B | DQ |
| P[Edge] [n+4] | A | DQ |
| | B | DQ |

Notes:

1. “n” is a row PIC number.
2. The DDR interface is designed for memories that support one DQS strobe up to 16 bits of data for the left and right edges and up to 18 bits of data for the top and bottom edges. In some packages, all the potential DDR data (DQ) pins may not be available. PIC numbering definitions are provided in the “Signal Names” column of the Signal Descriptions table.



4.3. Pin Information Summary

Table 4.3. Pin Information Summary

| Pin Type | | XP2-5 | | | | XP2-8 | | | | XP2-17 | | | XP2-30 | |
|---|-----------|--------------|-------------|-------------|--------------|--------------|-------------|-------------|--------------|-------------|--------------|--------------|--------------|--------------|
| | | 132 csBGA | 144 TQFP | 208 PQFP | 256 ftBGA | 132 csBGA | 144 TQFP | 208 PQFP | 256 ftBGA | 208 PQFP | 256 ftBGA | 484 fpBGA | 256 ftBGA | 484 fpBGA |
| Single Ended User I/O | | 86 | 100 | 146 | 172 | 86 | 100 | 146 | 201 | 146 | 201 | 358 | 201 | 363 |
| Differential Pair User I/O | Normal | 35 | 39 | 57 | 66 | 35 | 39 | 57 | 77 | 57 | 77 | 135 | 77 | 137 |
| | Highspeed | 8 | 11 | 16 | 20 | 8 | 11 | 16 | 23 | 16 | 23 | 44 | 23 | 44 |
| Configuration | TAP | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 | 5 |
| | Muxed | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 | 9 |
| | Dedicated | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Non Configuration | Muxed | 5 | 5 | 7 | 7 | 7 | 7 | 9 | 9 | 11 | 11 | 21 | 7 | 11 |
| | Dedicated | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Vcc | | 6 | 4 | 9 | 6 | 6 | 4 | 9 | 6 | 9 | 6 | 16 | 6 | 16 |
| Vccaux | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 8 | 4 | 8 |
| VCCPLL | | 2 | 2 | 2 | - | 2 | 2 | 2 | - | 4 | - | - | - | - |
| VCCIO | Bank0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank1 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank3 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank4 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank5 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank6 | 1 | 1 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| | Bank7 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 2 | 4 |
| GND, GND0-GND7 | | 15 | 15 | 20 | 20 | 15 | 15 | 22 | 20 | 22 | 20 | 56 | 20 | 56 |
| NC | | - | - | 4 | 31 | - | - | 2 | 2 | - | 2 | 7 | 2 | 2 |
| Single Ended/ Differential I/O per Bank | Bank0 | 18/9 | 20/10 | 20/10 | 26/13 | 18/9 | 20/10 | 20/10 | 28/14 | 20/10 | 28/14 | 52/26 | 28/14 | 52/26 |
| | Bank1 | 4/2 | 6/3 | 18/9 | 18/9 | 4/2 | 6/3 | 18/9 | 22/11 | 18/9 | 22/11 | 36/18 | 22/11 | 36/18 |
| | Bank2 | 16/8 | 18/9 | 18/9 | 22/11 | 16/8 | 18/9 | 18/9 | 26/13 | 18/9 | 26/13 | 46/23 | 26/13 | 46/23 |
| | Bank3 | 4/2 | 4/2 | 16/8 | 20/10 | 4/2 | 4/2 | 16/8 | 24/12 | 16/8 | 24/12 | 44/22 | 24/12 | 46/23 |
| | Bank4 | 8/4 | 8/4 | 18/9 | 18/9 | 8/4 | 8/4 | 18/9 | 26/13 | 18/9 | 26/13 | 36/18 | 26/13 | 38/19 |
| | Bank5 | 14/7 | 18/9 | 20/10 | 24/12 | 14/7 | 18/9 | 20/10 | 24/12 | 20/10 | 24/12 | 52/26 | 24/12 | 53/26 |
| | Bank6 | 6/3 | 8/4 | 18/9 | 22/11 | 6/3 | 8/4 | 18/9 | 27/13 | 18/9 | 27/13 | 46/23 | 27/13 | 46/23 |
| | Bank7 | 16/8 | 18/9 | 18/9 | 22/11 | 16/8 | 18/9 | 18/9 | 24/12 | 18/9 | 24/12 | 46/23 | 24/12 | 46/23 |

LatticeXP2 Family Data Sheet

[illegible]

***Note:** Minimum requirement to implement a fully functional 8-bit wide DDR bus. Available DDR interface consists of at least 12 I/O (1 DQS + 1 DQSB + 8

4.4. Logic Signal Connections

Package pinout information can be found under *Pin & Package* on the LatticeXP2 product page of the Lattice website (www.latticesemi.com/Products/FPGAandCPLD/LatticeXP2) and in the Lattice Diamond design software.

4.5. Thermal Management

Thermal management is recommended as part of any sound FPGA design methodology. To assess the thermal characteristics of a system, Lattice specifies a maximum allowable junction temperature in all device data sheets. Designers must complete a thermal analysis of their specific design to ensure that the device and package do not exceed the junction temperature limits. Refer to the Lattice [Thermal Management](#) document to find the device/package specific thermal values.

4.6. For Further Information

- [Power Estimation and Management for LatticeXP2 Devices \(TN1139\)](#)
- Power Calculator tool is included with the Lattice Diamond design tool or as a standalone download from www.latticesemi.com/products/designsoftware

5.2.1. Lead-Free Packaging

Commercial

Table 5.1. Lead-Free Packaging

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|--------------------|---------|-------|-----------------|------|-------|----------|
| LFXP2-5E-5MN132C | 1.2 V | –5 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-6MN132C | 1.2 V | –6 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-7MN132C | 1.2 V | –7 | Lead-Free csBGA | 132 | COM | 5 |
| LFXP2-5E-5TN144C | 1.2 V | –5 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-6TN144C | 1.2 V | –6 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-7TN144C | 1.2 V | –7 | Lead-Free TQFP | 144 | COM | 5 |
| LFXP2-5E-5QN208C | 1.2 V | –5 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-6QN208C | 1.2 V | –6 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-7QN208C | 1.2 V | –7 | Lead-Free PQFP | 208 | COM | 5 |
| LFXP2-5E-5FTN256C | 1.2 V | –5 | Lead-Free ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FTN256C | 1.2 V | –6 | Lead-Free ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FTN256C | 1.2 V | –7 | Lead-Free ftBGA | 256 | COM | 5 |
| LFXP2-8E-5MN132C | 1.2 V | –5 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-6MN132C | 1.2 V | –6 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-7MN132C | 1.2 V | –7 | Lead-Free csBGA | 132 | COM | 8 |
| LFXP2-8E-5TN144C | 1.2 V | –5 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-6TN144C | 1.2 V | –6 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-7TN144C | 1.2 V | –7 | Lead-Free TQFP | 144 | COM | 8 |
| LFXP2-8E-5QN208C | 1.2 V | –5 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-6QN208C | 1.2 V | –6 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-7QN208C | 1.2 V | –7 | Lead-Free PQFP | 208 | COM | 8 |
| LFXP2-8E-5FTN256C | 1.2 V | –5 | Lead-Free ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FTN256C | 1.2 V | –6 | Lead-Free ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FTN256C | 1.2 V | –7 | Lead-Free ftBGA | 256 | COM | 8 |
| LFXP2-17E-5QN208C | 1.2 V | –5 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-6QN208C | 1.2 V | –6 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-7QN208C | 1.2 V | –7 | Lead-Free PQFP | 208 | COM | 17 |
| LFXP2-17E-5FTN256C | 1.2 V | –5 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FTN256C | 1.2 V | –6 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FTN256C | 1.2 V | –7 | Lead-Free ftBGA | 256 | COM | 17 |
| LFXP2-17E-5FN484C | 1.2 V | –5 | Lead-Free fpBGA | 484 | COM | 17 |
| LFXP2-17E-6FN484C | 1.2 V | –6 | Lead-Free fpBGA | 484 | COM | 17 |
| LFXP2-17E-7FN484C | 1.2 V | –7 | Lead-Free fpBGA | 484 | COM | 17 |
| LFXP2-30E-5FTN256C | 1.2 V | –5 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FTN256C | 1.2 V | –6 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FTN256C | 1.2 V | –7 | Lead-Free ftBGA | 256 | COM | 30 |
| LFXP2-30E-5FN484C | 1.2 V | –5 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-6FN484C | 1.2 V | –6 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-7FN484C | 1.2 V | –7 | Lead-Free fpBGA | 484 | COM | 30 |
| LFXP2-30E-5FN672C | 1.2 V | –5 | Lead-Free fpBGA | 672 | COM | 30 |
| LFXP2-30E-6FN672C | 1.2 V | –6 | Lead-Free fpBGA | 672 | COM | 30 |
| LFXP2-30E-7FN672C | 1.2 V | –7 | Lead-Free fpBGA | 672 | COM | 30 |
| LFXP2-40E-5FN484C | 1.2 V | –5 | Lead-Free fpBGA | 484 | COM | 40 |

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|-------------------|---------|-------|-----------------|------|-------|----------|
| LFXP2-40E-6FN484C | 1.2 V | –6 | Lead-Free fpBGA | 484 | COM | 40 |
| LFXP2-40E-7FN484C | 1.2 V | –7 | Lead-Free fpBGA | 484 | COM | 40 |
| LFXP2-40E-5FN672C | 1.2 V | –5 | Lead-Free fpBGA | 672 | COM | 40 |
| LFXP2-40E-6FN672C | 1.2 V | –6 | Lead-Free fpBGA | 672 | COM | 40 |
| LFXP2-40E-7FN672C | 1.2 V | –7 | Lead-Free fpBGA | 672 | COM | 40 |

Table 5.2. Lead-Free Packaging

Industrial

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|--------------------|---------|-------|-----------------|------|-------|----------|
| LFXP2-5E-5MN132I | 1.2 V | –5 | Lead-Free csBGA | 132 | IND | 5 |
| LFXP2-5E-6MN132I | 1.2 V | –6 | Lead-Free csBGA | 132 | IND | 5 |
| LFXP2-5E-5TN144I | 1.2 V | –5 | Lead-Free TQFP | 144 | IND | 5 |
| LFXP2-5E-6TN144I | 1.2 V | –6 | Lead-Free TQFP | 144 | IND | 5 |
| LFXP2-5E-5QN208I | 1.2 V | –5 | Lead-Free PQFP | 208 | IND | 5 |
| LFXP2-5E-6QN208I | 1.2 V | –6 | Lead-Free PQFP | 208 | IND | 5 |
| LFXP2-5E-5FTN256I | 1.2 V | –5 | Lead-Free ftBGA | 256 | IND | 5 |
| LFXP2-5E-6FTN256I | 1.2 V | –6 | Lead-Free ftBGA | 256 | IND | 5 |
| LFXP2-8E-5MN132I | 1.2 V | –5 | Lead-Free csBGA | 132 | IND | 8 |
| LFXP2-8E-6MN132I | 1.2 V | –6 | Lead-Free csBGA | 132 | IND | 8 |
| LFXP2-8E-5TN144I | 1.2 V | –5 | Lead-Free TQFP | 144 | IND | 8 |
| LFXP2-8E-6TN144I | 1.2 V | –6 | Lead-Free TQFP | 144 | IND | 8 |
| LFXP2-8E-5QN208I | 1.2 V | –5 | Lead-Free PQFP | 208 | IND | 8 |
| LFXP2-8E-6QN208I | 1.2 V | –6 | Lead-Free PQFP | 208 | IND | 8 |
| LFXP2-8E-5FTN256I | 1.2 V | –5 | Lead-Free ftBGA | 256 | IND | 8 |
| LFXP2-8E-6FTN256I | 1.2 V | –6 | Lead-Free ftBGA | 256 | IND | 8 |
| LFXP2-17E-5QN208I | 1.2 V | –5 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-6QN208I | 1.2 V | –6 | Lead-Free PQFP | 208 | IND | 17 |
| LFXP2-17E-5FTN256I | 1.2 V | –5 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-6FTN256I | 1.2 V | –6 | Lead-Free ftBGA | 256 | IND | 17 |
| LFXP2-17E-5FN484I | 1.2 V | –5 | Lead-Free fpBGA | 484 | IND | 17 |
| LFXP2-17E-6FN484I | 1.2 V | –6 | Lead-Free fpBGA | 484 | IND | 17 |
| LFXP2-30E-5FTN256I | 1.2 V | –5 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-6FTN256I | 1.2 V | –6 | Lead-Free ftBGA | 256 | IND | 30 |
| LFXP2-30E-5FN484I | 1.2 V | –5 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-6FN484I | 1.2 V | –6 | Lead-Free fpBGA | 484 | IND | 30 |
| LFXP2-30E-5FN672I | 1.2 V | –5 | Lead-Free fpBGA | 672 | IND | 30 |
| LFXP2-30E-6FN672I | 1.2 V | –6 | Lead-Free fpBGA | 672 | IND | 30 |
| LFXP2-40E-5FN484I | 1.2 V | –5 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-6FN484I | 1.2 V | –6 | Lead-Free fpBGA | 484 | IND | 40 |
| LFXP2-40E-5FN672I | 1.2 V | –5 | Lead-Free fpBGA | 672 | IND | 40 |
| LFXP2-40E-6FN672I | 1.2 V | –6 | Lead-Free fpBGA | 672 | IND | 40 |

5.2.2. Conventional Packaging

Table 5.3. Conventional Packaging (Commercial)

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|-------------------|---------|-------|---------|------|-------|----------|
| LFXP2-5E-5M132C | 1.2 V | –5 | csBGA | 132 | COM | 5 |
| LFXP2-5E-6M132C | 1.2 V | –6 | csBGA | 132 | COM | 5 |
| LFXP2-5E-7M132C | 1.2 V | –7 | csBGA | 132 | COM | 5 |
| LFXP2-5E-5FT256C | 1.2 V | –5 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-6FT256C | 1.2 V | –6 | ftBGA | 256 | COM | 5 |
| LFXP2-5E-7FT256C | 1.2 V | –7 | ftBGA | 256 | COM | 5 |
| LFXP2-8E-5M132C | 1.2 V | –5 | csBGA | 132 | COM | 8 |
| LFXP2-8E-6M132C | 1.2 V | –6 | csBGA | 132 | COM | 8 |
| LFXP2-8E-7M132C | 1.2 V | –7 | csBGA | 132 | COM | 8 |
| LFXP2-8E-5FT256C | 1.2 V | –5 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-6FT256C | 1.2 V | –6 | ftBGA | 256 | COM | 8 |
| LFXP2-8E-7FT256C | 1.2 V | –7 | ftBGA | 256 | COM | 8 |
| LFXP2-17E-5FT256C | 1.2 V | –5 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-6FT256C | 1.2 V | –6 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-7FT256C | 1.2 V | –7 | ftBGA | 256 | COM | 17 |
| LFXP2-17E-5F484C | 1.2 V | –5 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-6F484C | 1.2 V | –6 | fpBGA | 484 | COM | 17 |
| LFXP2-17E-7F484C | 1.2 V | –7 | fpBGA | 484 | COM | 17 |
| LFXP2-30E-5FT256C | 1.2 V | –5 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-6FT256C | 1.2 V | –6 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-7FT256C | 1.2 V | –7 | ftBGA | 256 | COM | 30 |
| LFXP2-30E-5F484C | 1.2 V | –5 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-6F484C | 1.2 V | –6 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-7F484C | 1.2 V | –7 | fpBGA | 484 | COM | 30 |
| LFXP2-30E-5F672C | 1.2 V | –5 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-6F672C | 1.2 V | –6 | fpBGA | 672 | COM | 30 |
| LFXP2-30E-7F672C | 1.2 V | –7 | fpBGA | 672 | COM | 30 |
| LFXP2-40E-5F484C | 1.2 V | –5 | fpBGA | 484 | COM | 40 |
| LFXP2-40E-6F484C | 1.2 V | –6 | fpBGA | 484 | COM | 40 |
| LFXP2-40E-7F484C | 1.2 V | –7 | fpBGA | 484 | COM | 40 |
| LFXP2-40E-5F672C | 1.2 V | –5 | fpBGA | 672 | COM | 40 |
| LFXP2-40E-6F672C | 1.2 V | –6 | fpBGA | 672 | COM | 40 |
| LFXP2-40E-7F672C | 1.2 V | –7 | fpBGA | 672 | COM | 40 |

Table 5.4. Conventional Packaging (Industrial)

| Part Number | Voltage | Grade | Package | Pins | Temp. | LUTs (k) |
|-------------------|---------|-------|---------|------|-------|----------|
| LFXP2-5E-5M132I | 1.2 V | –5 | csBGA | 132 | IND | 5 |
| LFXP2-5E-6M132I | 1.2 V | –6 | csBGA | 132 | IND | 5 |
| LFXP2-5E-6FT256I | 1.2 V | –6 | ftBGA | 256 | IND | 5 |
| LFXP2-8E-5M132I | 1.2 V | –5 | csBGA | 132 | IND | 8 |
| LFXP2-8E-6M132I | 1.2 V | –6 | csBGA | 132 | IND | 8 |
| LFXP2-5E-5FT256I | 1.2 V | –5 | ftBGA | 256 | IND | 5 |
| LFXP2-8E-5FT256I | 1.2 V | –5 | ftBGA | 256 | IND | 8 |
| LFXP2-8E-6FT256I | 1.2 V | –6 | ftBGA | 256 | IND | 8 |
| LFXP2-17E-5FT256I | 1.2 V | –5 | ftBGA | 256 | IND | 17 |
| LFXP2-17E-6FT256I | 1.2 V | –6 | ftBGA | 256 | IND | 17 |
| LFXP2-17E-5F484I | 1.2 V | –5 | fpBGA | 484 | IND | 17 |
| LFXP2-17E-6F484I | 1.2 V | –6 | fpBGA | 484 | IND | 17 |
| LFXP2-30E-5FT256I | 1.2 V | –5 | ftBGA | 256 | IND | 30 |
| LFXP2-30E-6FT256I | 1.2 V | –6 | ftBGA | 256 | IND | 30 |
| LFXP2-30E-5F484I | 1.2 V | –5 | fpBGA | 484 | IND | 30 |
| LFXP2-30E-6F484I | 1.2 V | –6 | fpBGA | 484 | IND | 30 |
| LFXP2-30E-5F672I | 1.2 V | –5 | fpBGA | 672 | IND | 30 |
| LFXP2-30E-6F672I | 1.2 V | –6 | fpBGA | 672 | IND | 30 |
| LFXP2-40E-5F484I | 1.2 V | –5 | fpBGA | 484 | IND | 40 |
| LFXP2-40E-6F484I | 1.2 V | –6 | fpBGA | 484 | IND | 40 |
| LFXP2-40E-5F672I | 1.2 V | –5 | fpBGA | 672 | IND | 40 |
| LFXP2-40E-6F672I | 1.2 V | –6 | fpBGA | 672 | IND | 40 |

6. Supplemental Information

A variety of technical notes for the LatticeXP2 FPGA family are available on the Lattice Semiconductor web site at www.latticesemi.com.

- [LatticeXP2 sysI/O Usage Guide \(TN1136\)](#)
- [LatticeXP2 Memory Usage Guide \(FPGA-UG-02080\)](#)
- [LatticeXP2 High Speed I/O Interface \(TN1138\)](#)
- [LatticeXP2 sysCLOCK PLL Design and Usage Guide \(TN1126\)](#)
- [Power Estimation and Management for LatticeXP2 Devices \(TN1139\)](#)
- [LatticeXP2 sysDSP Usage Guide \(TN1140\)](#)
- [LatticeXP2 sysCONFIG Usage Guide \(TN1141\)](#)
- [LatticeXP2 Configuration Encryption and Security Usage Guide \(TN1142\)](#)
- [Minimizing System Interruption During Configuration Using TransFR Technology \(TN1087\)](#)
- [LatticeXP2 Dual Boot Feature \(TN1220\)](#)
- [LatticeXP2 Soft Error Detection \(SED\) Usage Guide \(TN1130\)](#)
- [LatticeXP2 Hardware Checklist \(TN1143\)](#)

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTTL, LVCMOS, SSTL, HSTL): www.jedec.org
- PCI: www.pcisig.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 2.5, July 2021

| Section | Change Summary |
|----------------------------------|---|
| DC and Switching Characteristics | Updated footnote 4 in Table 3.6 . |
| Architecture | Update link to LatticeXP2 sysCLOCK PLL Design and Usage Guide (TN1126) in On-Chip Oscillator section. |

Revision 2.4, January 2021

| Section | Change Summary |
|--------------------|--|
| All | <ul style="list-style-type: none"> Changed document ID from DS1009 to FPGA-DS-02088 Updated document template. |
| Disclaimers | Added this section. |
| Architecture | Updated link to the LatticeXP2 sysDSP Usage Guide (TN1140). |
| Pinout Information | Changed reference from <i>Data Sheet</i> to <i>Pin & Package</i> and updated link to the LatticeXP2 product page. |

Revision 2.3, June 2017

| Section | Change Summary |
|----------------------------------|--|
| DC and Switching Characteristics | Updated Hot Socketing Specifications table – Changed I_{PW} to I_{PD} in footnote 3. |
| Revision History | Changed the order of Revision History table. |

Revision 2.2, September 2014

| Section | Change Summary |
|----------------------------------|--|
| DC and Switching Characteristics | Updated Switching Test Conditions section. Re-linked missing figure. |
| Supplemental Information | Added MIPI D-PHY Bandwidth Matrix and Implementation reference. |

Revision 2.1, August 2014

| Section | Change Summary |
|--------------|---|
| Architecture | Updated Typical sysI/O I/O Behavior During Power-up section. Described user I/O during power up and before FPGA core logic is active. |

Revision 2.0, March 2014

| Section | Change Summary |
|--------------|--|
| Architecture | Updated Typical sysI/O I/O Behavior During Power-up section. Added information on POR signal deactivation. |

Revision 1.9, May 2013

| Section | Change Summary |
|----------------------------------|---|
| All | Updated document with new corporate logo. |
| Architecture | <ul style="list-style-type: none"> Architecture Overview – Added information on the state of the register on power up and after configuration. Added information regarding SED support. |
| DC and Switching Characteristics | Removed Input Clock Rise/Fall Time 1ns max from the sysCLOCK PLL Timing table. |
| Ordering Information | Updated topside mark in Ordering Information diagram. |

Revision 1.8, January 2012

| Section | Change Summary |
|----------------------------------|---|
| Multiple | Added support for Lattice Diamond design software. |
| Architecture | Corrected information regarding SED support. |
| DC and Switching Characteristics | Added reference to ESD Performance Qualification Summary information. |

Revision 1.7, April 2011

| Section | Change Summary |
|----------------------------------|--|
| DC and Switching Characteristics | <ul style="list-style-type: none"> Recommended Operating Conditions table, added footnote 5. On-Chip Flash Memory Specifications table, added footnote 1. BLVDS DC Conditions, corrected column title to be Z0 = 90 ohms. sysCONFIG Port Timing Specifications table, added footnote 1 for tDINIT. |

Revision 1.6, August 2008

| Section | Change Summary |
|----------------------------------|---|
| All | Data sheet status changed from preliminary to final. |
| Architecture | Clarification of the operation of the secondary clock regions. |
| DC and Switching Characteristics | <ul style="list-style-type: none"> Removed "8W" specification from Hot Socketing Specifications table. Removed "8W" footnote from DC Electrical Characteristics table. Updated Register-to-Register Performance table. |
| Ordering Information | <ul style="list-style-type: none"> Removed "8W" option from Part Number Description. Removed XP2-17 "8W" OPNs. |

Revision 1.5, June 2008

| Section | Change Summary |
|----------------------------------|--|
| Architecture | <ul style="list-style-type: none"> Removed Read-Before-Write sysMEM EBR mode. Clarification of the operation of the secondary clock regions. |
| DC and Switching Characteristics | Removed Read-Before-Write sysMEM EBR mode. |
| Pinout Information | Updated DDR Banks Bonding Out per I/O Bank section of Pin Information Summary Table. |

Revision 1.4, April 2008

| Section | Change Summary |
|----------------------------------|--|
| DC and Switching Characteristics | <ul style="list-style-type: none"> Updated Absolute Maximum Ratings footnotes. Updated Recommended Operating Conditions Table footnotes. Updated Supply Current (Standby) Table Updated Initialization Supply Current Table Updated Programming and Erase Flash Supply Current Table Updated Register to Register Performance Table Updated LatticeXP2 External Switching Characteristics Table Updated LatticeXP2 Internal Switching Characteristics Table Updated sysCLOCK PLL Timing Table Updated Flash Download Time (From On-Chip Flash to SRAM) Table Updated Flash Program Time Table Updated Flash Erase Time Table Updated FlashBAK (from EBR to Flash) Table Updated Hot Socketing Specifications Table footnotes |
| Pinout Information | Updated Signal Descriptions Table |

Revision 1.3, February 2008

| Section | Change Summary |
|----------------------------------|--|
| Architecture | <ul style="list-style-type: none"> Added LVCMOS33D to Supported Output Standards table. Clarified: "This Flash can be programmed through either the JTAG or Slave SPI ports of the device. The SRAM configuration space can also be infinitely reconfigured through the JTAG and Master SPI ports." Added External Slave SPI Port to Serial TAG Memory section. Updated Serial TAG Memory diagram. |
| DC and Switching Characteristics | <ul style="list-style-type: none"> Updated Flash Programming Specifications table. Added "8W" specification to Hot Socketing Specifications table. Updated Timing Tables. Clarifications for IIH in DC Electrical Characteristics table. Added LVCMOS33D section. Updated DOA and DOA (Regs) to EBR Timing diagrams. Removed Master Clock Frequency and Duty Cycle sections from the LatticeXP2 sysCONFIG Port Timing Specifications table. These are listed on the On-chip Oscillator and Configuration Master Clock Characteristics table. Changed CSSPIN to CSSPISN in description of tSCS, tSCSS, and tSCSH parameters. Removed tSOE parameter. Clarified On-chip Oscillator documentation. Added Switching Test Conditions. |
| Pinout Information | <ul style="list-style-type: none"> Added "True LVDS Pairs Bonding Out per Bank," "DDR Banks Bonding Out per I/O Bank," and "PCI capable I/O Bonding Out per Bank" to Pin Information Summary in place of previous blank table "PCI and DDR Capabilities of the Device-Package Combinations." Removed pinout listing. This information is available on the LatticeXP2 product web pages. |
| Ordering Information | Added XP2-17 "8W" and all other family OPNs. |

Revision 1.2, September 2007

| Section | Change Summary |
|----------------------------------|---|
| DC and Switching Characteristics | <ul style="list-style-type: none"> Added JTAG Port Timing Waveforms diagram. Updated sysCLOCK PLL Timing table. |
| Pinout Information | Added Thermal Management text section. |

Revision 1.1, May 2007

| Section | Change Summary |
|---------|------------------|
| All | Initial release. |



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