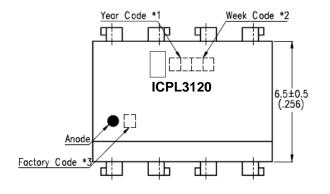
Ordering Information

Part	Option	Remarks
		DIP-8
	G	Wide Lead Spacing, DIP-8
ICPL3120	SM	Surface Mount, SMD-8
	T&R	Surface Mount, SMD-8, Pin 1 location at lower right of the reel
	T&R1	Surface Mount, SMD-8, Pin 1 location at upper left of the reel

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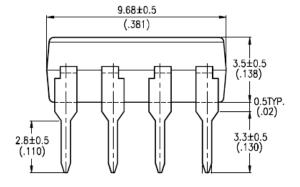
Package Dimensions

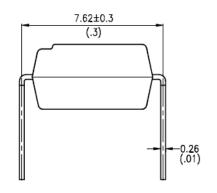
8-pin DIP Package (ICPL3120)



- *1. Year date code.
- *2. 2-digit work week.
- *3. Factory identification mark

Dimensions are in Millimeters and (Inches).





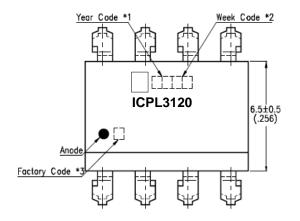
18

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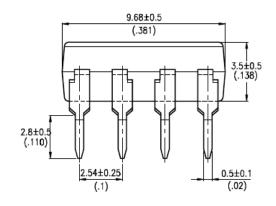
Package Dimensions

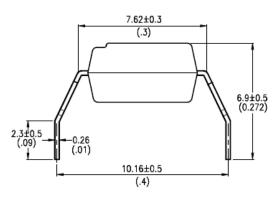
8-pin DIP Wide Lead Spacing Package (ICPL3120G)



- *1. Year date code.
- *2. 2-digit work week.
- *3. Factory identification mark

Dimensions are in Millimeters and (Inches).

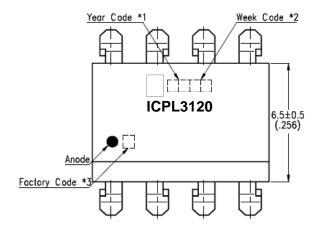




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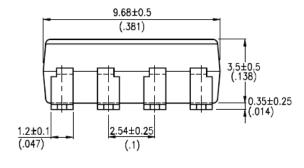
Package Dimensions

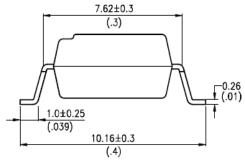
8-pin DIP Surface Mount Package (ICPL3120SM)



- *1. Year date code.
- *2. 2-digit work week.*3. Factory identification mark

Dimensions are in Millimeters and (Inches).

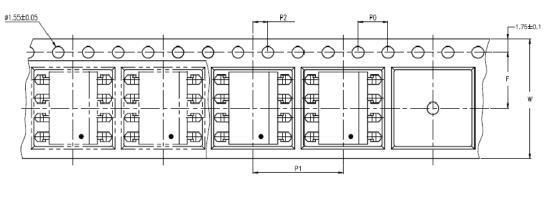


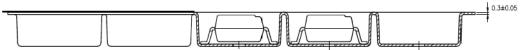


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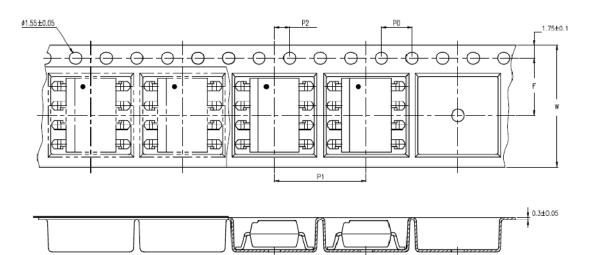
Taping Dimensions

ICPL3120SM-TA





ICPL3120SM-TA1



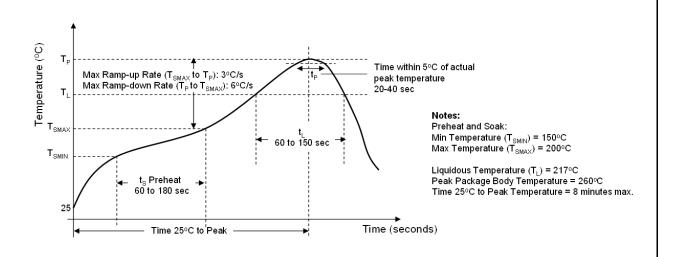
Description	Symbol	Dimensions in millimeters (inches)
Tape wide	W	16 ± 0.3 (.63)
Pitch of sprocket holes	P0	4 ± 0.1 (.15)
Distance of compartment	F P2	7.5 ± 0.1 (.295) 2 ± 0.1 (.079)
Distance of compartment to compartment	P1	12 ± 0.1 (.472)

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Recommended Lead Free Reflow Profile



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Absolute Maximum Ratings

Ambient temperature = 25°C, unless otherwise specified. Stresses exceeding the absolute maximum ratings can cause permanent damage to the device. Exposure to absolute maximum ratings for long periods of time can adversely affect reliability.

Parameter	Symbol	Min	Max	Units
Storage Temperature	T _{ST}	-55	125	°C
Operating Temperature	T _A	-40	110	°C
Isolation Voltage	V _{ISO}	5000		V _{RMS}
Supply Voltage	V _{cc}	0	35	V
Lead Solder Temperature (9)	T _{SOL}		260	°C
Input				
Average Forward Input Current	I _{F(AVG)}		25	mA
Reverse Input Voltage	V_R		5	V
Peak Transient Input Current (<1 µs pulse width, 300 pps)	I _{F(TRAN)}		1	А
Input Current (Rise/Fall Time)	$t_{r(IN)} / t_{f(IN)}$		500	ns
Input Power Dissipation (10)	Pı		45	mW
Output				
"High" Peak Output Current (1)	I _{OH(PEAK)}		2.5	Α
"Low" Peak Output Current (1)	I _{OL(PEAK)}		2.5	Α
Output Voltage	Vo		V _{CC}	V
Output Power Dissipation (11)	Po		250	mW
Total Power Dissipation	P _T		295	mW

- 8) At least a 0.1uF or bigger bypass capacitor must be connected across pin 8 and pin5. Failure to provide the bypass may impair the switching property.
- 9) 260°C for 10 seconds. Refer to Lead Free Reflow Profile
- 10) Derating Linearly above 70°C free-air temperature at a rate of -0.47 mW/°C
- 11) Derating Linearly above 70°C free-air temperature at a rate of 4.8mW/°C

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units
Operating Temperature	T _A	-40	110	°C
Supply Voltage	V _{CC}	15	30	V
Input Current (ON)	I _{FL(ON)}	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	0.8	V

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Electrical Specifications

Parameters	Test Condition	Symbol	Min	Тур	Max	Units	Figure
Input							
Input Forward Voltage	I _F = 10mA	V_{F}	1.2	1.37	1.8	V	15
Input Forward Voltage Temperature Coefficient	I _F = 10mA	ΔV _F / ΔΤ		-1.237		mV/ ^O C	
Input Reverse Voltage	I _R = 10μA	BV_R	5			V	
Input Threshold Current (Low to High)	V _O > 5V, I _O = 0A	I _{FLH}		2.89	5	mA	9,16,21
Input Threshold Voltage (High to Low)	$V_{\rm O}$ < 5V, $I_{\rm O}$ = 0A	V_{FHL}	0.8			V	
Input Capacitance	f = 1 MHz, V _F = 0 V	C _{IN}		33		рF	
Output							
High Level Supply Current	Output Open, I _F = 7 to 16 mA	Іссн		1	3.0	mA	7,8
Low Level Supply Current	Output Open, $V_F = -3 \text{ to } +0.8 \text{ V}$	I _{CCL}		1	3.0	mA	7,8
High level output current (1)	V _O = (V _{CC} - 6 V)	I _{OH}	-2.0			Α	2,3,19
Low level output current (1)	V _O = (V _{EE} + 6 V)	I _{OL}	2.0			Α	5,6,20
High level output voltage	I _F = 10mA, I _O = -100mA	V_{OH}	V _{CC -} 0.25	V _{CC} - 0.1		V	1,3,17
Low level output voltage	I _F = 0mA, I _O = 100mA	V_{OL}		V _{EE +} 0.1	V _{EE +} 0.25	V	4,6,18
LIVII O Throchold	$V_{\rm O}$ > 5V, $I_{\rm F}$ = 10 mA	$V_{\text{UVLO+}}$	11.5		13.5	V	
UVLO Threshold	$V_{\rm O}$ < 5V, $I_{\rm F}$ = 10 mA	V_{UVLO}	10	11.5	12	V	22
UVLO Hysteresis		UVLO _{HYS}		1.6		V	

Specified over recommended operating conditions.

All Typical values at TA = 25°C and V_{CC} = 30 V, unless otherwise specified.

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Switching Specifications

Parameter	Test Condition	Symbol	Min	Тур	Max	Units	Figure
Propagation Delay Time to High Output Level	I_F = 7 to 16 mA, Rg = 10 Ω, Cg = 10 nF,	T _{PLH}	0.1	0.28	0.5	μs	
Propagation Delay Time to Low Output Level	f = 10 kHz, Duty Cycle = 50%	T_{PHL}	0.1	0.31	0.5	μs	10,11, 12,13,
Pulse Width Distortion (7)		PWD			0.1	μs	14,23
Propagation delay difference between any two parts or channels ⁽⁴⁾		PDD	-0.30		0.30	μs	
Output Rise Time (10 to 90%)		Tr		0.1		μs	23
Output Fall Time (90 to 10%)		Tf		0.1		μs	23
UVLO turn on delay	I _F = 10 mA, V _O > 5 V	T _{UVLO ON}		1.5		μs	
UVLO turn off delay	I _F = 10 mA, V _O < 5 V	T _{UVLO OFF}		0.2		μs	
Common mode transient immunity at high level output ⁽⁵⁾	$I_F = 10 \text{ to } 16 \text{ mA},$ $V_{CM} = 1500 \text{ V},$ $TA = 25^{\circ}\text{C},$ $V_{CC} = 30 \text{ V}$	СМН	25	35		kV/μs	24
Common mode transient immunity at low level output ⁽⁶⁾	V _F = 0 V, V _{CM} = 1500 V, TA = 25°C, V _{CC} = 30 V	CML	25	35		kV/μs	24

Specified over recommended operating conditions.

All Typical values at TA = 25°C and V_{CC} = 30 V, unless otherwise specified.

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Isolation Characteristics

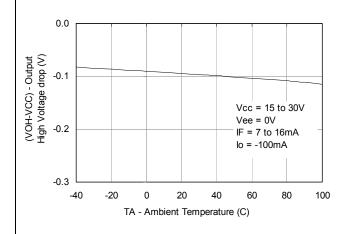
Parameter	Test Condition	Symbol	Min	Тур	Max	Units
Withstand Insulation Test Voltage (2) (3)	RH ≤ 40-60%, t = 1min, T _A = 25°C	V _{ISO}	5000			V
Input-Output Resistance (2)	V _{I-O} = 500V DC	R _{I-O}		10 ¹²		Ω
Input-Output Capacitance ⁽²⁾	f = 1MHz, T _A = 25°C	C _{I-O}		0.92		pF

Notes:

- 1) Maximum pulse width = 10us, maximum duty cycle = 0.2%.
- 2) Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
- 3) According to UL1577, each optocoupler is tested by applying an insulation test voltage ≥ 6000 Vrms for 1 second (leakage detection current limit, I_{I-O} ≤ 6 uA).
- 4) The difference between T_{PHL} and T_{PLH} between any two ICPL3120 parts under same test conditions.
- 5) Common mode transient immunity in high stage is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, Vcm, to assure that the output will remain high.
- 6) Common mode transient immunity in low stage is the maximum tolerable positive dVcm/dt on the leading edge of the common mode impulse signal, Vcm, to assure that the output will remain low.
- 7) Pulse Width Distortion is defined as |T_{PHL} T_{PLH}| for any given device.

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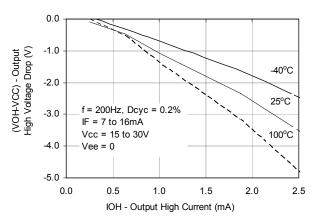
Typical Performance Curves



5.0 f = 200Hz, Rg = 10 ohm Dcyc = 0.2% 4.0 IOH - Output High Current (A) Vcc = 15 to 30V IF = 7 to 16mA 3.0 2.0 Vcc = 30V 1.0 0.0 40 60 80 100 -40 -20 0 20 TA - Ambient Temperature (C)

Figure 1: Output High Voltage drop vs Temperature

Figure 2: Output High Current vs Temperature



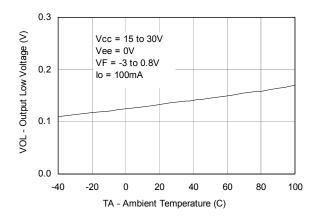
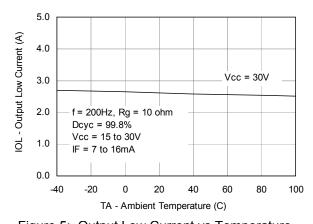


Figure 3: Output High Voltage drop vs High Current

Figure 4: Output Low Voltage vs Temperature



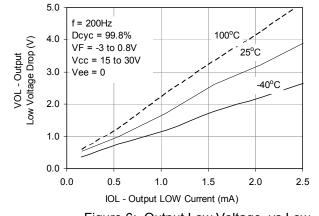


Figure 5: Output Low Current vs Temperature Current

Figure 6: Output Low Voltage vs Low

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2.0

15

1.0

0.5

ICC - Supply Current (mA)

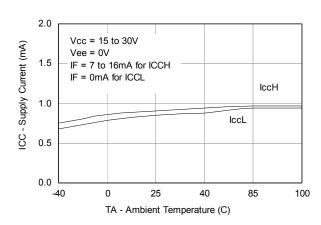
 $TA = 25 \deg$

IF = 7 to 16mA for ICCH

IF = 0mA for ICCL

Vee = 0V

Typical Performance Curves (Continued)

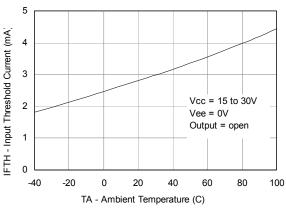


0.0 15 27 30 33 VCC - Supply Voltage (V)

lccH

lccL

Figure 7: Supply Current vs Temperature



500

Figure 8: Supply Current vs Supply Voltage

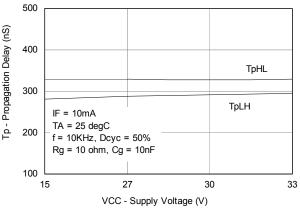


Figure 9: Low to High Threshold Current vs Temperature

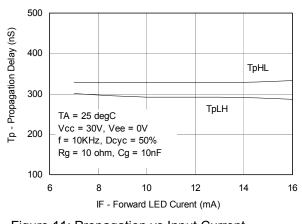


Figure 10: Propagation vs Vcc

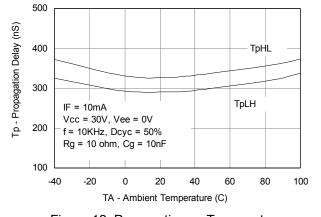


Figure 11: Propagation vs Input Current

Figure 12: Propagation vs Temperature

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Typical Performance Curves (Continued)

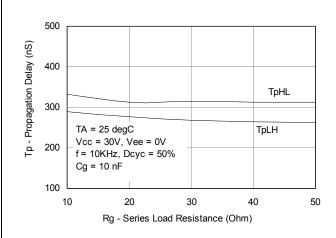


Figure 13: Propagation vs Series Load Resistance

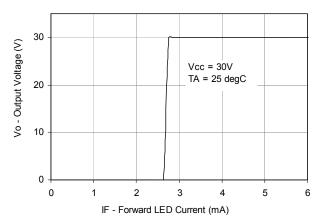


Figure 16: Transfer Characteristics

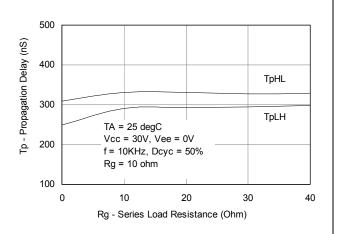


Figure 14: Propagation vs Load Capacitance (nF)

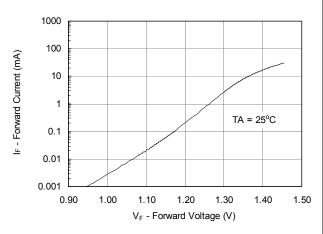
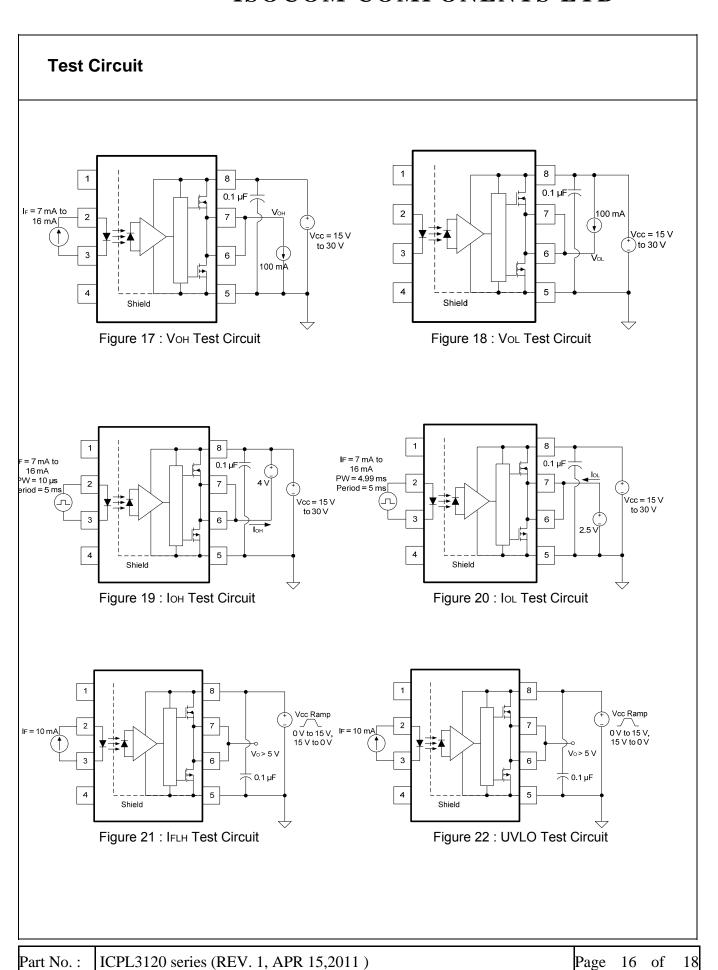


Figure 15: Input Current vs Forward Voltage

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Test Circuit (Continued)

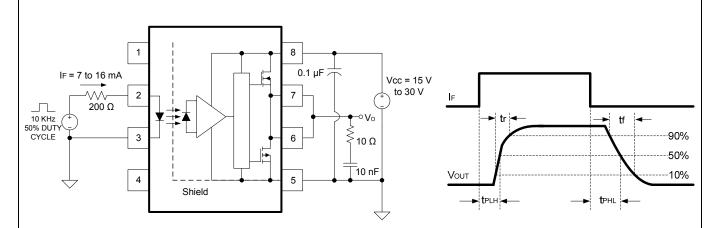


Figure 23: tr, tf, tplh and tphl Test Circuit and Waveforms

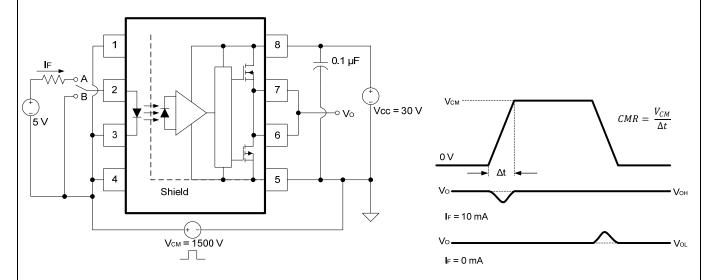


Figure 24: CMR Test Circuit and Waveforms

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