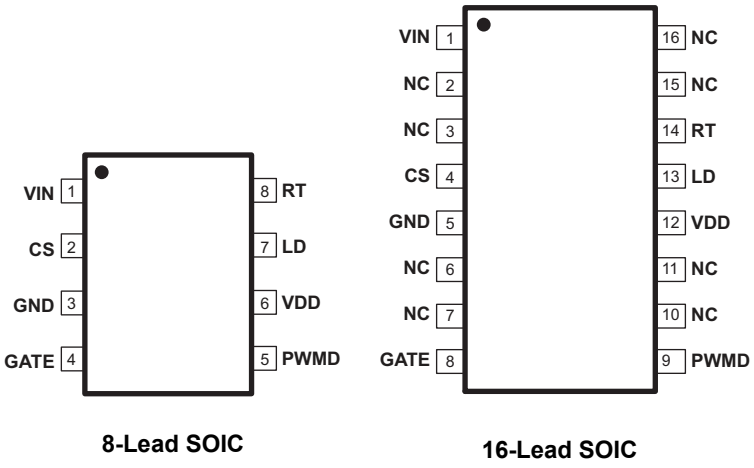
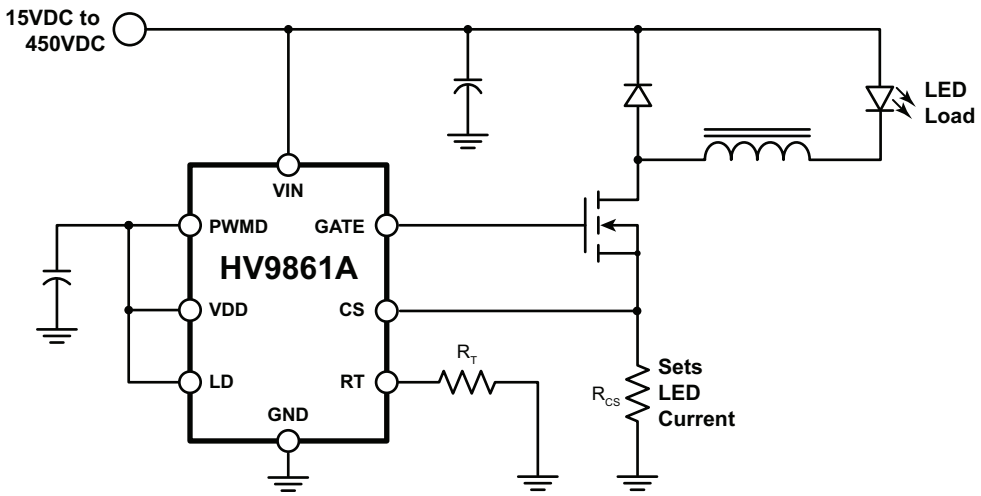
Package Types



See Table 2-1 for pin information

Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND ..... -0.5V to +470V
V_{DD} to GND 12V
LD, PWMD, GATE to GND ..... -0.3V to (V_{DD} + 0.3V)
CS, RT to GND ..... -0.3V to 5.0V
Operating temperature ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Continuous power dissipation (T_A = +25°C)
8-lead SOIC ..... 650 mW
16-lead SOIC ..... 1000 mW

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS (SHEET 1 OF 2)[1]

Symbol	Parameter	Note	Min	Typ	Max	Units	Conditions
Input							
V_{INDC}	Input DC supply voltage range[2]	3	15	-	450	V	DC input voltage
I_{INSD}	Shut-down mode supply current	3	-	0.5	1.1	mA	Pin PWMD to GND
Internal Regulator							
V_{DD}	Internally regulated voltage	-	7.25	7.50	8.20	V	500pF at GATE; RT = 226kΩ
ΔV_{DD}, line	Line regulation of V_{DD}	-	-	-	1	V	V_{IN} = 15 - 450V, 500pF at GATE; RT = 226kΩ
ΔV_{DD}, load	Load regulation of V_{DD}	-	-	-	100	mV	$I_{DD(ext)}$ = 0 - 1mA, 500pF at GATE; RT = 226kΩ
UVLO	V_{DD} under-voltage lockout threshold	3	6.45	-	-	V	V_{IN} rising
ΔUVLO	V_{DD} under-voltage lockout hysteresis	-	-	500	-	mV	V_{IN} falling
$\Delta V_{DD(UV)}$	V_{DD} voltage margin	3	500	-	-	mV	$\Delta V_{DD(UV)} = V_{DD}$ - UVLO
$I_{IN,MAX}$	Maximum input current (limited by UVLO)	4	3.5	-	-	mA	V_{IN} = 15V, T_A = 25°C
		4	1.5	-	-		V_{IN} = 15V, T_A = 125°C
PWM Dimming							
$V_{EN(lo)}$	PWMD input low voltage	3	-	-	0.8	V	V_{IN} = 15 - 450V
$V_{EN(hi)}$	PWMD input high voltage	3	2.2	-	-	V	V_{IN} = 15 - 450V
I_{EN}	Internal pull-down current at PWMD	-	8.5	-	13.5	µA	V_{PWMD} = 0.8V

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED) (SHEET 2 OF 2)[1]

Symbol	Parameter	Note	Min	Typ	Max	Units	Conditions
Average Current Sense Logic							
V_{CS}	Current sense reference voltage	-	262	-	280	mV	
$A_{V(LD)}$	LD-to-CS voltage ratio	-	0.175	-	0.182	-	
$A_V \bullet V_{LD(OFFSET)}$	LD-to-CS voltage offset	-	-10	-	10	mV	Offset = V_{CS} - ($A_{V(LD)} \bullet V_{LD}$); V_{LD} = 1.2V
$\Delta V_{CS(TEMP)}$	CS threshold temp regulation	4	-	-	5	mV	
$V_{LD(OFF)}$	LD input voltage, shutdown	-	-	150	-	mV	V_{LD} falling
$\Delta V_{LD(OFF)}$	LD input voltage, enable	-	-	200	-	mV	V_{LD} rising
T_{BLANK}	Current sense blanking interval	3	140	-	290	ns	
$T_{ON(min)}$	Minimum on-time	-	-	-	760	ns	CS = V_{CS} + 30mV
D_{MAX}	Maximum steady-state duty cycle	3	80	-	-	%	Reduction in output LED current may occur beyond this duty cycle
Short Circuit Protection							
V_{CS}	Hiccup threshold voltage	3	410	-	510	mV	
T_{DELAY}	Current limit delay CS-to-GATE	-	-	-	150	ns	CS = V_{CS} + 30mV
T_{HICCUP}	Short circuit hiccup time	-	400	-	850	µs	
$T_{ON(min)}$	Minimum on-time (short circuit)	-	-	-	430	ns	CS = 4V
TOFF Timer							
T_{OFF}	Off-time	-	32	40	48	µs	R_T = 1MΩ
		-	8	10	12		R_T = 226kΩ
GATE Driver							
I_{SOURCE}	Sourcing current	-	0.165	-	-	A	V_{GATE} = 0V, V_{DD} = 7.5V
I_{SINK}	Sinking current	-	0.165	-	-	A	V_{GATE} = VDD, V_{DD} = 7.5V
t_{RISE}	Output rise time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V
t_{FALL}	Output fall time	-	-	30	50	ns	C_{GATE} = 500pF, V_{DD} = 7.5V
Over-Temperature Protection							
T_{SD}	Shut-down temperature	4	128	140	-	°C	---
ΔT_{SD}	Hysteresis	4	-	20	-	°C	---

1 Specifications are T_A = 25°C, V_{IN} = 15V, V_{LD} = V_{DD}, PWMD = V_{DD} unless otherwise noted.
2 Also limited by package-power dissipation limit; Whichever is lower.
3 Applies over the full operating ambient temperature range of -40°C < T_A < +125°C.
4 For design guidance only

TABLE 1-2: THERMAL RESISTANCE

Package	θja
8-Lead SOIC	101°C/W
16-Lead SOIC	83°C/W

2.0 PIN DESCRIPTION

The locations of the pins are listed in Package Types.

TABLE 2-1: PIN DESCRIPTION

Pin #		Function	Description
8-Lead SOIC	16-Lead SOIC		
1	1	VIN	Input of a 15 - 450V linear regulator.
2	4	CS	Current sense pin used to sense the FET current by means of an external sense resistor.
3	5	GND	Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train.
4	8	GATE	Output GATE driver for an external N-channel power MOSFET.
5	9	PWMD	PWM-dimming input of the IC. When this pin is pulled to GND, the gate driver is turned off. When the pin is pulled high, the gate driver operates normally.
6	12	VDD	Power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1µF).
7	13	LD	Linear-dimming input. Sets the current sense threshold as long as the voltage at this pin is less than 1.5V. If voltage at LD falls below 150mV, the GATE output is disabled. The GATE signal recovers at 200mV at LD.
8	14	RT	A resistor connected between this pin and GND programs the GATE off-time.
-	2, 3, 6, 7, 10, 11, 15, 16	NC	No connection.

3.0 APPLICATION INFORMATION

Peak-current control (as in the HV9910B) of a buck converter is the most economical and simple way to regulate its output current. However, this method suffers accuracy and regulation problems that arise from the so-called peak-to-average current error, contributed to by the current ripple in the output inductor and the propagation delay in the current-sense comparator. The full inductor-current signal is unavailable for direct sensing at the ground potential in a buck converter when the control switch is referenced to the same ground potential. While it is very simple to detect the peak current in the switch, controlling the average inductor current is usually implemented by level translating the sense signal from the positive supply rail. Though this is practical for relatively low input voltage, this type of average-current control may become excessively complex and expensive in off line AC or other high-voltage DC applications.

HV9861A employs a patented control scheme, achieving fast and very accurate control of average current in the buck inductor through sensing the switch current only. No compensation of the current-control loop is required. The LED current response to PWMD input is similar to that of the HV9910B. The inductor-current ripple amplitude does not affect this control scheme significantly. Therefore, the LED current is independent of the variation in inductance, switching frequency, or output voltage. Constant off-time control of the buck converter is used for stability and to improve the LED-current regulation over a wide range of input voltages. (Note that, unlike the HV9910B, this IC does not support the constant-frequency mode of operation.)

3.1 OFF Timer

The timing resistor connected to RT determines the off-time of the gate driver, and it must be wired to GND. Wiring this resistor to GATE as with the HV9910B is no longer supported. The equation governing the off-time of the GATE output is given by:

$$T_{OFF}(\mu s) = \frac{R_T(k\Omega)}{25} + 0.3$$

Within the range of 30kΩ ≤ R_T ≤ 1.0MΩ.

3.2 Average Current Control Feedback and Output Short Circuit Protection

The current through the switching MOSFET source is averaged and used to give constant-current feedback. This current is detected using a sense resistor at the CS pin. The feedback operates in a fast open-loop mode. No compensation is required. Output current is programmed simply as:

$$I_{LED} = \frac{0.27V}{R_{CS}}$$

When the voltage at the LD input V_{LD} ≥ 1.5V. Otherwise:

$$I_{LED} = \frac{V_{LD} \cdot 0.18}{R_{CS}}$$

The above equations are only valid for continuous conduction of the output inductor. It is a good practice to design the inductor such that the switching ripple current in it is 30~40% of its average peak-to-peak, full load, DC current. Hence, the recommended inductance can be calculated as:

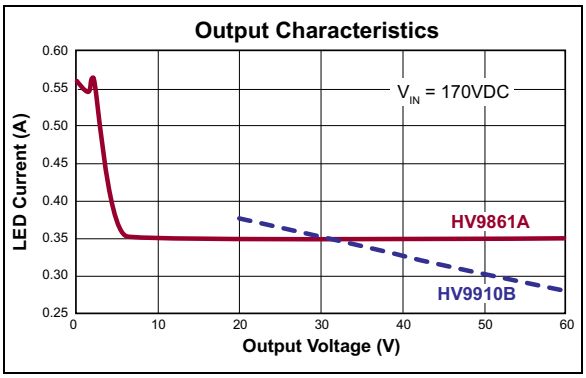
$$L = \frac{V_{O(MAX)} \cdot T_{OFF}}{0.4 \cdot I_O}$$

The duty-cycle range of the current control feedback is limited to D ≤ 0.8. A reduction in the LED current may occur when the LED string voltage V_O is greater than 80% of the input voltage V_{IN} of the HV9861A LED driver.

Reducing the output LED voltage V_O below $V_{O(MIN)}$ = V_{IN} • D_{MIN}, where D_{MIN} = 760ns/(T_{OFF} +760ns), may also result in the loss of regulation of the LED current. However, this condition causes an increase in the LED current and can potentially trip the short-circuit protection comparator.

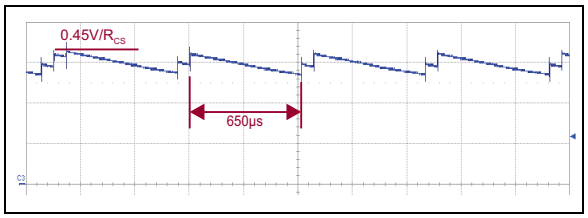
A typical output characteristic of the HV9861A LED driver is shown in Figure 3-1. The corresponding HV9910B characteristic is given for comparison.

FIGURE 3-1: TYPICAL OUTPUT CHARACTERISTIC OF AN HV9861A LED DRIVER



The short circuit protection comparator trips when the voltage at CS exceeds 0.45V. When this occurs, the GATE off-time T_{HICCUP} = 650µs is generated to prevent stair-casing of the inductor current, and potentially its saturation, due to insufficient output voltage. The typical short-circuit current is shown in the waveform of Figure 3-2.

FIGURE 3-2: SHORT-CIRCUIT INDUCTOR CURRENT

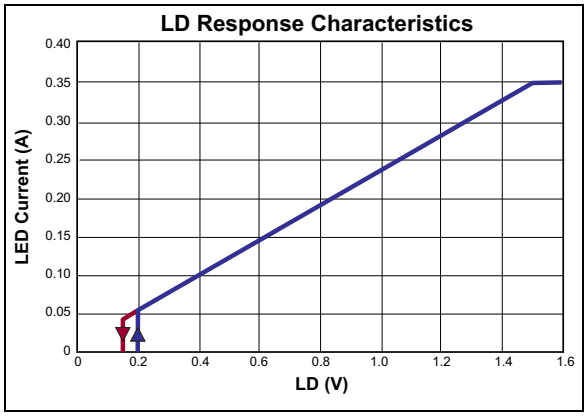


A leading-edge blanking delay is provided at CS to prevent false triggering of the current feedback and the short circuit protection.

3.3 Linear Dimming

When the voltage at LD falls below 1.5V, the internal 270mV reference to the constant-current feedback becomes overridden by V_{LD} • 0.18. As long as the current in the inductor remains continuous, the LED current is given by the equation in Section 3.2. However, when V_{LD} falls below 150mV, the GATE output becomes disabled. The GATE signal recovers, when V_{LD} exceeds 200mV. This is required in some applications to be able to shut the LED lamp off with the same signal input that controls the brightness. The typical linear dimming response is shown in Figure 3-3.

FIGURE 3-3: TYPICAL LINEAR DIMMING RESPONSE OF AN HV9861A LED DRIVER



The linear dimming input could also be used for "mixed-mode" dimming to expand the dimming ratio. In such case a pulse-width modulated signal of a measured amplitude below 1.5V should be applied at LD.

3.4 Input Voltage Regulator

HV9861A can be powered directly from a 15 – 450VDC supply through its VIN input. When this voltage is applied at the VIN pin, the HV9861A maintains a constant 7.5V level at VDD. This voltage can be used to power the IC and external circuitry connected to VDD within the rated maximum current or within the thermal ratings of the package, whichever limit is lower. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the GATE output. The HV9861A can also be powered through the VDD pin directly with a voltage greater than the internally regulated 7.5V, but less than 12V.

Despite the instantaneous voltage rating of 450V, continuous voltage at VIN is limited by the power dissipation in the package. For example, when these ICs draw I_{IN} = 3.0mA from the VIN input, and the 8-lead SOIC package is used, the maximum continuous voltage at VIN is limited to the following:

$$V_{IN(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta, J-A} \cdot I_{IN}} = 330V$$

In this instance, the ambient temperature T_A = 25°C, the maximum working junction temperature $T_{J(MAX)}$ = 125°C, and the junction-to-ambient thermal resistance $R_{\theta,JA}$ = 101°C/W.

In such cases, when it is needed to operate the HV9861A from a higher voltage, a resistor or a Zener diode can be added in series with the VIN input to divert some of the power loss from the IC. In the above example, using a 100V Zener diode will allow the circuit to work up to 430V. The input current drawn from the VIN pin is represented by the following equation:

$$I_{IN} \approx 1.0mA + Q_G \cdot f_s$$

In the above equation, f_S is the switching frequency, and Q_G is the GATE charge of the external FET obtained from the manufacturer's data sheet.

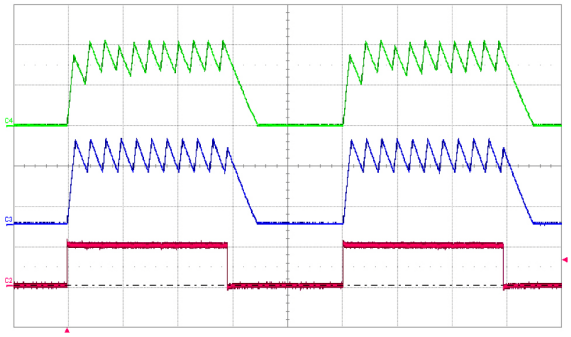
3.5 GATE Output

The GATE output of HV9861A is used to drive an external MOSFET. The gate charge, Q_G, of the external MOSFET should be less than 25nC for switching frequencies ≤100kHz and less than 15nC for switching frequencies >100kHz.

3.6 PWM Dimming

Due to the fast open-loop response of the average-mode, current-control loop of the HV9861A, the PWM dimming performance nearly matches that of the HV9910B. The inductor current waveform comparison is shown in Figure 3-4.

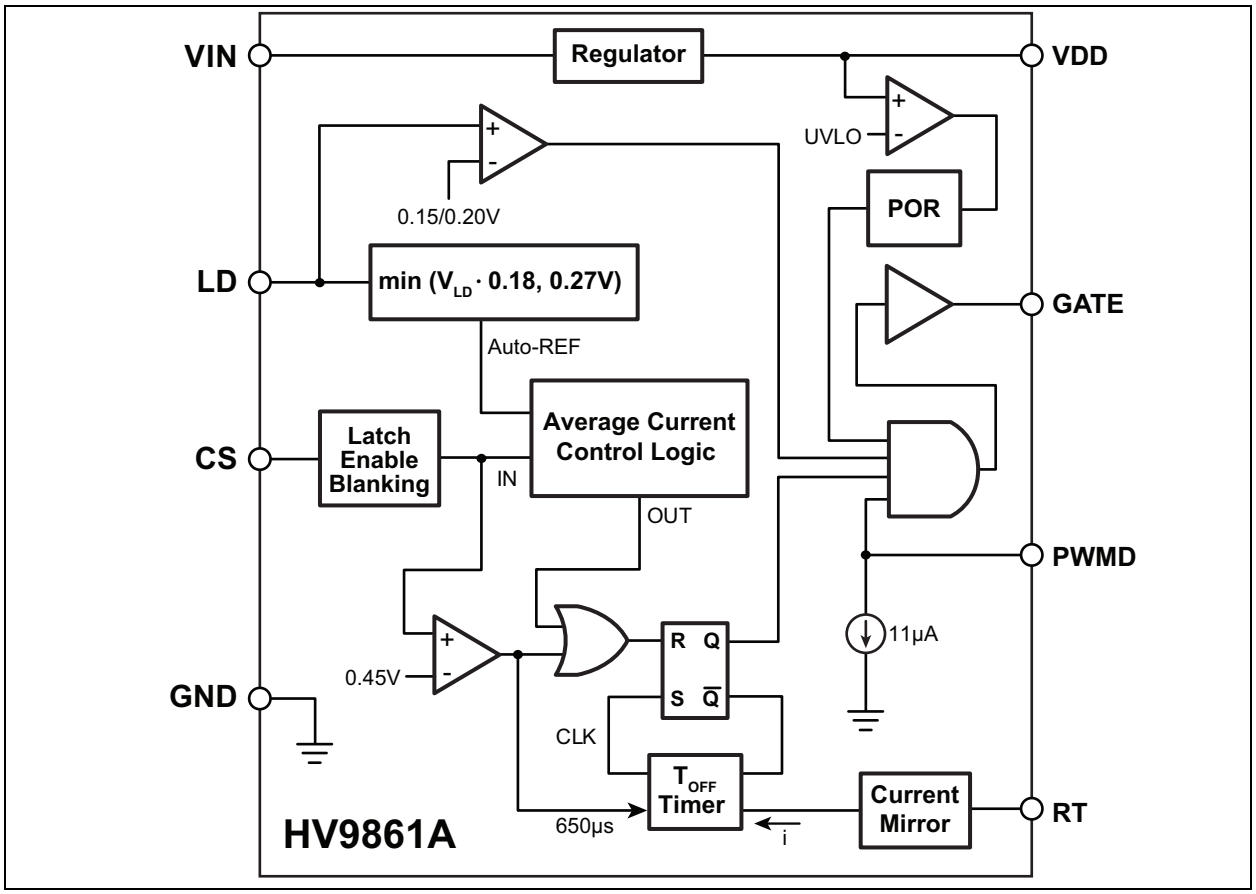
FIGURE 3-4: TYPICAL PWM DIMMING RESPONSE OF AN HV9861A LED DRIVER



CH2 (red): PWMD
CH4 (green): Inductor Current
CH3 (blue): Same as HV9910B, for comparison

The rising and falling edges are limited by the current slew rate in the inductor. The first switching cycle is terminated upon reaching the 270mV (V_{LD} • 0.18) level at CS. The circuit is further reaching its steady-state within 3–4 switching cycles regardless of the switching frequency.

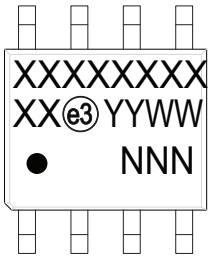
FIGURE 3-5: FUNCTIONAL BLOCK DIAGRAM



4.0 PACKAGING INFORMATION

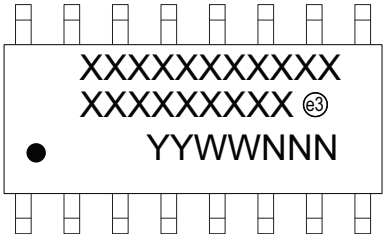
4.1 Package Marking Information

8-lead SOIC



Example

16-lead SOIC



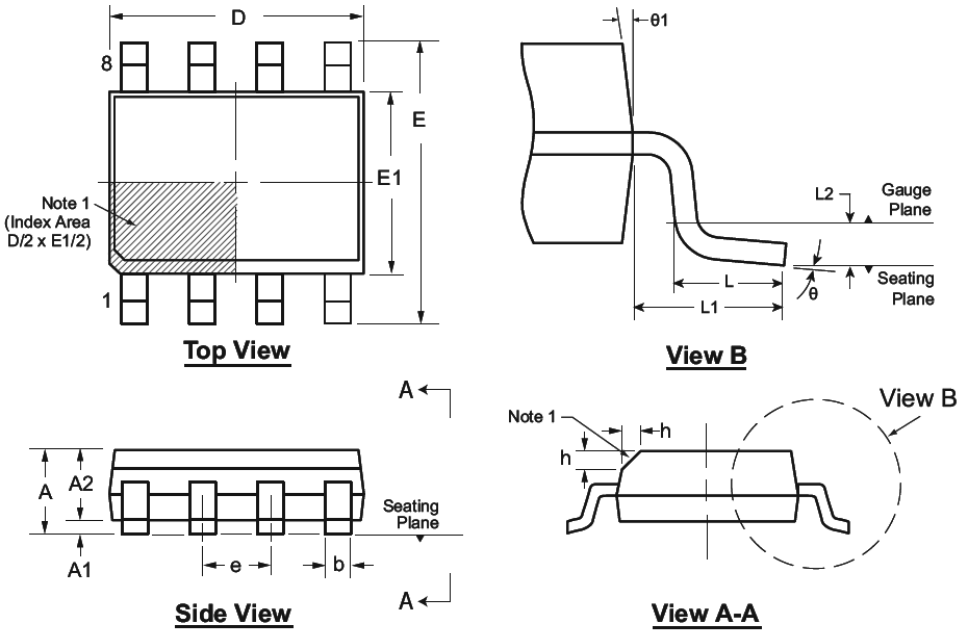
Example

Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

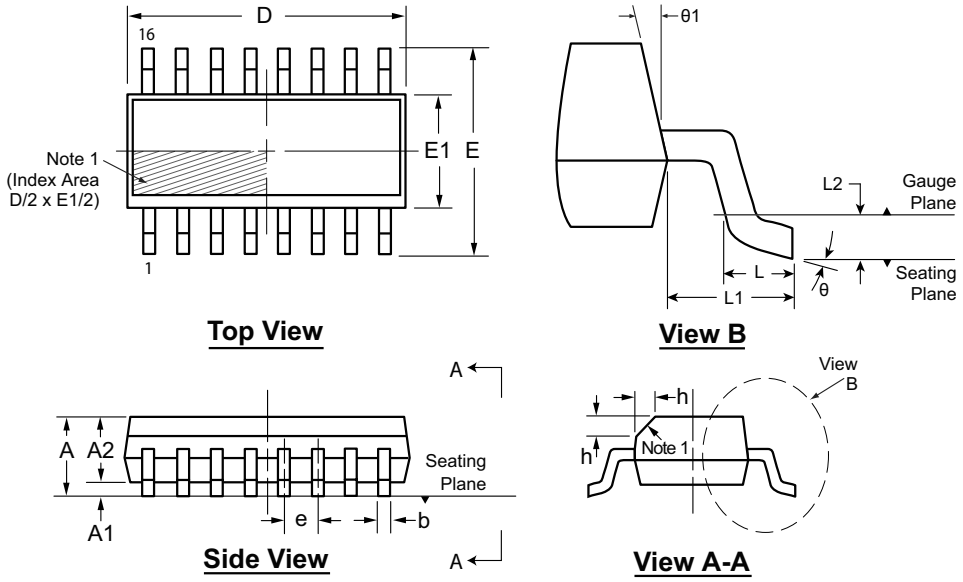
1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.

16-Lead SOIC (Narrow Body) Package Outline (NG)

9.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	9.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	9.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	10.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AC, Issue E, Sept. 2005.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (December 2014)

- Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HV9861A=	LED Driver with Average-Mode Constant Current Control
Package:	LG	= 8-lead SOIC
	NG	= 16-lead SOIC
Environmental	G	= Lead (Pb)-free/ROHS-compliant package
Media Type:	(blank)	= Reel for LG package, Tube for NG package

Examples:

a) HV9861ALG-G: 8-lead SOIC package, 2500/Reel.

b) HV9861ANG-G 16-lead SOIC package, 45/Tube

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Korea - Daegu
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Korea - Seoul
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Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
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Philippines - Manila
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