



75 dB LOGARITHMIC DETECTOR / CONTROLLER 50 - 4000 MHz

Electrical Specifications, (continued)

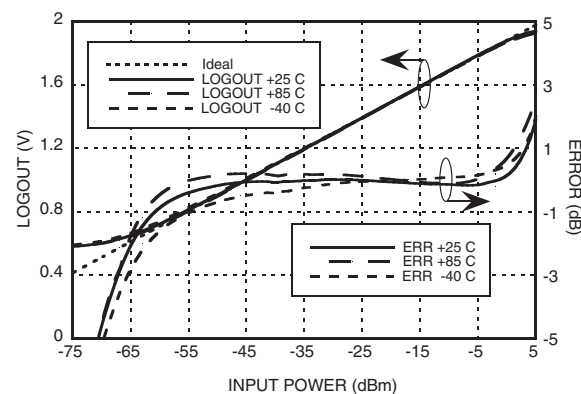
Parameter	Conditions	Min.	Typ.	Max.	Units
Current Drive (Sink)	For 1% change in the output voltage		2.25		mA
Output Voltage Range		0		V _{CC} - 0.13	V
Small Signal Response Time (10% to 90%)	Pin = -60 to -57 dBm		50		ns
Large Signal Response Time (±0.5 dB Settling)	Pin = No Signal to 0 dBm		150		ns
Output Rise Time	From 0% to 90%		90		ns
Ripple	Fin = 100 MHz		<2		mVpp
VSET Interface					
Input Impedance			30		kΩ
Input Voltage Range			0.6 to 1.9		V
Low Frequency Gain	VSET to LOGOUT		78		dB
Open Loop Corner Frequency			1.6		kHz
Power Down (PWD) Interface					
Voltage Range for Normal Mode		0		0.2 x V _{CC}	V
Voltage Range for Shutdown Mode		0.8 x V _{CC}		V _{CC}	V
Threshold Voltage			V _{CC} /2		V
Power-up Response Time	50% PWD to ±0.5 dB Settling of LOGOUT		1		μs
Power-Down Response Time	50% PWD to 10% I _{CC}		2.5		μs
Power Supply (V_{CC1}, V_{CC2})					
Operating Voltage Range		2.7		5.5	V
Supply Current in Normal Mode	V _{CC} = +3.3V, PWD = 0V		29	36	mA
Supply Current in Power Down Mode	V _{CC} = +3.3V, PWD = V _{CC}		1		mA

Test Conditions

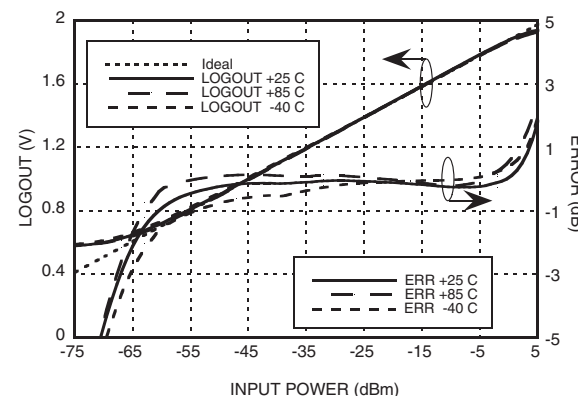
Parameter	Condition
V _{CC1} , V _{CC2}	+3.3V
Input Z ₀	50Ω
T _A	+25°C
Fin	900 MHz

INN Port connected to ground through a 1000pF capacitor

LOGOUT Voltage & Error vs. Input Power, Fin = 50 MHz



LOGOUT Voltage & Error vs. Input Power, Fin = 100 MHz



Unless otherwise noted: V_{CC1}, V_{CC2} = +3.3V, T_A = +25°C

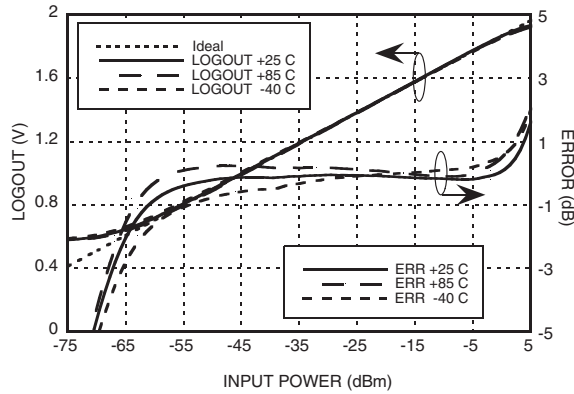
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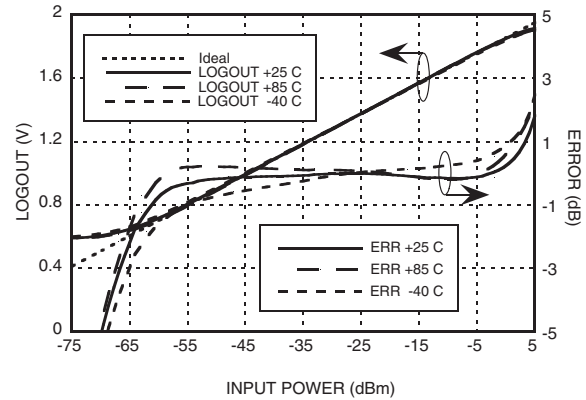


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DETECTOR / CONTROLLER 50 - 4000 MHz**

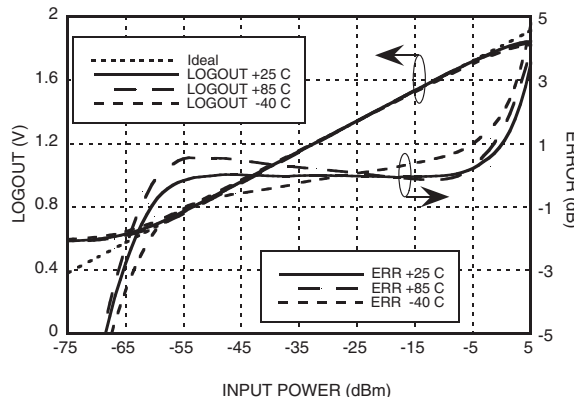
**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 500$ MHz**



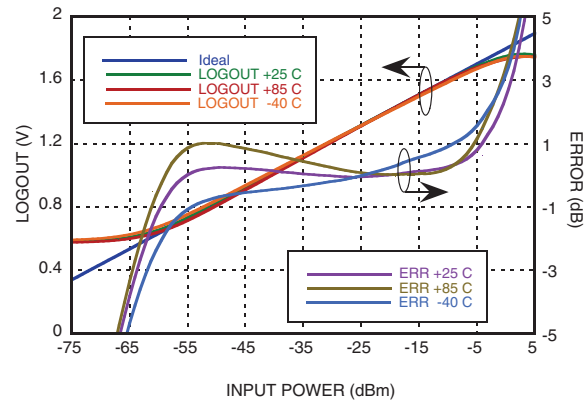
**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 900$ MHz**



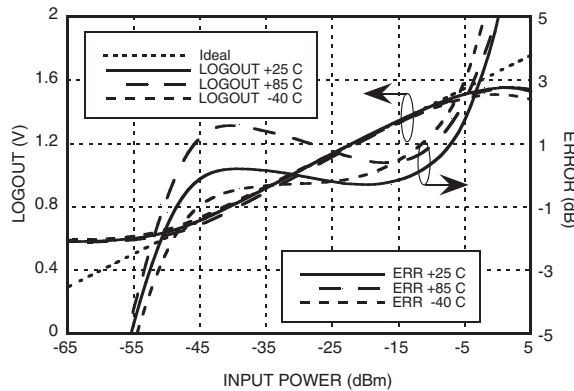
**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 1900$ MHz**



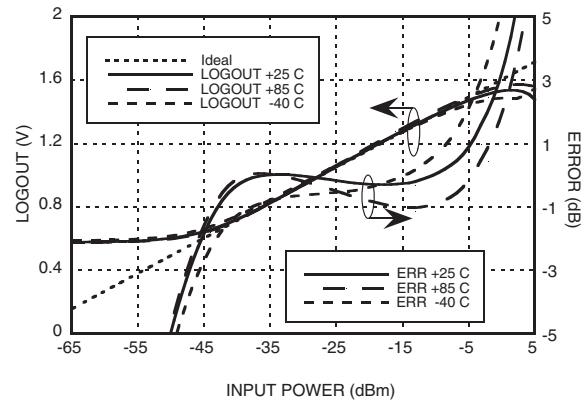
**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 2500$ MHz**



**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 3500$ MHz**



**LOGOUT Voltage & Error
vs. Input Power, $f_{in} = 4000$ MHz**



Unless otherwise noted: V_{cc1} , $V_{cc2} = +3.3V$, $T_A = +25C$

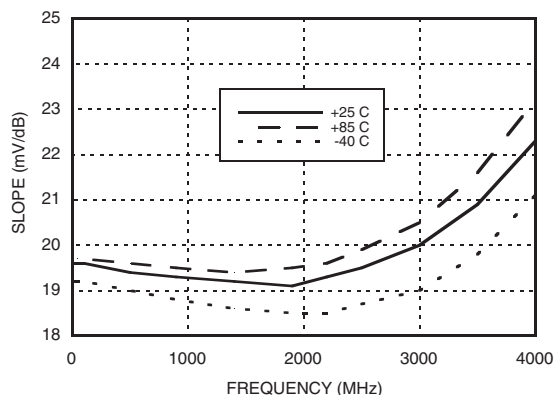
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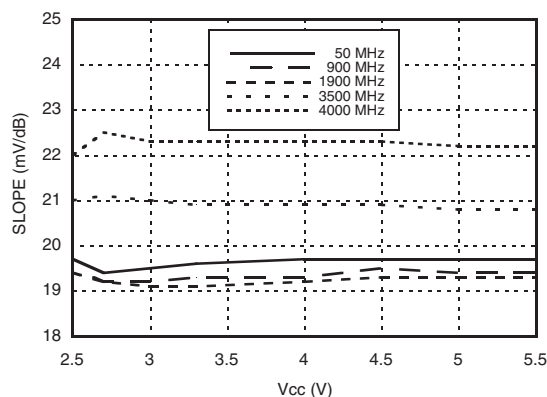


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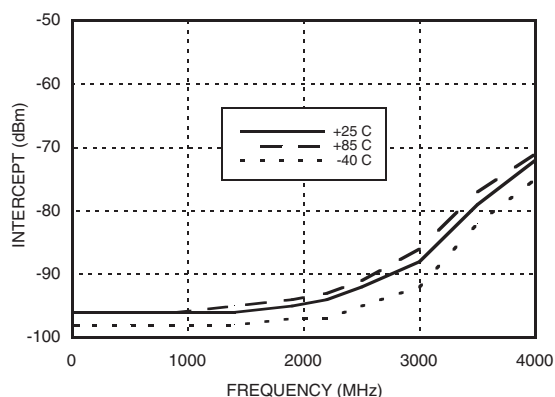
LOGOUT Slope vs. Frequency,
V_{CC} = 3.3V



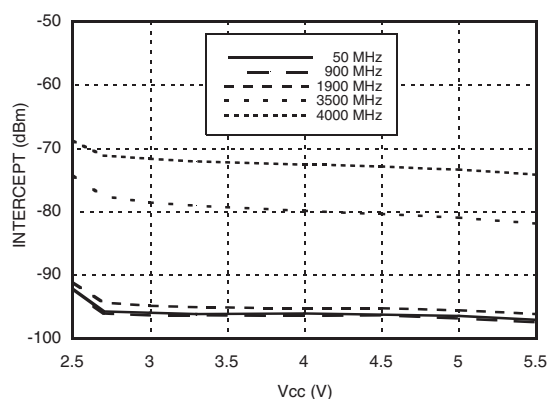
LOGOUT Slope vs. Supply Voltage,
T_A = +25°C



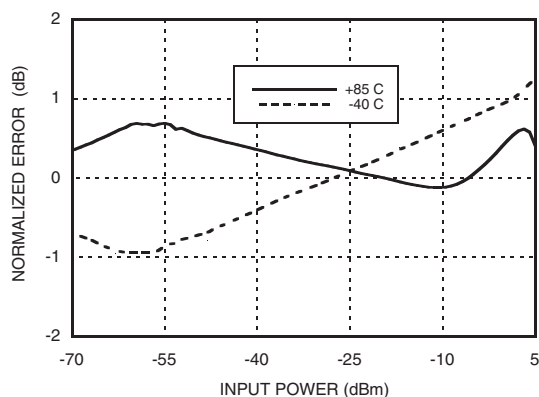
LOGOUT Intercept vs. Frequency,
V_{CC} = +3.3V



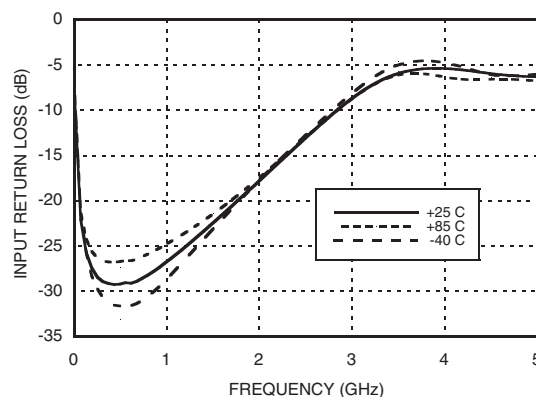
LOGOUT Intercept vs. Bias Voltage
T_A = +25°C



LOGOUT Error vs. Input Power,
Normalized^[2], F_{in} = 1900 MHz



Input Return Loss



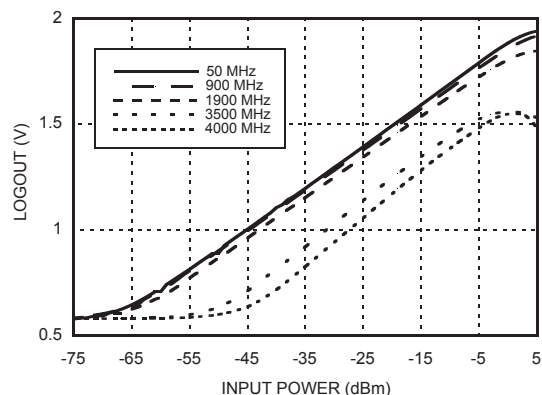
[1] Unless otherwise noted: V_{CC1}, V_{CC2} = +3.3V, T_A = +25°C

[2] This data is relative to the room temperature performance of the HMC600LP4



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LOGOUT Voltage vs. Input Power and Frequency, $T_A = +25^\circ\text{C}$



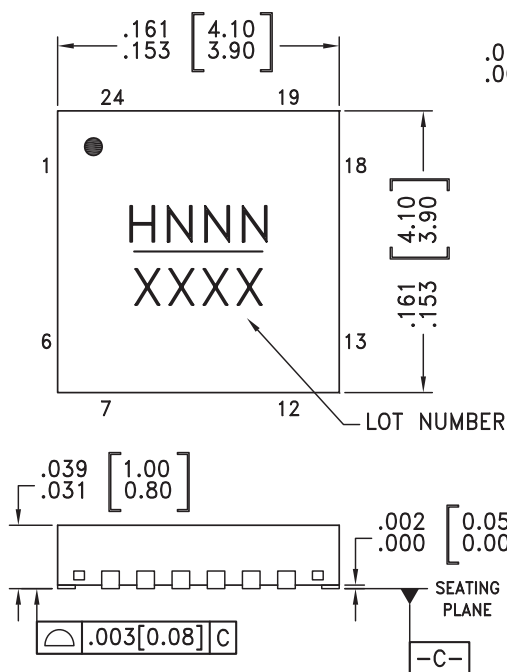
Absolute Maximum Ratings

Vcc1, Vcc2	0V to +5.5V
PWD	0V to +5.5V
VSET Input Voltage	0V to +5.5V
LOGOUT Output Current	3 mA
RF Input Power	+12 dBm
Junction Temperature	125 °C
Continuous P _{diss} (T = 85°C) (Derate 7.95 mW/°C above 85°C)	0.32 Watts
Thermal Resistance (R _{th}) (junction to lead)	126 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

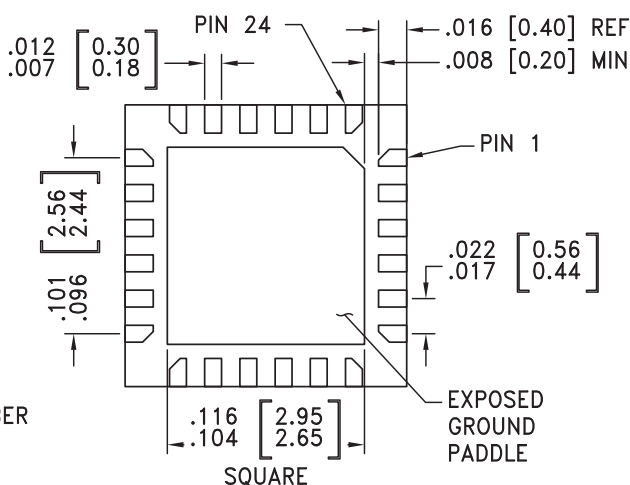


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



BOTTOM VIEW



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Unless otherwise noted: Vcc1, Vcc2 = +3.3V, $T_A = +25^\circ\text{C}$

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Package Information

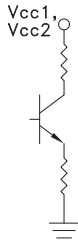
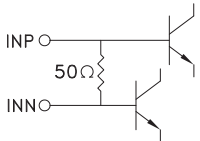
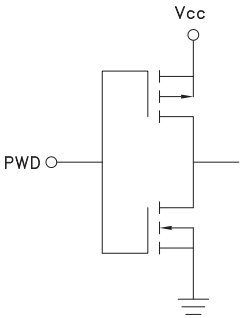
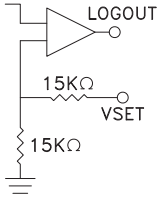

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC600LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 ^[1]	H600 XXXX
HMC600LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H600 XXXX

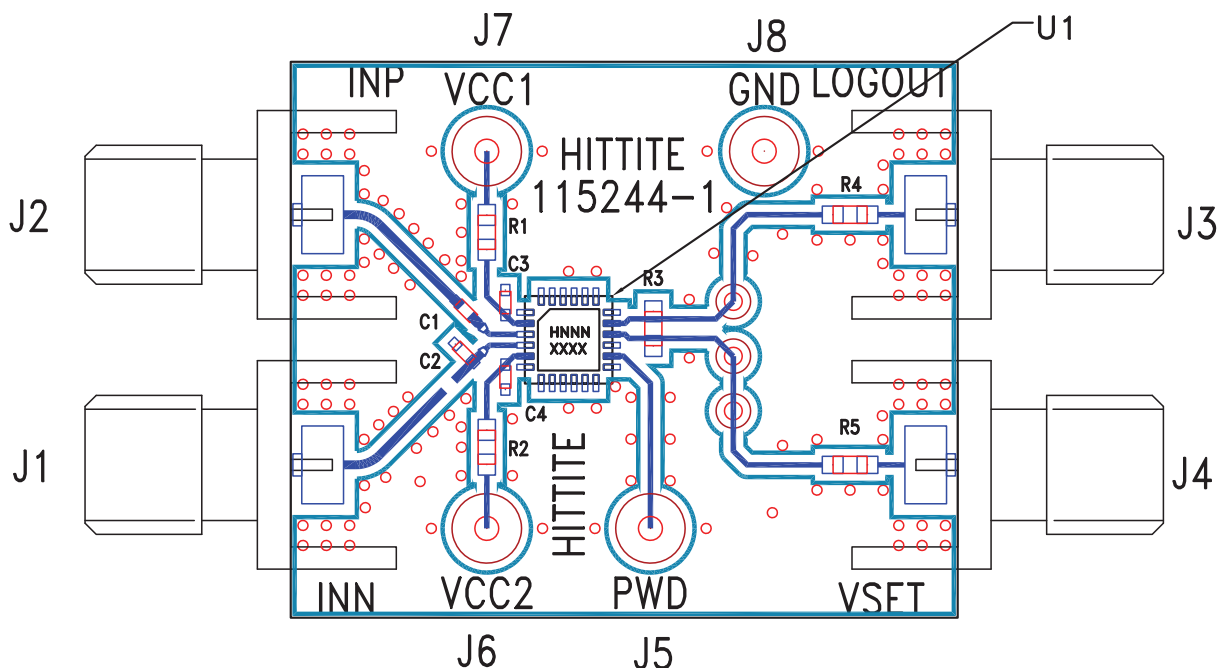
[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7-13, 15, 18-24	N/C	These pins are not connected internally; however, this product is specified with these pins connected to RF/DC ground.	
2, 6	Vcc1, Vcc2	Bias supply. Connect supply voltage to both pins.	
3, 4	INP, INN	RF Input pins. Connect RF to INP, and AC couple INN to ground for single-ended operation.	
14	PWD	Connect to 0V for normal operation. Applying voltage >0.8 x Vcc will initiate a power saving shutdown mode. To ensure proper start-up apply the power-up sequence shown in the "Power-Up Timing Diagram" attached to the application circuit.	
16	VSET	VSET input in controller mode. Short this pin to LOGOUT for detector mode.	
17	LOGOUT	Logarithmic output that converts the input power to a DC level in detector mode. Short this pin to VSET for detector mode.	
Package Base	GND	Exposed paddle must be connected to RF and DC ground.	


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Evaluation PCB

List of Materials for Evaluation PCB 115242 [1]

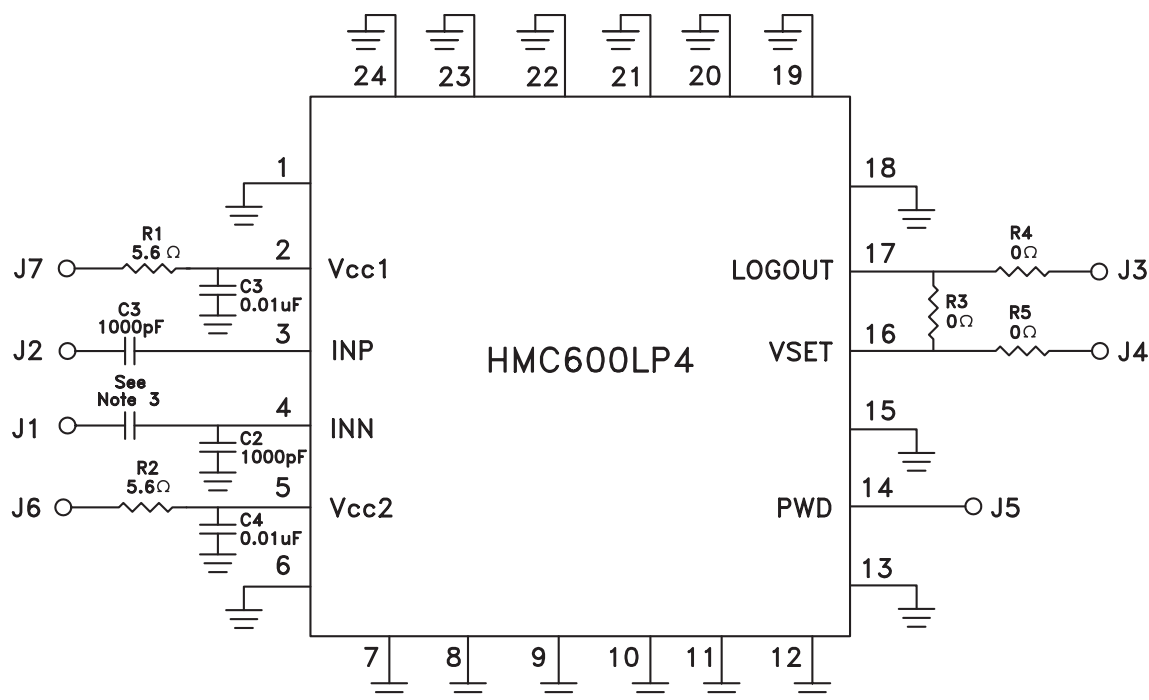
Item	Description
J1 - J4	PC Mount SMA Connector
J5 - J8	DC Pin
C1, C2	1000 pF Capacitor, 0402 Pkg.
C3, C4	0.1µF Capacitor, 0402 Pkg.
R1, R2	5.6Ω Resistor, 0603 Pkg.
R3-R5	0Ω Resistor, 0603 Pkg.
U1	HMC600LP4 / HMC600LP4E Logarithmic Detector / Controller
PCB [2]	115244 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application & Evaluation PCB Schematic



Notes

Note 1: The HMC600LP4 & HMC600LP4E evaluation boards are pre-assembled for single-ended input, and detector/RSSI mode.

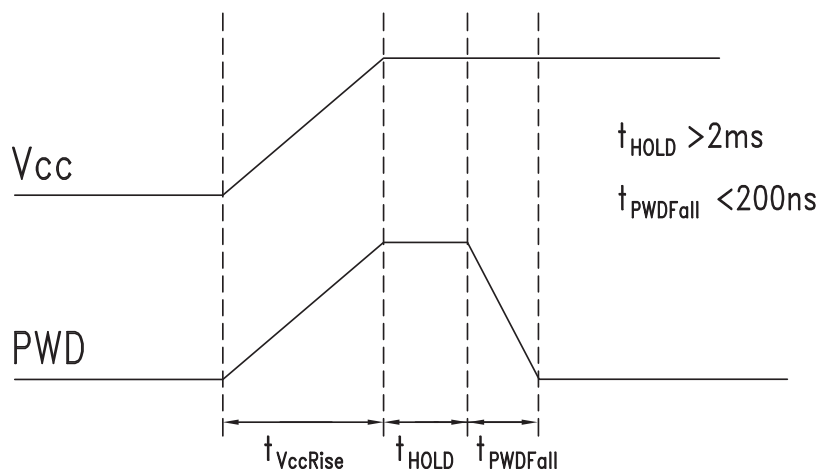
Note 2: For single-ended input operation, use the INP port and make no connection to INN. INN is AC coupled to ground by C2

Note 3: For differential input, remove C2, and install a 1000pF capacitor in series with INN at location shown.

Note 4: For detector mode, connect high impedance volt meter to the LOGOUT port, and make no connection to VSET. LOGOUT is shorted to VSET by R3, as required for detector mode.

Note 5: For controller mode, remove R3 and make appropriate connection to LOGOUT and VSET. In controller mode, the LOGOUT output can be used to drive a variable gain amplifier, or a variable attenuator, either directly or through a buffer or microcontroller. VSET should be connected to an external supply, typically between +0.6 and +1.9V.

Power-Up Timing Diagram



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