

August 2014

# FCP16N60 / FCPF16N60 N-Channel SuperFET<sup>®</sup> MOSFET 600 V, 16 A, 260 m $\Omega$

#### **Features**

- 650V @ T<sub>J</sub> = 150°C
- Typ.  $R_{DS(on)}$  = 220  $m\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 55 \text{ nC}$  )
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 110 pF )
- 100% Avalanche Tested

### **Applications**

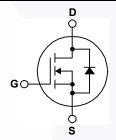
- · Solar Inverter
- AC-DC Power Supply

# Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low onresistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.







# **Absolute Maximum Ratings**

Symbol		Parameter		FCP16N60	FCPF16N60	Unit
$V_{DSS}$	Drain-Source Volta	age		6	00	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)		16 10.1	16* 10.1*	A A
I <sub>DM</sub>	Drain Current	- Pulsed	(Note 1)	48	48*	Α
$V_{GSS}$	Gate-Source Voltage			± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy		(Note 2)	450		mJ
I <sub>AR</sub>	Avalanche Current		(Note 1)	16		Α
E <sub>AR</sub>	Repetitive Avalance	che Energy	(Note 1)	2	0.8	mJ
dv/dt	Peak Diode Recov	/ery dv/dt	(Note 3)	4	1.5	V/ns
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C) - Derate Above 25°C		167 1.33	37.9 0.3	W/°C
T <sub>J,</sub> T <sub>STG</sub>	Operating and Sto	rage Temperature Range		-55 to	+150	°C
T <sub>L</sub>	Maximum Lead Te 1/8" from Case for	emperature for Soldering, 5 Seconds		3	00	°C

<sup>\*</sup>Drain current limited by maximum junction temperature.

#### Thermal Characteristics

Symbol	Parameter	FCP16N60	FCPF16N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.75	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

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# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP16N60	FCP16N60	TO-220	Tube	N/A	N/A	50 units
FCPF16N60	FCPF16N60	TO-220F	Tube	N/A	N/A	50 units

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
D\/	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	600	-	-	V
BV <sub>DSS</sub>	Drain to Source Breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 150^{\circ} C$	-	650	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	-	0.6	-	V/°C
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 16 A	_	700	-	V
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	-	-	1	
IDSS	Zero Gate voltage Drain Current	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	-	10	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

#### **On Characteristics**

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$	-	0.55	0.26	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 40 V, I <sub>D</sub> = 8 A	-	11.5	-	S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 05.V V 0.V	-	1730	2250	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1  MHz	-	960	1150	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1011 12	-	85	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	45	60	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	110	-	pF
Qg	Total Gate Charge at 10V	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 16 A,	-	55	70	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>GS</sub> = 10 V	-	10.5	13	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	(Note 4)	-	28	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-/	1.7	-	Ω

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	42	85	ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 16 A,	-	130	270	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS}$ = 10 V, $R_G$ = 25 $\Omega$	-	165	340	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	90	190	ns

#### **Drain-Source Diode Characteristics**

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	16	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current			-	48	Α
$V_{SD}$	Drain to Source Diode Forward Voltage V <sub>GS</sub> =	= 0 V, I <sub>SD</sub> = 16 A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time V <sub>GS</sub> =	= 0 V, I <sub>SD</sub> = 16 A,	-	435	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge dI <sub>F</sub> /dt	t = 100 A/μs	-	7.0	-	μC

#### Notes:

- ${\it 1:} \ \ {\it Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$
- 2:  $I_{AS}$  = 8 A,  $V_{DD}$  = 50 V,  $R_G$  = 25  $\Omega$ , starting  $T_J$  = 25°C.
- 3:  $I_{SD} \le 16$  A, di/dt  $\le 200$  A/ $\mu$ s,  $V_{DD} \le BV_{DSS}$ , starting  $T_J = 25^{\circ}C$ .
- 4: Essentially independent of operating temperature typical characteristics.

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

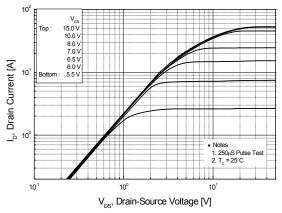


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

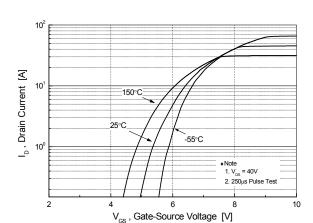
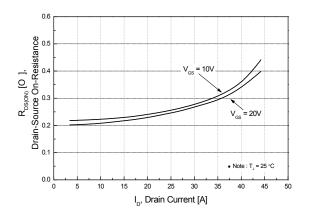


Figure 2. Transfer Characteristics

Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue



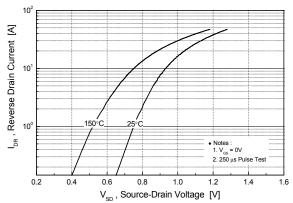


Figure 5. Capacitance Characteristics

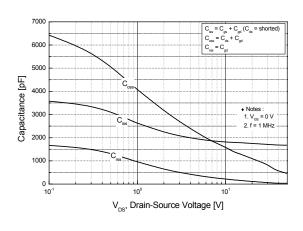
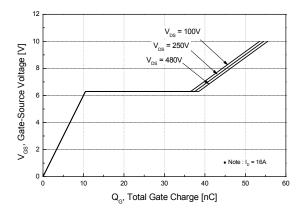


Figure 6. Gate Charge Characteristics



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# **Typical Performance Characteristics** (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

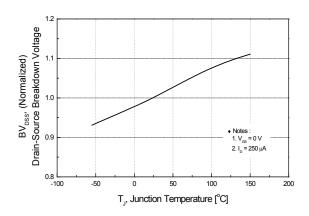


Figure 8. On-Resistance Variation vs. Temperature

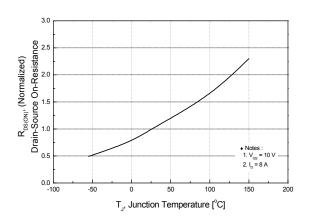
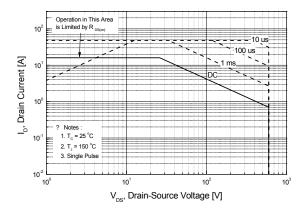


Figure 9-1. Maximum Safe Operating Area for FCP16N60





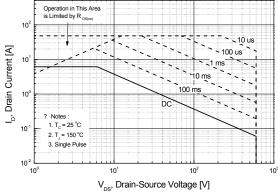
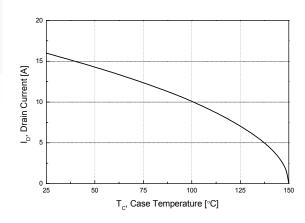


Figure 10. Maximum Drain Current vs. Case Temperature



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# **Typical Performance Characteristics** (Continued)

Figure 11-1. Transient Thermal Response Curve for FCP16N60

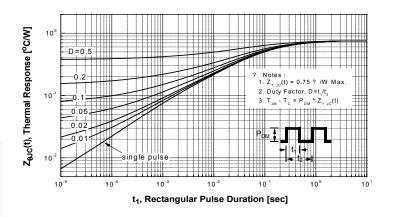
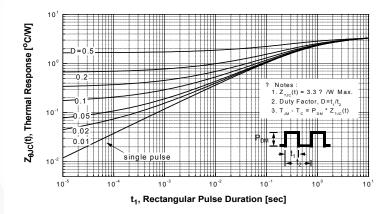


Figure 11-2. Transient Thermal Response Curve for FCPF16N60



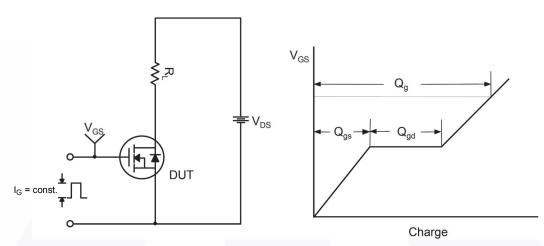


Figure 12. Gate Charge Test Circuit & Waveform

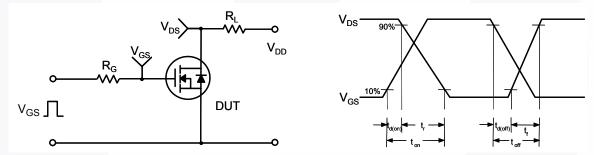


Figure 13. Resistive Switching Test Circuit & Waveforms

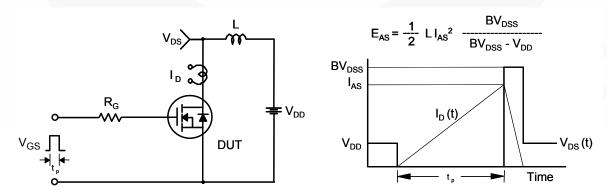


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

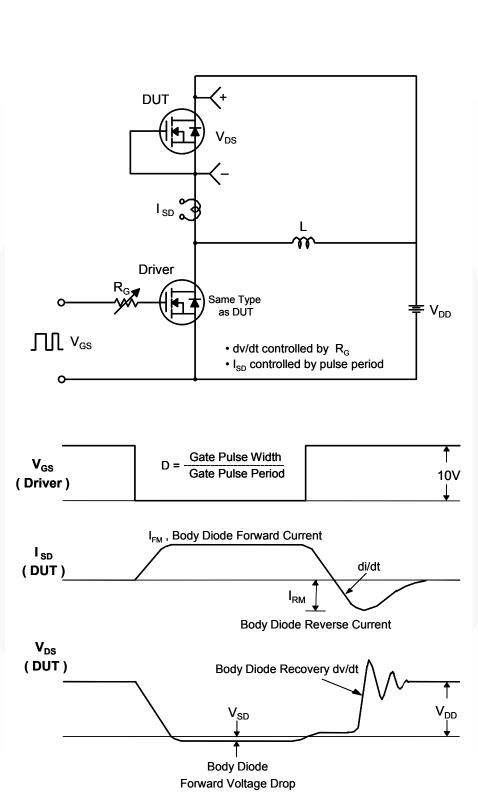
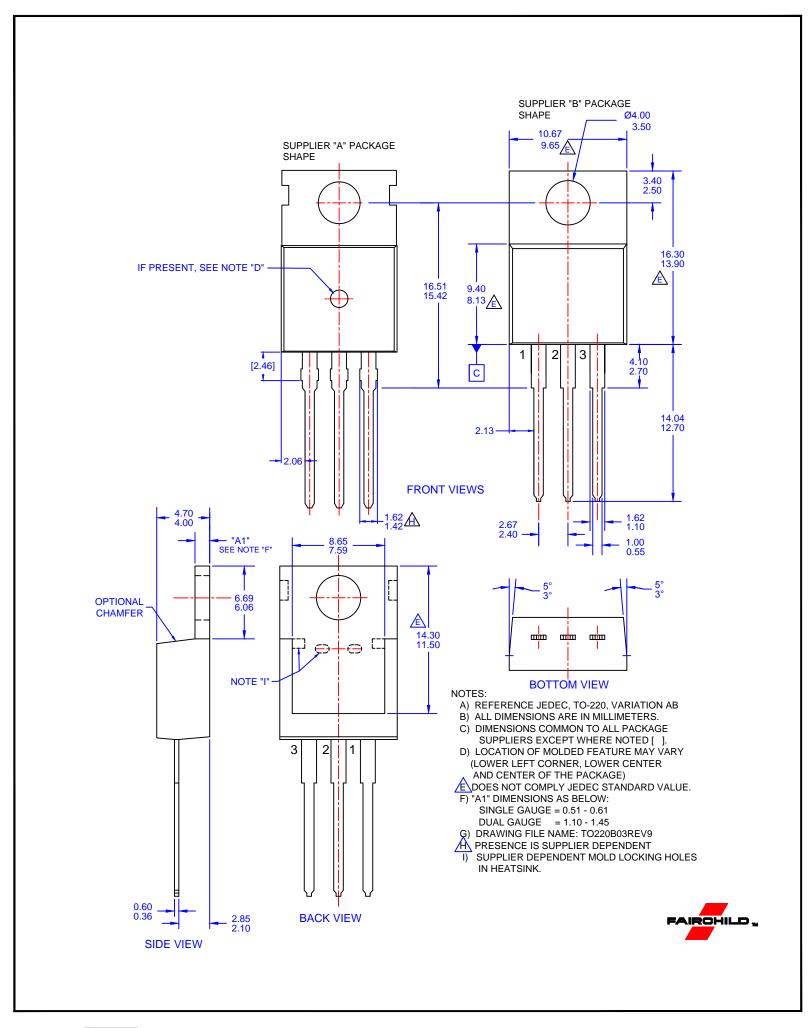
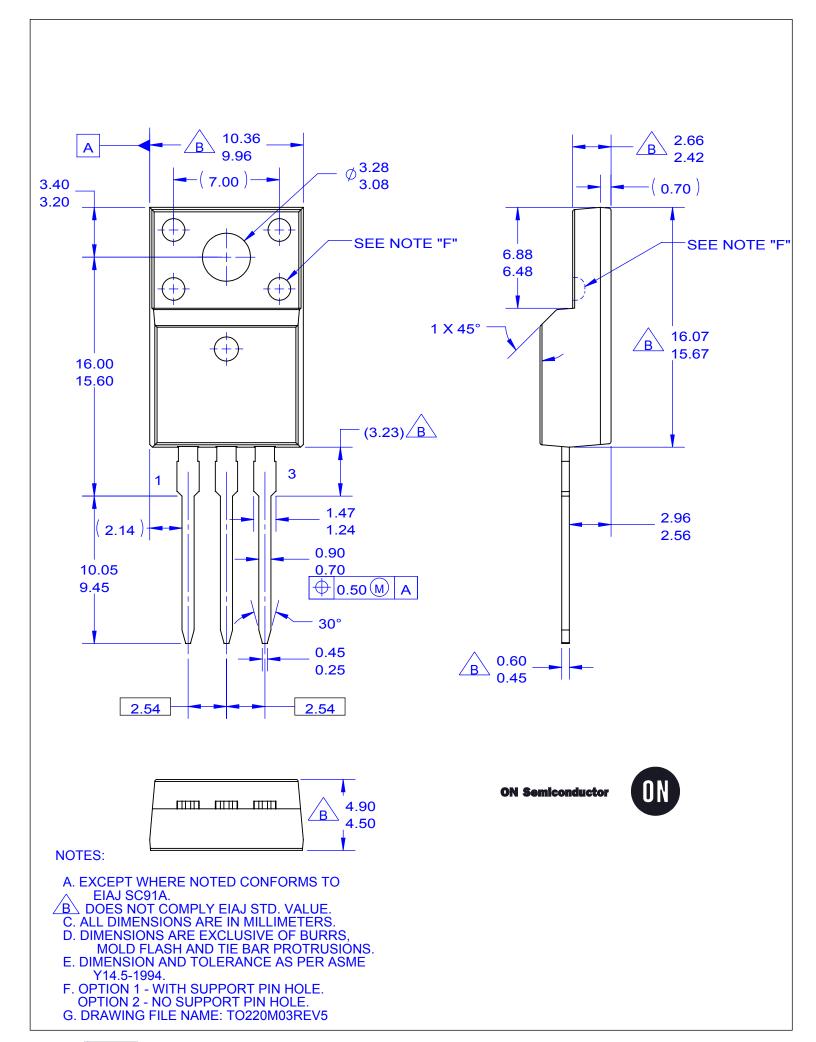


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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