# 1        Characteristics

**Figure 1. Functional diagram**
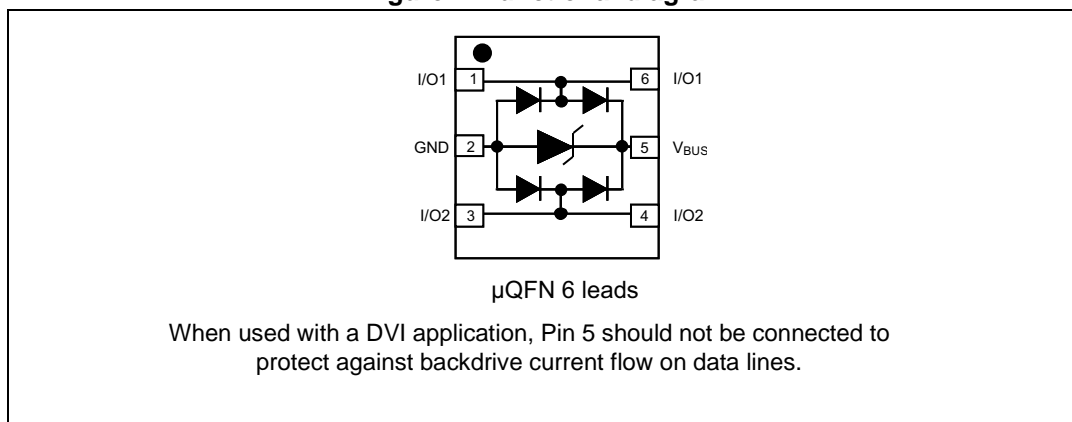


μQFN 6 leads

When used with a DVI application, Pin 5 should not be connected to
protect against backdrive current flow on data lines.

**Table 1. Absolute ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{PP}$ | Peak pulse voltage | IEC61000-4-2 air discharge<br>IEC61000-4-2 contact discharge<br>MIL STD883G-Method 3015-7 | ±15<br>±15<br>±25 | kV |
| $T_{stg}$ | Storage temperature range | | -55 to +150 | °C |
| $T_j$ | Maximum junction temperature | | 125 | °C |
| $T_L$ | Lead solder temperature (10 seconds duration) | | 260 | °C |

**Table 2. Electrical characteristics ($T_{amb}$ = 25 °C)**

| Symbol | Parameter | Test Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max | |
| $I_{RM}$ | Leakage current | $V_{RM}$ = 5 V | | | 0.5 | μA |
| $V_{BR}$ | Breakdown voltage between $V_{BUS}$ and GND | $I_R$ = 1 mA | 6 | | | V |
| $V_{CL}$ | Clamping voltage | $I_{PP}$ = 1 A, $t_p$ = 8/20 μs<br>Any I/O pin to GND | | | 12 | V |
| | | $I_{PP}$ = 5 A, $t_p$ = 8/20 μs<br>Any I/O pin to GND | | | 17 | V |
| $C_{i/o\text{-}GND}$ | Capacitance between I/O and GND | $V_R$ = 0 V, F= 825 MHz | | | 0.85 | pF |
| $\Delta C_{i/o\text{-}GND}$ | Capacitance variation between I/O and GND | $V_R$ = 0 V, F= 1 MHz | | 0.02 | | pF |
| $C_{i/o\text{-}i/o}$ | Capacitance between I/O | $V_R$ = 0 V, F= 825 MHz | | | 0.5 | pF |

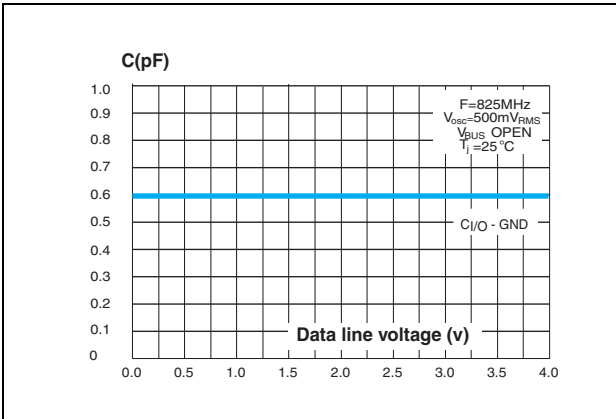### Figure 2. Line capacitance versus line voltage (typical values)



### Figure 3. Line capacitance versus frequency (typical values) DVIULC6-2M6
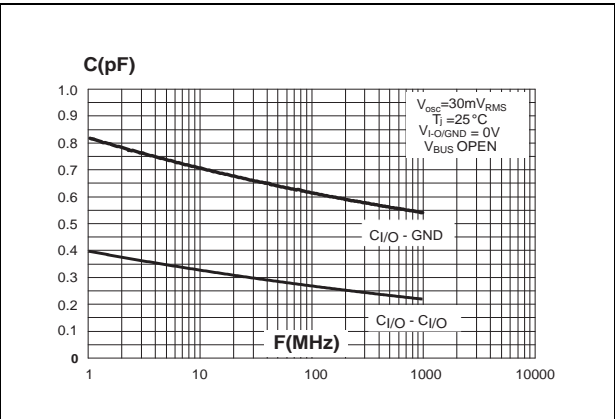


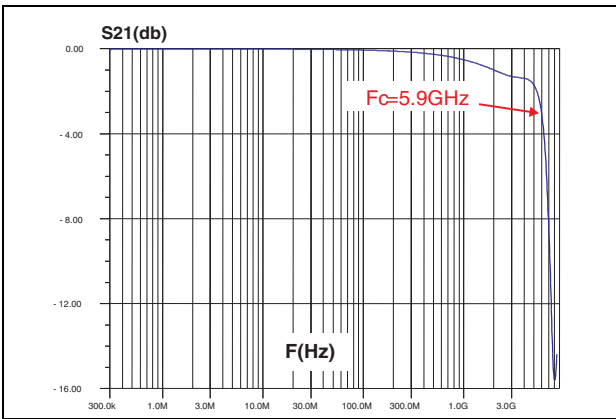### Figure 4. Frequency response (typical values) DVIULC6-2M6



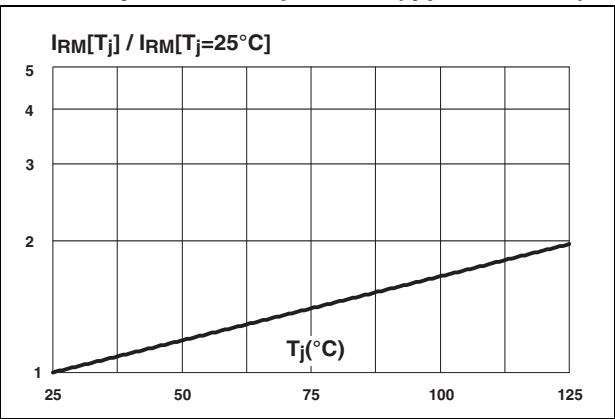### Figure 5. Relative variation of leakage current versus junction temperature (typical values)



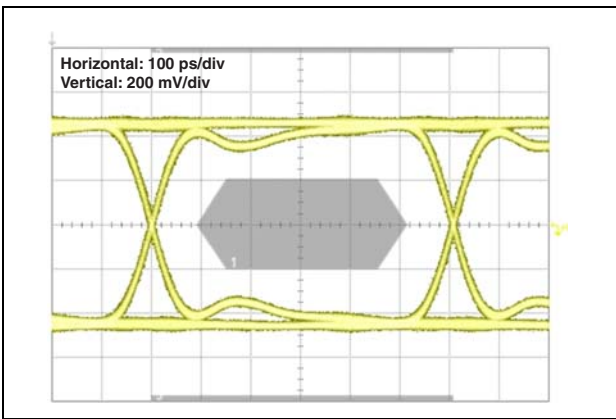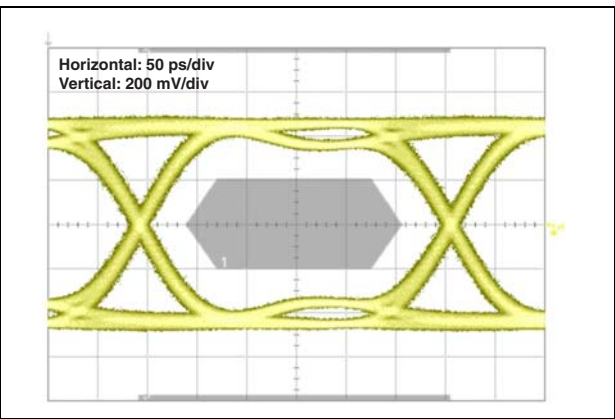### Figure 6. Eye diagram at 1.65 Gbps amplitude 500 mV PCB + DVIULC6-2M6



### Figure 7. Eye diagram at 3.2 Gbps amplitude 500 mV PCB + DVIULC6-2M6

# 2 Application examples
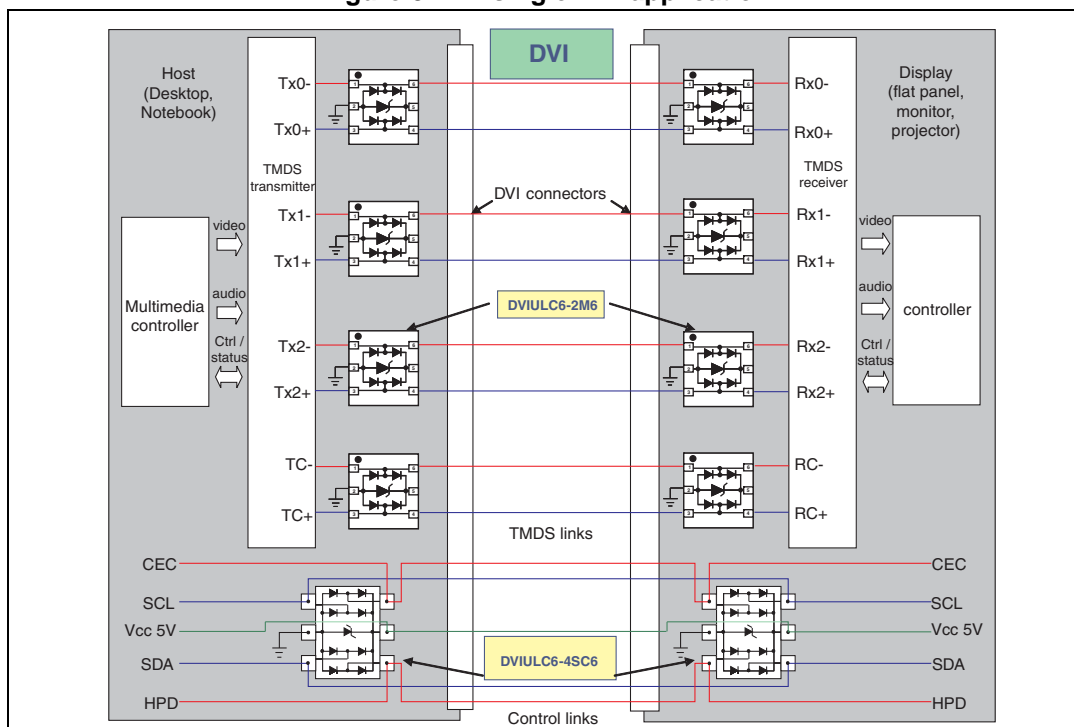
**Figure 8. DVI single link application**



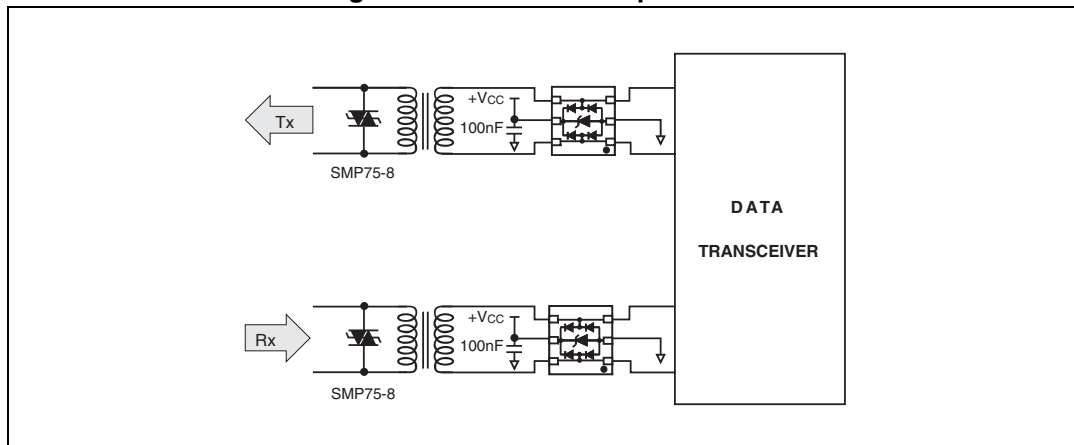**Figure 9. T1/E1/Ethernet protection**

## 2.1 PCB layout considerations

**Figure 10. PCB layout example**



Width=100 μm
Space=400 μm

All dimensions in μm

Width=215μm
Space=100μm
$Z_0$diff=100 Ω

3160

3160

**PCB Characteristics**
Substrate: H = 730 m, Er =3.9
Tracks: H = 35 μm copper
Coatinbg: H = 35 μm above substrate: H = 10 μm above tracks, Er = 3.4
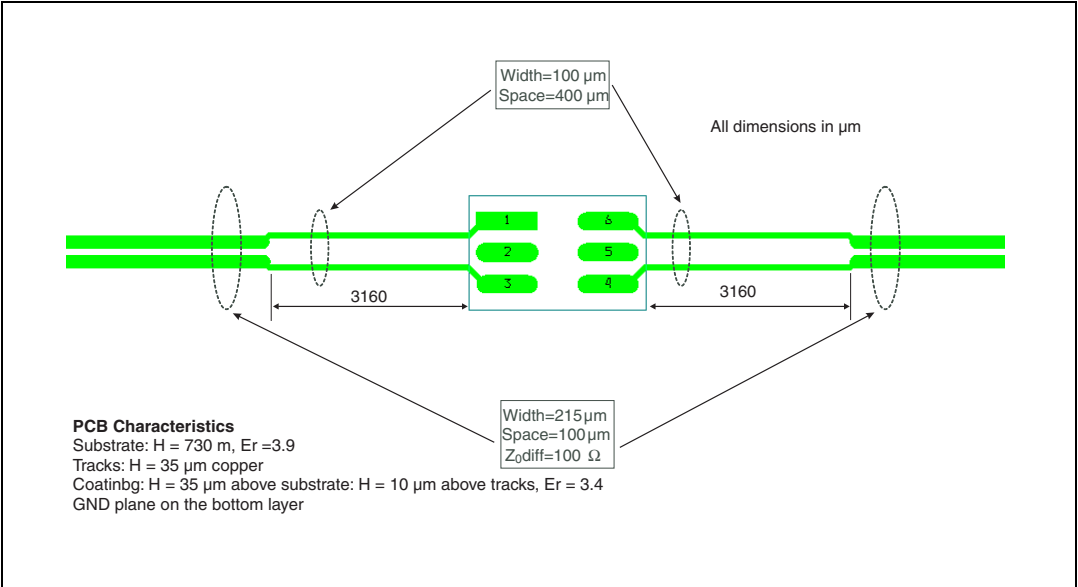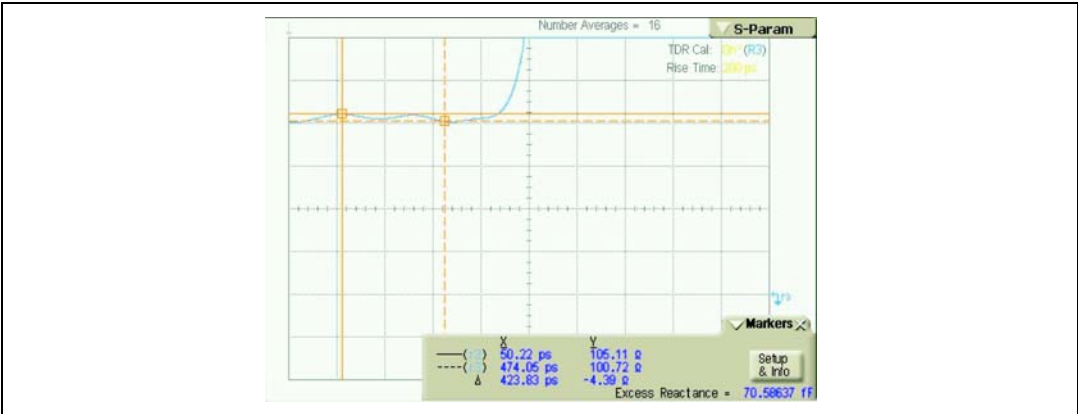GND plane on the bottom layer

**Figure 11. TDR results for DVIULC6-2M6 with PCB layout example**

# 3 Technical information

## 3.1 Surge protection

The DVIULC6-2M6 is particularly optimized to perform ESD surge protection based on the rail to rail topology.

The clamping voltage $V_{CL}$ can be calculated as follows:

$$V_{CL}+ = V_{TRANSIL} + V_F \quad \text{for positive surges}$$

$$V_{CL}- = - V_F \quad \quad \quad \text{for negative surges}$$

with: $V_F = V_T + R_d.I_p$

($V_F$ forward drop voltage) / ($V_T$ forward drop threshold voltage)

and $V_{TRANSIL} = V_{BR} + R_{d\_TRANSIL} \cdot I_P$

**Calculation example**

We assume that the value of the dynamic resistance of the clamping diode is typically: $R_d = 0.5 \ \Omega$ and $V_T = 1.1$ V.

We assume that the value of the dynamic resistance of the transil diode is typically $R_{d\_TRANSIL} = 0.5 \ \Omega$ and $V_{BR} = 6.1$ V

For an IEC 61000-4-2 surge Level 4 (Contact Discharge: $V_g$= 8 kV, $R_g$= 330 $\Omega$), $V_{BUS}$ = +5 V, and, in first approximation, we assume that: $I_p = V_g / R_g = 24$ A.

We find:

$$V_{CL}+ = +31.2 \text{ V}$$

$$V_{CL}- = -13.1 \text{ V}$$

*Note:* *The calculations do not take into account phenomena due to parasitic inductances.*

## 3.2 Surge protection application example

If we consider that the connections from the pin $V_{BUS}$ to $V_{CC}$, from I/O to data line, and from GND to PCB GND plane are two tracks 10 mm long and 0.5 mm wide, we can assume that the parasitic inductances, $L_{VBUS}$, $L_{I/O}$, and $L_{GND}$, of these tracks are about 6 nH. So when an IEC 61000-4-2 surge occurs on the data line, due to the rise time of this spike (tr = 1 ns), the voltage $V_{CL}$ has an extra value equal to $L_{I/O}.dI/dt + L_{GND}.dI/dt$.

The dI/dt is calculated as: dI/dt = Ip/tr = 24 A/ns for an IEC 61000-4-2 surge level 4 (contact discharge $V_g$ = 8 kV, $R_g$ = 330 $\Omega$)

The over voltage due to the parasitic inductances is:
$L_{I/O}.dI/dt = L_{GND}.dI/dt = 6 \times 24 = 144$ V

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be:

$$V_{CL}+ = +31.2 + 144 + 144 = 319.2 \text{ V}$$

$$V_{CL}- = -13.1 - 144 - 144 = -301.1 \text{ V}$$

We can reduce as much as possible these phenomena with simple layout optimization.

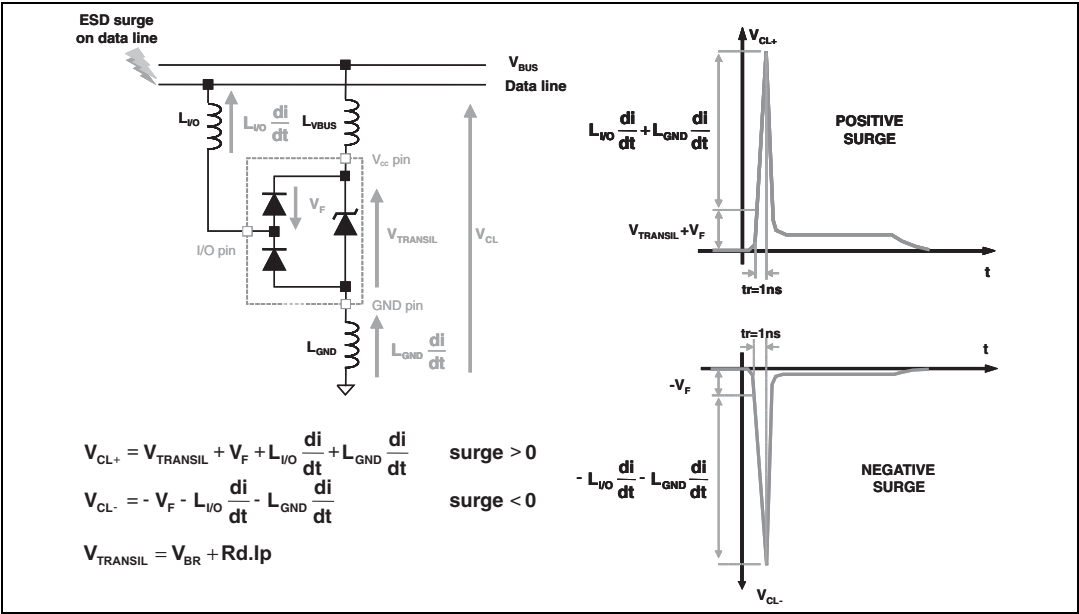**Figure 12. IESD behavior: parasitic phenomena due to unsuitable layout**



$$V_{CL+} = V_{TRANSIL} + V_F + L_{I/O}\frac{di}{dt} + L_{GND}\frac{di}{dt} \qquad \text{surge} > 0$$

$$V_{CL-} = -V_F - L_{I/O}\frac{di}{dt} - L_{GND}\frac{di}{dt} \qquad \text{surge} < 0$$

$$V_{TRANSIL} = V_{BR} + Rd.Ip$$

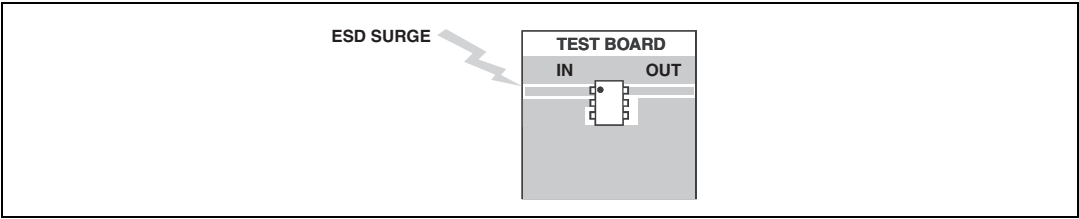**Figure 13. ESD behavior - measurement conditions**



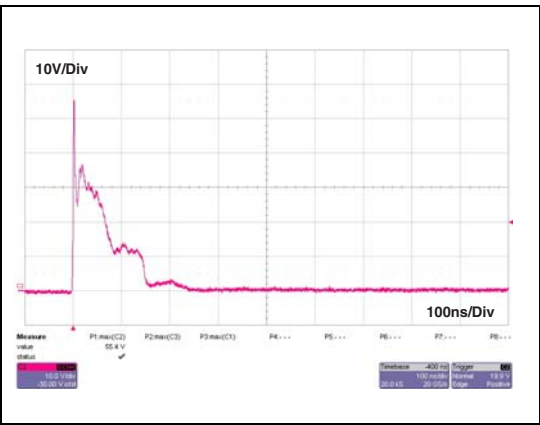**Figure 14. Remaining voltage after the DVIULC6-2M6 during positive ESD surge**

**Figure 15. Remaining voltage after the DVIULC6-2M6 during negative ESD surge**
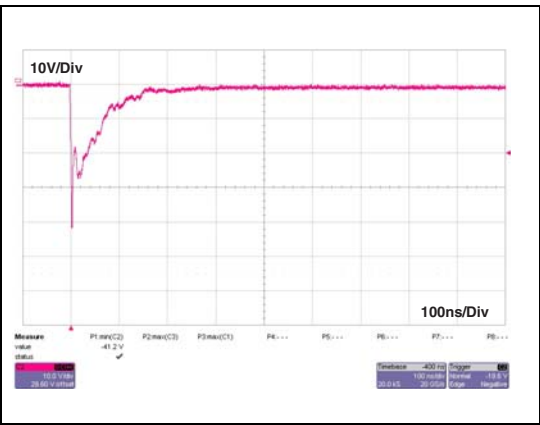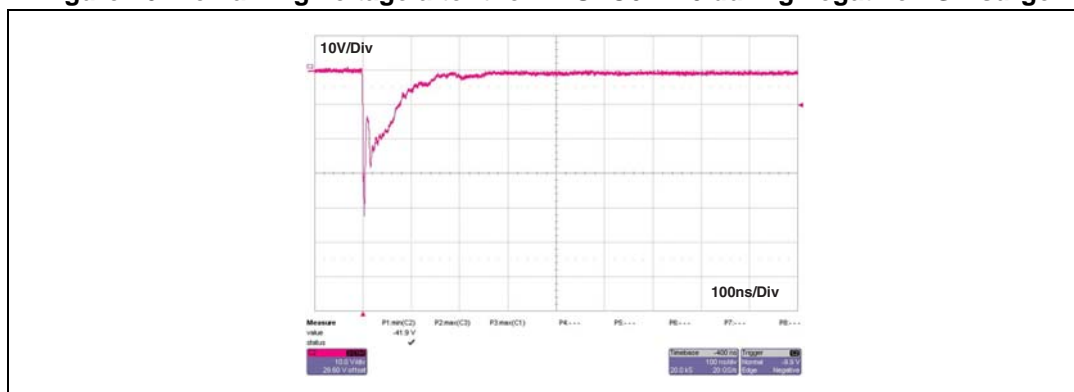
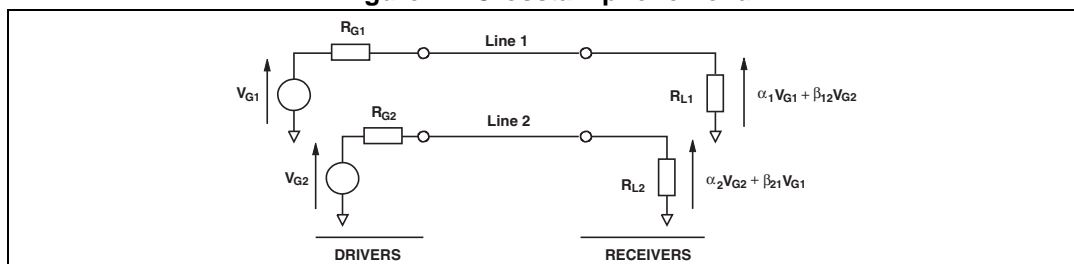**Figure 16. Remaining voltage after the DVIULC6-2M6 during negative ESD surge**



## Important

An important precaution to take is to put the protection device as close as possible to the disturbance source (generally the connector).

## 3.3 Crosstalk behavior

**Figure 17. Crosstalk phenomena**



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor ($\beta_{12}$ or $\beta_{21}$) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load $R_{L2}$ is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the $V_{G1}$ signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few k$\Omega$).

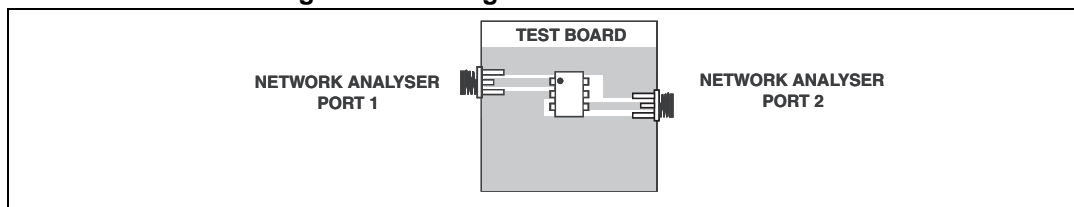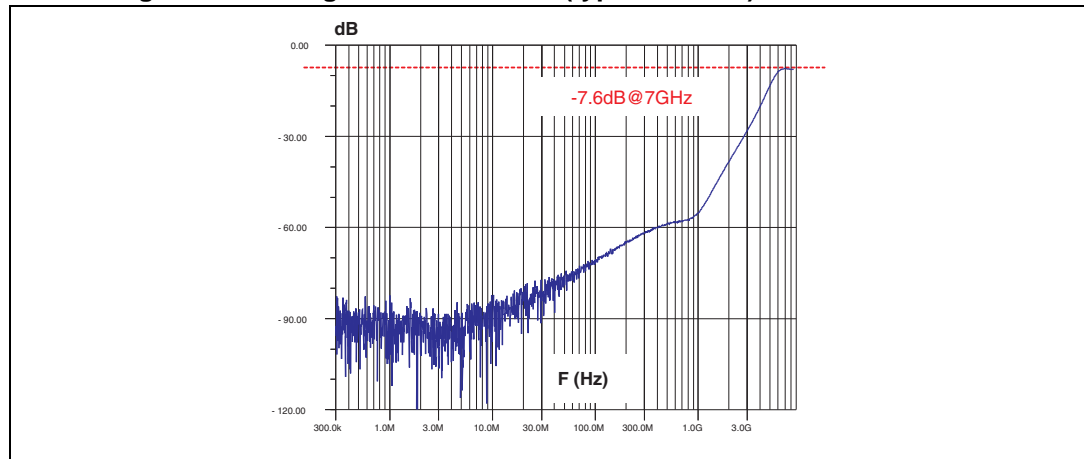**Figure 18. Analog crosstalk measurements**



*Figure 18* gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240 MHz) the effect on disturbed line is less than -40 dB (see *Figure 19*).

### Figure 19. Analog crosstalk results (typical values) for DVIULC6-2M6

# 4 Recommendation on PCB assembly

## 4.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness)

**Figure 20. Stencil opening dimensions.**
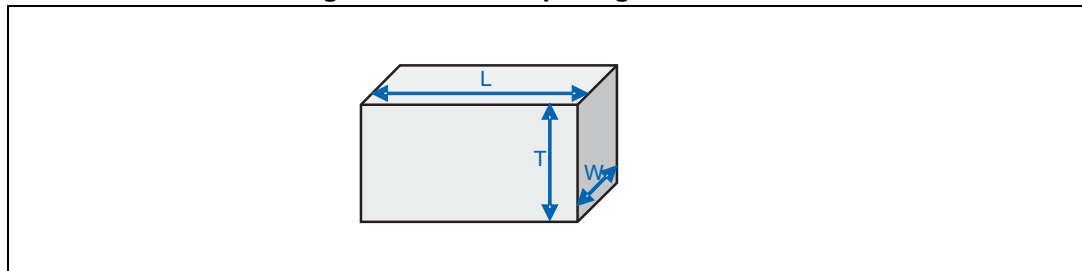


   b) General Design Rule

   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

**Figure 21. Recommended stencil window position (µQFN only)**

## 4.2       Solder paste

1.   Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
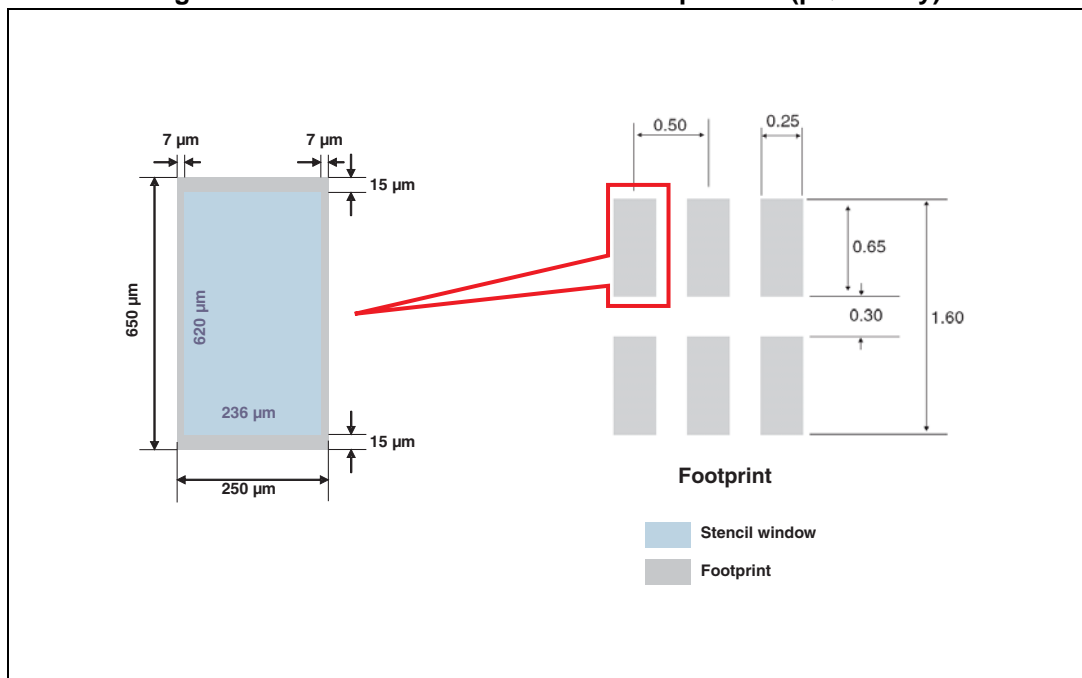
2.   "No clean" solder paste is recommended.

3.   Offers a high tack force to resist component movement during high speed.

4.   Solder paste with fine particles: powder particle size is 20-45 µm.

## 4.3       Placement

1.   Manual positioning is not recommended.

2.   It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.

3.   Standard tolerance of ± 0.05 mm is recommended.

4.   3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.

5.   To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.

6.   For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

## 4.4       PCB design preference

1.   To control the solder paste amount, the closed via is recommended instead of open vias.

2.   The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

## 4.5     Reflow profile

**Figure 22. ST ECOPACK® recommended soldering reflow profile for PCB mounting**
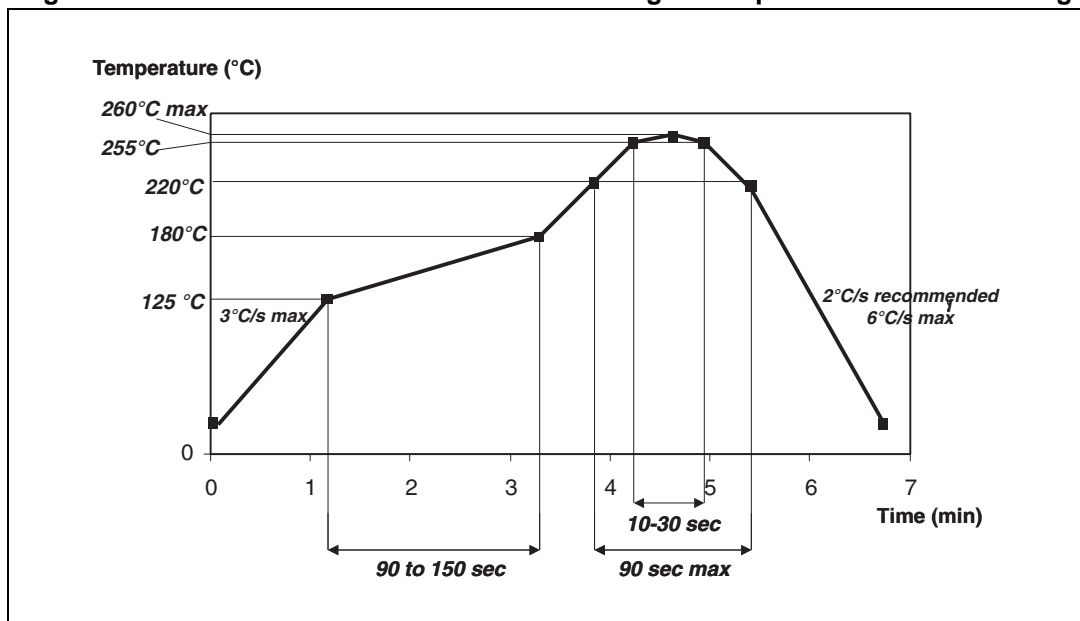


*Note:*         *Minimize air convection currents in the reflow oven to avoid component movement.*

# 5      Package information

• Epoxy meets UL94, V0

In order to meet environmental requirements, ST offers these devices in ECOPACK®
packages. These packages have a lead-free second level interconnect. The category of
second level interconnect is marked on the inner box label, in compliance with JEDEC
Standard JESD97. The maximum ratings related to soldering conditions are also marked on
the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available
at *www.st.com*.

**Table 3. Micro QFN 1.45x1.00 6L dimensions**

| Ref. | Millimeters | | | Inches | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.50 | 0.55 | 0.60 | 0.020 | 0.022 | 0.024 |
| A1 | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D | | 1.45 | | | 0.057 | |
| E | | 1.00 | | | 0.039 | |
| e | | 0.50 | | | 0.020 | |
| K | 0.20 | | | 0.008 | | |
| L | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |

**Figure 23. µQFN 6 leads footprint dimensions in mm [inches]**
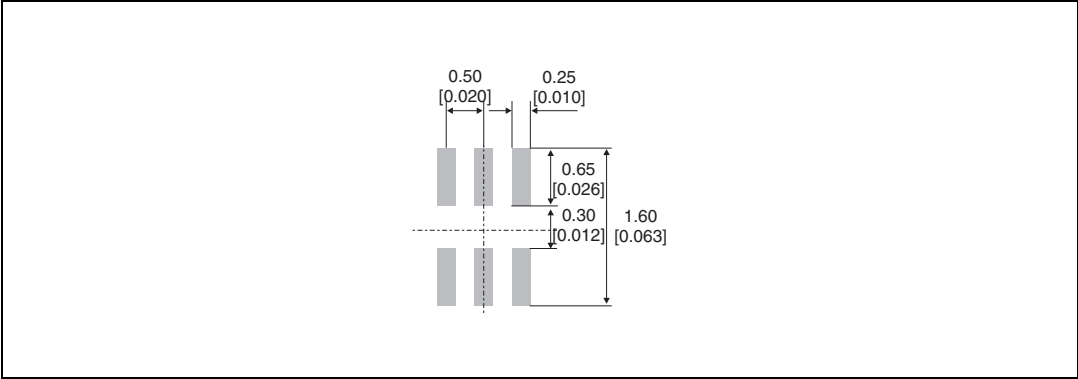
*Note:*      *Product marking may be rotated by 90° for assembly plant differentiation. In no case should
this product marking be used to orient the component for its placement on a PCB. Only pin
1 mark is to be used for this purpose.*

# 6      Ordering information

**Table 4. Ordering information**

| Order code | Marking | Package | Weight | Base qty | Delivery mode |
|---|---|---|---|---|---|
| DVIULC6-2M6 | T[1] | µQFN 6 leads | 2.2 mg | 3000 | Tape and reel |

1. The marking can be rotated by 90° to differentiate assembly location

# 7      Revision history

**Table 5.      Document revision history**

| Date | Revision | Description of changes |
|---|---|---|
| 06-May-2008 | 1 | First issue. |
| 13-Oct-2015 | 2 | Removed device in SOT-666 package.<br>Modified document accordingly. |

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