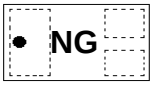
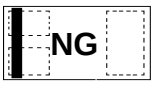
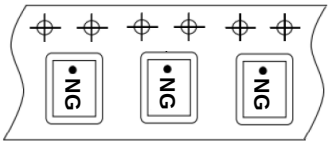
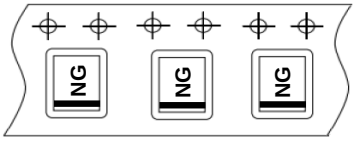
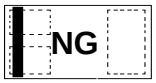
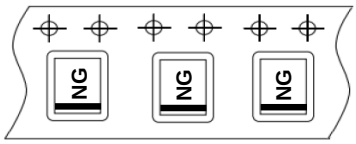
Marking Information

DMP21D0UFB-7	 Top View Dot Denotes Drain Side From date code 1527 (YYWW), this changes to:  Top View Bar Denotes Gate and Source Side  
DMP21D0UFB-7B	 Top View Bar Denotes Gate and Source Side NG = Part Marking Code 

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-20	V
Gate-Source Voltage			V_{GSS}	±8	V
Continuous Drain Current	Steady State V_{GS}=-4.5V	T_A = +25°C (Note 5) T_A = +85°C (Note 5) T_A = +25°C (Note 6)	I_D	-0.77 -0.55 -1.17	A
Pulsed Drain Current (Note 7)			I_{DM}	-5.0	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Power Dissipation (Note 5)	P_D	0.43	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	293	°C/W
Power Dissipation (Note 6)	P_D	0.99	W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	126	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Thermal Characteristics

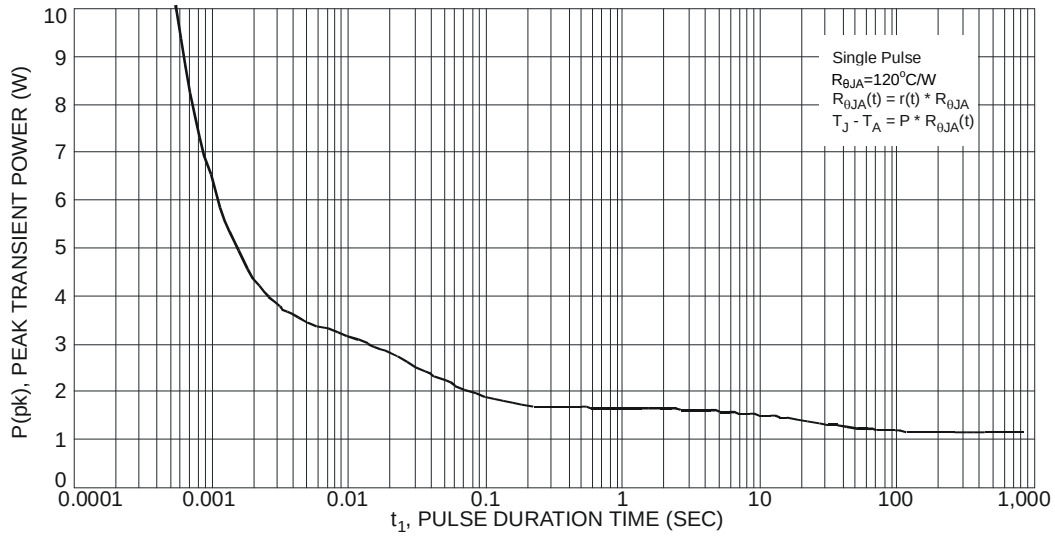


Fig. 1 Single Pulse Maximum Power Dissipation

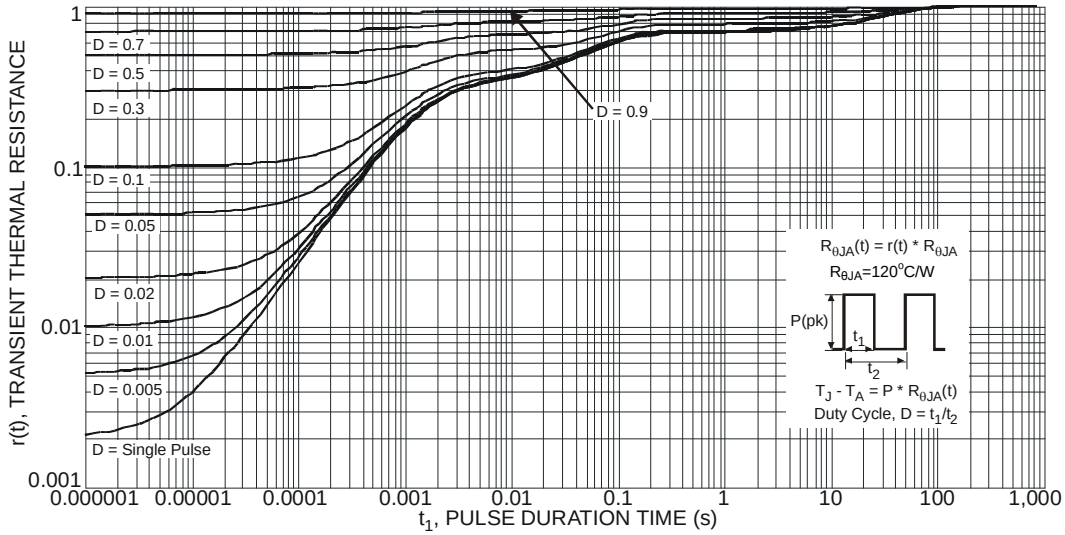


Fig. 2 Transient Thermal Response

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 8)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current, T_J = +25°C	I_{DSS}	—	—	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	µA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.5	-0.7	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	—	495	mΩ	V_{GS} = -4.5V, I_D = -400mA
		—	—	690		V_{GS} = -2.5V, I_D = -300mA
		—	—	960		V_{GS} = -1.8V, I_D = -100mA
Forward Transfer Admittance	$\|Y_{fs}\|$	50	—	—	mS	V_{DS} = -3V, I_D = -300mA
Diode Forward Voltage	V_{SD}	—	—	-1.2	V	V_{GS} = 0V, I_S = -300mA
DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C_{iss}	—	76.5	—	pF	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	13.7	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	10.7	—	pF	
Gate Resistance	R_g	—	195	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	—	1.5	—	nC	V_{GS} = -8V, V_{DS} = -15V, I_D = -1A
Total Gate Charge	Q_g	—	1.0	—	nC	V_{GS} = -4.5V, V_{DS} = -15V, I_D = -1A
Gate-Source Charge	Q_{gs}	—	0.2	—	nC	
Gate-Drain Charge	Q_{gd}	—	0.3	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	7.1	—	ns	V_{DS} = -10V, I_D = -1A, V_{GS} = -4.5V, R_G = 6Ω
Turn-On Rise Time	t_R	—	8.0	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	31.7	—	ns	
Turn-Off Fall Time	t_F	—	18.5	—	ns	

Notes:
5. Device mounted on FR-4 substrate PCB, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PCB, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
7. Device mounted on minimum recommended pad layout test board, 10µs pulse duty cycle = 1%.
8. Short duration pulse test used to minimize self-heating effect.
9. Guaranteed by design. Not subject to product testing.

Typical Characteristics

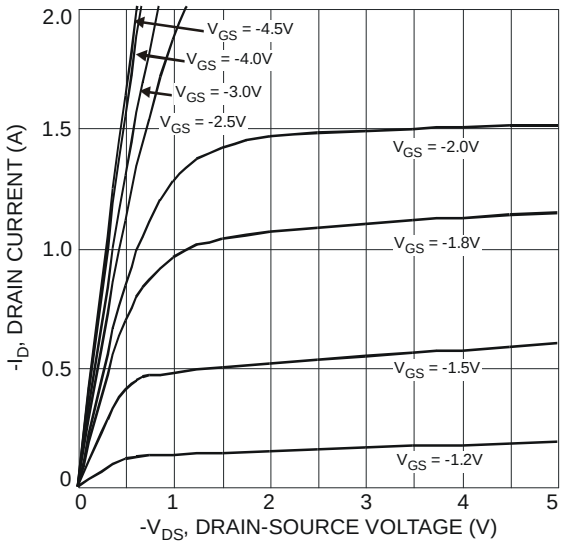


Fig. 3 Typical Output Characteristic

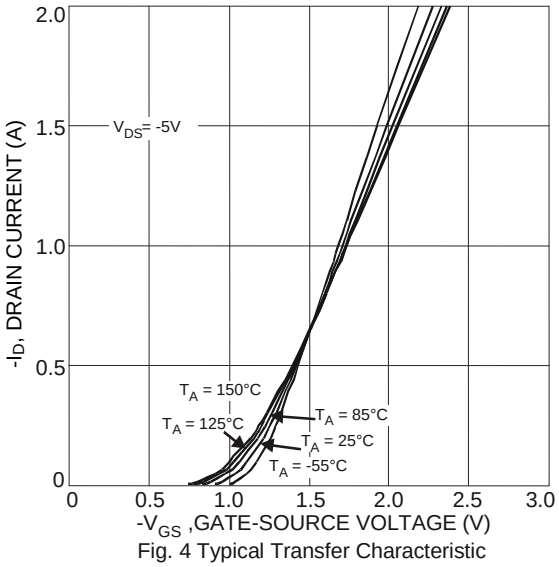


Fig. 4 Typical Transfer Characteristic

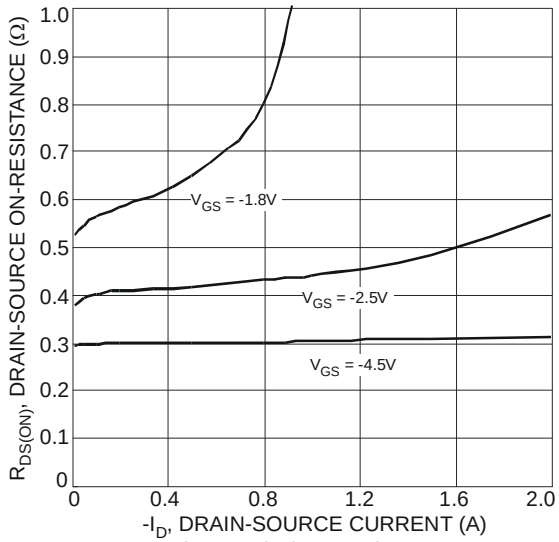


Fig. 5 Typical On-Resistance
vs. Drain Current and Gate Voltage

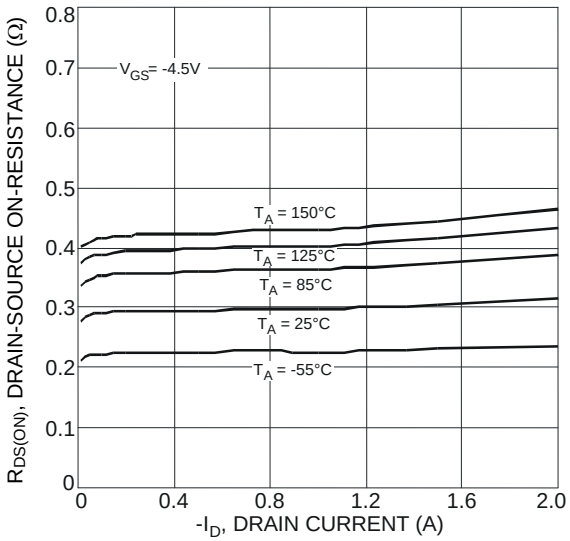


Fig. 6 Typical On-Resistance
vs. Drain Current and Temperature

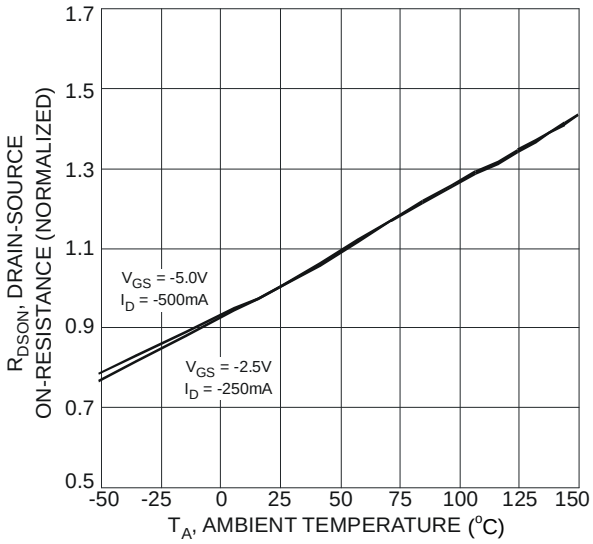


Fig. 7 On-Resistance Variation with Temperature

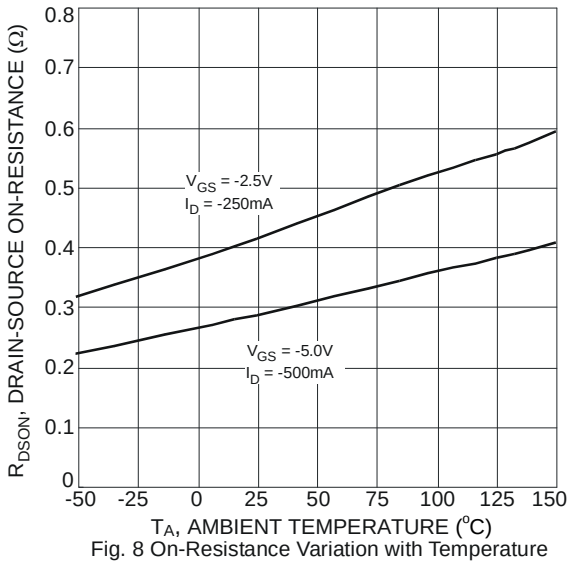


Fig. 8 On-Resistance Variation with Temperature

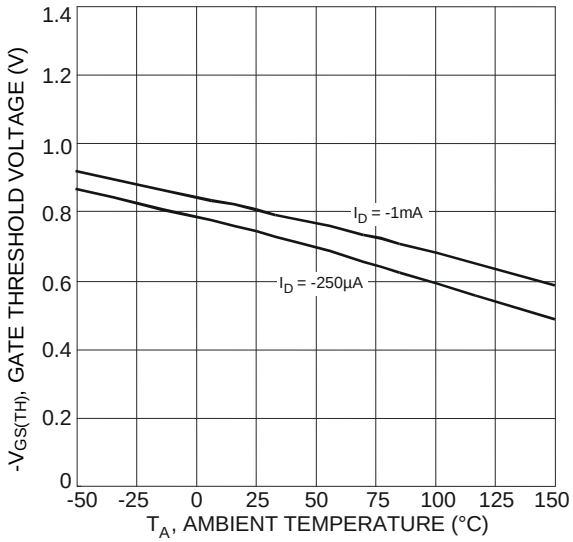


Fig. 9 Gate Threshold Variation vs. Ambient Temperature

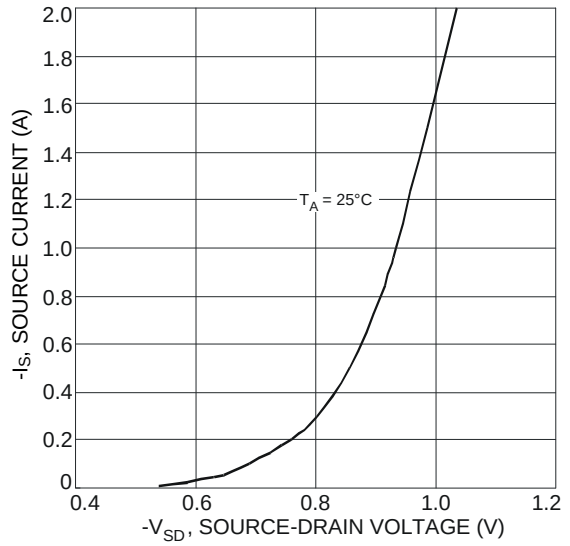


Fig. 10 Diode Forward Voltage vs. Current

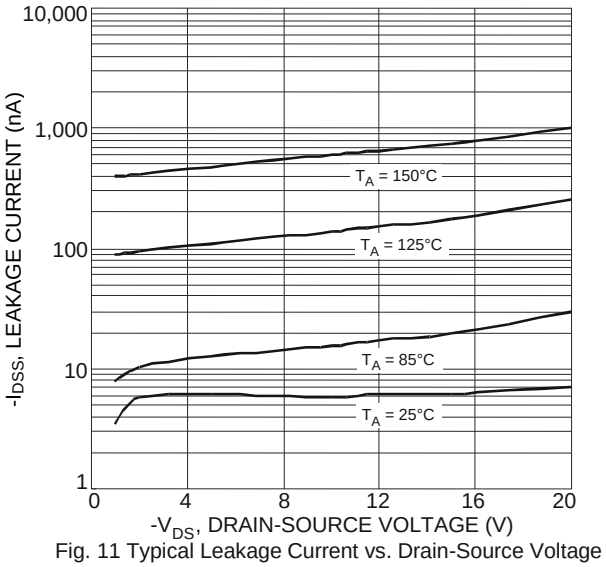


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

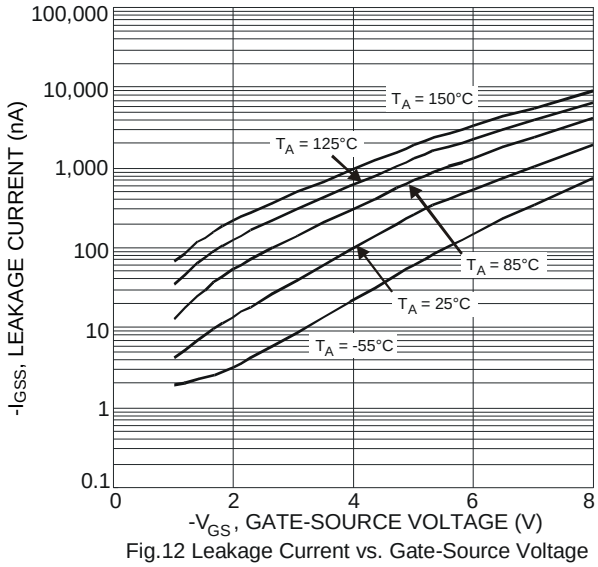


Fig.12 Leakage Current vs. Gate-Source Voltage

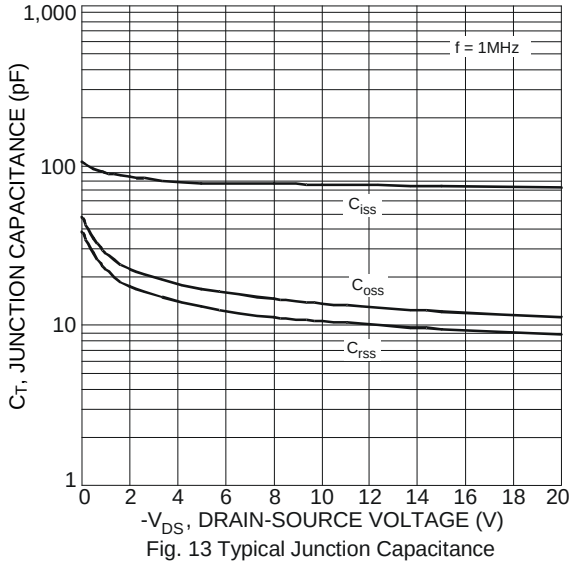


Fig. 13 Typical Junction Capacitance

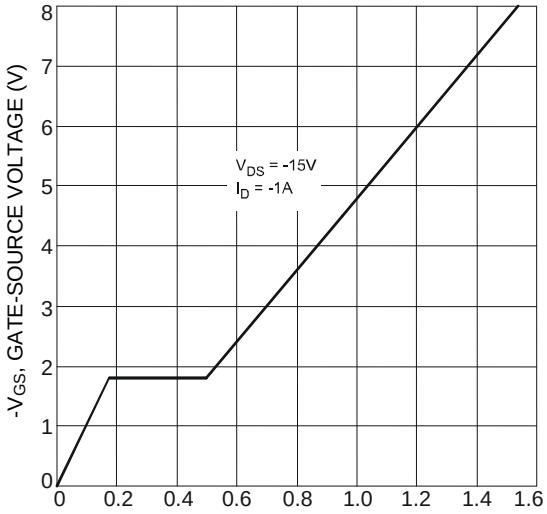


Fig. 14 Gate-Charge Characteristics

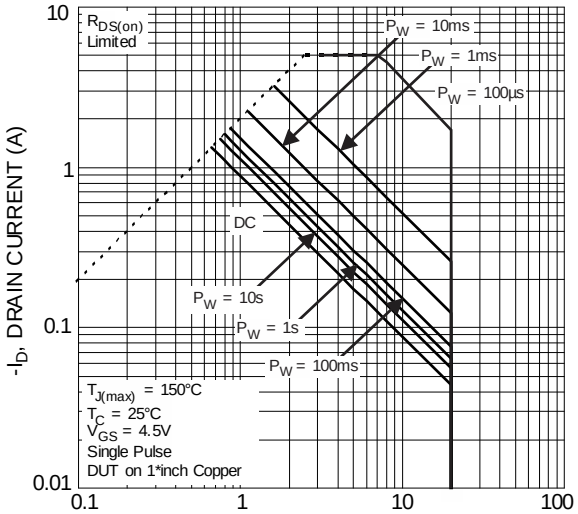
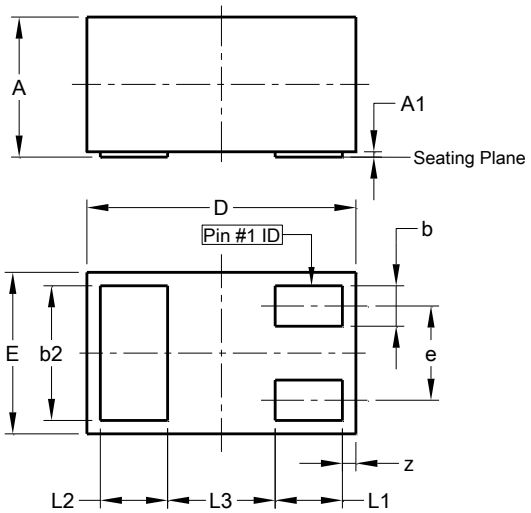


Figure 15 SOA, Safe Operation Area

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1006-3

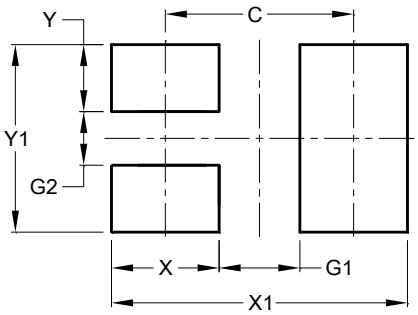


X1-DFN1006-3			
Dim	**Min**	**Max**	**Typ**
A	0.47	0.53	0.50
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.075	1.00
E	0.55	0.675	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

X1-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

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