

## Contents

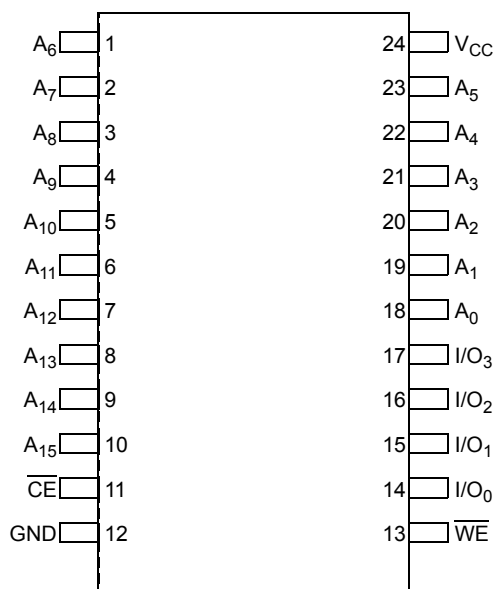
<b>Product Portfolio .....</b>	<b>3</b>	<b>Ordering Information .....</b>	<b>11</b>
<b>Pin Layout and Specification .....</b>	<b>4</b>	Ordering Code Definitions .....	11
<b>Pin Description .....</b>	<b>5</b>	<b>Package Diagrams .....</b>	<b>12</b>
<b>CY7C194BN Truth Table .....</b>	<b>5</b>	<b>Acronyms .....</b>	<b>13</b>
<b>Maximum Ratings .....</b>	<b>5</b>	<b>Document Conventions .....</b>	<b>13</b>
<b>Operating Range .....</b>	<b>5</b>	Units of Measure .....	13
<b>DC Electrical Characteristics .....</b>	<b>6</b>	<b>Document History Page .....</b>	<b>14</b>
<b>Capacitance .....</b>	<b>6</b>	<b>Sales, Solutions, and Legal Information .....</b>	<b>15</b>
<b>Thermal Resistance .....</b>	<b>6</b>	Worldwide Sales and Design Support .....	15
<b>AC Test Loads .....</b>	<b>7</b>	Products .....	15
<b>AC Test Conditions .....</b>	<b>7</b>	PSoC Solutions .....	15
<b>AC Electrical Characteristics .....</b>	<b>8</b>		
<b>Timing Waveforms .....</b>	<b>8</b>		

**Product Portfolio**

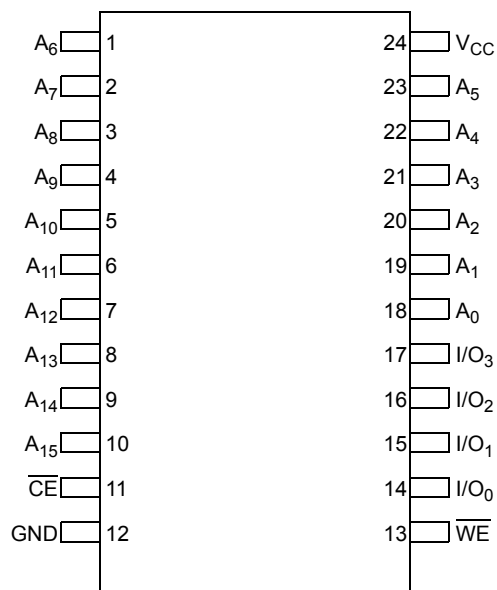
Description	-15	Unit
Maximum access time	15	ns
Maximum operating current	80	mA
Maximum CMOS standby current	10	mA

## Pin Layout and Specification

### CY7C194BN 24-pin SOJ (8 × 15 × 3.5 mm)



### CY7C194BN 24-pin DIP (6.6 × 31.8 × 3.5 mm)



## Pin Description

Pin	Type	Description	CY7C194BN	
			24-pin DIP	24-pin SOJ
A <sub>X</sub>	Input	Address inputs	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 18, 19, 20, 21, 22, 23
$\overline{\text{CE}}$	Control	Chip enable	11	11
I/O <sub>X</sub>	Input or output	Data input/outputs	14, 15, 16, 17	14, 15, 16, 17
NC	–	No connect. pins are not internally connected to the die	–	–
V <sub>CC</sub>	Supply	Power (V)	24	24
$\overline{\text{WE}}$	Control	Write enable	13	13

## CY7C194BN Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	I/O <sub>X</sub>	Mode	Power
H	X	High Z	Power-down	Standby (I <sub>SB</sub> )
L	H	Data out	Read	Active (I <sub>CC</sub> )
L	L	Data in	Write	Active (I <sub>CC</sub> )

## Maximum Ratings

Above which the useful life may be impaired. For user guidelines, not tested.

Parameter	Description	Value	Unit
T <sub>STG</sub>	Storage temperature	–65 to +150	°C
T <sub>AMB</sub>	Ambient temperature with power applied (i.e. case temperature)	–55 to +125	°C
V <sub>CC</sub>	Core supply voltage relative to V <sub>SS</sub>	–0.5 to +7.0	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC voltage applied to any pin relative to V <sub>SS</sub>	–0.5 to V <sub>CC</sub> + 0.5	V
I <sub>OUT</sub>	Output short-circuit current	20	mA
V <sub>ESD</sub>	Static discharge voltage (per MIL-STD-883, Method 3015)	> 2001	V
I <sub>LU</sub>	Latch-up current	> 200	mA

## Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	Voltage Range (V <sub>CC</sub> )
Commercial	0 °C to 70 °C	5.0 V ± 10%

## DC Electrical Characteristics

Parameter <sup>[1]</sup>	Description	Condition	15 ns		Unit
			Min	Max	
V <sub>IH</sub>	Input HIGH voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW voltage		−0.3	0.8	V
V <sub>OH</sub>	Output HIGH voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = −4.0 mA	2.4	–	V
V <sub>OL</sub>	Output LOW voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8.0 mA	–	0.4	V
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, f = F <sub>MAX</sub> = 1 / t <sub>RC</sub>	–	80	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-down current – TTL inputs	V <sub>CC</sub> = Max, $\overline{CE} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = F <sub>MAX</sub>	–	30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-down current – CMOS inputs	V <sub>CC</sub> = Max, $\overline{CE} \geq V_{CC} - 0.3$ V, V <sub>IN</sub> > V <sub>CC</sub> − 0.3 V or V <sub>IN</sub> ≤ 0.3 V, f = 0, Commercial	–	10	mA
I <sub>OZ</sub>	Output leakage current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , output disabled	−5	+5	μA
I <sub>IX</sub>	Input load current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	−5	+5	μA

## Capacitance

Parameter <sup>[2]</sup>	Description	Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	7	pF
C <sub>OUT</sub>	Output capacitance		10	–

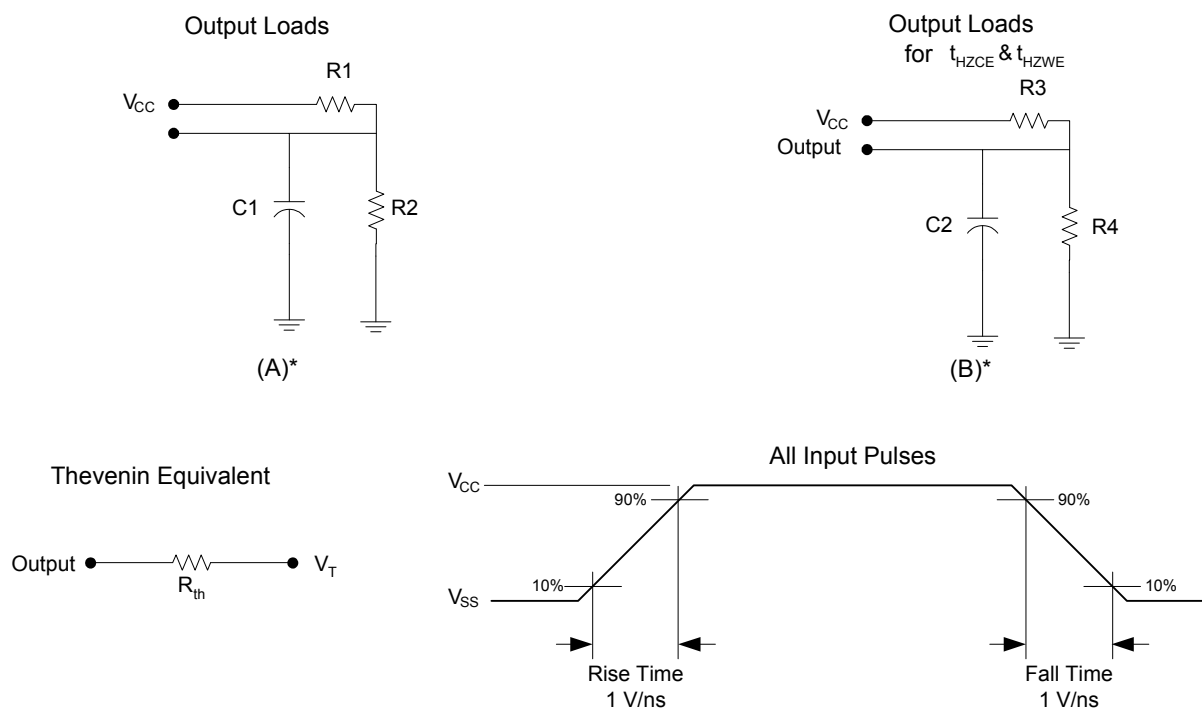
## Thermal Resistance

Parameter <sup>[2, 3]</sup>	Description	Conditions	CY7C194BN		Unit
			24-pin DIP	24-pin SOJ	
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 x 4.5 square inches, two-layer printed circuit board	75.69	84.15	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		33.80	37.56	

### Notes

1. V<sub>IL</sub>(min) = −2.0 V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process change that may affect these parameters
3. Test Conditions assume a transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

## AC Test Loads



\* including scope and jig capacitance

## AC Test Conditions

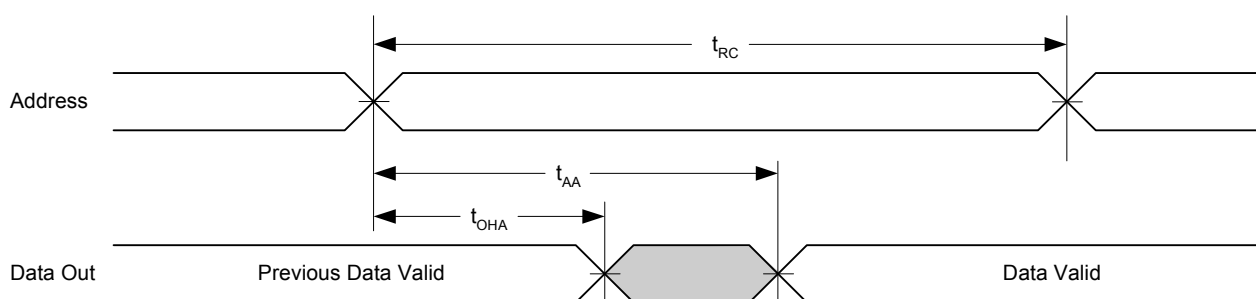
Parameter	Description	Nom	Unit
C1	Capacitor 1	30	pF
C2	Capacitor 2	5	
R1	Resistor 1	480	$\Omega$
R2	Resistor 2	255	
R3	Resistor 3	480	
R4	Resistor 4	255	
$R_{TH}$	Resistor Thevenin	167	
$V_{TH}$	Voltage Thevenin	1.73	V

## AC Electrical Characteristics

Parameter <sup>[4, 5, 6, 7]</sup>	Description	15 ns		Unit
		Min	Max	
$t_{RC}$	Read cycle time	15	–	ns
$t_{AA}$	Address to data valid	–	15	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ to data valid	–	15	ns
$t_{LZCE}$	$\overline{CE}$ to Low Z	3	–	ns
$t_{HZCE}$	$\overline{CE}$ to High Z	–	7	ns
$t_{PU}$	$\overline{CE}$ to Power-up	0	–	ns
$t_{PD}$	$\overline{CE}$ to Power-down	–	15	ns
$t_{WC}$	Write cycle time	15	–	ns
$t_{SCE}$	$\overline{CE}$ to write end	10	–	ns
$t_{AW}$	Address set-up to write end	10	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address set-up to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	9	–	ns
$t_{SD}$	Data set-up to write end	8	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z	–	7	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z	3	–	ns

## Timing Waveforms

**Figure 1. Read Cycle No. 1** <sup>[8, 9]</sup>

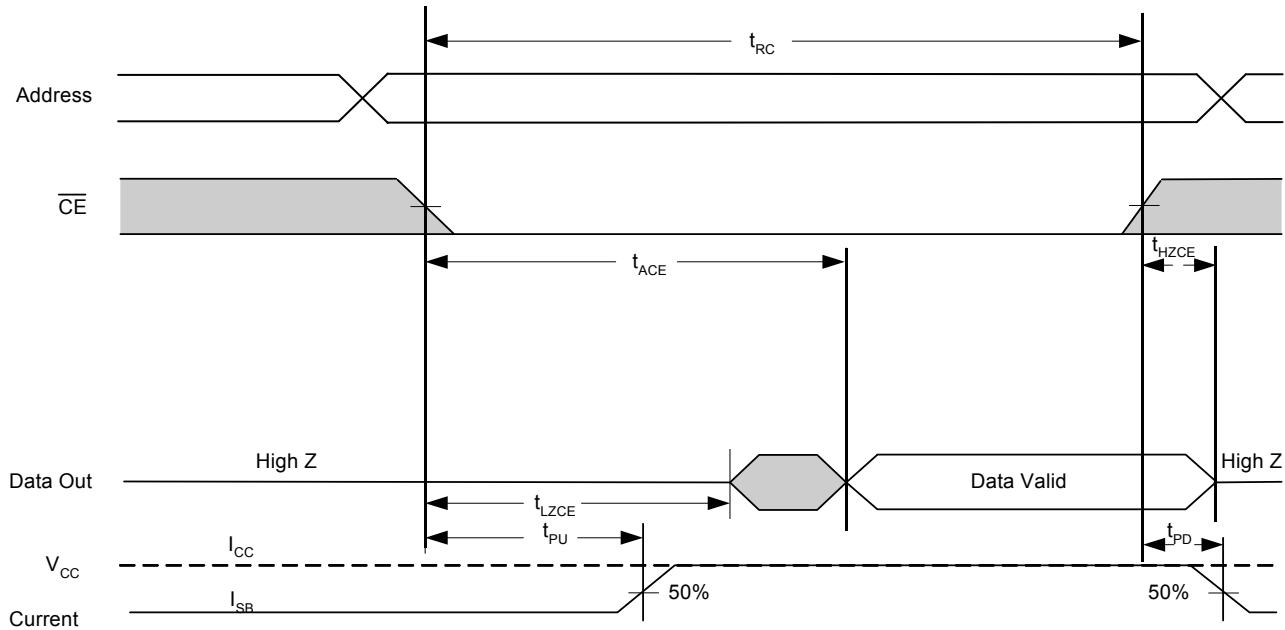


### Notes

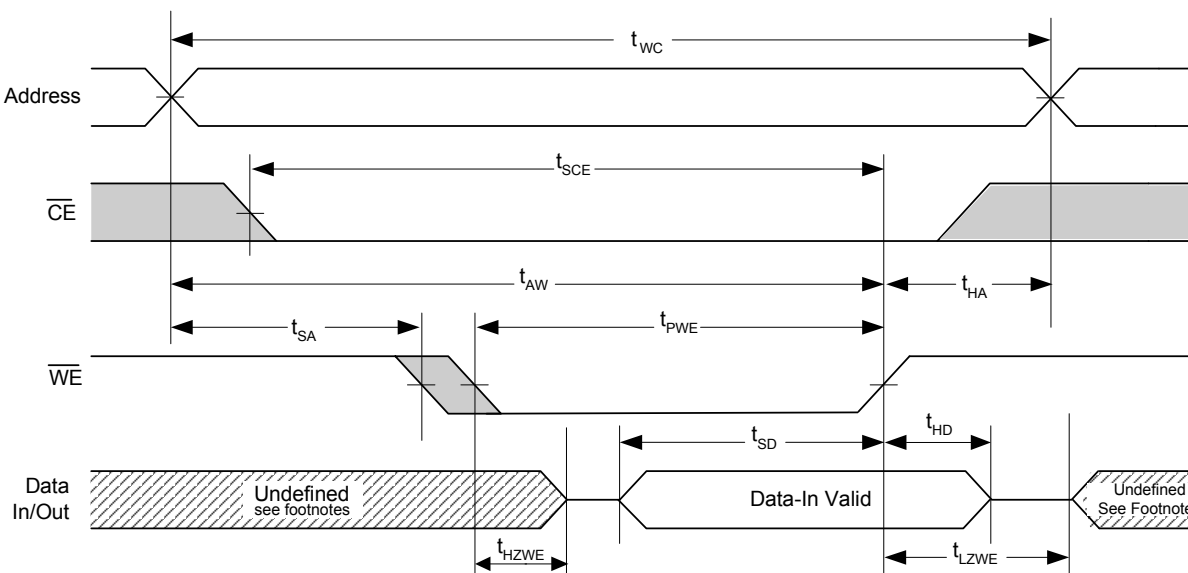
- Tested initially and after any design or process change that may affect these parameters
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- $t_{HZCE}$ ,  $t_{HZWE}$  are specified as in part (b) of the A/C Test Loads. Transitions are measured  $\pm 200$  mV from steady state voltage.
- Device is continuously selected.  $\overline{CE} = V_{IL}$ .
- $\overline{WE}$  is HIGH for Read Cycle.

## Timing Waveforms (continued)

**Figure 2. Read Cycle No. 2** [10, 11, 12]



**Figure 3. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled)** [10, 13]



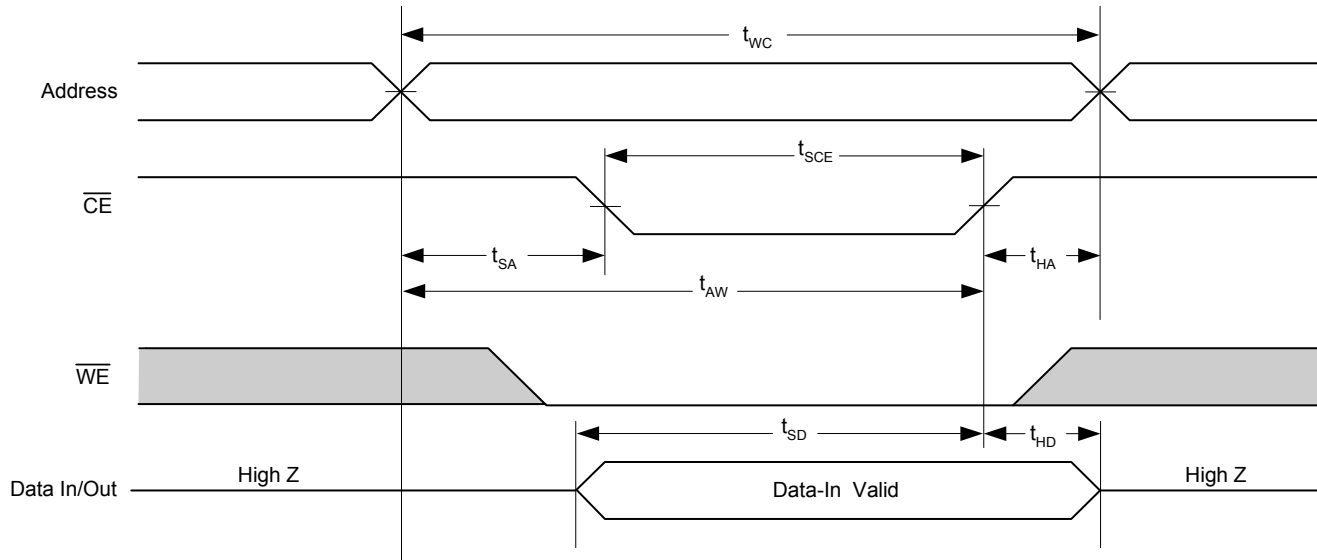
### Notes

10. Tested initially and after any design or process change that may affect these parameters
11.  $\overline{\text{WE}}$  is HIGH in read cycle.
12. Address valid prior to or coincident with  $\overline{\text{CE}}$  transition LOW.
13. The minimum write cycle time is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .



## Timing Waveforms *(continued)*

**Figure 4. Write Cycle No. 2 ( $\overline{\text{CE}}$  Controlled)** <sup>[14, 15]</sup>



### Notes

14. This cycle is  $\overline{\text{CE}}$  controlled.

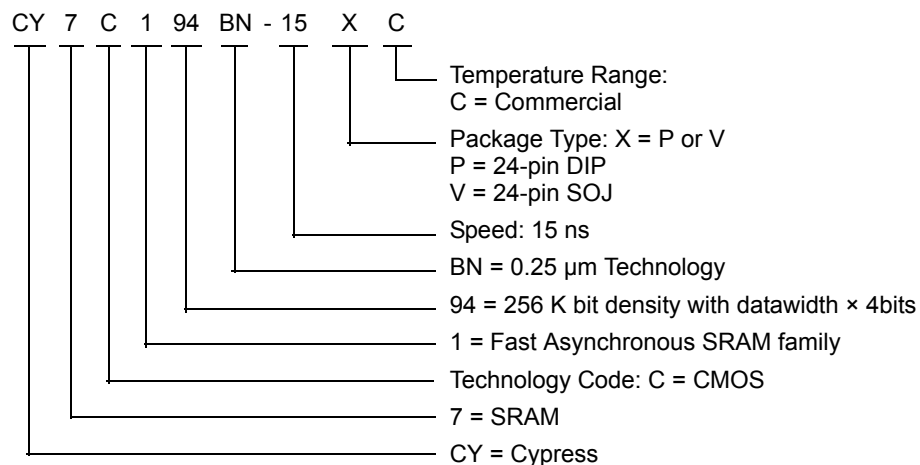
15. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high-impedance state.

## Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Power Option	Operating Range
15	CY7C194BN-15PC	51-85013	24-pin DIP (6.6 × 31.8 × 3.5 mm)	Standard	Commercial
	CY7C194BN-15VC	51-85030	24-pin SOJ (8 × 15 × 3.5 mm)	Standard	Commercial

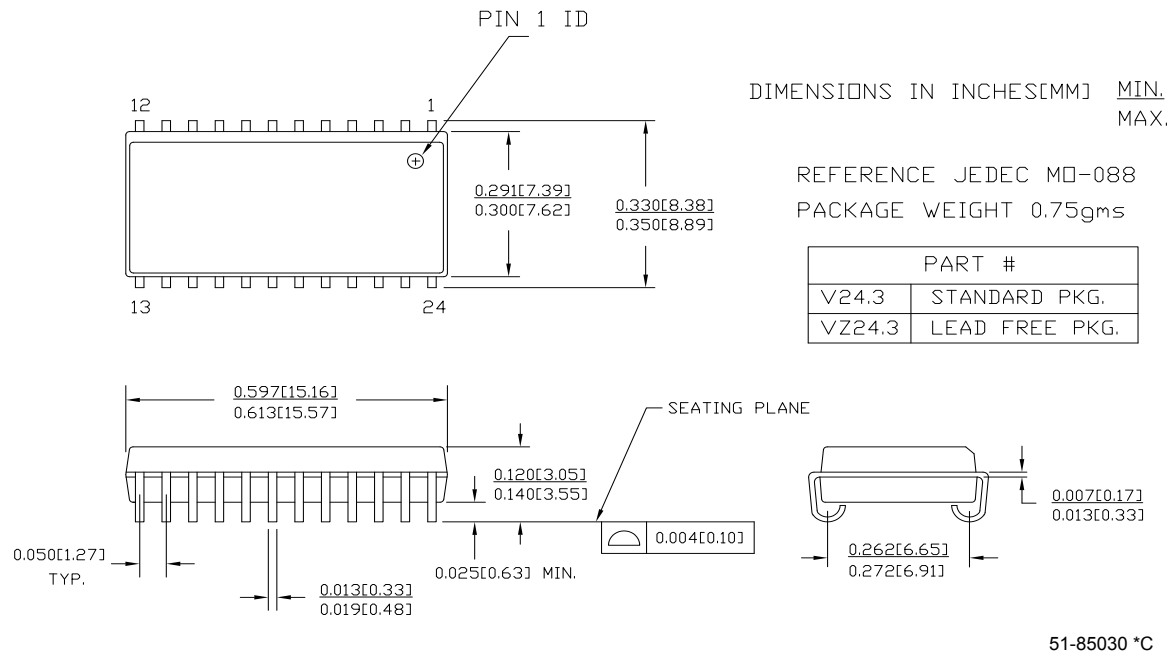
Please contact local sales representative regarding availability of these parts.

## Ordering Code Definitions

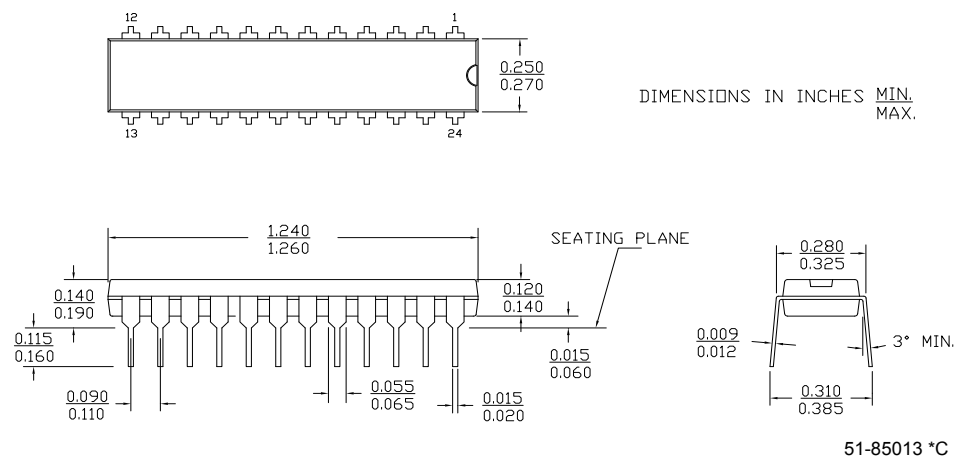


## Package Diagrams

**Figure 5. 24-pin (300-mil) SOJ V24.3/VZ24.3 (Molded SOJ V13), 51-85030**



**Figure 6. 24-pin PDIP (1.260 × 0.270 × 0.140 Inches) P24.3, 51-85013**



## Acronyms

Acronym	Description
CE	chip enable
CMOS	complementary metal oxide semiconductor
DIP	dual in-line package
ESD	electrostatic discharge
I/O	input/output
SOJ	small outline J-lead
SRAM	static random access memory
TTL	transistor-transistor logic
WE	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

## Document History Page

Document Title: CY7C194BN, 256 Kb (64 K × 4) Static RAM Document Number: 001-06446				
REV.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	424111	See ECN	NXR	New Data Sheet
*A	2892510	03/18/2010	VKN	Removed 25ns speed bin Updated Ordering Information table Updated Package Diagram Added Sales, Solutions, and Legal Information
*B	3108898	12/13/2010	AJU	Added <a href="#">Ordering Code Definitions</a> .
*C	3219087	04/18/2011	PRAS	Updated as per template Added TOC Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> .
*D	3271782	06/02/2011	PRAS	Updated <a href="#">General Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated in new template.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

### Products

Automotive	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
Clocks & Buffers	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
Interface	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
Lighting & Power Control	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
Memory	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
Optical & Image Sensing	<a href="http://cypress.com/go/image">cypress.com/go/image</a>
PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
USB Controllers	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
Wireless/RF	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

### PSoC Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)

PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.