Contents

Selection Guide

Description		-8	-10	-12	-15	Unit
Maximum Access Time		8	10	12	15	ns
Maximum Operating Current	Commercial	95	90	85	80	mA
	Industrial		90	85		mA
	Automotive-A		90		80	mA
	Automotive-E			90		mA
Maximum CMOS Standby Current	Commercial	5	5	5	5	mA
	Industrial	5	5	5		mA
	Automotive-A		5		5	mA
	Automotive-E			10		mA

Pin Configuration

Figure 1. 44-Pin SOJ/TSOP II [1]

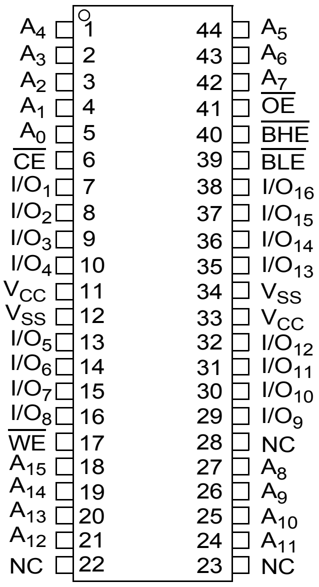
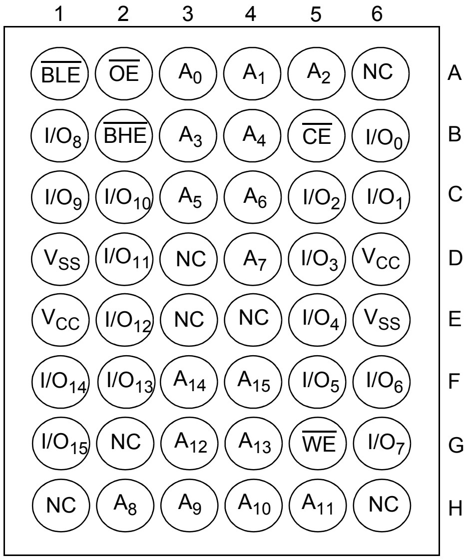


Figure 2. 48-Ball FBGA Pinout [1]



1	2	3	4	5	6	
$\overline{\text{BLE}}$	$\overline{\text{OE}}$	A_0	A_1	A_2	NC	A
I/O$_8$	$\overline{\text{BHE}}$	A_3	A_4	$\overline{\text{CE}}$	I/O$_0$	B
I/O$_9$	I/O$_{10}$	A_5	A_6	I/O$_2$	I/O$_1$	C
V_{SS}	I/O$_{11}$	NC	A_7	I/O$_3$	V_{CC}	D
V_{CC}	I/O$_{12}$	NC	NC	I/O$_4$	V_{SS}	E
I/O$_{14}$	I/O$_{13}$	A_{14}	A_{15}	I/O$_5$	I/O$_6$	F
I/O$_{15}$	NC	A_{12}	A_{13}	$\overline{\text{WE}}$	I/O$_7$	G
NC	A_8	A_9	A_{10}	A_{11}	NC	H

Note

1. NC pins are not connected on the die.

Pin Definitions

Pin Name	SOJ, TSOP Pin Number	BGA Pin Number	I/O Type	Description
A_0–A_{15}	1–5, 18–21, 24–27, 42–44	A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4	Input	**Address Inputs.** Used to select one of the address locations.
I/O_1–I/O_{16} [2]	7–10, 13–16, 29–32, 35–38	B6, C6, C5, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	Input or Output	**Bidirectional Data I/O lines**. Used as input or output lines depending on operation.
NC	22, 23, 28	A6, D3, E3, E4, G2, H1, H6	No Connect	**No Connects**. Not connected to the die.
$\overline{WE}$	17	G5	Input or Control	**Write Enable Input, Active LOW**. When selected LOW, a write is conducted. When deselected HIGH, a read is conducted.
$\overline{CE}$	6	B5	Input or Control	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{BHE}$, $\overline{BLE}$	40, 39	B2, A1	Input or Control	**Byte Write Select Inputs, Active LOW**. $\overline{BHE}$ controls I/O_{16} – I/O_9, BLE controls I/O_8 – I/O_1.
$\overline{OE}$	41	A2	Input or Control	**Output Enable, Active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, the I/O pins are tristated and act as input data pins.
V_{SS}	12, 34	D1, E6	Ground	**Ground for the Device**. Connected to ground of the system.
V_{CC}	11, 33	D6, E1	Power Supply	**Power Supply Inputs to the Device.**

Note

[2] I/O_1–I/O_{16} for SOJ/TSOP and I/O_0–I/O_{15} for BGA packages.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[3] .....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[3] .... –0.5V to V_{CC}+0.5V

DC Input Voltage[3] .... –0.5V to V_{CC}+0.5V

Current into Outputs (LOW).. 20 mA

Static Discharge Voltage.. >2001V
(MIL-STD-883, Method 3015)

Latch Up Current .... >200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	–40°C to +85°C	
Automotive-A	–40°C to +85°C	
Automotive -E	–40°C to +125°C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-8		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I/O_H = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I/O_L = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND $\leq V_I \leq V_{CC}$	Commercial	–1	+1	–1	+1	–1	+1	–1	+1	µA
			Industrial			–1	+1	–1	+1			
			Automotive-A			–1	+1			–1	+1	
			Automotive-E					–12	+12			
I/O_Z	Output Leakage Current	GND $\leq V_I \leq V_{CC}$, Output disabled	Commercial	–1	+1	–1	+1	–1	+1	–1	+1	µA
			Industrial			–1	+1	–1	+1			
			Automotive-A			–1	+1			–1	+1	
			Automotive-E					–12	+12			
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I/O_{UT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Commercial		95		90		85		80	mA
			Industrial				90		85			
			Automotive-A				90				80	
			Automotive-E						90			
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max V_{CC}, $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}	Commercial		15		15		15		15	mA
			Industrial				15		15			
			Automotive-A				15				15	
			Automotive-E						20			
I_{SB2}	Automatic CE Power Down Current — CMOS Inputs	Max V_{CC}, $\overline{CE} \geq V_{CC}$ – 0.3V, $V_{IN} \geq V_{CC}$ – 0.3V, or $V_{IN} \leq$ 0.3V, f = 0	Commercial		5		5		5		5	mA
			Industrial				5		5			
			Automotive-A				5				5	
			Automotive-E						10			

Note

3. V_{IL} (min) = –2.0V and V_{IH}(max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

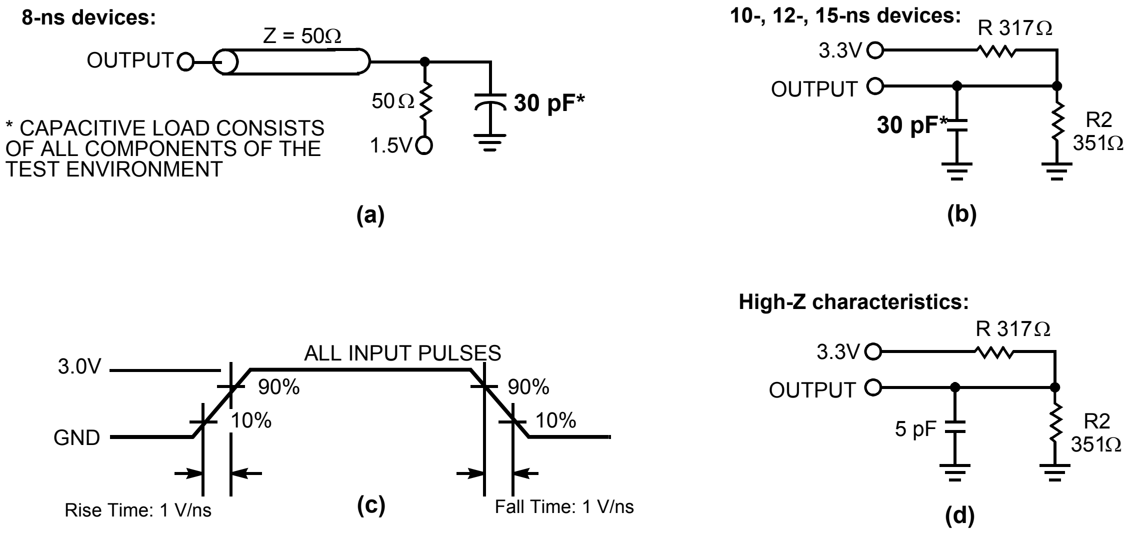
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = 3.3V$	8	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	SOJ	TSOP II	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51	65.06	76.92	95.32	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		34.21	15.86	10.68	°C/W

Figure 3. AC Test Loads and Waveforms [4]



Note

4. AC characteristics (except High-Z) for all 8-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

Switching Characteristics

Over the Operating Range [5]

Parameter	Description	-8		-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle										
t_{power}[6]	V_{CC}(Typical) to the First Access	100		100		100		100		µs
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[7]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[7, 8]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[7, 8]		4		5		6		7	ns
t_{PU}[9]	$\overline{CE}$ LOW to Power Up	0		0		0		0		ns
t_{PD}[9]	$\overline{CE}$ HIGH to Power Down		8		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		5		6		7	ns
t_{LZBE}	Byte Enable to Low Z	0		0		0		0		ns
t_{HZBE}	Byte Disable to High Z		4		5		6		7	ns
Write Cycle[10]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		9		10		ns
t_{AW}	Address Setup to Write End	7		8		9		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Setup to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		10		ns
t_{SD}	Data Setup to Write End	5		5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[7, 8]		4		5		6		7	ns
t_{BW}	Byte Enable to End of Write	6		7		8		9		ns

Notes

5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V.
6. t_{POWER} gives the minimum amount of time that the power supply is at typical V_{CC} values until the first memory access is performed.
7. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZBE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms [4]" on page 6. Transition is measured ±500 mV from steady state voltage.
9. This parameter is guaranteed by design and is not tested.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, $\overline{WE}$ LOW, and $\overline{BHE}$/$\overline{BLE}$ LOW. $\overline{CE}$, $\overline{WE}$, and $\overline{BHE}$/$\overline{BLE}$ is LOW to initiate a write. The transition of these signals terminate the write. The input data setup and hold timing is referenced to the leading edge of the signal that terminates the write.

Switching Waveforms

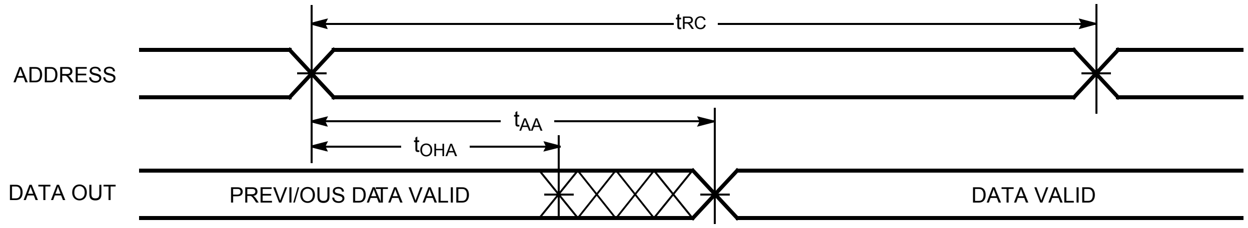


Figure 4. Read Cycle No. 1 (Address Transition Controlled)[11, 12]

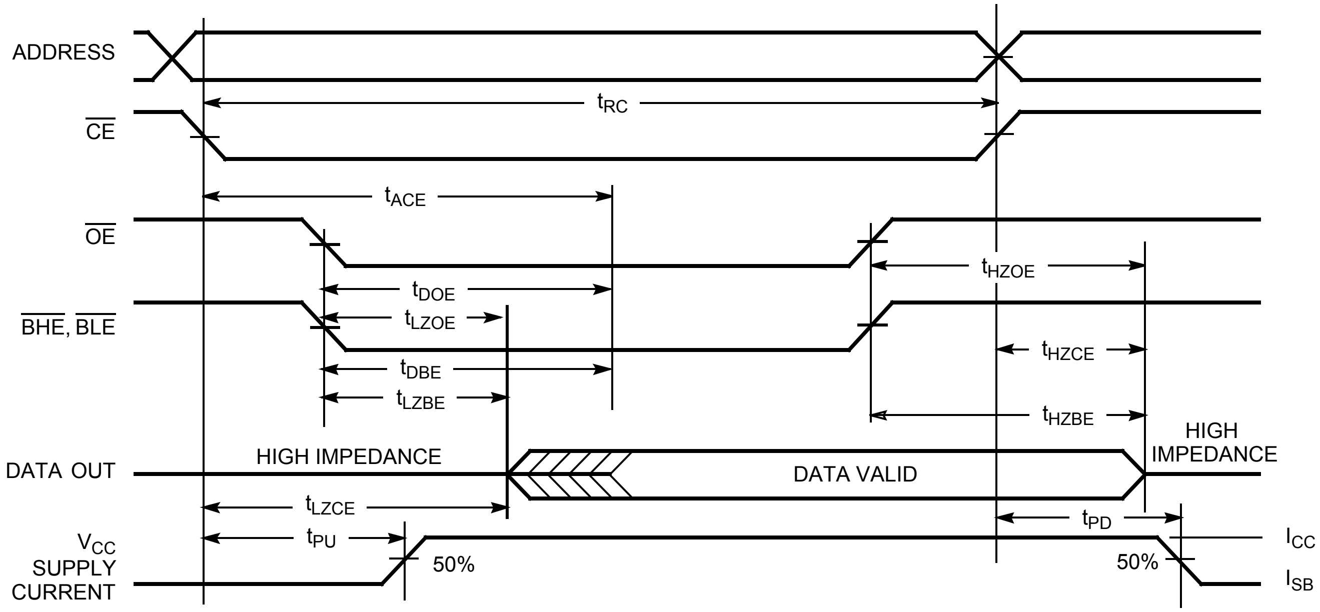


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)[12, 13]

Notes

[11] Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IL}.

[12] $\overline{WE}$ is HIGH for read cycle.

[13] Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled)[14, 15]

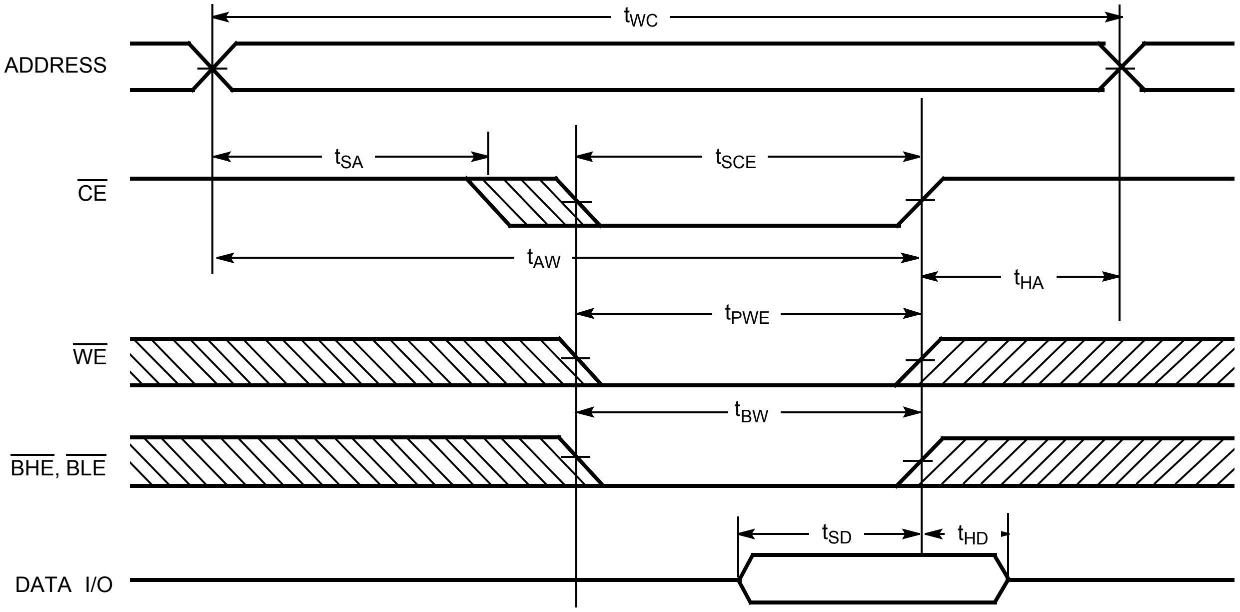
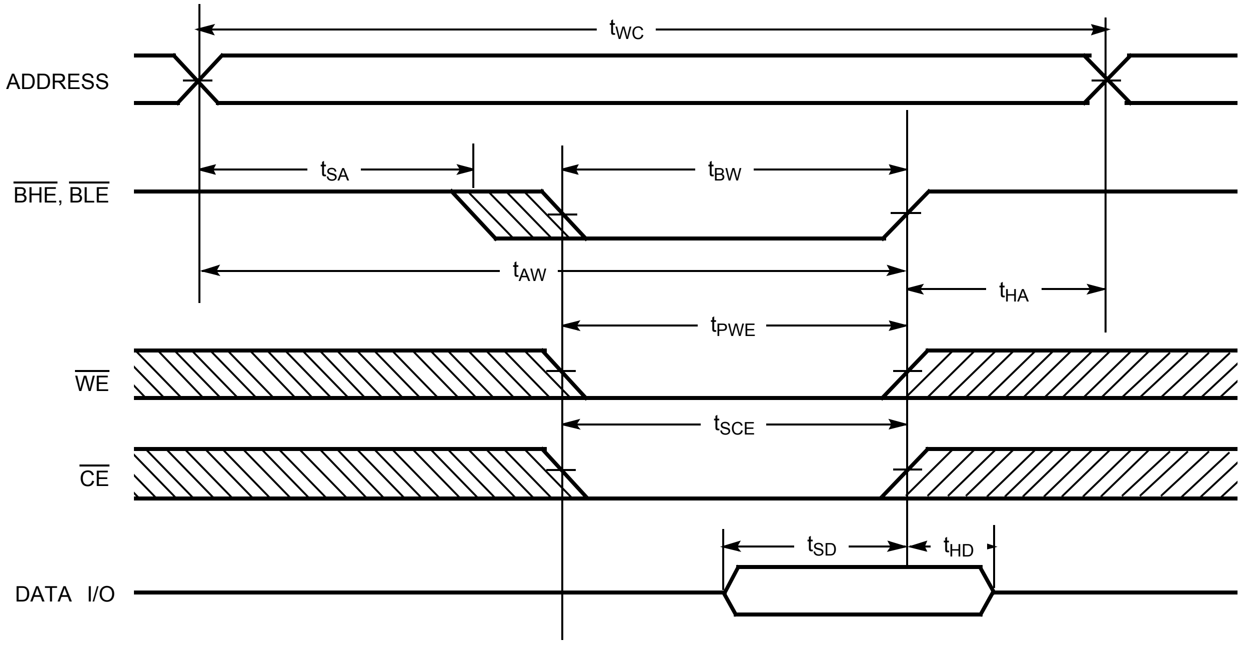


Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes

[14] Data I/O is high impedance if $\overline{OE}$, $\overline{BHE}$, and/or $\overline{BLE}$= V_{IH}.

[15] If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

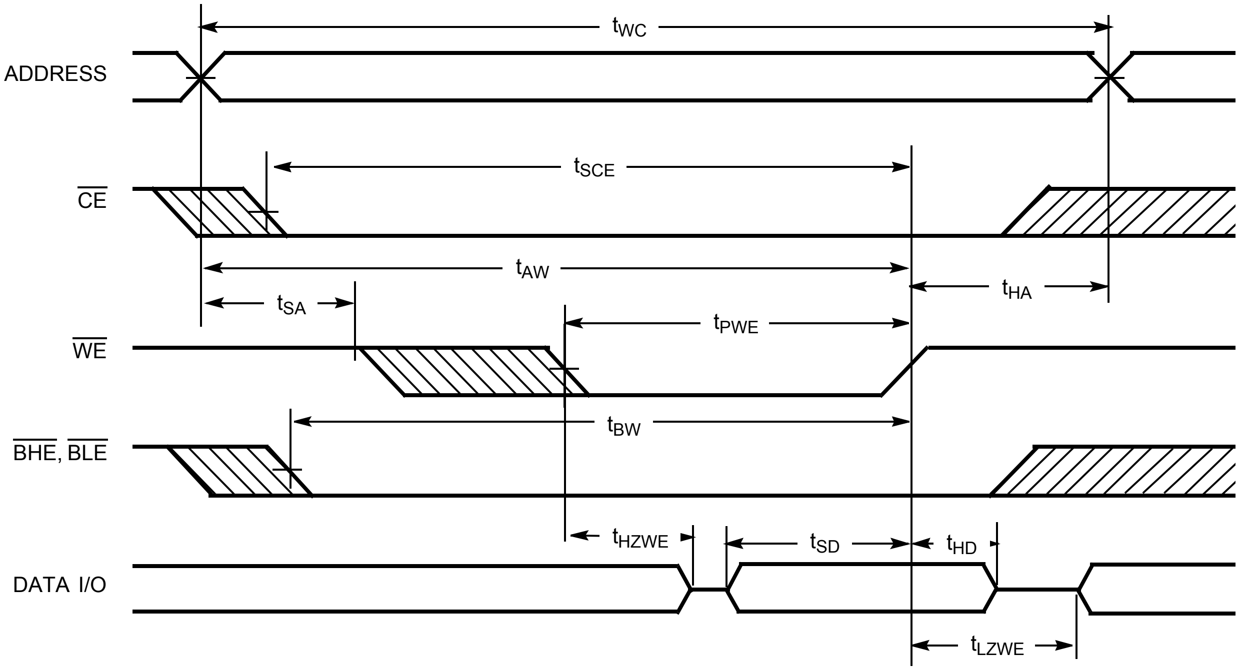


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, LOW)

Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_1 – I/O_8$	$I/O_9 – I/O_{16}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read – All Bits	Active (I_{CC})
			L	H	Data Out	High Z	Read – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data Out	Read – Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write – All Bits	Active (I_{CC})
			L	H	Data In	High Z	Write – Lower Bits Only	Active (I_{CC})
			H	L	High Z	Data In	Write – Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High Z	High Z	Selected, Outputs Disabled	Active (I_{CC})

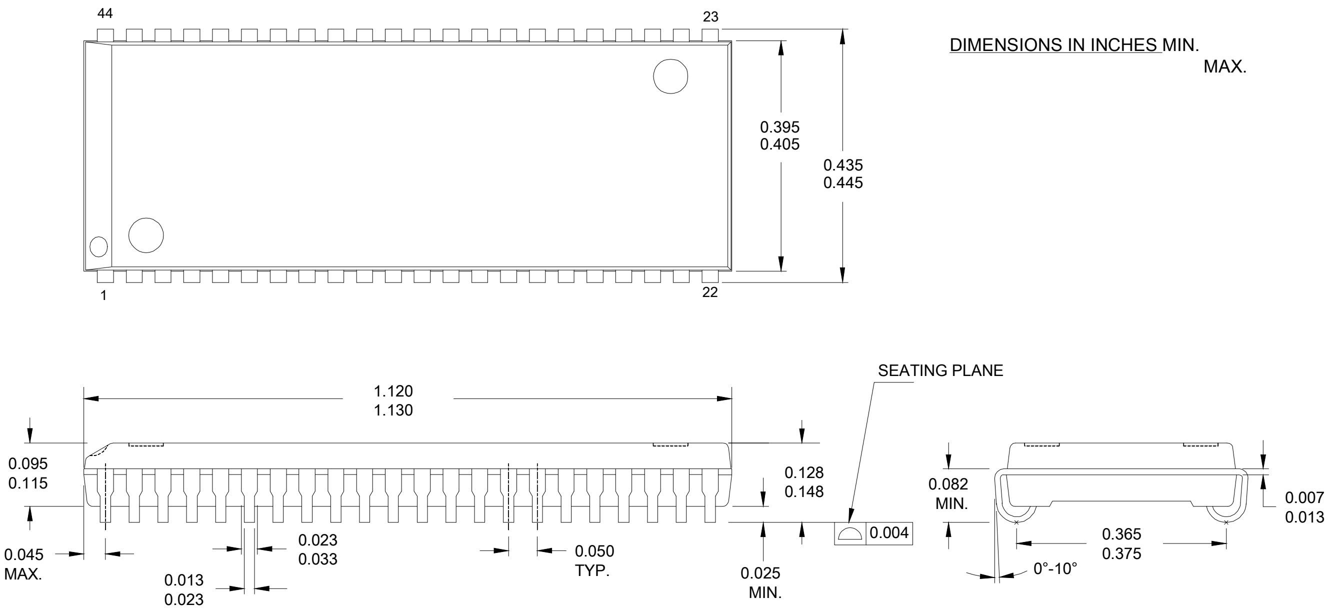
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1021CV33-10VXC	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Commercial
	CY7C1021CV33-10ZXC	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-10BAXI	51-85096	48-ball FBGA (Pb-free)	Industrial
	CY7C1021CV33-10ZXI	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-10ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A
12	CY7C1021CV33-12ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial
	CY7C1021CV33-12VXE	51-85082	44-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1021CV33-12ZSXE	51-85087	44-pin TSOP Type II (Pb-free)	
	CY7C1021CV33-12BAE	51-85096	48-ball FBGA	
15	CY7C1021CV33-15ZSXA	51-85087	44-pin TSOP Type II (Pb-free)	Automotive-A

The 44 pin TSOP II package containing the Automotive grade device is designated as “ZS”, while the same package containing the Commercial/Industrial grade device is “Z”.

Package Diagrams

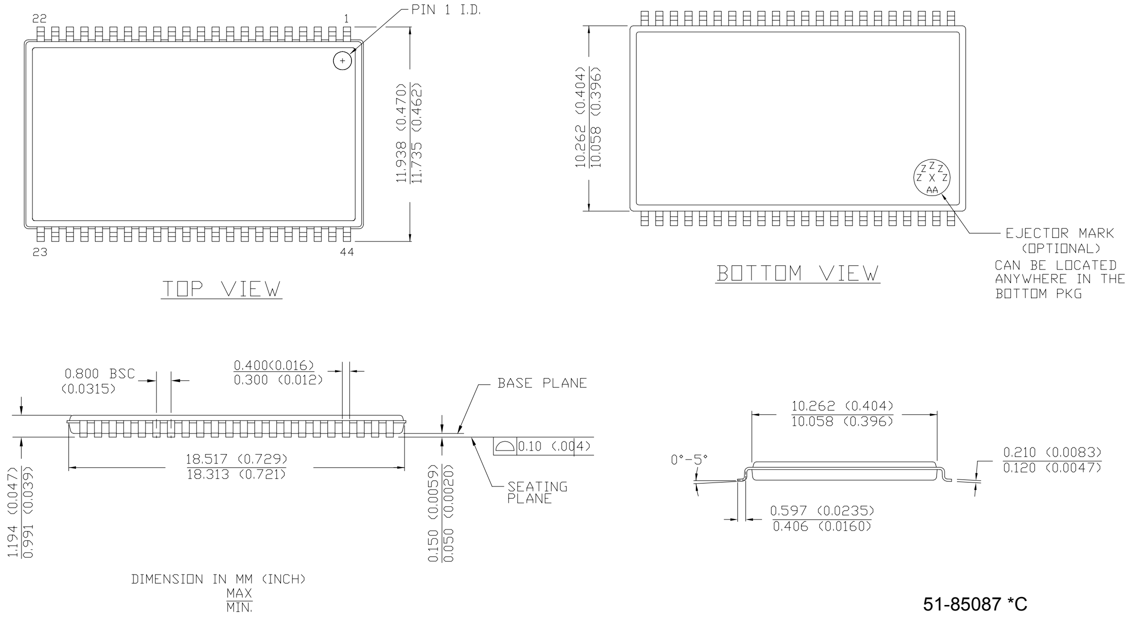
Figure 9. 44-Pin (400 Mil) Molded SOJ



51-85082 *C

Package Diagrams (continued)

Figure 10. 44-Pin Thin Small Outline Package Type II



Package Diagrams (continued)

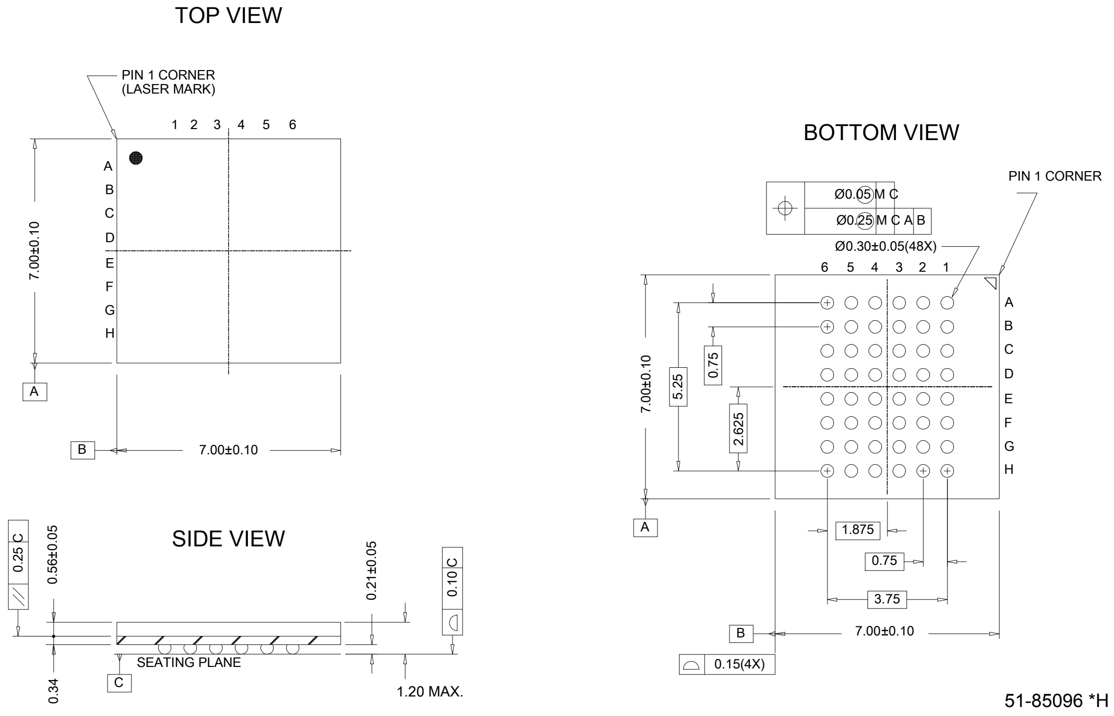


Figure 11. 48-Ball FBGA (7 x 7 x 1.2 mm)

Document History Page

Document Title: CY7C1021CV33, 1-Mbit (64K x 16) Static RAM **Document Number: 38-05132**				
REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	109472	12/06/01	HGK	New data sheet
*A	115044	05/08/02	HGK	Ram7 version C4K x 16 Async Removed “Preliminary”
*B	115808	06/25/02	HGK	I_{SB1} and I_{CC} values changed
*C	120413	10/31/02	DFP	Updated BGA pin E4 to NC
*D	238454	See ECN	RKF	1) Added Automotive Specifications to datasheet 2) Added Pb-free devices in the Ordering Information
*E	334398	See ECN	SYT	Added Pb-free on page 9 and 10
*F	493565	See ECN	NXR	Added Automotive-A operating range Corrected typo in the Pin Definition table Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I/O_S parameter from DC Electrical Characteristics table Updated the ordering information table
*G	563963	See ECN	VKN	Added t_{POWER} specification in the AC Switching Characteristics table Added footnote 8
*H	1390863	See ECN	VKN/AESA	Corrected TSOP II package outline
*I	1891366	See ECN	VKN/AESA	Added -10ZSXA part in the Ordering Information table Updated Ordering Information Table
*J	2880096	02/17/2010	VKN/AESA	Added “CY7C1021CV33-10ZXI” part in the Ordering Information table Updated package diagrams.
*K	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams

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