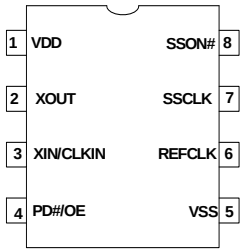
Pinouts

Figure 1. CY25100 8-Pin SOIC/TSSOP



Pin Description

Pin	Name	Description
1	VDD	3.3V power supply.
2	XOUT	Crystal output. Leave this pin floating if external clock is used.
3	XIN/CLKIN	Crystal input or reference clock input.
4	PD#/OE	Power down pin: Active LOW. If PD# = 0, PLL and Xtal are powered down, and outputs are weakly pulled low. Output Enable pin: Active HIGH. If OE = 1, SSCLK and REFCLK are enabled. User has the option of choosing either PD# or OE function.
5	VSS	Power supply ground.
6	REFCLK	Buffered reference output.
7	SSCLK	Spread spectrum clock output.
8	SSON#	Spread spectrum control. 0 = spread on. 1 = spread off.

General Description

The CY25100 is a Spread Spectrum Clock Generator (SSCG) IC used to reduce EMI found in today's high speed digital electronic systems.

The device uses a Cypress proprietary PLL and Spread Spectrum Clock (SSC) technology to synthesize and modulate the frequency of the input clock. By frequency modulating the clock, the measured EMI at the fundamental and harmonic frequencies are greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory agency (EMC) requirements and improve time-to-market without degrading system performance.

The CY25100 uses a factory or field-programmable configuration memory array to synthesize output frequency, spread percentage, crystal load capacitor, reference clock output on/off, spread spectrum on/off function, and PD#/OE options.

The spread percentage is programmed to either center spread or down spread with various spread percentages. The range for center spread is from ±0.25% to ±2.50%. The range for down spread is from –0.5% to –5.0%. Contact the factory for smaller or larger spread percentage amounts, if required.

The input to the CY25100 can either be a crystal or a clock signal. The input frequency range for crystals is 8 to 30 MHz, and for clock signals is 8 to 166 MHz.

The CY25100 has two clock outputs, REFCLK and SSCLK. The non spread spectrum REFCLK output has the same frequency as the input of the CY25100. The frequency modulated SSCLK output can be programmed from 3 to 200 MHz.

The CY25100 products are available in 8-pin SOIC and TSSOP packages with commercial and industrial operating temperature ranges.

Table 1.

Pin Function	Input Frequency	Total Xtal Load Capacitance	Output Frequency	Spread Percent (0.5% – 5%, 0.25% Intervals)	Reference Output	Power down or Output Enable	Frequency Modulation
Pin Name	XIN and XOUT	XIN and XOUT	SSCLK	SSCLK	REFOUT	PD#/OE	SSCLK
Pin#	3 and 2	3 and 2	7	7	6	4	7
Unit	MHz	pF	MHz	%	On or Off	Select PD# or OE	kHz
Program Value	ENTER DATA	ENTER DATA	ENTER DATA	ENTER DATA	ENTER DATA	ENTER DATA	31.5

Programming Description

Field Programmable CY25100

The CY25100 is programmed at the package level, that is, in a programmer socket. The CY25100 is Flash based, so the parts can be reprogrammed up to 100 times. This allows fast and easy design changes and product updates, and eliminates any issues with old and out-of-date inventory.

Samples and small prototype quantities can be programmed on the CY3672 programmer with CY3690 (TSSOP) or CY3691 (SOIC) socket adapter.

CyberClocks™ Online Software

CyberClocks™ Online Software is a web based software application that allows the user to custom-configure the CY25100. All the parameters in Table 1 given as “Enter Data” can be programmed into the CY25100. CyberClocks Online outputs an industry-standard JEDEC file used for programming the CY25100. CyberClocks Online is available at www.cyberclocksonline.com web site through user registration. To register, fill out the registration form and make sure to check the “non-standard devices” box. For more information on the registration process refer to CY3672 data sheet

For information regarding spread spectrum software programming solutions, contact your local Cypress sales representative or Field Application Engineer (FAE).

CY3672 FTG Programming Kit and CY3690/CY3691 Socket Adapter

The Cypress CY3672 FTG programmer and CY3690 and CY3691 socket adapters are required to program the CY25100. The CY3690 enables users to program CY25100ZCF and CY25100ZIF (TSSOP). CY3691 provides the ability to program CY25100SCF and CY25100SIF (SOIC). Each socket adapter comes with small prototype quantities of CY25100. The CY3690 and CY3691 is a separate orderable item, so the existing users of the CY3672 FTG development kit or CY3672-PRG programmer need to order only the socket adapters to program the CY25100.

Factory Programmable CY25100

Factory programming is available for volume manufacturing by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. A sample request form (refer to “CY25100 Sample Request Form” at www.cypress.com) must be completed. After the request is processed, you will receive a new part number, samples, and data sheet with the programmed values. This part number is used for additional sample requests and production orders.

Additional information on the CY25100 can be obtained from the Cypress web site at www.cypress.com.

Product Functions

Input Frequency (XIN, Pin 3 and XOUT, Pin 2)

The input to the CY25100 can be a crystal or a clock. The input frequency range for crystals is 8 to 30 MHz, and for clock signals is 8 to 166 MHz.

C_{XIN} and C_{XOUT} (Pin 3 and Pin 2)

The load capacitors at Pin 1 ($\mathbf{C_{XIN}}$) and Pin 8 ($\mathbf{C_{XOUT}}$) can be programmed from 12 pF to 60 pF with 0.5 pF increments. The programmed value of these on-chip crystal load capacitors are the same (XIN = XOUT = 12 to 60 pF).

The required values of $\mathbf{C_{XIN}}$ **and** $\mathbf{C_{XOUT}}$ are calculated using the following formula:

$C_{XIN} = C_{XOUT} = 2C_L – C_P$

where C_L is the crystal load capacitor as specified by the crystal manufacturer and C_P is the parasitic PCB capacitance.

For example, if a fundamental 16 MHz crystal with C_L of 16 pF is used and C_P is 2 pF, C_{XIN} and C_{XOUT} are calculated as:

$C_{XIN} = C_{XOUT} = (2 \times 16) – 2 = 30$ pF

If using a driven reference, set C_{XIN} and C_{XOUT} to the minimum value 12 pF.

Output Frequency, SSCLK Output (SSCLK, Pin 7)

The modulated frequency at the SSCLK output is produced by synthesizing the input reference clock. The modulation can be stopped by SSON# digital control input (SSON# = HIGH, no modulation). If modulation is stopped, the clock frequency is the nominal value of the synthesized frequency without modulation (spread percentage = 0). The range of synthesized clock is from 3 to 200 MHz.

Spread Percentage (SSCLK, Pin 7)

The SSCLK spread can be programmed at any percentage value from ±0.25% to ±2.5% for center spread and from –0.5% to –5.0% down spread.

Reference Output (REFOUT, Pin 6)

The reference clock output has the same frequency and the same phase as the input clock. This output can be programmed to be enabled (clock on) or disabled (High-Z, clock off). If this output is not required, it is recommended that users request the disabled (High-Z, Clock Off) option.

Frequency Modulation

The frequency modulation is programmed at 31.5 kHz for all SSCLK frequencies from 3 to 200 MHz. Contact the factory if a higher modulation frequency is required.

Power Down or Output Enable (PD# or OE, Pin 4)

The part can be programmed to include either PD# or OE function. PD# function powers down the oscillator and PLL. The OE function disables the outputs.

Absolute Maximum Rating

Supply Voltage (V_{DD}) ..... –0.5 to +7.0V
DC Input Voltage ..... –0.5V to V_{DD} + 0.5
Storage Temperature (Non condensing) ..... –55°C to +125°C
Junction Temperature ..... –40°C to +125°C
Data Retention at Tj = 125°C ..... > 10 years
Package Power Dissipation ..... 350 mW
Static Discharge Voltage ..... ≥ 2000V (per MIL-STD-883, Method 3015)

Recommended Crystal Specifications

Parameter	Description	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal Crystal Frequency	Parallel resonance, fundamental mode, AT cut	8	–	30	MHz
C_{LNOM}	Nominal Load Capacitance	Internal load caps	6	–	30	pF
R_1	Equivalent Series Resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of Third Overtone Mode ESR to Fundamental Mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	–
DL	Crystal Drive Level	No external series resistor assumed	–	0.5	2	mW

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	3.13	3.30	3.45	V
T_A	Ambient Commercial Temperature	0	–	70	°C
	Ambient Industrial Temperature	–40	–	85	°C
C_{LOAD}	Maximum Load Capacitance at Pin 6 and Pin 7	–	–	15	pF
F_{ref}	External Reference Crystal (Fundamental tuned crystals only)	8	–	30	MHz
	External Reference Clock	8	–	166	MHz
F_{SSCLK}	SSCLK Output Frequency, C_{LOAD} = 15 pF	3	–	200	MHz
F_{REFCLK}	REFCLK Output Frequency, C_{LOAD} = 15 pF	8	–	166	MHz
F_{MOD}	Spread Spectrum Modulation Frequency	30.0	31.5	33.0	kHz
T_{PU}	Power Up Time for all VDDs to reach minimum specified voltage (power ramp must be monotonic)	0.05	–	500	ms

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, V_{DD} = 3.3V (source)	10	12		mA
I_{OL}	Output Low Current	V_{OL} = 0.5, V_{DD}= 3.3V (sink)	10	12		mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7V_{DD}	–	V_{DD}	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3V_{DD}	V
I_{IH}	Input High Current, PD#/OE and SSON# Pins	$V_{in} = V_{DD}$	–	–	10	µA
I_{IL}	Input Low Current, PD#/OE and SSON# Pins	$V_{in} = V_{SS}$	–	–	10	µA
I_{OZ}	Output Leakage Current	Three-state output, PD#/OE = 0	–10		10	µA
C_{XIN} or C_{XOUT}[1]	Programmable Capacitance at Pin 2 and Pin 3	Capacitance at minimum setting	–	12	–	pF
		Capacitance at maximum setting	–	60	–	pF
C_{IN}[1]	Input Capacitance at Pin 4 and Pin 8	Input pins excluding XIN and XOUT	–	5	7	pF

Note
1. Guaranteed by characterization, not 100% tested.

DC Electrical Characteristics (continued)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{VDD}	Supply Current	V_{DD} = 3.45V, Fin = 30 MHz, REFCLK = 30 MHz, SSCLK = 66 MHz, C_{LOAD} = 15 pF, PD#/OE = SSON# = V_{DD}	–	25	35	mA
I_{DDS}	Standby Current	V_{DD} = 3.45V, Device powered down with PD# = 0V (driven reference pulled down)	–	15	30	µA

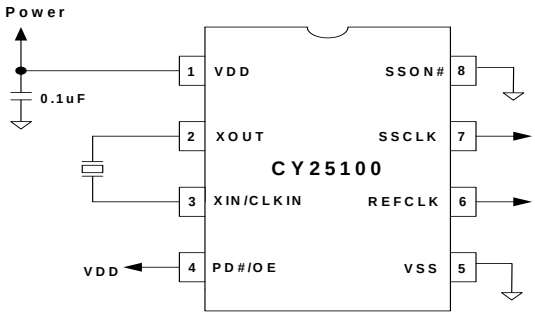
AC Electrical Characteristics [1]

Parameter	Description	Condition	Min	Typ	Max	Unit
DC	Output Duty Cycle	SSCLK, Measured at V_{DD}/2	45	50	55	%
	Output Duty Cycle	REFCLK, Measured at V_{DD}/2 Duty Cycle of CLKIN = 50% at input bias	40	50	60	%
SR1	Rising Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz. 20%–80% of V_{DD}	0.7	1.1	3.6	V/ns
SR2	Falling Edge Slew Rate	SSCLK from 3 to 100 MHz; REFCLK from 3 to 100 MHz. 80%–20% of V_{DD}	0.7	1.1	3.6	V/ns
SR3	Rising Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz 20%–80% of V_{DD}	1.0	1.6	4.0	V/ns
SR4	Falling Edge Slew Rate	SSCLK from 100 to 200 MHz; REFCLK from 100 to 166 MHz 80%–20% of V_{DD}	1.2	1.6	4.0	V/ns
T_{CCJ1}[2]	Cycle-to-Cycle Jitter SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK off	–	90	120	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK off	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK off	–	130	170	ps
T_{CCJ2}[2]	Cycle-to-Cycle Jitter SSCLK (Pin 7)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	105	140	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	200	260	ps
T_{CCJ3}[2]	Cycle-to-Cycle Jitter REFCLK (Pin 6)	CLKIN = SSCLK = 166 MHz, 2% spread, REFCLK on	–	80	100	ps
		CLKIN = SSCLK = 66 MHz, 2% spread, REFCLK on	–	100	130	ps
		CLKIN = SSCLK = 33 MHz, 2% spread, REFCLK on	–	135	180	ps
t_{STP}	Power down Time (pin 4 = PD#)	Time from falling edge on PD# to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE1}	Output Disable Time (pin 4 = OE)	Time from falling edge on OE to stopped outputs (Asynchronous)	–	150	350	ns
T_{OE2}	Output Enable Time (pin 4 = OE)	Time from rising edge on OE to outputs at a valid frequency (Asynchronous)	–	150	350	ns
t_{PU1}	Power Up Time, Crystal is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous)	–	3.5	5	ms
t_{PU2}	Power Up Time, Reference clock is used	Time from rising edge on PD# to outputs at valid frequency (Asynchronous), reference clock at correct frequency	–	2	3	ms

Note
2. Jitter is configuration dependent. Actual jitter is dependent on XIN jitter and edge rate, number of active outputs, output frequencies, spread percentage, temperature, and output load.

Application Circuit

Figure 2. Application Circuit Diagram[3, 4, 5]



Switching Waveforms

Figure 3. Duty Cycle Timing (DC = t_{1A}/t_{1B})

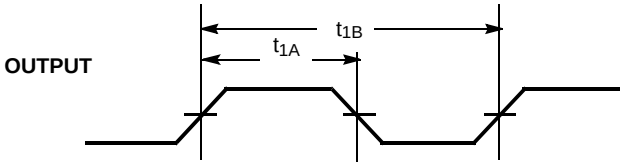
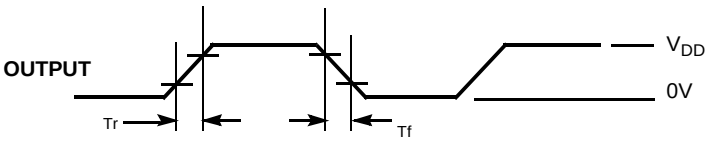


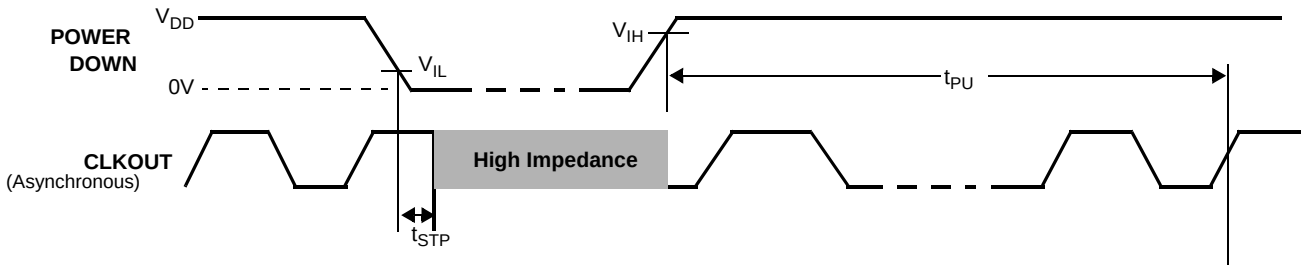
Figure 4. Output Rise/Fall Time (SSCLK and REFCLK)



Output Rise time (Tr) = (0.6 x V_{DD})/SR1 (or SR3)
Output Fall time (Tf) = (0.6 x V_{DD})/SR2 (or SR4)

Refer to AC Electrical Characteristics table for SR (Slew Rate) values.

Figure 5. Power Down and Power Up Timing

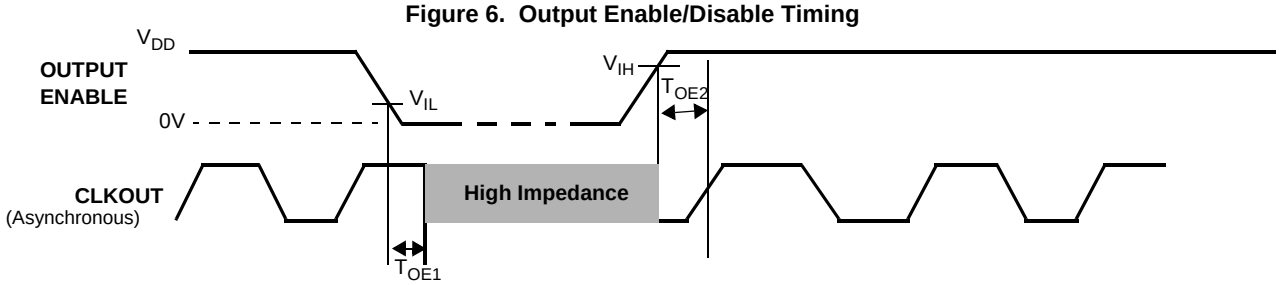


Notes

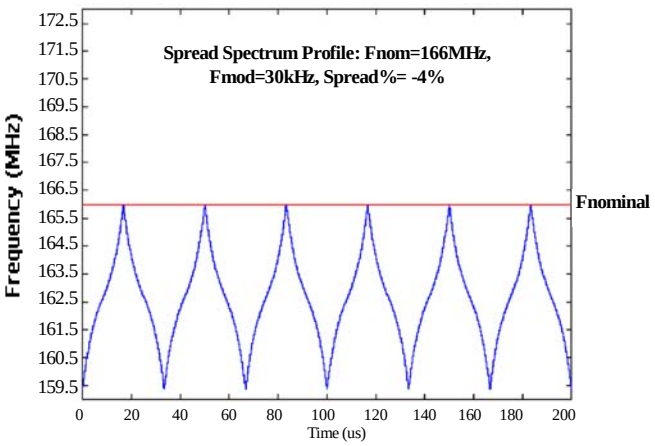
3. Because the load capacitors (C_{XIN} and C_{XOUT}) are provided by the CY25100, no external capacitors are needed on the XIN and XOUT pins to match the crystal load capacitor (C_L). Only a single 0.1-µF bypass capacitor is required on the V_{DD} pin.
4. If an external clock is used, apply the clock to XIN (pin 3) and leave XOUT (pin 2) floating (unconnected).
5. If SSON# (pin 8) is LOW (V_{SS}), the frequency modulation is on at SSCLK pin (pin 7).

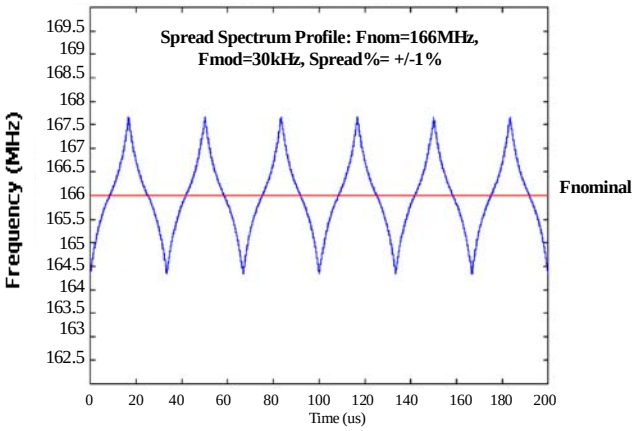
Switching Waveforms

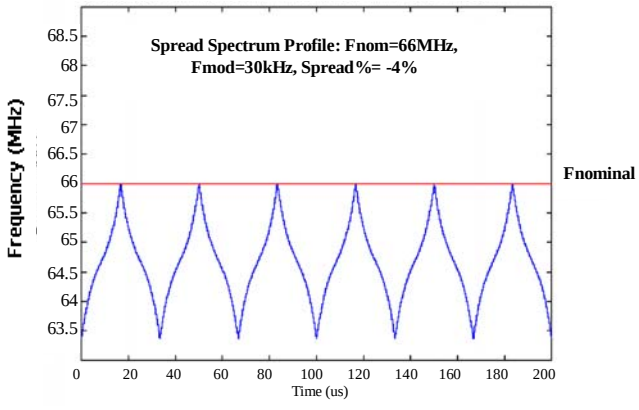
Figure 6. Output Enable/Disable Timing

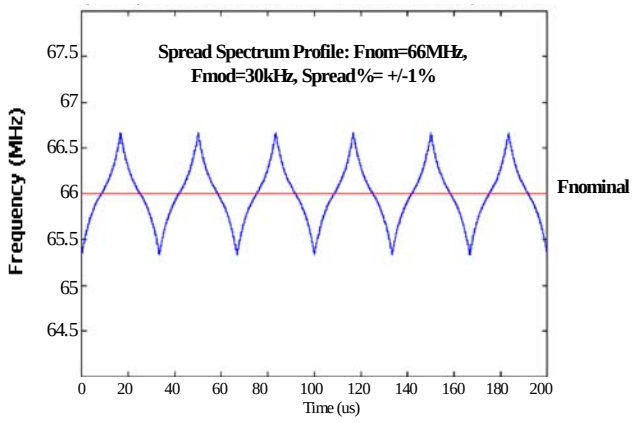


Informational Graphs [6]

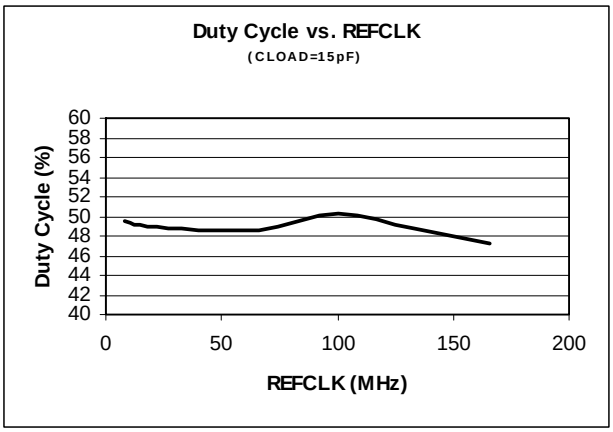


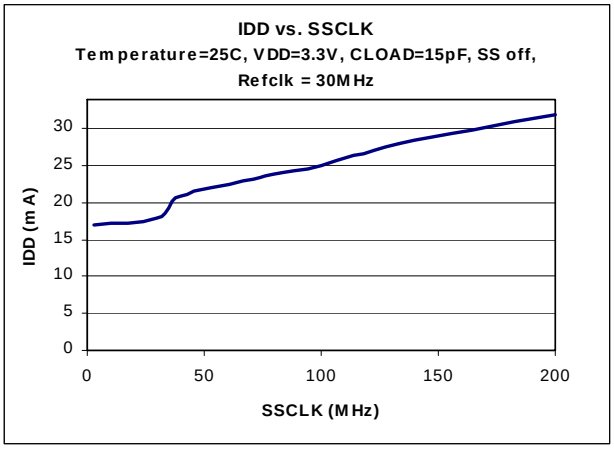


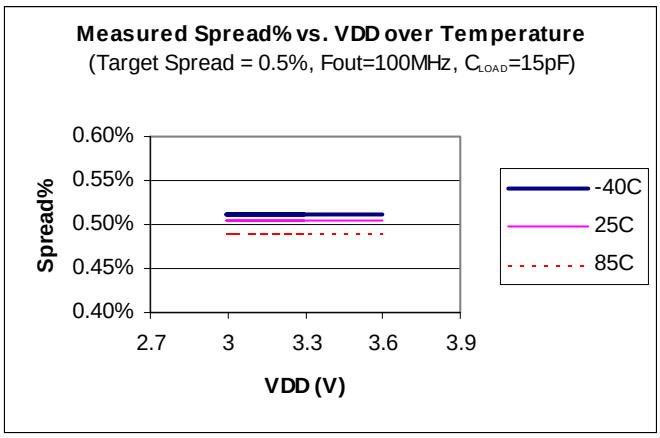


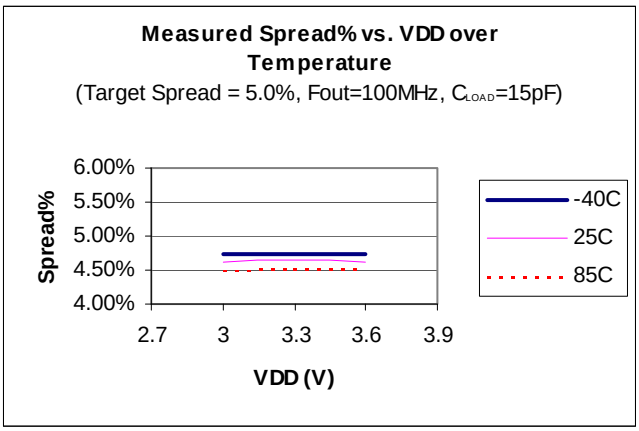


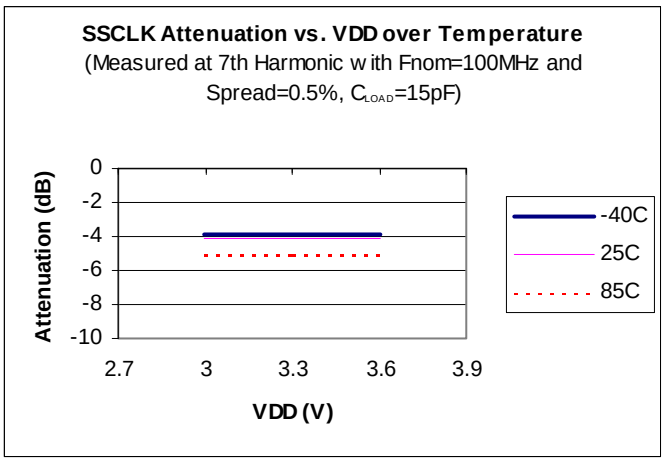
Informational Graphs (continued)[6]

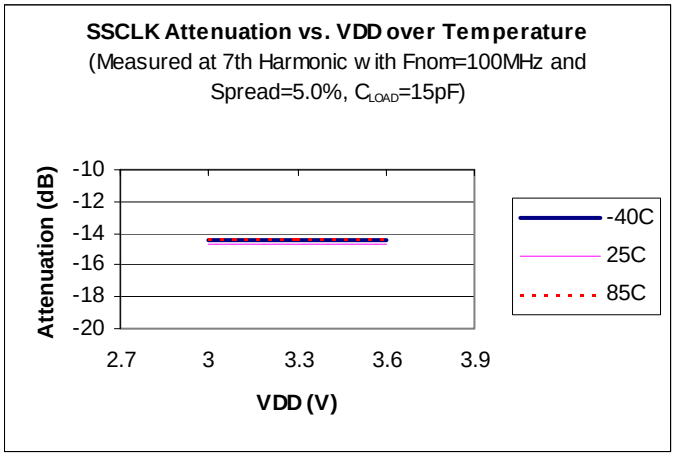










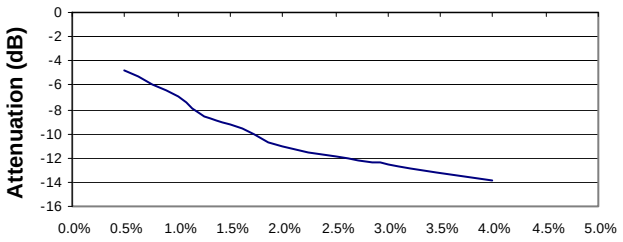


Note

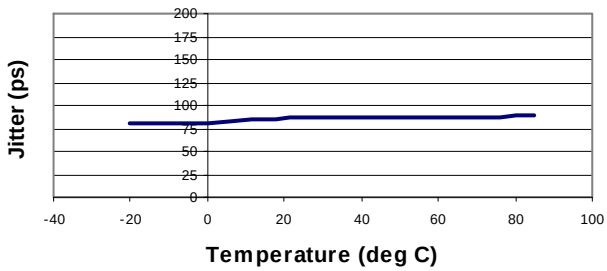
6. The Informational Graphs are meant to convey the typical performance levels. No performance specifications is implied or guaranteed. Refer to the tables on pages 4 and 5 for device specifications.

Informational Graphs (continued)[6]

SSCLK EMI Attenuation vs. Spread%
(Measured at 7th Harmonic Temp=25C, VDD=3.3V, SSCLK=100MHz, Measured on Cypress Characterization board with CLOAD=15pF)



Max Cycle-Cycle Jitter on SSCLK vs. Temperature
(SSCLK=100MHz, VDD=3.3V, CLOAD=15pF, +/- 2%spread, REFCLK off)

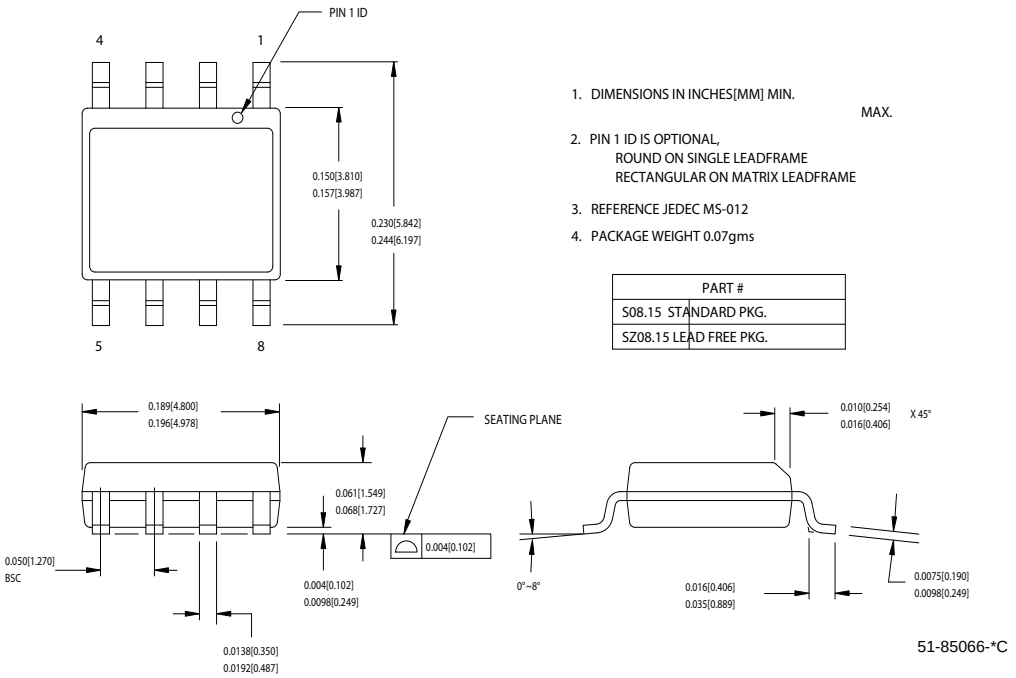


Ordering Information

Part Number	Package Description	Product Flow
Pb-Free		
CY25100SXCF	8-Pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25100SXIF	8-Pin Small Outline Integrated Circuit (SOIC)	Industrial, –40 to 85°C
CY25100ZXCF	8-Pin Thin Shrunk Small Outline Package (TSSOP)	Commercial, 0 to 70°C
CY25100ZXIF	8-Pin Thin Shrunk Small Outline Package (TSSOP)	Industrial, –40 to 85°C
CY25100SXC-xxxw[7]	8-Pin Small Outline Integrated Circuit (SOIC)	Commercial, 0 to 70°C
CY25100SXC-xxxwT[7]	8-Pin Small Outline Integrated Circuit (SOIC) - Tape and Reel	Commercial, 0 to 70°C
CY25100SXI-xxxw[7]	8-Pin Small Outline Integrated Circuit (SOIC)	Industrial, –40 to 85°C
CY25100SXI-xxxwT[7]	8-Pin Small Outline Integrated Circuit (SOIC) -Tape and Reel	Industrial, –40 to 85°C
CY25100ZXC-xxxw[7]	8-Pin Thin Shrunk Small Outline Package (TSSOP)	Commercial, 0 to 70°C
CY25100ZXC-xxxwT[7]	8-Pin Thin Shrunk Small Outline Package (TSSOP) - Tape and Reel	Commercial, 0 to 70°C
CY25100ZXI-xxxw[7]	8-Pin Thin Shrunk Small Outline Package (TSSOP)	Industrial, –40 to 85°C
CY25100ZXI-xxxwT[7]	8-Pin Thin Shrunk Small Outline Package (TSSOP) -Tape and Reel	Industrial, –40 to 85°C
CY3672-USB	FTG Programmer, for part numbers ending in “F”	n/a
CY3690	CY25100ZXCF/IF Socket Adapter (TSSOP) for use with CY3672-USB	n/a
CY3691	CY25100SXCF/IF Socket Adapter (SOIC) for use with CY3672-USB	n/a

Package Diagrams

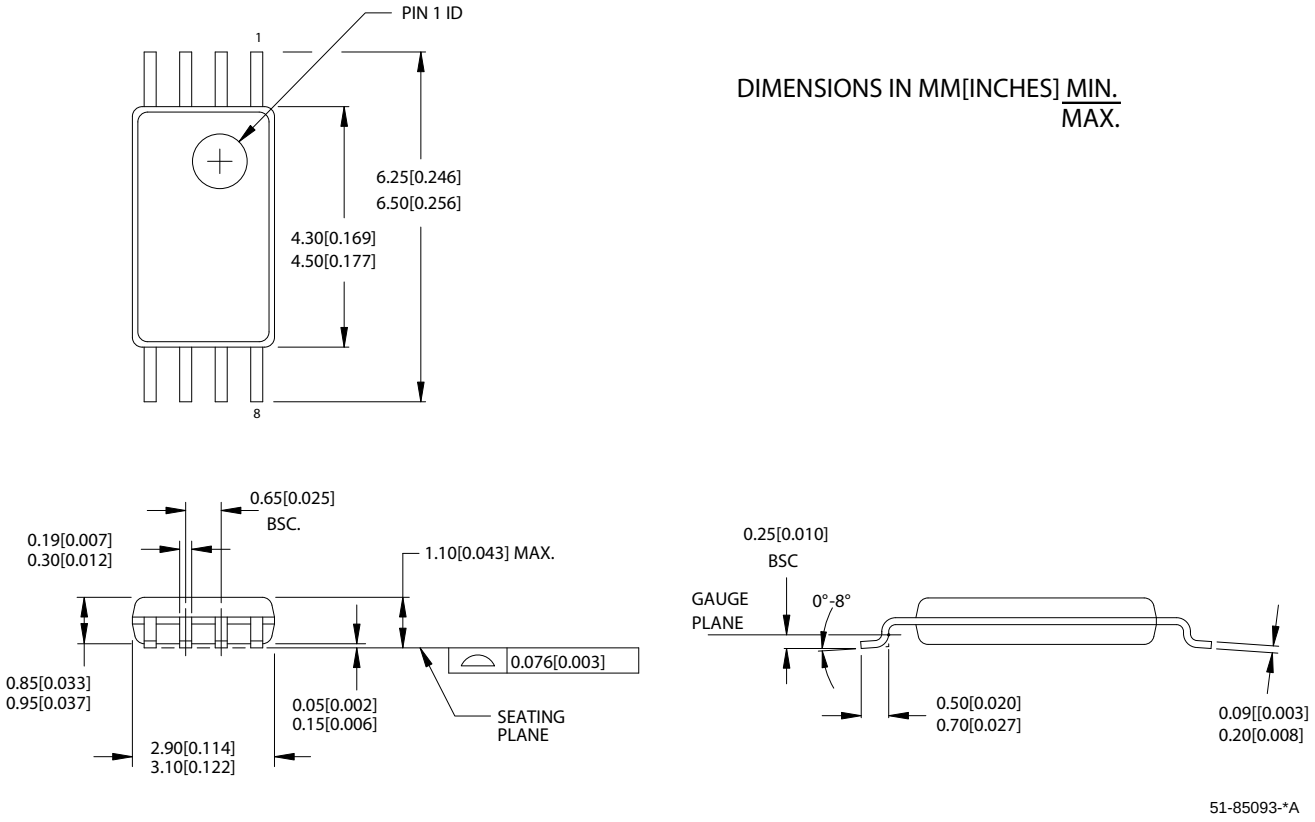
Figure 6. 8-Pin (150-Mil) SOIC S8



Notes
7. “xxx” denotes the assigned product dash number. “w” denotes the different programmed frequency and spread percentage options.
8. Not recommended for new designs.

Package Diagrams (continued)

Figure 7. 8-Pin Thin Shrunk Small Outline Package (4.40 mm Body) Z8



Document History Page

Document Title: CY25100 Field and Factory Programmable Spread Spectrum Clock Generator for EMI Reduction Document Number: 38-07499				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	126578	CKN	06/27/03	New Data Sheet
*A	128753	IJATMP	08/29/03	Changes to reflect field programmability
*B	130342	RGL	12/02/03	Changes to Application Circuit diagram and correction to the package description listed under the Ordering Information table for CY3690 and CY3691.
*C	204121	RGL	See ECN	Add Industrial Temperature Range Corrected the Ordering Information to match the DevMaster
*D	215392	RGL	See ECN	Added Lead Free devices
*E	2513909	AESA	06/10/08	Updated template. Added Note “Not recommended for new designs.” Added part number CY25100KSXCF, CY25100KSXIF, CY25100KSXI-xxx, CY25100KZXC-xxx, CY25100KZXI-xxx, CY25100KSXI-xxxT, CY25100KZXC-xxxT, CY25100KZXI-xxxT, and CY25100KZXIF in ordering information table. Added Pb-Free header in the ordering information table. Removed Pb-Free from Package description in the ordering information table. Changed CY3672-PRG with CY3672-USB in the ordering information table. Removed CY25100SCF, CY25100SIF, CY25100ZCF, CY25100ZIF, and CY3672 in the ordering information table. Changed Lead free to Pb-Free.
*F	2601881	KVM/PYRS	11/06/08	Rising edge slew rate (SR3) minimum limit changed from 1.2V/ns to 1.0V/ns. Removed part numbers added in rev *E.

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