

CM3202-00

DDR VDDQ and VTT Termination Voltage Regulator

Product Description

The CM3202-00 is a dual-output low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFET's, the CM3202-00 can source up to 2 A of V_{DDQ} continuous current, and source or sink up to 2 A V_{TT} continuous current. The typical dropout voltage for V_{DDQ} is 500 mV at 2 A load current.

The CM3202-00 provides fast response to transient load changes. Load regulation is excellent, from no load to full load. It also has built-in over-current limits and thermal shutdown at 170°C.

The CM3202-00 supports Suspend-To-RAM (STR) and ACPI compliance with shutdown mode which tri-states V_{TT} to minimize quiescent system current.

The CM3202-00 is packaged in an easy-to-use WDFN8. Low thermal resistance allows it to withstand high power dissipation at 85°C ambient. It operates over the industrial ambient temperature range of -40°C to 85°C.

Features

- Two Linear Regulators
 - ♦ Maximum 2 A Current from V_{DDQ}
 - ♦ Source and Sink Up to 2 A V_{TT} Current
- 1.7 V to 2.8 V Adjustable V_{DDQ} Output Voltage
- 500 mV Typical V_{DDQ} Dropout Voltage at 2 A
- V_{TT} Tracking at 50% of V_{DDQ}
- Excellent Load and Line Regulation, Low Noise
- Fast Transient Response
- Meet JEDEC DDR-I and DDR-II Memory Power Spec.
- Linear Regulator Design Requires No Inductors and Has Low External Component Count
- Integrated Power MOSFETs
- Dual Purpose ADJ/Shutdown Pin
- Built-In Over-Current Limit and Thermal Shutdown for V_{DDQ} and V_{TT}
- Fast Transient Response
- Low Quiescent Current
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DDR Memory and Active Termination Buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems
- Routers and Switchers
- DVD Recorders
- 3D AGP Cards
- LCD TV and STB



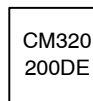
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WDFN8
DE SUFFIX
CASE 511BH

MARKING DIAGRAM



CM320 200DE = CM3202-00DE

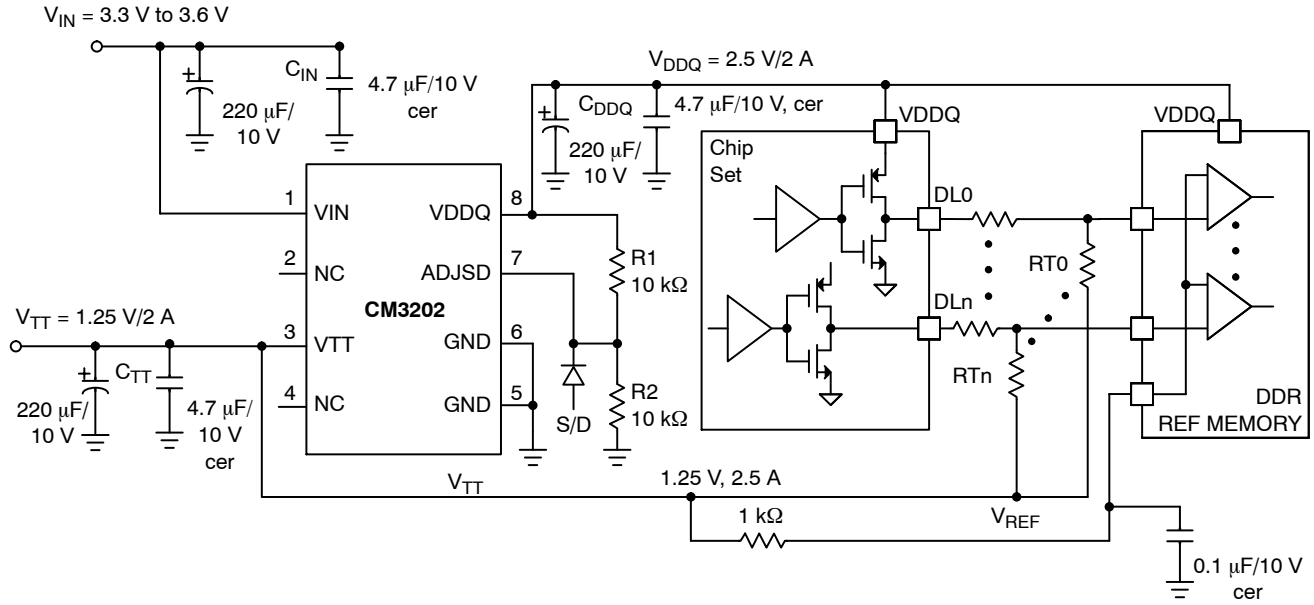
ORDERING INFORMATION

Device	Package	Shipping†
CM3202-00DE	WDFN8 (Pb-Free)	3000/Tape & Reel

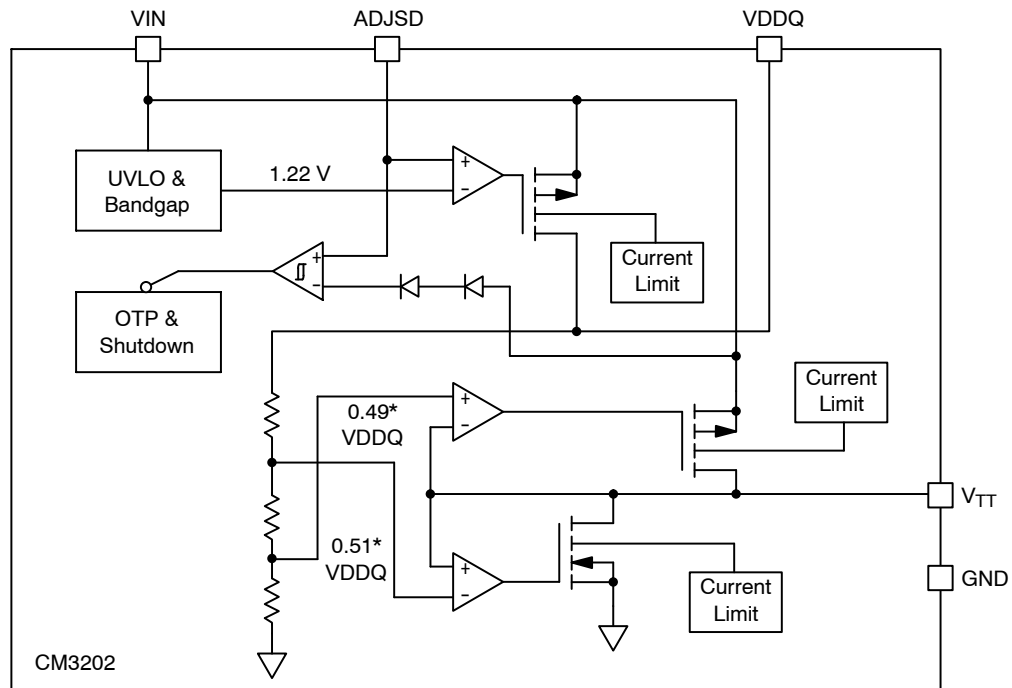
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CM3202-00

TYPICAL APPLICATION



FUNCTIONAL BLOCK DIAGRAM



CM3202-00

PACKAGE / PINOUT DIAGRAMS

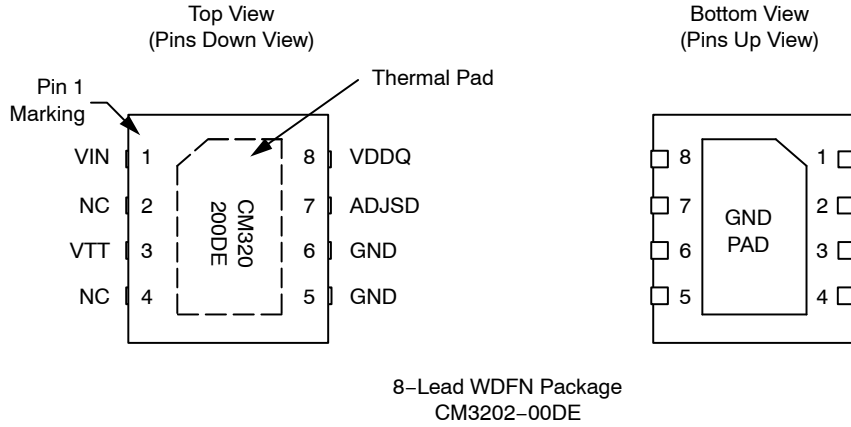


Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	VIN	Input supply voltage pin. Bypass with a 220 μ F capacitor to GND.
2	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
3	VTT	V_{TT} regulator output pin, which is preset to 50% of V_{DDQ} .
4	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
5	GND	Ground pin (analog).
6	GND	Ground pin (power).
7	ADJSD	<p>This pin is for V_{DDQ} output voltage adjustment. It is available as long as V_{DDQ} is enabled. During Manual/Thermal shutdown, it is tightened to GND. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD:</p> $V_{DDQ} = 1.25 \text{ V} \times ((R1 + R2) / R2)$ <p>Where R1 is the upper resistor and R2 is the ground-side resistor. In addition, the ADJSD pin functions as a Shutdown pin. When ADJSD voltage is higher than 2.7 V (SHDN_H), the circuit is in Shutdown mode. When ADJSD voltage is below 1.5 V (SHDN_L), both V_{DDQ} and V_{TT} are enabled. A low-leakage Schottky diode in series with ADJSD pin is recommended to avoid interference with the voltage adjustment setting.</p>
8	VDDQ	V_{DDQ} regulator output voltage pin.
EPad	GND	The backside exposed pad which serves as the package heatsink. Must be connected to GND.

SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
VIN to GND	[GND – 0.3] to +6.0	V
Pin Voltages VDDQ, VTT to GND ADJSD to GND	[GND – 0.3] to +6.0 [GND – 0.3] to +6.0	V
Output Current VDDQ / VTT, Continuous (Note 1) VDDQ / VTT, Peak VDDQ Source + VTT Source	2.0 / ± 2.0 2.8 / ± 2.8 3	A
Temperature Operating Ambient Operating Junction Storage	–40 to +85 –40 to +170 –40 to +150	°C
Thermal Resistance, RJA (Note 2) WDFN8, 3 mm x 3 mm	55	°C / W
Continuous Power Dissipation (Note 2) WDFN8, TA = 25°C / 85°C	2.6 / 1.5	W
ESD Protection (HBM)	2000	V
Lead Temperature (Soldering, 10 sec)	300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Despite the fact that the device is designed to handle large continuous/peak output currents, it is not capable of handling these under all conditions. Limited by the package thermal resistance, the maximum output current of the device cannot exceed the limit imposed by the maximum power dissipation value.
2. Measured with the package using a 4 in² / 2 layers PCB with thermal vias.

Table 3. STANDARD OPERATING CONDITIONS

Parameter	Rating	Units
Ambient Operating Temperature Range	–40 to +85	°C
VDDQ Regulator DDR–1 Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 s) CDDQ	3.1 to 3.6 0 to 2 2.5 220	V A A μ F
VTT Regulator DDR–1 Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 s) CTT	3.1 to 3.6 0 to ± 2.0 ± 2.50 220	V A A μ F
VIN Supply Voltage Range	3.10 to 3.60	V
VDDQ Source + VTT Source Load Current, Continuous Load Current, Peak (1 s)	2.5 3.5	A
Junction Operating Temperature Range	–40 to +150	°C

SPECIFICATIONS (Cont'd)

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
I_Q	Quiescent Current	$I_{DDQ} = 0, I_{TT} = 0$		8	15	mA
I_{SHDN}	Shutdown Current	$V_{ADJSD} = 3.3 \text{ V}$ (Shutdown)		0.1	0.5	mA
SHDN_H	ADJSD Logic High	(Note 2)	2.7			V
SHDN_L	ADJSD Logic Low				1.50	V
UVLO	Under-Voltage Lockout	Hysteresis = 100 mV	2.40	2.70	2.90	V
T_{OVER}	Thermal SHDN Threshold		150	170		°C
T_{HYS}	Thermal SHDN Hysteresis			50		°C
TEMPCO	V_{DDQ}, V_{TT} TEMP CO			150		ppm/°C

VDDQ Regulator

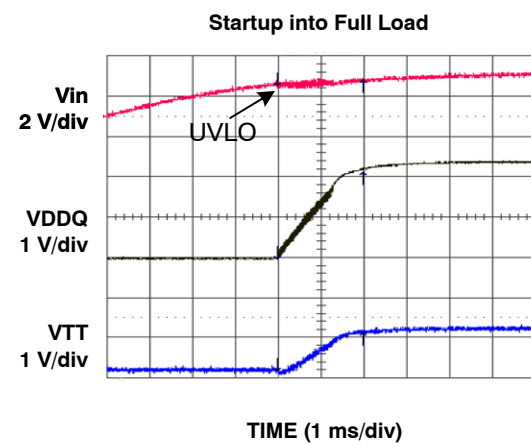
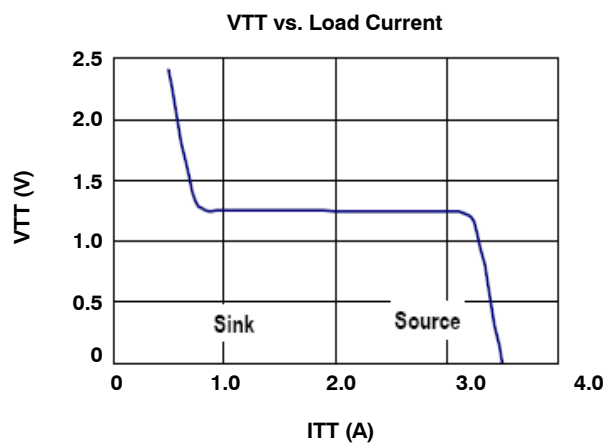
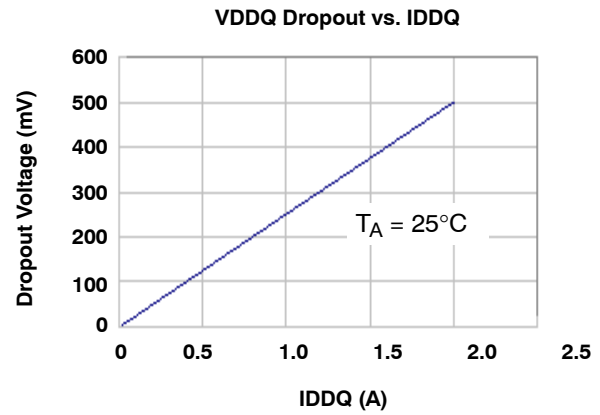
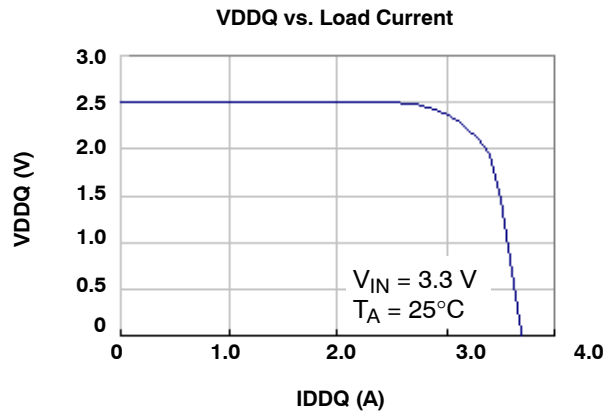
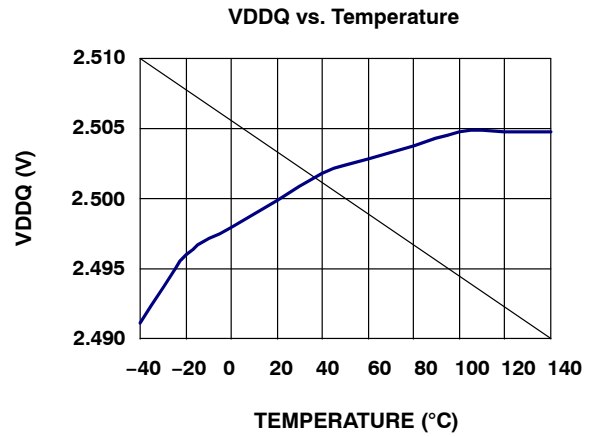
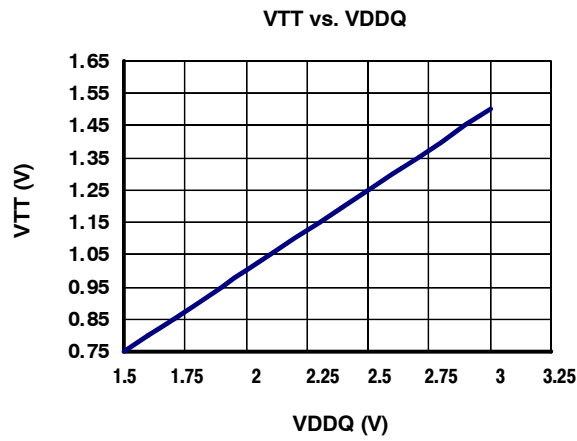
$V_{DDQ \text{ DEF}}$	VDDQ Output Voltage	$I_{DDQ} = 100 \text{ mA}$	2.450	2.500	2.550	V
$V_{DDQ \text{ LOAD}}$	VDDQ Load Regulation	$10 \text{ mA} \leq I_{DDQ} \leq 2 \text{ A}$ (Note 3)		10	25	mV
$V_{DDQ \text{ LINE}}$	VDDQ Line Regulation	$3.1 \text{ V} \leq V_{IN} \leq 3.6 \text{ V}, I_{DDQ} = 0.1 \text{ A}$		5	25	mV
V_{DROP}	VDDQ Dropout Voltage	$I_{DDQ} = 2 \text{ A}$ (Note 4)		500		mV
I_{ADJ}	ADJSD Bias Current			0.8	3.0	μA
$I_{DDQ \text{ LIM}}$	VDDQ Current Limit		2.0	2.5		A

VTT Regulator

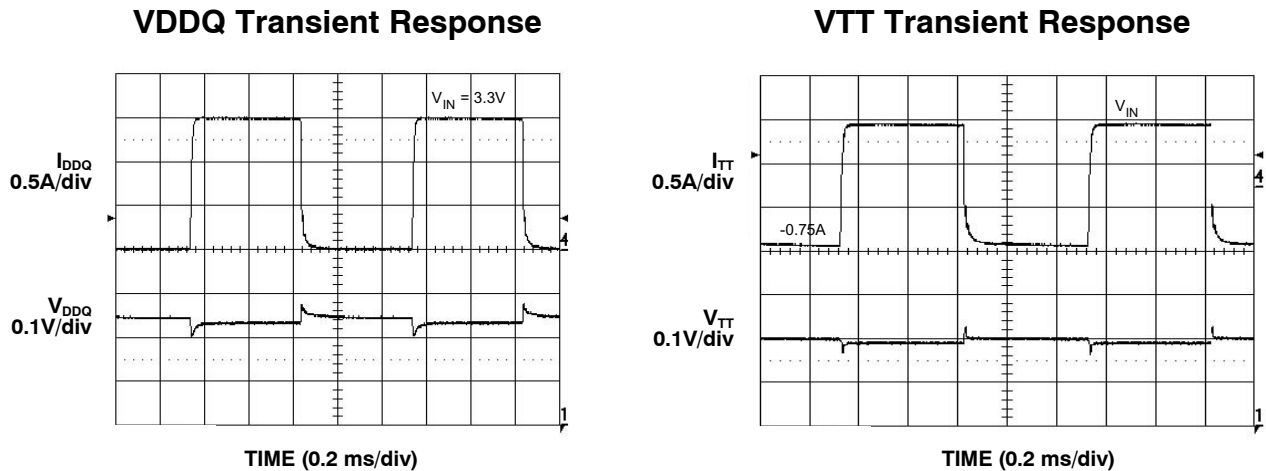
$V_{TT \text{ DEF}}$	VTT Output Voltage	$I_{TT} = 100 \text{ mA}$	1.225	1.250	1.275	V
$V_{TT \text{ LOAD}}$	VTT Load Regulation	Source, $0 \leq I_{TT} \leq 2 \text{ A}$ (Note 3) Sink, $-2 \text{ A} \leq I_{TT} \leq 0$ (Note 3)	-30	10 -10	30	mV
$V_{TT \text{ LINE}}$	VTT Line Regulation	$3.1 \text{ V} \leq V_{IN} \leq 3.6 \text{ V}, I_{TT} = 0.1 \text{ A}$		5	15	mV
$I_{TT \text{ LIM}}$	ITT Current Limit	Source / Sink (Note 3)	±2.0	±2.5		A
$I_{VTT \text{ OFF}}$	VTT Shutdown Leakage Current	Thermal Shutdown Enabled			10	μA

- $V_{IN} = 3.3 \text{ V}$, $V_{DDQ} = 2.50 \text{ V}$, $V_{TT} = 1.25 \text{ V}$ (default values), $C_{DDQ} = C_{TT} = 47 \text{ μF}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.
- The SHDN Logic High value is normally satisfied for full input voltage range by using a low leakage current (below 1 μA). Schottky diode at ADJSD control pin.
- Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed up to the maximum power dissipation.
- Dropout voltage is input to output voltage differential at which output voltage has dropped 100 mV from the nominal value obtained at 3.3 V input. It depends on load current and junction temperature.

TYPICAL OPERATING CHARACTERISTICS



TYPICAL OPERATING CHARACTERISTICS (Cont'd)



APPLICATION INFORMATION

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAM's transmit data at both the rising and falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2), and by the use of a termination voltage, V_{TT} . SSTL_2 is an industry standard defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ} , V_{TT} , and V_{REF} (see Typical DDR terminations, Class II). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5 V with a tolerance of ± 200 mV. The active bus termination voltage, V_{TT} , is half of V_{DDQ} . V_{REF} is a reference voltage that tracks half of V_{DDQ} , $\pm 1\%$, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ± 40 mV of V_{REF} .

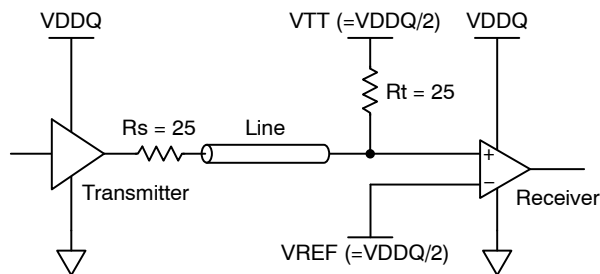


Figure 1. Typical DDR Terminations, Class II

APPLICATION INFORMATION (Cont'd)

The V_{TT} power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{\text{termination}} = \frac{405 \text{ mV}}{Rt(25 \Omega)} = 16.2 \text{ mA}$$

A typical 64 Mbyte SSTL-2 memory system, with 128 terminated lines, has a worst-case maximum V_{TT} supply current up to ±2.07 A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ±200 mA.

The VDDQ power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5 A to 1 A, with peaks up to 2 A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3202-00 Regulator

The CM3202-00 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TDFN-8 package. VDDQ regulator can supply up to 2 A current, and the two-quadrant V_{TT} termination regulator has current sink and source capability to ±2 A. The VDDQ linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500 mV at a 2 A output. The output voltage of VDDQ can be set by an external voltage divider. The use of regulators for both the upper and lower side of the VDDQ output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, V_{TT}, is regulated at VDDQ/2 by an internal resistor divider. Same as VDDQ, V_{TT} has the same fast transient response to load change in both directions. The V_{TT} regulator can source, as well as sink, up to 2 A current. The CM3202-00 is designed for optimal operation from a nominal 3.3 VDC bus, but can work with VIN as high as 5 V. When operating at higher VIN voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation.

V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from VDDQ to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The CM3202-00 requires that at least a 220 µF electrolytic capacitor be located near the V_{IN} pin for stability and to maintain the input bus voltage during load transients. An additional 4.7 µF ceramic capacitor between the V_{IN} and the GND, located as close as possible to those pins, is recommended to ensure stability.

At a minimum of a 220 µF electrolytic capacitor is recommended for the VDDQ output. An additional 4.7 µF ceramic capacitor between the VDDQ and GND, located very close to those pins, is recommended.

At a minimum of a 220 µF electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7 µF ceramic capacitor between the V_{TT} pin and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40 mV during the transition for source to sink. An average current step of ±0.5 A requires:

$$ESR < \frac{40 \text{ mV}}{1 \text{ A}} = 40 \text{ m}\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions.

APPLICATION INFORMATION (Cont'd)

Adjusting VDDQ Output Voltage

The CM3202-00 internal bandgap reference is set at 1.25 V. The V_{DDQ} voltage is adjustable by using a resistor divider, R₁ and R₂:

$$V_{DDQ} = V_{ADJ} \times \frac{R_1 + R_2}{R_2}$$

where V_{ADJ} = 1.25 V. For best regulator stability, we recommend that R₁ and R₂ not exceed 10 kΩ each.

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the VDDQ and the VTT outputs tri-state and could sink/source less than 10 μA. During shutdown, the quiescent current is reduced to less than 0.5 mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3202-00 is again enabled.

Current Limit, Foldback and Over-temperature Protection

The CM3202-00 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 2 A and V_{TT} limits the output current to approximately ±2 A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level, about 1 A, until the over-current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170°C (typical), the thermal protection circuitry triggers and tri-states both VDDQ and VTT outputs. Once the junction temperature has cooled to below about 120°C the CM3202-00 returns to normal operation.

Thermal Considerations**Typical Thermal Characteristics**

The overall junction to ambient thermal resistance (θ_{JA}) for device power dissipation (P_D) primarily consists of two paths in the series. The first path is the junction to the case (θ_{JC}) which is defined by the package style and the second path is case to ambient (θ_{CA}) thermal resistance which is dependent on board layout. The final operating junction temperature for any condition can be estimated by the following thermal equation:

$$\begin{aligned} T_{JUNC} &= T_{AMB} + P_D \times (\theta_{JC}) + P_D \times (\theta_{CA}) \\ &= T_{AMB} + P_D \times (\theta_{JA}) \end{aligned}$$

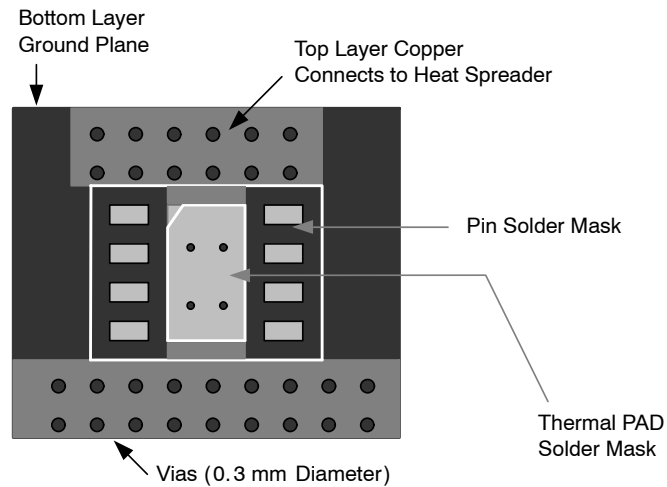
When a CM3202-00 using WDFN8 package is mounted on a double-sided printed circuit board with four square inches of copper allocated for "heat spreading," the θ_{JA} is approximately 55°C/W. Based on the over temperature limit of 170°C with an ambient temperature of 85°C, the available power of the package will be:

$$P_D = \frac{170^\circ C - 85^\circ C}{55^\circ C/W} = 1.5 W$$

APPLICATION INFORMATION (Cont'd)

PCB Layout Considerations

The CM3202-00 has a heat spreader attached to the bottom of the WDFN8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during the manufacturing, the heat will be transferred between the two pads. See the Thermal Layout, the CM3202-00 shows the recommended PCB layout. Please be noted that there are four vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can be resulted in blocking of the solder. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat-dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202-00 to ambient, θ_{JA} , of approximately 55°C/W.

Top View**Figure 2. Thermal Layout for WDFN8 Package**

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

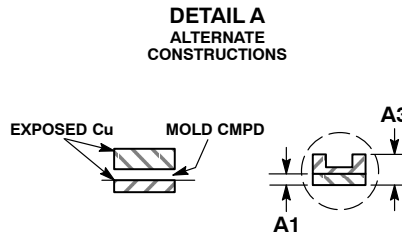
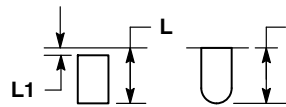
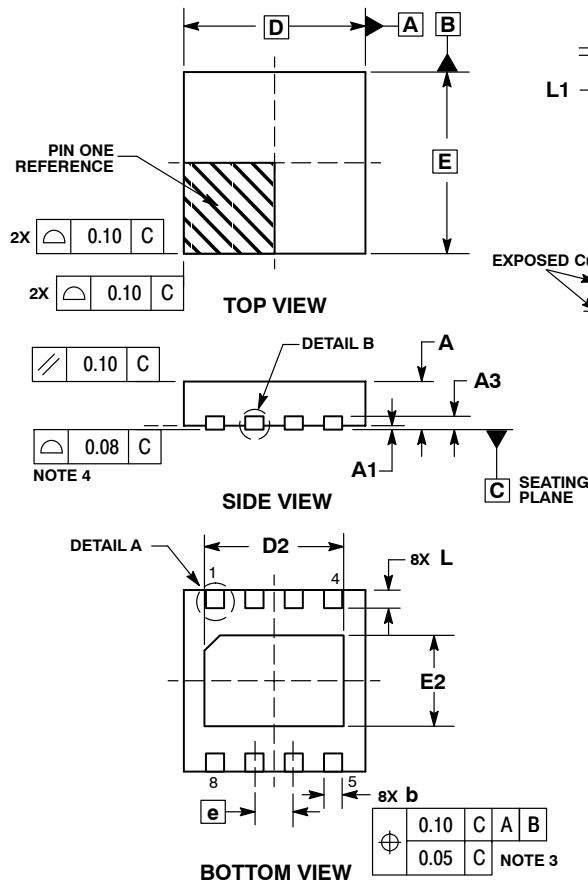
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SCALE 2:1

WDFN8 3x3, 0.65P
CASE 511BH-01
ISSUE O

DATE 21 JUL 2010

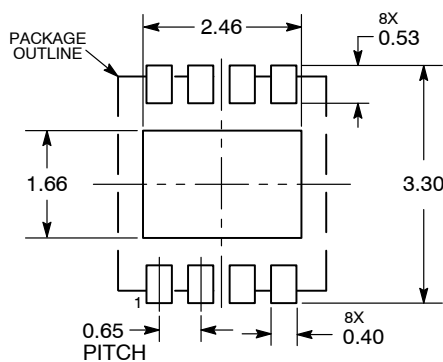


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
K	0.45 REF	
L	0.20	0.40
L1		0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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