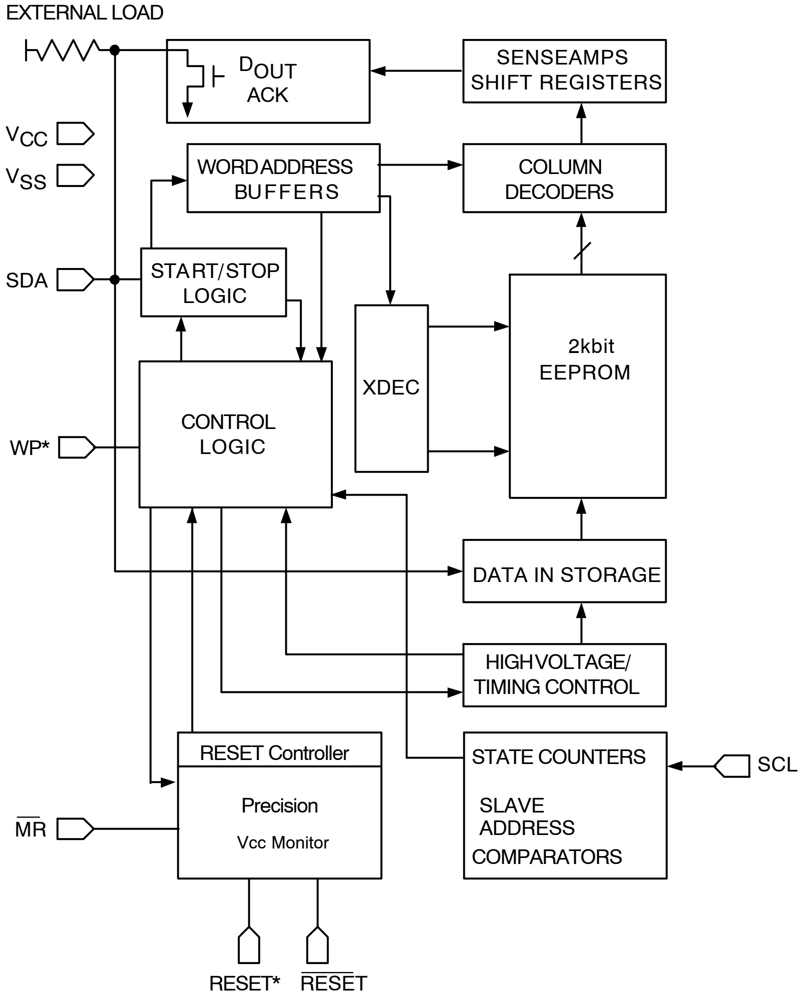
### Table 1. THRESHOLD VOLTAGE OPTION

| Part Dash Number | Minimum Threshold | Maximum Threshold |
|---|---|---|
| –45 | 4.50 | 4.75 |
| –42 | 4.25 | 4.50 |
| –30 | 3.00 | 3.15 |
| –28 | 2.85 | 3.00 |
| –25 | 2.55 | 2.70 |

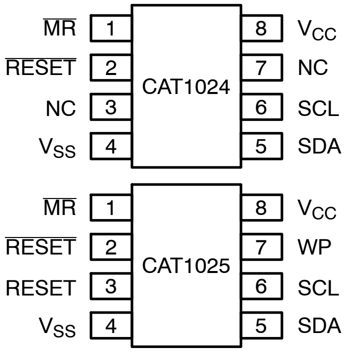
## BLOCK DIAGRAM



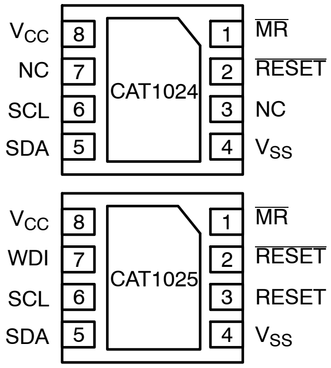
*CAT1025 Only

## PIN CONFIGURATION

**DIP Package (L)**
**SOIC Package (W)**
**TSSOP Package (Y)**
**MSOP Package (Z)**



**(Bottom View)**
**TDFN Package: 3 mm x 3 mm**
**0.8mm maximum height – (ZD4)**



## PIN DESCRIPTION

**RESET/$\overline{\text{RESET}}$**: RESET OUTPUTs (RESET CAT1025 Only)

These are open drain pins and $\overline{\text{RESET}}$ can be used as a manual reset trigger input. By forcing a reset condition on the pin the device will initiate and maintain a reset condition. The RESET pin must be connected through a pull−down resistor, and the $\overline{\text{RESET}}$ pin must be connected through a pull−up resistor.

**SDA**: SERIAL DATA ADDRESS

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs.

**SCL**: SERIAL CLOCK

Serial clock input.

**$\overline{\text{MR}}$**: MANUAL RESET INPUT

Manual Reset input is a debounced input that can be connected to an external source for Manual Reset. Pulling the MR input low will generate a Reset condition. Reset outputs are active while MR input is low and for the reset timeout period after MR returns to high. The input has an internal pull up resistor.

**WP** (CAT1025 Only): WRITE PROTECT INPUT

When WP input is tied to $V_{SS}$ or left unconnected write operations to the entire array are allowed. When tied to $V_{CC}$, the entire array is protected. This input has an internal pull down resistor.

**Table 2. PIN FUNCTION**

| Pin Name | Function |
|---|---|
| NC | No Connect |
| $\overline{\text{RESET}}$ | Active Low Reset Input/Output |
| $V_{SS}$ | Ground |
| SDA | Serial Data/Address |
| SCL | Clock Input |
| RESET | Active High Reset Output (CAT1025 Only) |
| $V_{CC}$ | Power Supply |
| WP | Write Protect (CAT1025 Only) |
| $\overline{\text{MR}}$ | Manual Reset Input |

**Table 3. OPERATING TEMPERATURE RANGE**

| | |
|---|---|
| Industrial | −40°C to 85°C |
| Extended | −40°C to 125°C |

**Table 4. CAT102X FAMILY OVERVIEW**

| Device | Manual Reset Input Pin | Watchdog | Watchdog Monitor Pin | Write Protection Pin | Independent Auxiliary Voltage Sense | RESET: Active High and LOW | EEPROM |
|---|---|---|---|---|---|---|---|
| CAT1021 | ✓ | ✓ | SDA | ✓ |  | ✓ | 2k |
| CAT1022 | ✓ | ✓ | SDA |  |  |  | 2k |
| CAT1023 | ✓ | ✓ | WDI |  |  | ✓ | 2k |
| CAT1024 | ✓ |  |  |  |  |  | 2k |
| CAT1025 | ✓ |  |  | ✓ |  | ✓ | 2k |
| CAT1026 |  |  |  |  | ✓ | ✓ | 2k |
| CAT1027 |  | ✓ | WDI |  | ✓ |  | 2k |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

## SPECIFICATIONS

**Table 5. ABSOLUTE MAXIMUM RATINGS**

| Parameters | Ratings | Units |
|---|---|---|
| Temperature Under Bias | –55 to +125 | °C |
| Storage Temperature | –65 to +150 | °C |
| Voltage on any Pin with Respect to Ground (Note 1) | –2.0 to $V_{CC}$ + 2.0 | V |
| $V_{CC}$ with Respect to Ground | –2.0 to 7.0 | V |
| Package Power Dissipation Capability ($T_A$ = 25°C) | 1.0 | W |
| Lead Soldering Temperature (10 s) | 300 | °C |
| Output Short Circuit Current (Note 2) | 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The minimum DC input voltage is –0.5 V. During transitions, inputs may undershoot to –2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is $V_{CC}$ +0.5 V, which may overshoot to $V_{CC}$ +2.0 V for periods of less than 20 ns.
2. Output shorted for no more than one second. No more than one output shorted at a time.

**Table 6. D.C. OPERATING CHARACTERISTICS**

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | –2 |  | 10 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{IN}$ = GND to $V_{CC}$ | –10 |  | 10 | µA |
| $I_{CC1}$ | Power Supply Current (Write) | $f_{SCL}$ = 400 kHz<br>$V_{CC}$ = 5.5 V |  |  | 3 | mA |
| $I_{CC2}$ | Power Supply Current (Read) | $f_{SCL}$ = 400 kHz<br>$V_{CC}$ = 5.5 V |  |  | 1 | mA |
| $I_{SB}$ | Standby Current | $V_{CC}$ = 5.5 V<br>$V_{IN}$ = GND or $V_{CC}$ |  |  | 40 | µA |
| $V_{IL}$ (Note 3) | Input Low Voltage |  | –0.5 |  | 0.3 x $V_{CC}$ | V |
| $V_{IH}$ (Note 3) | Input High Voltage |  | 0.7 x $V_{CC}$ |  | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage (SDA, $\overline{\text{RESET}}$) | $I_{OL}$ = 3 mA<br>$V_{CC}$ = 2.7 V |  |  | 0.4 | V |
| $V_{OH}$ | Output High Voltage (RESET) | $I_{OH}$ = –0.4 mA<br>$V_{CC}$ = 2.7 V | $V_{CC}$ – 0.75 |  |  | V |

### Table 6. D.C. OPERATING CHARACTERISTICS

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions unless otherwise specified.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{TH}$ | Reset Threshold | CAT102x−45<br>($V_{CC}$ = 5.0 V) | 4.50 | | 4.75 | V |
| | | CAT102x−42<br>($V_{CC}$ = 5.0 V) | 4.25 | | 4.50 | |
| | | CAT102x−30<br>($V_{CC}$ = 3.3 V) | 3.00 | | 3.15 | |
| | | CAT102x−28<br>($V_{CC}$ = 3.3 V) | 2.85 | | 3.00 | |
| | | CAT102x−25<br>($V_{CC}$ = 3.0 V) | 2.55 | | 2.70 | |
| $V_{RVALID}$ | Reset Output Valid $V_{CC}$ Voltage | | 1.00 | | | V |
| $V_{RT}$ (Note 4) | Reset Threshold Hysteresis | | 15 | | | mV |

3. $V_{IL}$ min and $V_{IH}$ max are reference values only and are not tested.
4. This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.

### Table 7. CAPACITANCE

$T_A$ = 25°C, f = 1.0 MHz, $V_{CC}$ = 5 V

| Symbol | Test | Test Conditions | Max | Units |
|---|---|---|---|---|
| $C_{OUT}$ (Note 5) | Output Capacitance | $V_{OUT}$ = 0 V | 8 | pF |
| $C_{IN}$ (Note 5) | Input Capacitance | $V_{IN}$ = 0 V | 6 | pF |

### Table 8. AC CHARACTERISTICS

$V_{CC}$ = 2.7 V to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

**Memory Read & Write Cycle** (Note 6)

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $f_{SCL}$ | Clock Frequency | | 400 | kHz |
| $t_{SP}$ | Input Filter Spike Suppression (SDA, SCL) | | 100 | ns |
| $t_{LOW}$ | Clock Low Period | 1.3 | | μs |
| $t_{HIGH}$ | Clock High Period | 0.6 | | μs |
| $t_R$ (Note 5) | SDA and SCL Rise Time | | 300 | ns |
| $t_F$ (Note 5) | SDA and SCL Fall Time | | 300 | ns |
| $t_{HD; STA}$ | Start Condition Hold Time | 0.6 | | μs |
| $t_{SU; STA}$ | Start Condition Setup Time (for a Repeated Start) | 0.6 | | μs |
| $t_{HD; DAT}$ | Data Input Hold Time | 0 | | ns |
| $t_{SU; DAT}$ | Data Input Setup Time | 100 | | ns |
| $t_{SU; STO}$ | Stop Condition Setup Time | 0.6 | | μs |
| $t_{AA}$ | SCL Low to Data Out Valid | | 900 | ns |
| $t_{DH}$ | Data Out Hold Time | 50 | | ns |
| $t_{BUF}$ (Note 5) | Time the Bus must be Free Before a New Transmission Can Start | 1.3 | | μs |
| $t_{WC}$ (Note 7) | Write Cycle Time (Byte or Page) | | 5 | ms |

5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. Test Conditions according to "AC Test Conditions" table.
7. The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

### Table 9. RESET CIRCUIT AC CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PURST}$ | Power−Up Reset Timeout | Note 2 | 130 | 200 | 270 | ms |
| $t_{RDP}$ | $V_{TH}$ to RESET output Delay | Note 3 | | | 5 | μs |
| $t_{GLITCH}$ | $V_{CC}$ Glitch Reject Pulse Width | Notes 4 and 5 | | | 30 | ns |
| MR Glitch | Manual Reset Glitch Immunity | Note 1 | | | 100 | ns |
| $t_{MRW}$ | MR Pulse Width | Note 1 | 5 | | | μs |
| $t_{MRD}$ | MR Input to RESET Output Delay | Note 1 | | | 1 | μs |

### Table 10. POWER−UP TIMING (Notes 5 and 6)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PUR}$ | Power−Up to Read Operation | | | | 270 | ms |
| $t_{PUW}$ | Power−Up to Write Operation | | | | 270 | ms |

### Table 11. AC TEST CONDITIONS

| Parameter | Test Conditions |
|---|---|
| Input Pulse Voltages | 0.2 x $V_{CC}$ to 0.8 x $V_{CC}$ |
| Input Rise and Fall Times | 10 ns |
| Input Reference Voltages | 0.3 x $V_{CC}$ , 0.7 x $V_{CC}$ |
| Output Reference Voltages | 0.5 x $V_{CC}$ |
| Output Load | Current Source: $I_{OL}$ = 3 mA; $C_L$ = 100 pF |

### Table 12. RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Max | Units |
|---|---|---|---|---|---|
| $N_{END}$ (Note 5) | Endurance | MIL−STD−883, Test Method 1033 | 1,000,000 | | Cycles/Byte |
| $T_{DR}$ (Note 5) | Data Retention | MIL−STD−883, Test Method 1008 | 100 | | Years |
| $V_{ZAP}$ (Note 5) | ESD Susceptibility | MIL−STD−883, Test Method 3015 | 2000 | | Volts |
| $I_{LTH}$ (Notes 5 & 7) | Latch−Up | JEDEC Standard 17 | 100 | | mA |

1. Test Conditions according to “AC Test Conditions” table.
2. Power−up, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
3. Power−Down, Input Reference Voltage $V_{CC} = V_{TH}$, Reset Output Reference Voltage and Load according to “AC Test Conditions” Table
4. $V_{CC}$ Glitch Reference Voltage = $V_{THmin}$; Based on characterization data
5. This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
6. $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified memory operation can be initiated.
7. Latch−up protection is provided for stresses up to 100 mA on input and output pins from −1 V to $V_{CC}$ + 1 V.

## DEVICE OPERATON

### Reset Controller Description

The CAT1024/25 precision RESET controllers ensure correct system operation during brownout and power up/down conditions. They are configured with open drain RESET outputs.

During power−up, the RESET outputs remain active until $V_{CC}$ reaches the $V_{TH}$ threshold and will continue driving the outputs for approximately 200 ms ($t_{PURST}$) after reaching $V_{TH}$. After the $t_{PURST}$ timeout interval, the device will cease to drive the reset outputs. At this point the reset outputs will be pulled up or down by their respective pull up/down resistors.

During power−down, the RESET outputs will be active when $V_{CC}$ falls below $V_{TH}$. The $\overline{\text{RESET}}$ output will be valid so long as $V_{CC}$ is > 1.0 V ($V_{RVALID}$). The device is designed to ignore the fast negative going $V_{CC}$ transient pulses (glitches).

Reset output timing is shown in Figure 1.

### Manual Reset Operation

The $\overline{\text{RESET}}$ pin can operate as reset output and manual reset input. The input is edge triggered; that is, the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition.

When $\overline{\text{RESET}}$ I/O is driven to the active state, the 200 ms timer will begin to time the reset interval. If external reset is shorter than 200 ms, Reset outputs will remain active at least 200 ms.

The CAT1024/25 also have a separate manual reset input. Driving the $\overline{\text{MR}}$ input low by connecting a pushbutton (normally open) from $\overline{\text{MR}}$ pin to GND will generate a reset condition. The input has an internal pull up resistor.

Reset remains asserted while $\overline{\text{MR}}$ is low and for the Reset Timeout period after $\overline{\text{MR}}$ input has gone high.

Glitches shorter than 100 ns on $\overline{\text{MR}}$ input will not generate a reset pulse. No external debouncing circuits are required. Manual reset operation using $\overline{\text{MR}}$ input is shown in Figure 2.

### Hardware Data Protection

The CAT1024/25 supervisors have been designed to solve many of the data corruption issues that have long been associated with serial EEPROMs. Data corruption occurs when incorrect data is stored in a memory location which is assumed to hold correct data.

Whenever the device is in a Reset condition, the embedded EEPROM is disabled for all operations, including write operations. If the Reset output(s) are active, in progress communications to the EEPROM are aborted and no new communications are allowed. In this condition an internal write cycle to the memory can not be started, but an in progress internal nonvolatile memory write cycle can not be aborted. An internal write cycle initiated before the Reset condition can be successfully finished if there is enough time (5ms) before $V_{CC}$ reaches the minimum value of 2 V.

In addition, the CAT1025 includes a Write Protection Input which when tied to $V_{CC}$ will disable any write operations to the device.

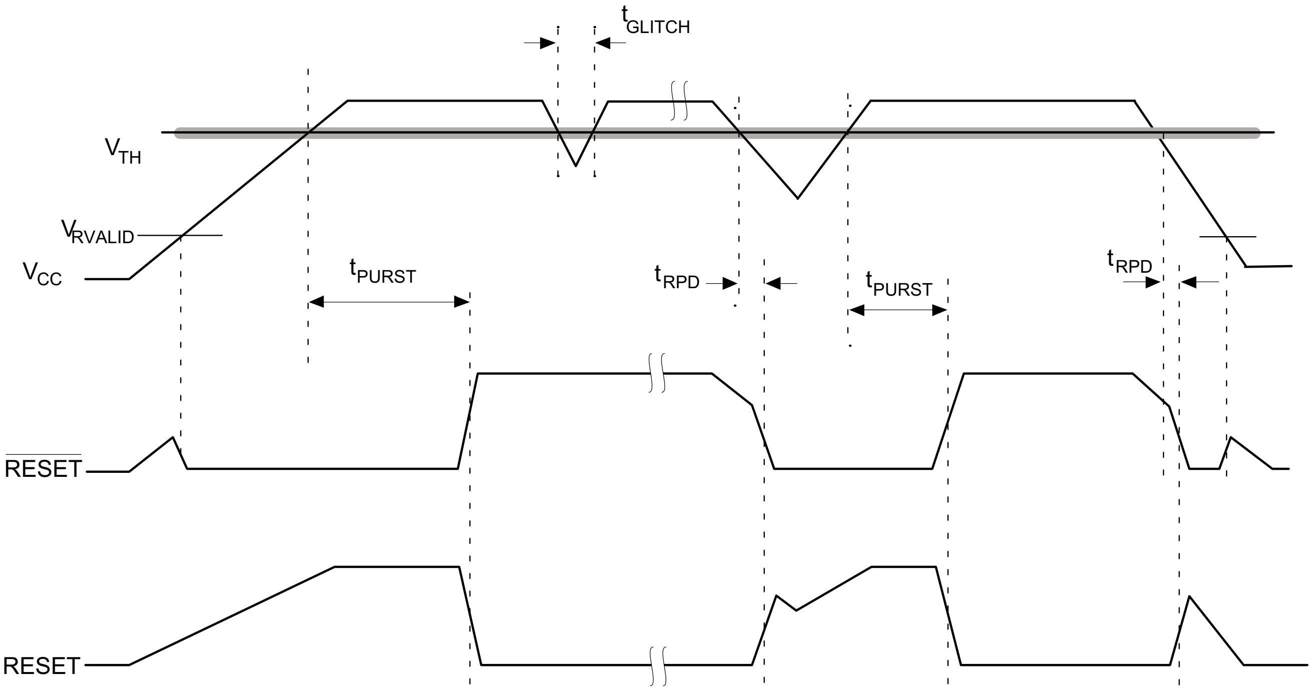


**Figure 1. RESET Output Timing**

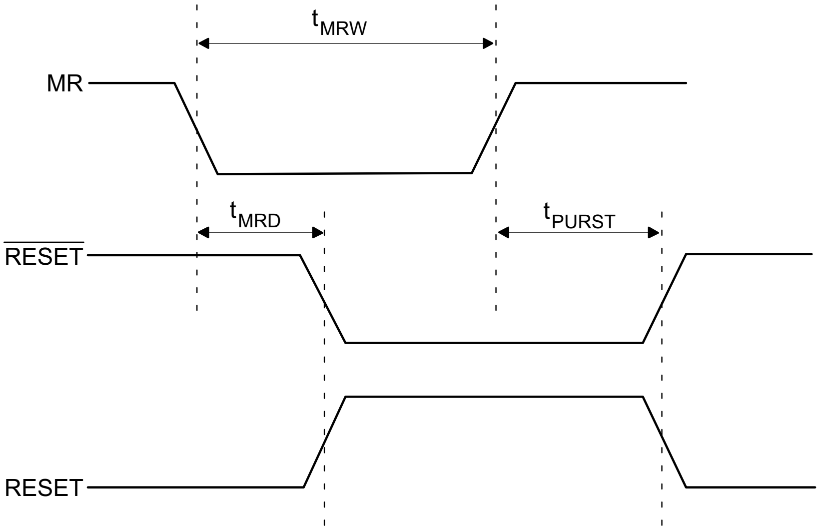


**Figure 2. $\overline{MR}$ Operation and Timing**

## EMBEDDED EEPROM OPERATON

The CAT1024 and CAT1025 feature a 2−kbit embedded serial EEPROM that supports the I$^2$C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

### I$^2$C Bus Protocol

The features of the I$^2$C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

### Start Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT1024/25 monitors the SDA and SCL lines and will not respond until this condition is met.

### Stop Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

## DEVICE ADDRESSING

The Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The four most significant bits of the 8−bit slave address are programmable in metal and the default is 1010.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT1024/25 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT1024/25 then perform a Read or Write operation depending on the R/$\overline{\text{W}}$ bit.

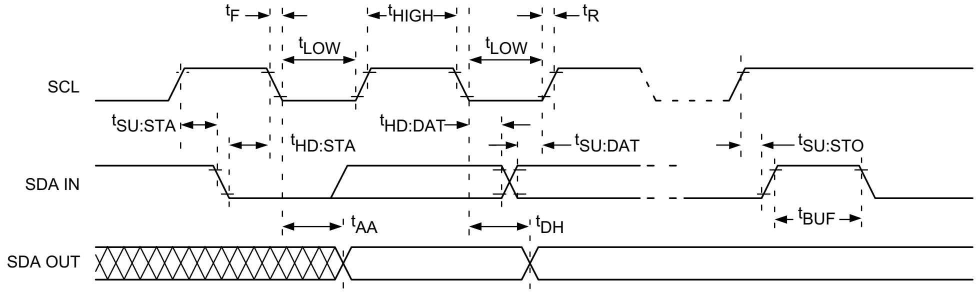


**Figure 3. Bus Timing**

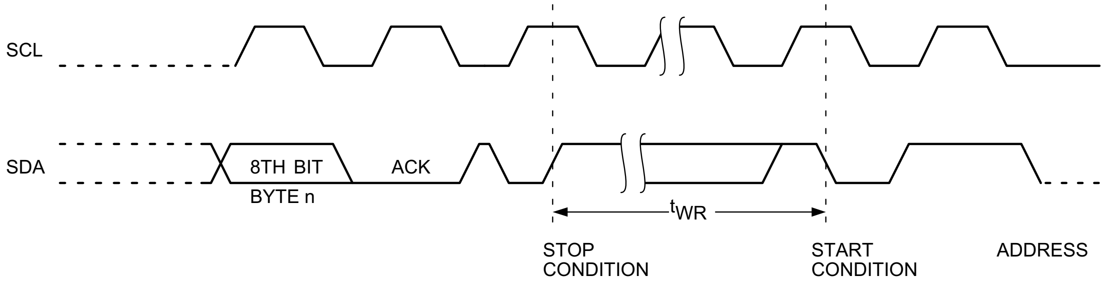


**Figure 4. Write Cycle Timing**

## ACKNOWLEDGE

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT1024/25 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8−bit byte.

When the CAT1024/25 begins a READ mode it transmits 8 bits of data, releases the SDA line and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT1024/25 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

## WRITE OPERATIONS

### Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends a 8−bit address that is to be written into the address pointers of the device. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT1024/25 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to non−volatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

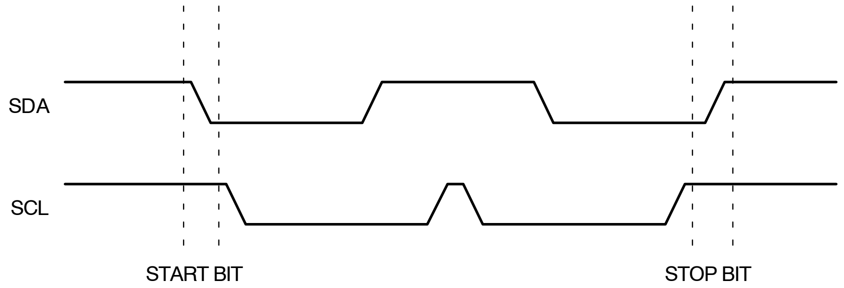


**Figure 5. Start/Stop Timing**

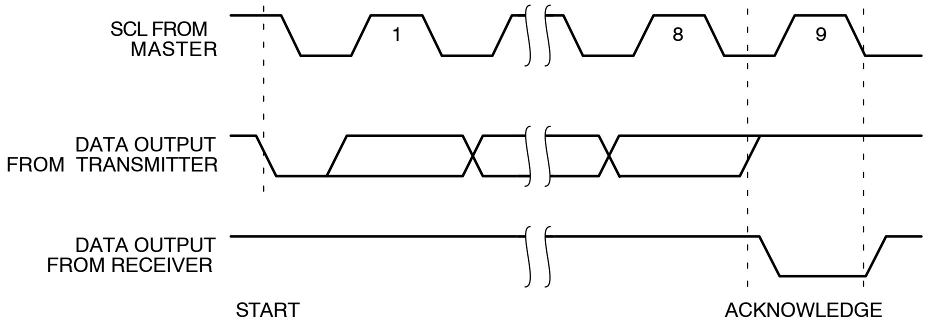


**Figure 6. Acknowledge Timing**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Default Configuration | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |

**Figure 7. Slave Address Bits**

### Page Write

The CAT1024/25 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted, the CAT1024/25 will respond with an acknowledge and internally increment the lower order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes before sending the STOP condition, the address counter 'wraps around,' and previously transmitted data will be overwritten.

When all 16 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT1024/25 in a single write cycle.

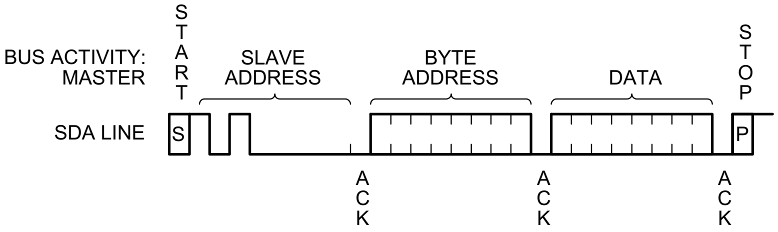


Figure 8. Byte Write Timing

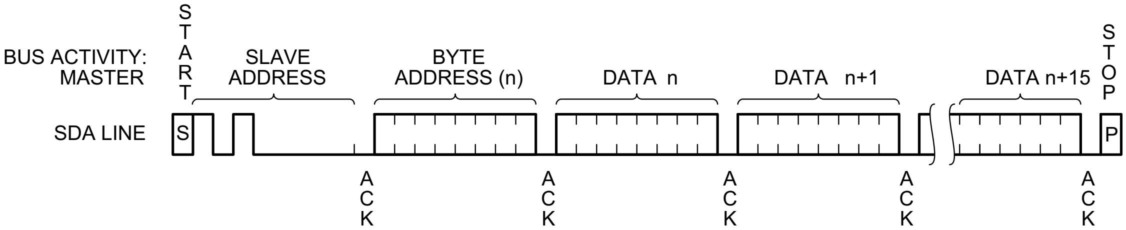


Figure 9. Page Write Timing

### Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT1024/25 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the device is still busy with the write operation, no ACK will be returned. If a write operation has completed, an ACK will be returned and the host can then proceed with the next read or write operation.

## WRITE PROTECTION PIN (WP)

The Write Protection feature (CAT1025 only) allows the user to protect against inadvertent memory array programming. If the WP pin is tied to $V_{CC}$, the entire memory array is protected and becomes read only. The CAT1025 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

## READ OPERATIONS

The READ operation for the CAT1024/25 is initiated in the same manner as the write operation with one exception, the R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

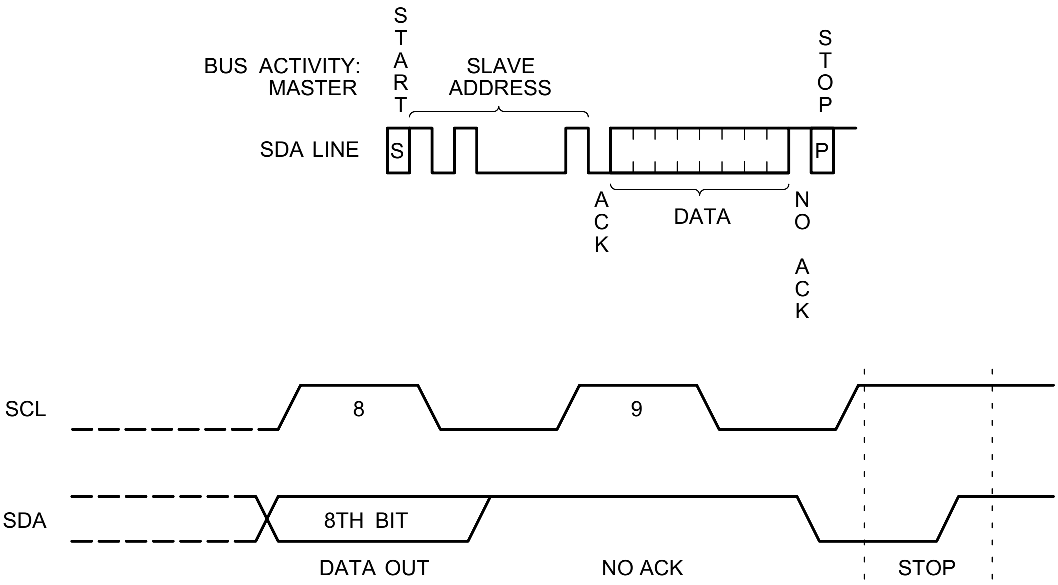


**Figure 10. Immediate Address Read Timing**

### Immediate/Current Address Read

The CAT1024 and CAT1025 address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. For N = E = 255, the counter will wrap around to zero and continue to clock out valid data. After the CAT1024/1025 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8−bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

### Selective/Random Read

Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a ‘dummy’ write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After the CAT1024 and CAT1025 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT1024 and CAT1025 then responds with its acknowledge and sends the 8−bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

### Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT1024 and CAT1025 sends the initial 8− bit byte requested, the Master will responds with an acknowledge which tells the device it requires more data. The CAT1024 and CAT1025 will continue to output an 8−bit byte for each acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT1024 and CAT1025 is sent sequentially with the data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT1024 and CAT1025 address bits so that the entire memory array can be read during one operation.

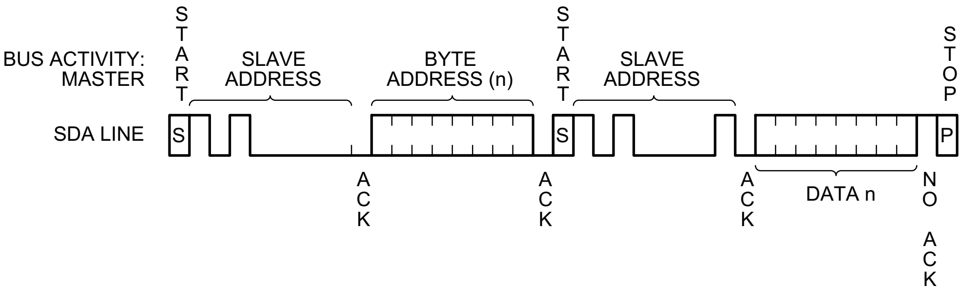


**Figure 11. Selective Read Timing**

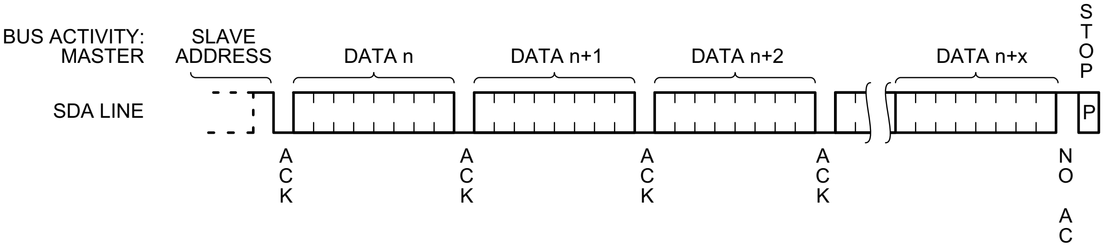


**Figure 12. Sequential Read Timing**

## ORDERING INFORMATION

| Orderable Part Numbers – CAT1024 Series<br>(See Notes 1 – 5) | | | |
|---|---|---|---|
| Device | Reset Threshold | Package | Shipping† |
| CAT1024WI–45–GT3 | 4.50 V – 4.75 V | SOIC | 3000 Tape & Reel |
| CAT1024WI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1024WI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1024WI–28–GT3 | 2.85 V – 3.00 V | | |
| CAT1024WI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1024YI–45–GT3 | 4.50 V – 4.75 V | TSSOP | |
| CAT1024YI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1024YI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1024YI–28–GT3 | 2.85 V – 3.00 V | | |
| CAT1024YI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1024ZI–45–GT3 | 4.50 V – 4.75 V | MSOP | |
| CAT1024ZI–42–GT3 | 4.25 V – 4.50 V | | |
| CAT1024ZI–30–GT3 | 3.00 V – 3.15 V | | |
| CAT1024ZI–25–GT3 | 2.55 V – 2.70 V | | |
| CAT1024ZD4I–45T3* | 4.50 V – 4.75 V | TDFN | |
| CAT1024ZD4I–42T3* | 4.25 V – 4.50 V | | |
| CAT1024ZD4I–30T3* | 3.00 V – 3.15 V | | |
| CAT1024ZD4I–28T3* | 2.85 V – 3.00 V | | |
| CAT1024ZD4I–25T3* | 2.55 V – 2.70 V | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. All packages are RoHS–compliant (Lead–free, Halogen–free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (–G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

| **Orderable Part Numbers – CAT1025 Series**<br>(See Notes 1 – 5) | | | |
|---|---|---|---|
| Device | Reset Threshold | Package | Shipping† |
| CAT1025WI−45−GT3 | 4.50 V – 4.75 V | SOIC | 3000 Tape & Reel |
| CAT1025WI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1025WI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1025WI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1025WI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1025YI−45−GT3 | 4.50 V – 4.75 V | TSSOP | |
| CAT1025YI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1025YI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1025YI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1025YI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1025ZI−45−GT3 | 4.50 V – 4.75 V | MSOP | |
| CAT1025ZI−42−GT3 | 4.25 V – 4.50 V | | |
| CAT1025ZI−30−GT3 | 3.00 V – 3.15 V | | |
| CAT1025ZI−28−GT3 | 2.85 V – 3.00 V | | |
| CAT1025ZI−25−GT3 | 2.55 V – 2.70 V | | |
| CAT1025ZD4I−45T3* | 4.50 V – 4.75 V | TDFN | |
| CAT1025ZD4I−42T3* | 4.25 V – 4.50 V | | |
| CAT1025ZD4I−30T3* | 3.00 V – 3.15 V | | |
| CAT1025ZD4I−28T3* | 2.85 V – 3.00 V | | |
| CAT1025ZD4I−25T3* | 2.55 V – 2.70 V | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. All packages are RoHS−compliant (Lead−free, Halogen−free).
2. The standard lead finish is NiPdAu.
3. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
4. TDFN not available in NiPdAu (–G) version.
5. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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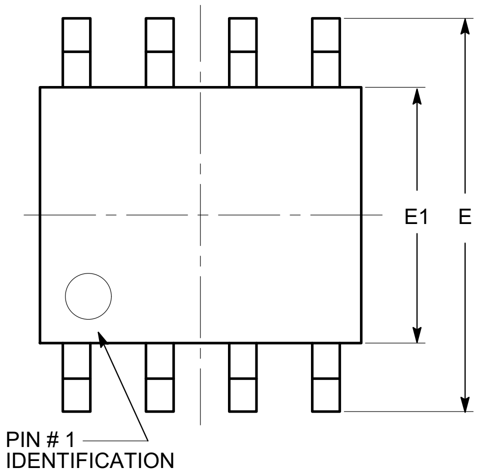
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**ON Semiconductor®**

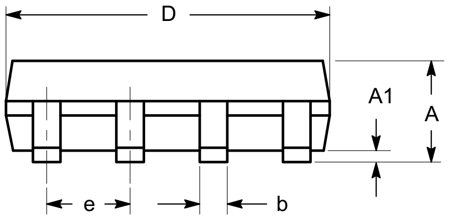
**SOIC 8, 150 mils**
CASE 751BD−01
ISSUE O

DATE 19 DEC 2008

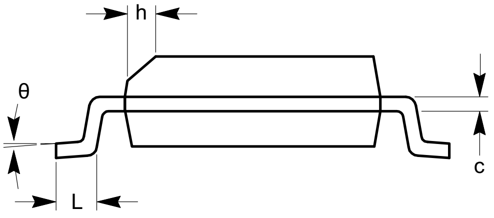


**TOP VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 1.35 | | 1.75 |
| A1 | 0.10 | | 0.25 |
| b | 0.33 | | 0.51 |
| c | 0.19 | | 0.25 |
| D | 4.80 | | 5.00 |
| E | 5.80 | | 6.20 |
| E1 | 3.80 | | 4.00 |
| e | 1.27 BSC | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| θ | 0º | | 8º |



**SIDE VIEW**



**END VIEW**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

| | | |
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| **REFERENCE:** | | |
| **DESCRIPTION:** | **SOIC 8, 150 MILS** | **PAGE 1 OF 2** |

**ON Semiconductor**®

| | |
|---|---|
| **DOCUMENT NUMBER:**<br>**98AON34272E** | **PAGE 2 OF 2** |

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION FROM POD #SOIC8−002−01 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN. | 19 DEC 2008 |
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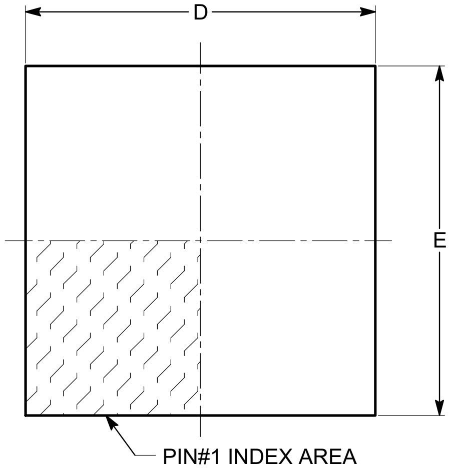
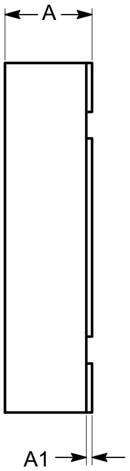
# TDFN8, 3x3

CASE 511AL−01
ISSUE A

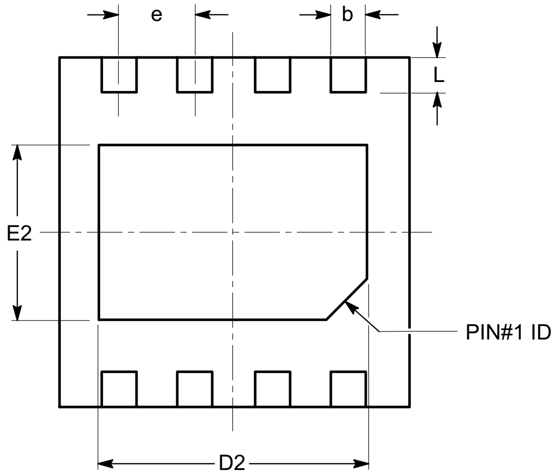
DATE 24 MAR 2009



**TOP VIEW**

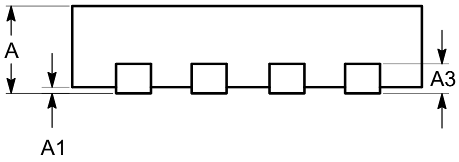


**SIDE VIEW**



**BOTTOM VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.20 REF | |
| b | 0.23 | 0.30 | 0.37 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.20 | −−− | 2.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.40 | −−− | 1.80 |
| e | | 0.65 TYP | |
| L | 0.20 | 0.30 | 0.40 |



**FRONT VIEW**

**Notes:**

(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

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| **REFERENCE:** | | |
| **DESCRIPTION:** | **TDFN8, 3X3** | **PAGE 1 OF 2** |

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION FROM POD #TDFN8−040−02 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN. | 19 DEC 2008 |
| A | CHANGED DESCRIPTION FROM WDFN TO TDFN. | 24 MAR 2009 |
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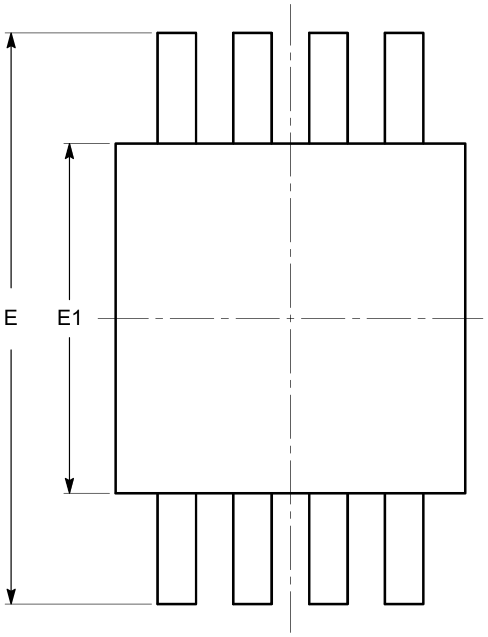
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**ON Semiconductor®**

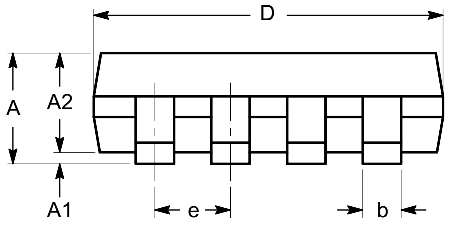
### MSOP 8, 3x3
CASE 846AD−01
ISSUE O

DATE 19 DEC 2008

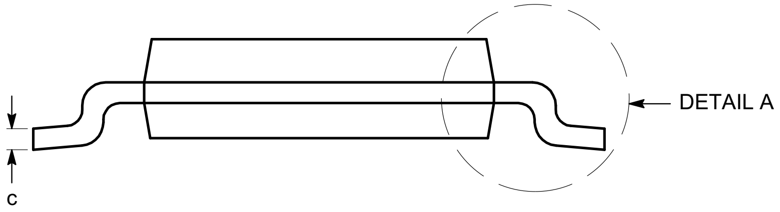
| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | | | 1.10 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.22 | | 0.38 |
| c | 0.13 | | 0.23 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.80 | 4.90 | 5.00 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | | 0.65 BSC | |
| L | 0.40 | 0.60 | 0.80 |
| L1 | | 0.95 REF | |
| L2 | | 0.25 BSC | |
| θ | 0º | | 6º |



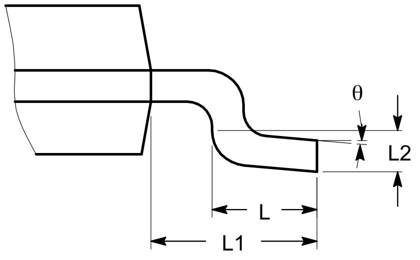
**TOP VIEW**



**SIDE VIEW**



**END VIEW**



**DETAIL A**

**Notes:**
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-187.

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| | |
|---|---|
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| | **PAGE 2 OF 2** |

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|---|---|---|
| O | RELEASED FOR PRODUCTION FROM POD #MSOP8−003−01 TO ON SEMICONDUCTOR. REQ. BY B. BERGMAN. | 19 DEC 2008 |
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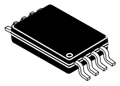
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

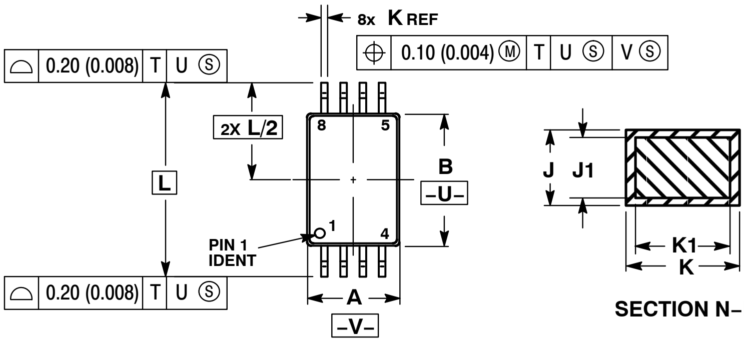
**ON Semiconductor®**



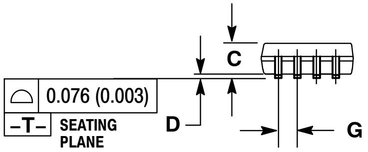
SCALE 2:1

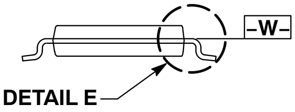
### TSSOP−8
CASE 948S−01
ISSUE C

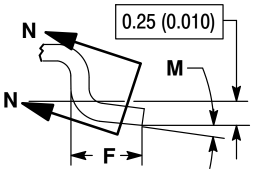
DATE 20 JUN 2008



SECTION N−N







DETAIL E

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

### GENERIC MARKING DIAGRAM*

○ XXX
YWW
A ▪
▪

XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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| **DESCRIPTION:** | **TSSOP−8** | **PAGE 1 OF 2** |

| ISSUE | REVISION | DATE |
|---|---|---|
| O | RELEASED FOR PRODUCTION. | 18 APR 2000 |
| A | ADDED MARKING DIAGRAM INFORMATION. REQ. BY V. BASS. | 13 JAN 2006 |
| B | CORRECTED MARKING DIAGRAM PIN 1 LOCATION AND MARKING. REQ. BY C. REBELLO. | 13 MAR 2006 |
| C | REMOVED EXPOSED PAD VIEW AND DIMENSIONS P AND P1. CORRECTED MARKING INFORMATION. REQ. BY C. REBELLO. | 20 JUN 2008 |
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